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ISO-CMOS MT3070/71/74/75
Wide Dynamic Range DTMF Receiver

Preliminary Information

9161-002-102-NA ISSUE 4 October 1989

Features

- 45 dB dynamic range
- Simultaneous DTMF and supervisory tone detection (MT3070/MT3071)
- Powerdown mode
- 4-bit binary serial data output
- For use with microprocessor controlled guard time (MT3070/MT3074)
- Internal guard time circuitry (MT3071/MT3075)

Applications

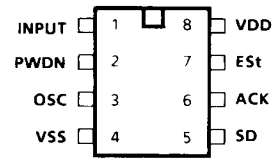
- Integrated telephone answering machine
- End-to-end signalling

Description

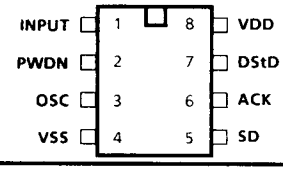
The MT3070/MT3071/MT3074/MT3075 is a high performance DTMF Receiver which decodes all 16 DTMF tone pairs into a 4-bit binary code. The device incorporates an AGC for wide dynamic range which is suitable for end-to-end signalling. The MT3070/MT3071 also indicates the presence of all supervisory tones using internal detection circuitry. The MT3074/MT3075 does not detect the presence of supervisory tones. The powerdown function provides low standby current. The MT3070/MT3074 is useful in applications where DTMF validation period is determined by external control. The MT3071/MT3075 uses internal counters to provide a preset DTMF validation period. The MT3070/MT3071/MT3074/MT3075 uses a crystal or a ceramic resonator to complete the oscillator circuit.

Pin Connections

MT3070/MT3074



MT3071/MT3075



Ordering Information - 40 °C to + 85 °C

MT3070/71/74/75AE	Plastic DIP
MT3070/71/74/75AC	Cerdip

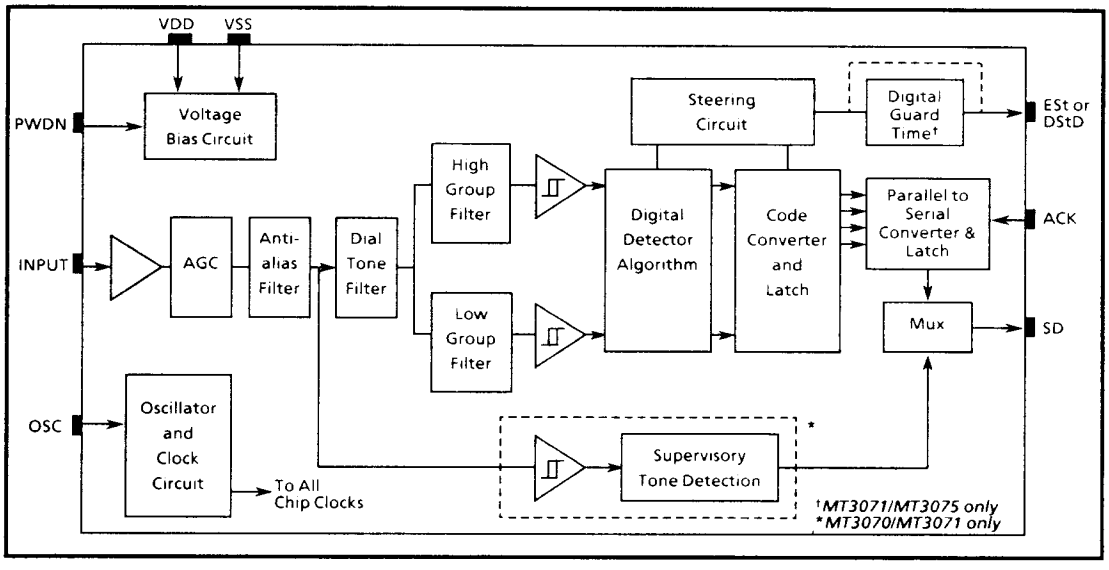


Figure 1 - Functional Block Diagram

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}-V_{SS}		6	V
2	Voltage on any pin (other than supply)	$V_{I/O}$	V_{SS} – 0.3	V_{DD} + 0.3	V
3	Current at any pin (other than supply)	$I_{I/O}$		10	mA
4	Storage temperature	T_{STG}	– 65	+ 150	°C
5	Package power dissipation	P_D		500	mW

†Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Derate above 85 °C at 9 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Positive Power Supply	V_{DD}	4.75	5.0	5.25	V	V_{SS} = 0V
2		Oscillator Clock Frequency	fc		4.194304		MHz	
3		Oscillator Frequency Tolerance	Δfc		± 0.1		%	
4		Operating temperature	To	-40	25	+ 85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics- Over recommended operating conditions unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Operating supply current	I_{DD}		3.0		mA	
2		Standby supply current	I_{DDQ}			100	μA	PWDN = V_{DD}
3		Input High Voltage (except OSC Input)	V_{IH}	V_{DD}-1.5			V	
4		Input High Voltage (for OSC Input only)	V_{IH}	V_{DD}-1.0			V	
5		Input Low Voltage	V_{IL}			V_{SS} + 1.5	V	
6		Input Leakage Current (Pins 2 & 6)			0.1		μA	
7		Input impedance (Pin 1)	R_{IN}	10			kΩ	
8		Input impedance (Pin 3)	R_{IN}		4		kΩ	
9		Output high (source) current	I_{OH}	0.4			mA	V_{OUT} = V_{DD}-0.4V (SD,ESt,DStD)
10		Output low (sink) current	I_{OL}	1.0			mA	V_{OUT} = V_{SS} + 0.4V (SD,ESt,DStD)

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

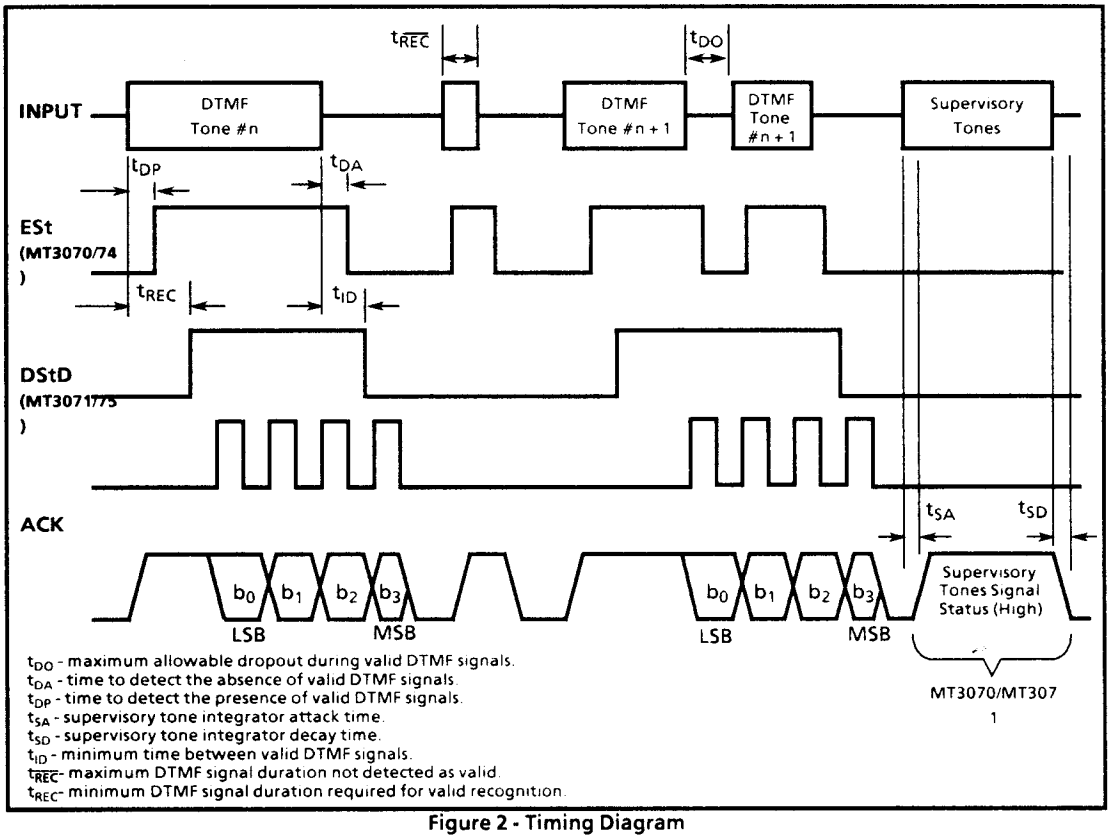
AC Electrical Characteristics- over recommended operating conditions unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions*
1	Valid input signal level (each tone of composite signal).		-45		0	dBm	1,2,3,5,6,9
			4.36		775	mV_{RMS}	1,2,3,5,6,9
2	Positive twist accept				6	dB	1,2,3,4,9,14
3	Negative twist accept				6	dB	1,2,3,4,9,14
4	Frequency deviation accept		± 1.5% ± 2Hz				1,2,3, 5, 9
5	Frequency deviation reject		±3.5%				1,2,3, 5, 9
6	Third tone tolerance			– 16		dB	1,2,3,4,5,9, 12
7	Noise tolerance			– 12		dB	7,9, 10
8	Dial tone tolerance			+ 22		dB	8, 9, 11
9	Supervisory tones detect level (Total power)			-30		dBm	13 for MT3070/3071
10	Supervisory tones non-detect level (Total power)			-35		dBm	13 for MT3070/3071
11	Supervisory tone integrator attack time	t_{SA}		1.0		ms	for MT3070/3071
12	Supervisory tones integrator decay time	t_{SD}		500		ms	for MT3070/3071
13	Tone present detect time (ESt)	t_{DP}	3		20	ms	for MT3070/3074
14	Tone absent detect time (ESt)	t_{DA}	0.5		20	ms	for MT3070/3074
15	Tone duration accept (DStD)	t_{REC}			40	ms	for MT3071/3075
16	Tone duration reject (DStD)	$t_{\overline{REC}}$	20			ms	for MT3071/3075
17	Interdigit pause accept (DStD)	t_{ID}			40	ms	for MT3071/3075
18	Interdigit pause reject (DStD)	t_{DO}	20			ms	for MT3071/3075
19	Data shift rate (ACK) duty cycle 40%-60%				1	MHz	
20	Propagation delay (ACK to Data)	t_{PAD}		100		ns	
21	Set-up time delay (ESt/DStD to ACK)	t_{DL}	0			ns	
22	Data hold time (ACK to SD)	t_{DH}	30			ns	

‡Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing

*** Test Conditions**

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5 % ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 Hz and 440 Hz (± 2 %).
9. For an error rate of better than 1 in 10,000. External guard time for MT3070/MT3074 = 20 ms.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Worst case interfering frequency
13. For testing purposes a C-message filter is connected at the input.
14. Both tones must be within valid input signal range.



t_{DO} - maximum allowable dropout during valid DTMF signals.
t_{DA} - time to detect the absence of valid DTMF signals.
t_{DP} - time to detect the presence of valid DTMF signals.
t_{SA} - supervisory tone integrator attack time.
t_{SD} - supervisory tone integrator decay time.
t_{ID} - minimum time between valid DTMF signals.
$t_{\overline{REC}}$ - maximum DTMF signal duration not detected as valid.
t_{REC} - minimum DTMF signal duration required for valid recognition.

Figure 2 - Timing Diagram

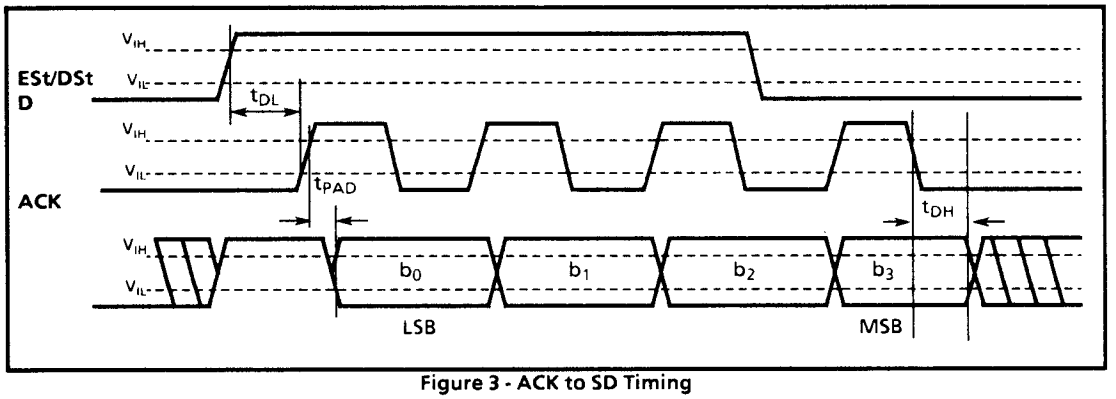


Figure 3 - ACK to SD Timing

Pin Description

Pin #	Name	Description
1	**INPUT**	**Audio Input.** Input signal must be AC coupled as shown in Fig.4.
2	**PWDN**	**Power Down Input.** A logic high on this pin will power down the device to reduce power consumption. The ACK pin must be logic low before a logic high is applied on this pin. For normal operation, PWDN pin must be logic low.
3	**OSC**	**Oscillator Input.** This pin can either be driven by : 1) an external digital output with defined input logic levels. No coupling capacitor is required. 2) connecting a crystal between OSC Input and V_{SS}. No loading capacitor is required. 3) connecting a ceramic resonator between OSC Input and V_{SS}. No loading capacitor is required. Frequency of oscillation should be maintained at 4.194304 MHz ± 0.1%.
4	**V_{SS}**	**Ground.** (0V)
5	**SD**	**Serial Data Output.** In the absence of ACK input signal, a logic high output indicates the presence of tones: DTMF or supervisory tones (MT3070/MT3071 only) . If ESt is high and the ACK pulse sequence is applied, the SD output provides a 4-bit binary code representing the decoded DTMF digit. Refer to Fig. 3.
6	**ACK**	**Acknowledge Pulse Input.** After ESt or DStD goes high, applying a sequence of four pulses on this pin will shift out four bits on the SD pin, representing the decoded DTMF digit. The rising edge of the first pulse will latch the data prior to shifting. Refer to Fig. 3.
7	**ESt (MT3070/ MT3074)** **DStD (MT3071/ MT3075)**	**Early Steering Output.** A logic high on ESt indicates that a DTMF signal is present. **Delayed Steering Output.** A logic high on DStD indicates that a valid DTMF digit has been detected.
8	**V_{DD}**	**Positive Power Supply** . (5V Typ.) Performance of the device can be optimized by minimizing noise on the supply rails. Decoupling capacitors across V_{DD} and V_{SS} are therefore recommended.

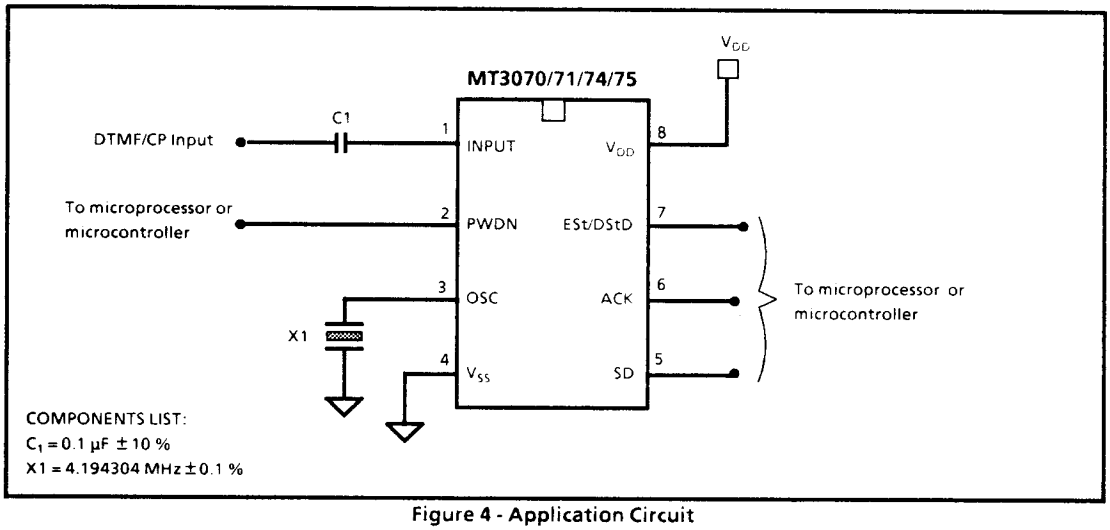


Figure 4 - Application Circuit

Functional Description

The MT3070/MT3071/MT3074/MT3075 is a high performance and low power consumption DTMF Receiver. The receiver provides a wide dynamic range and a serial data output port. The MT3070/MT3071 also provides a supervisory tone detection function. The input signal is applied to a DTMF tone detection circuit and a supervisory tone detection circuit (MT3070/MT3071) via an Automatic Gain Control (AGC). The device incorporates a bandsplit filter section to separate the input DTMF signal into high and low group tones and a digital counting section to verify that the incoming signal corresponds to standard DTMF frequencies. Following verification, the DTMF signal is decoded into a 4-bit code and shifted out in a serial format.

Automatic Gain Control (AGC)

The input signal is buffered by an internal op-amp, followed by an AGC circuit to provide a wide dynamic range. This signal is filtered by a lowpass filter to prevent aliasing distortion. This anti-aliasing filter also serves as the front end filter for the supervisory tone detection. The input signal is then routed to both the DTMF detection circuitry and the supervisory tone detection circuitry.

Filter and Decoder Section

Signals entering the DTMF detection circuitry are filtered by a notch filter at 350 and 440 Hz for dial tone rejection. This signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared by high gain limiting comparators. The resulting squarewaves are applied to a digital detection circuit where a complex averaging algorithm is employed to determine the valid DTMF signal. Upon recognition of a valid frequency from each tone group, the Early Steering (ESt) output of MT3070/MT3074 will go high, indicating that a DTMF tone has been detected. Any subsequent loss of DTMF signal condition will cause ESt pin to go low. For MT3071/MT3075, an internal delayed steering counter validates the early steering signal for a predetermined guard time which requires no external components. The Delayed Steering (DStD) output will go high only when the validation period has elapsed. Once the DStD output is high, any subsequent loss of early steering signal due to DTMF signal dropout will activate the internal counter for a validation of tone absent guard time. The DStD output will go low only after this validation period.

Supervisory Tone Detection (MT3070/MT3071)

The output signal from the AGC circuit is also applied to the supervisory tone detection circuit. When the signal level is above the threshold of the internal comparator, the supervisory tone detection circuit produces a tone present indication on the SD output. The detector circuit incorporates an integrator such that in the presence of supervisory tones, the SD output will remain a continuous high. Since the DTMF signals are in the detection bandwidth, the presence of a DTMF signal will also cause the SD to go high. Therefore, the SD and ESt/DStD output pins should be monitored by a microprocessor in real time, so that various supervisory tones, presence of speech or DTMF signals can be identified. The supervisory tone detection circuit is enabled at all times except during the time between the rising edge of the first pulse and the falling edge of the fourth pulse on ACK pin (see Figure 2).

Serial Data (SD) Output

When a valid DTMF signal is present, ESt /DStD will go high. The application of four clock pulses on the ACK pin will provide a 4-bit serial binary code representing the decoded DTMF digit on the SD pin output. The rising edge of the first pulse applied on the ACK pin latches the data and the least significant bit of the decoded digit is also shifted out on the SD pin. The next three pulses on ACK pin will shift the remaining latched bits in a serial format (see Figure 3). If less than four pulses are applied to the ACK pin, new data cannot be latched even though ESt/DStD is valid. Clock pulses should be applied to shift out any remaining data bits and to resume normal operation. Any transition in excess of four pulses will be ignored until the next rising edge of the ESt/DStD. The 4-bit binary codes representing all 16 standard DTMF digits are shown in Table 1.

Powerdown Mode

The device has a powerdown function to reduce power consumption. To enter powerdown mode, the ACK pin must be logic low before a logic high is applied on the PWDN pin. See Table 2 for setup.

Oscillator

The on-chip oscillator is completed by connecting a 4.194304 MHz crystal or ceramic resonator from OSC pin to ground. The oscillator circuit can also be driven by an external clock at 4.194304 MHz.

F_{LOW}	F_{HIGH}	DIGIT	b_3	b_2	b_1	b_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = LOGIC LOW, 1 = LOGIC HIGH

Table 1 - Serial Decode Bit Table

PWDN (Input)	**ACK** (Input)	**ESt/DStD** (Output)	**SD** (Output)	**MT3070/71/74/75 Status**
Low	Refer to Figs. 2 and 3 for Timing Waveforms			Normal operation
High†	Low	Low	Low	Powerdown mode
High	High	X	X	Undefined

† = enters powerdown mode on the rising edge

X = don't care

Table 2 - Powerdown Mode

Applications

The circuit shown in Figure 4 illustrates the use of the MT3070/MT3071/MT3074/MT3075 in a typical receiver application. It requires only a coupling capacitor and a crystal or ceramic resonator.

The MT3070/MT3074 is designed for the user who wishes to tailor the guard time for specific applications. When a DTMF signal is present, the ESt pin will go high. An external microprocessor monitors ESt in real time for a period of time set by the user. A guard time algorithm must be implemented such that DTMF signals not meeting the timing requirements are rejected. The MT3071/MT3075 uses an internal counter to provide a preset DTMF validation period. It requires no external components. The DStD output high indicates that a valid DTMF digit has been detected.

The 4.194304 MHz frequency has a secondary advantage in some applications where a real time clock is required. A 22-bit counter will count 4194304 cycles to provide a one second time base.

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