

MC14001UB, MC14011UB

UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

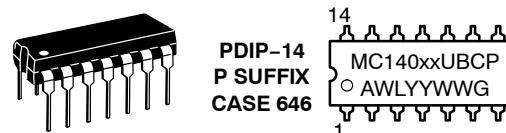
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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MARKING DIAGRAMS



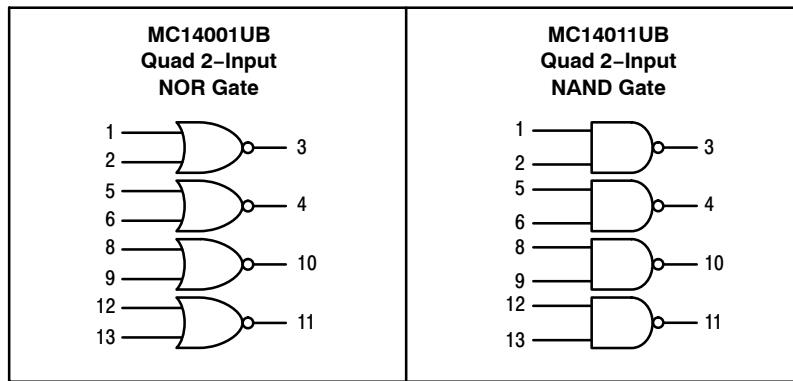
xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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LOGIC DIAGRAMS



V_{DD} = PIN 14
 V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

MC14001UB
Quad 2-Input NOR Gate

IN 1 _A	1 •	14	V_{DD}
IN 2 _A	2	13	IN 2 _D
OUT _A	3	12	IN 1 _D
OUT _B	4	11	OUT _D
IN 1 _B	5	10	OUT _C
IN 2 _B	6	9	IN 2 _C
V_{SS}	7	8	IN 1 _C

MC14011UB
Quad 2-Input NAND Gate

IN 1 _A	1 •	14	V_{DD}
IN 2 _A	2	13	IN 2 _D
OUT _A	3	12	IN 1 _D
OUT _B	4	11	OUT _D
IN 1 _B	5	10	OUT _C
IN 2 _B	6	9	IN 2 _C
V_{SS}	7	8	IN 1 _C

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} V _{dc}	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
		10	–	0.05	–	0	0.05	–	0.05		
		15	–	0.05	–	0	0.05	–	0.05		
	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–		
		10	9.95	–	9.95	10	–	9.95	–		
		15	14.95	–	14.95	15	–	14.95	–		
Input Voltage "0" Level (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	V _{IL}	5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc	
		10	–	2.0	–	4.50	2.0	–	2.0		
		15	–	2.5	–	6.75	2.5	–	2.5		
	V _{IH}	5.0	4.0	–	4.0	2.75	–	4.0	–		
		10	8.0	–	8.0	5.50	–	8.0	–		
		15	12.5	–	12.5	8.25	–	12.5	–		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	–1.0	–	–0.75	–1.7	–	–0.55	–	mAdc
		5.0	–0.25	–	–	–0.2	–0.36	–	–0.14	–	
		10	–0.62	–	–	–0.4	–0.9	–	–0.15	–	
		15	–1.8	–	–	–1.5	–3.5	–	–1.0	–	
	Sink	I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	
		10	1.6	–	–	1.1	2.25	–	0.7	–	
		15	4.2	–	–	3.4	8.8	–	2.4	–	
Input Current	I _{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate C _L = 50 pF)	I _T	5.0	I _T = (0.3 μA/kHz) f + I _{DD} /N						μAdc		
		10	I _T = (0.6 μA/kHz) f + I _{DD} /N								
		15	I _T = (0.8 μA/kHz) f + I _{DD} /N								

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μH (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ (Note 6)	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	t _{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 30 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 22 ns t _{PLH} , t _{PHL} = (0.50 ns/pF) C _L + 15 ns	t _{PLH} , t _{PHL}	5.0 10 15	– – –	90 50 40	180 100 80	ns

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

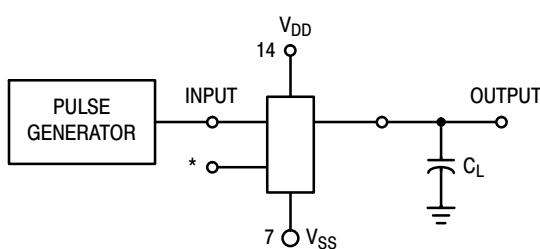
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ORDERING INFORMATION

Device	Package	Shipping [†]
MC14001UBCPG	PDIP-14 (Pb-Free)	25 Units / Rail
MC14001UBDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14001UBDG*		
MC14001UBDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14001UBDR2G*		
MC14011UBCPG	PDIP-14 (Pb-Free)	25 Units / Rail
NLV14011UBCPG*		
MC14011UBDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14011UBDG*		
MC14011UBDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14011UBDR2G*		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

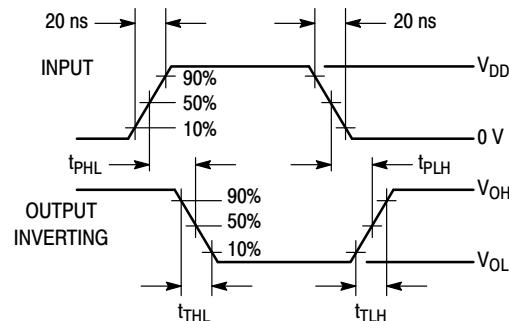
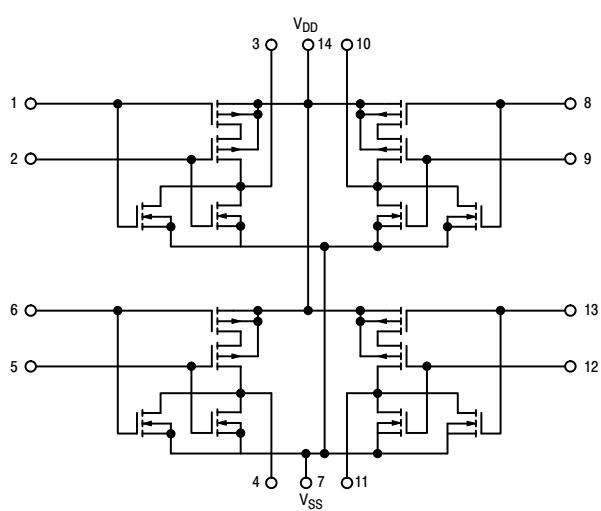


Figure 1. Switching Time Test Circuit and Waveforms

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MC14001UB CIRCUIT SCHEMATIC



MC14011UB CIRCUIT SCHEMATIC (1/4 of Device Shown)

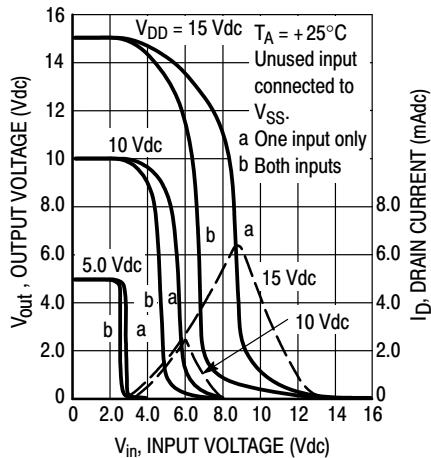
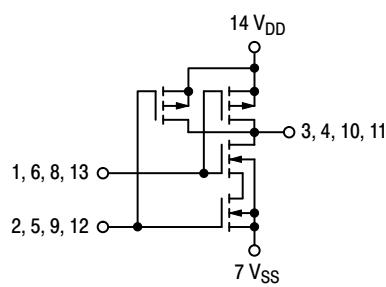


Figure 2. Typical Voltage and Current Transfer Characteristics

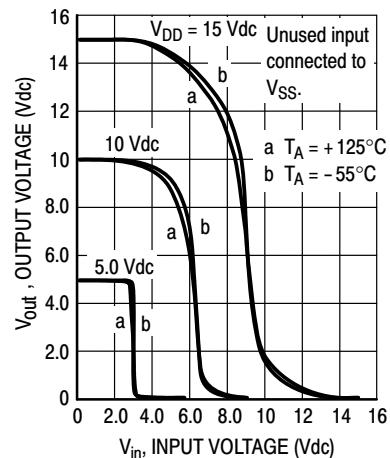


Figure 3. Typical Voltage Transfer Characteristics versus Temperature

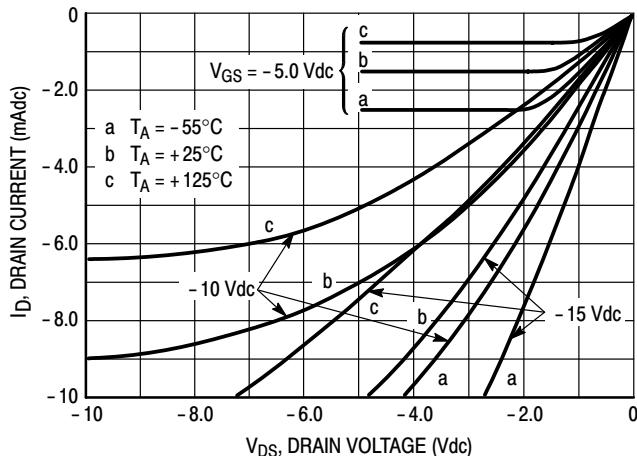


Figure 4. Typical Output Source Characteristics

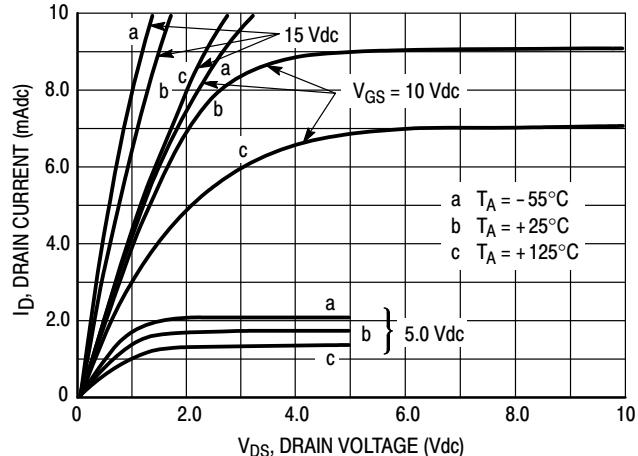
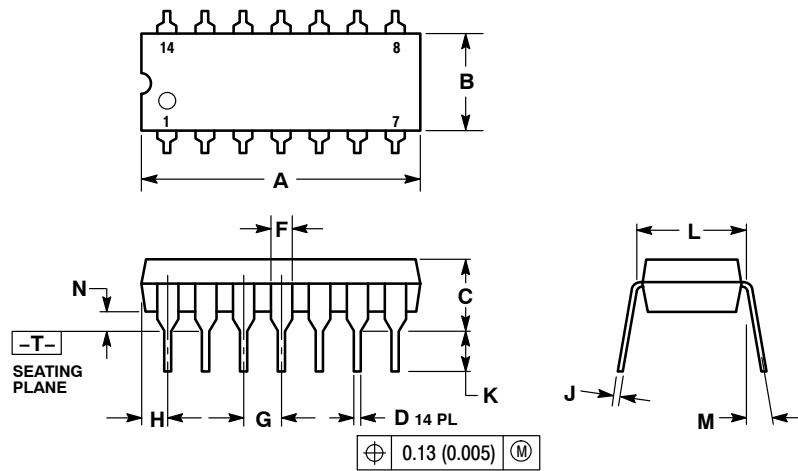


Figure 5. Typical Output Sink Characteristics

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

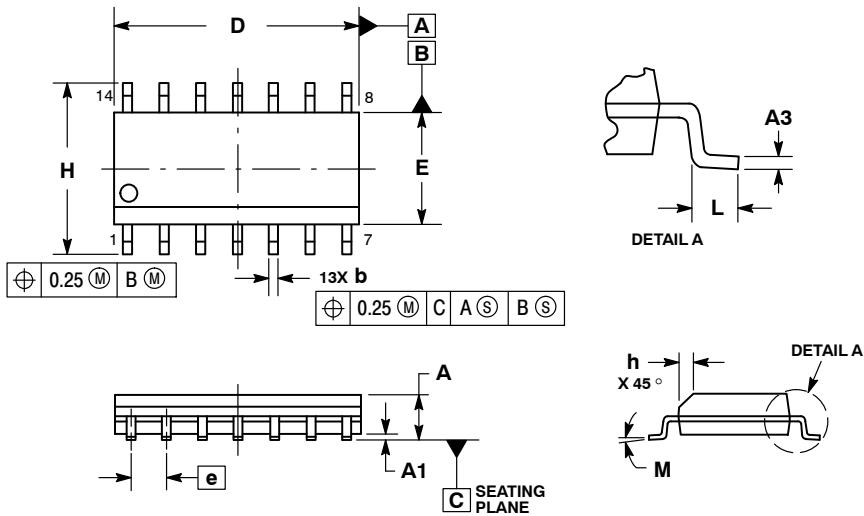
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100	BSC	2.54	BSC
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

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PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K

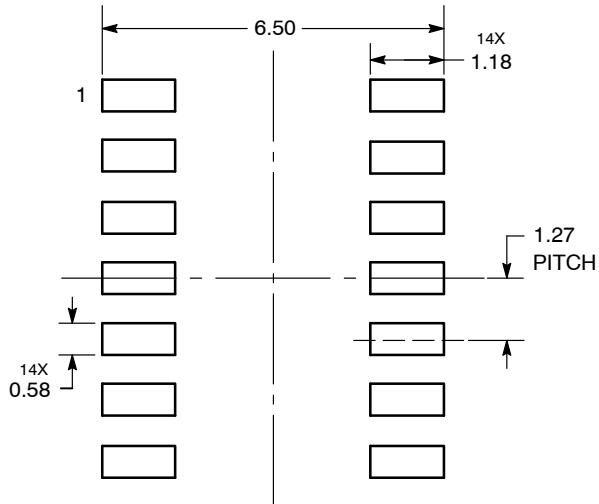


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
<i>A</i>	1.35	1.75	0.054	0.068
<i>A</i> 1	0.10	0.25	0.004	0.010
<i>A</i> 3	0.19	0.25	0.008	0.010
<i>b</i>	0.35	0.49	0.014	0.019
<i>D</i>	8.55	8.75	0.337	0.344
<i>E</i>	3.80	4.00	0.150	0.157
<i>e</i>	1.27 BSC		0.050 BSC	
<i>H</i>	5.80	6.20	0.228	0.244
<i>h</i>	0.25	0.50	0.010	0.019
<i>L</i>	0.40	1.25	0.016	0.049
<i>M</i>	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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