



# μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

## General Description

The MAX6323/MAX6324 microprocessor (μP) supervisory circuits monitor power supplies and μP activity in digital systems. A watchdog timer looks for activity outside an expected window of operation. Six laser-trimmed reset thresholds are available with  $\pm 2.5\%$  accuracy from +2.32V to +4.63V. Valid  $\overline{\text{RESET}}$  output is guaranteed down to  $V_{CC} = +1.2\text{V}$ .

The  $\overline{\text{RESET}}$  output is either push-pull (MAX6323) or open-drain (MAX6324).  $\overline{\text{RESET}}$  is asserted low when  $V_{CC}$  falls below the reset threshold, or when the manual reset input ( $\overline{\text{MR}}$ ) is asserted low.  $\overline{\text{RESET}}$  remains asserted for at least 100ms after  $V_{CC}$  rises above the reset threshold and  $\overline{\text{MR}}$  is deasserted.

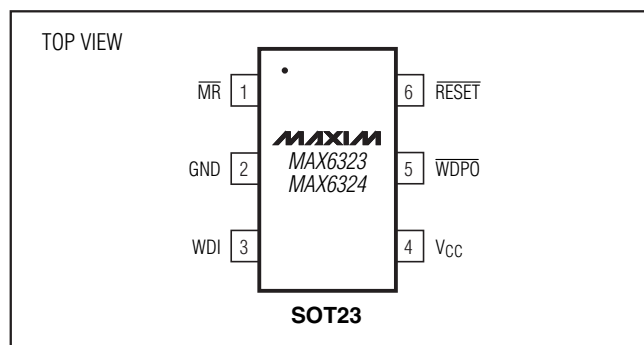
The watchdog pulse output ( $\overline{\text{WDPO}}$ ) utilizes an open-drain configuration. It can be triggered either by a fast timeout fault (watchdog input pulses are too close to each other) or a slow timeout fault (no watchdog input pulse is observed within the timeout period). The watchdog timeout is measured from the last falling edge of watchdog input (WDI) with a minimum pulse width of 300ns.  $\overline{\text{WDPO}}$  is asserted for 1ms when a fault is observed. Eight laser-trimmed timeout periods are available.

The MAX6323/MAX6324 are offered in a 6-pin SOT23 package and operate over the extended temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ).

## Applications

Automotive  
Industrial  
Medical  
Embedded Control Systems

## Pin Configuration



Typical Operating Circuit appears at end of data sheet.

## Features

- ◆ Min/Max (Windowed) Watchdog, 8 Factory-Trimmed Timing Options
- ◆ Pulsed Open-Drain, Active-Low Watchdog Output
- ◆ Power-On Reset
- ◆ Precision Monitoring of +2.5V, +3.0V, +3.3V, and +5.0V Power Supplies
- ◆ Open-Drain or Push-Pull  $\overline{\text{RESET}}$  Outputs
- ◆ Low-Power Operation (23μA typ)
- ◆ Debounced Manual Reset Input
- ◆ Guaranteed Reset Valid to  $V_{CC} = +1.2\text{V}$

## Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE	RESET OUTPUT
MAX6323_UT__-T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6 SOT23-6	Push-Pull
MAX6324_UT__-T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6 SOT23-6	Open Drain

\*These devices are factory trimmed to one of eight watchdog-timeout windows and one of six reset voltage thresholds. Insert the letter corresponding to the desired watchdog-timeout window (A, B, C, D, E, F, G, or H) into the blank following the number 6323 or 6324 (see Watchdog Timeout table). Insert the two-digit code (46, 44, 31, 29, 26, or 23) after the letters UT for the desired nominal reset threshold (see Reset Threshold Range table at end of data sheet).

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing “-T” with “+T” when ordering.

**Note:** There are eight standard versions of each device available (see Standard Versions table). Sample stock is generally held on standard versions only. Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.

## Watchdog Timeout

WATCHDOG TIMEOUT*				
SUFFIX	FAST		SLOW	
	MAX	UNITS	MIN	UNITS
A	1.5	ms	10	ms
B	15	ms	100	
C	15	ms	300	
D	15	ms	10	s
E	15	ms	60	
F	23	ms	47	ms
G	39	ms	82	
H	719	ms	1.3	s

\*See Figure 1 for operation.



Maxim Integrated Products 1

**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

MAX6323/MAX6324

# μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

$V_{CC}$  ..... -0.3V to +6.0V  
 $\overline{MR}$ ,  $\overline{RESET}$  (MAX6323),  $\overline{WDI}$  ..... -0.3V to ( $V_{CC}$  + +0.3V)  
 $\overline{WDPO}$ ,  $\overline{RESET}$  (MAX6324) ..... -0.3V to +6.0V  
 Input Current,  $V_{CC}$ ,  $\overline{WDI}$ ,  $\overline{MR}$  ..... 20mA  
 Output Current,  $\overline{RESET}$ ,  $\overline{WDPO}$  ..... 20mA  
 Rate of Rise,  $V_{CC}$  ..... 100V/μs

Continuous Power Dissipation ( $T_A$  = +70°C)

6-Pin SOT23 (derate 8.7mW/°C above +70°C) ..... 696mW  
 Operating Temperature Range ..... -40°C to +125°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC}$  = full range,  $T_A$  = -40°C to +125°C, unless otherwise noted. Typical values are at  $V_{CC}$  = 3V,  $T_A$  = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	$V_{CC}$		1.2		5.5	V
Supply Current	$I_{CC}$	No load, $\overline{RESET}$ deasserted	$V_{CC}$ = 2.5V or 3.3V		23	μA
			$V_{CC}$ = 5.5V		27	
Reset Threshold Voltage	$V_{TH}$	MAX632_ _UT46	4.50	4.63	4.75	V
		MAX632_ _UT44	4.25	4.38	4.50	
		MAX632_ _UT31	3.00	3.08	3.15	
		MAX632_ _UT29	2.85	2.93	3.00	
		MAX632_ _UT26	2.55	2.63	2.70	
		MAX632_ _UT23	2.25	2.32	2.38	
Reset Timeout Delay	$t_{RP}$	$\overline{RESET}$ deasserted	100	180	280	ms
$V_{CC}$ to $\overline{RESET}$ Delay		10mV/ms, $V_{TH}$ +100mV to $V_{TH}$ -100mV		20		μs
$\overline{WDPO}$ , $\overline{RESET}$ Output Voltage	$V_{OL}$	$I_{SINK}$ = 1.2mA, $V_{CC}$ = 2.25V (MAX632_ _UT23, MAX632_ _UT26, MAX632_ _UT29, MAX632_ _UT31)			0.4	V
		$I_{SINK}$ = 3.2mA, $V_{CC}$ = 4.25V (MAX632_ _UT44, MAX632_ _UT46)			0.4	
		$I_{SINK}$ = 100μA, $V_{CC}$ > 1.2V, $\overline{RESET}$ asserted			0.4	
$\overline{RESET}$ Output Voltage (MAX6323)	$V_{OH}$	$I_{SOURCE}$ = 500μA, $V_{CC}$ = 3.15V, $\overline{RESET}$ deasserted (MAX632_ _UT23, MAX632_ _UT26, MAX632_ _UT29, MAX632_ _UT31)	0.8 × $V_{CC}$			V
		$I_{SOURCE}$ = 800μA, $V_{CC}$ = 4.75V, $\overline{RESET}$ deasserted, (MAX632_ _UT44, MAX632_ _UT46)	$V_{CC}$ - 1.5			
$\overline{WDPO}$ , $\overline{RESET}$ Output Leakage	$I_{LKG}$	$V_{\overline{RESET}} = V_{\overline{WDPO}} = +5.5V$ , $\overline{RESET}$ , $\overline{WDPO}$ deasserted			1	μA

# μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

MAX6323/MAX6324

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = full range, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = 3V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG INPUT AND OUTPUT						
Watchdog Timeout (Fast) (Notes 2, 3)	tWD1	MAX632_AUT_ _	1		1.5	ms
		MAX632_BUT_ _	10		15	
		MAX632_CUT_ _	10		15	
		MAX632_DUT_ _	10		15	
		MAX632_EUT_ _	10		15	
		MAX632_FUT_ _	17		23	
		MAX632_GUT_ _	29		39	
		MAX632_HUT_ _	543		719	
Watchdog Timeout (Slow) (Note 4)	tWD2	MAX632_AUT_ _	10		15	ms
		MAX632_BUT_ _	100		150	
		MAX632_CUT_ _	300		450	
		MAX632_DUT_ _	10		15	s
		MAX632_EUT_ _	60		90	
		MAX632_FUT_ _	47		63	ms
		MAX632_GUT_ _	82		108	
		MAX632_HUT_ _	1.3		1.8	s
Minimum Watchdog Input Pulse Width			300			ns
WDI Glitch Immunity		VCC = 5.5V		100		ns
WDI Input Voltage	VIH		0.75 x VCC			V
	VIL		0.8			
WDI Input Current		WDI = 0	-1.5	-1		μA
		WDI = VCC		1	1.5	
WDPO Pulse Width		VIL = 0.8V, VIH = 0.75V x VCC	0.5	1	3	ms
MANUAL RESET INPUT						
MR Input Voltage	VIH		0.7 x VCC			V
	VIL		0.3 x VCC			
MR Minimum Pulse Width			1			μs
MR Glitch Immunity		VCC = 2.5V		100		ns
MR to Reset Delay		VCC = 2.5V		120		ns
MR Pullup Resistance			50	85		kΩ

**Note 1:** Devices are tested at T<sub>A</sub> = +25°C and guaranteed by design for T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, as specified.

**Note 2:** WDPO will pulse low if a falling edge is detected on WDI before this timeout period expires.

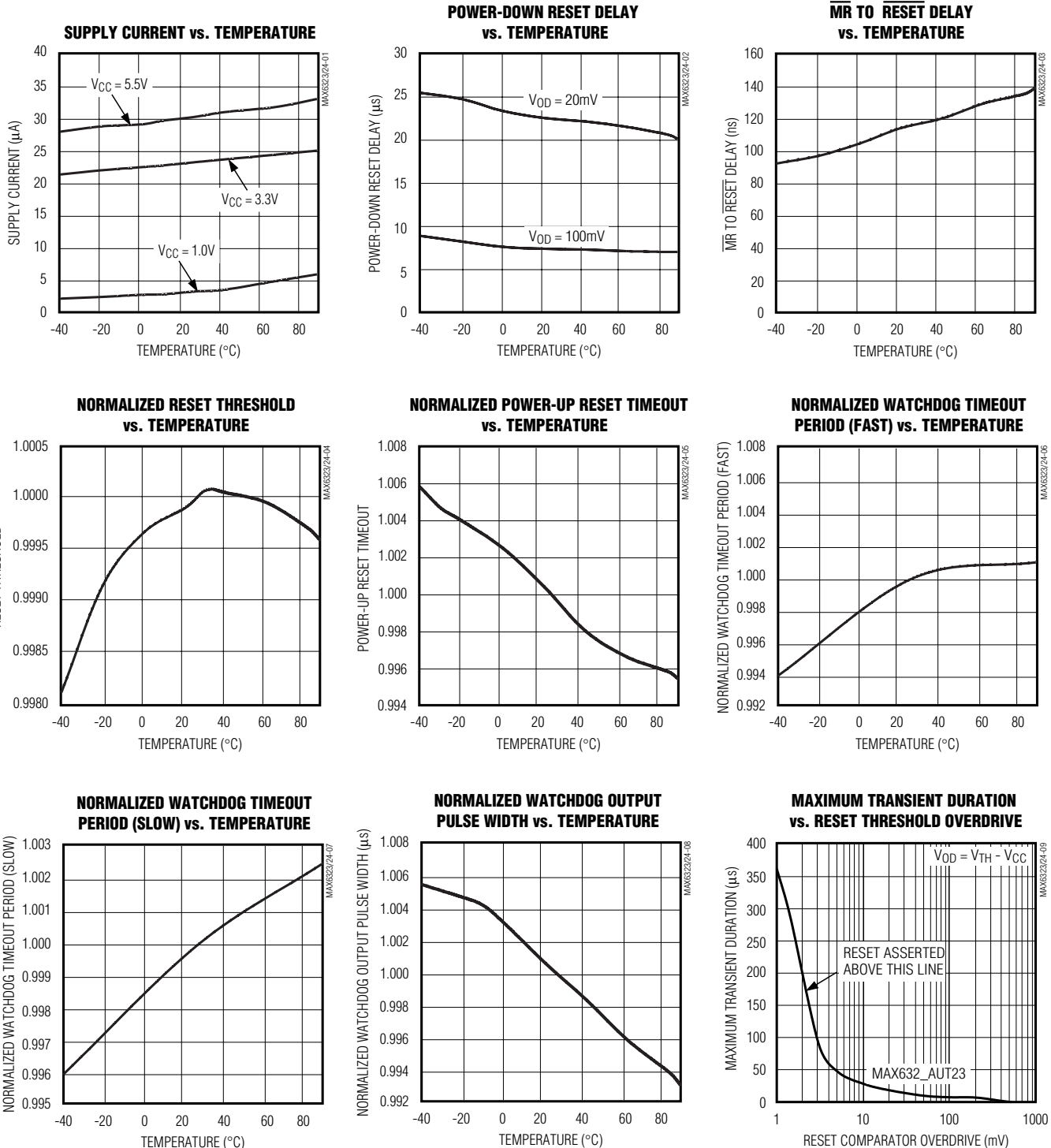
**Note 3:** To avoid a potential fake fault, the first WDI pulse after the rising edge of RESET or WDPO will not create a fast watchdog timeout fault.

**Note 4:** WDPO will pulse low if no falling edge is detected on WDI after this timeout period expires.

# **μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset**

## **Typical Operating Characteristics**

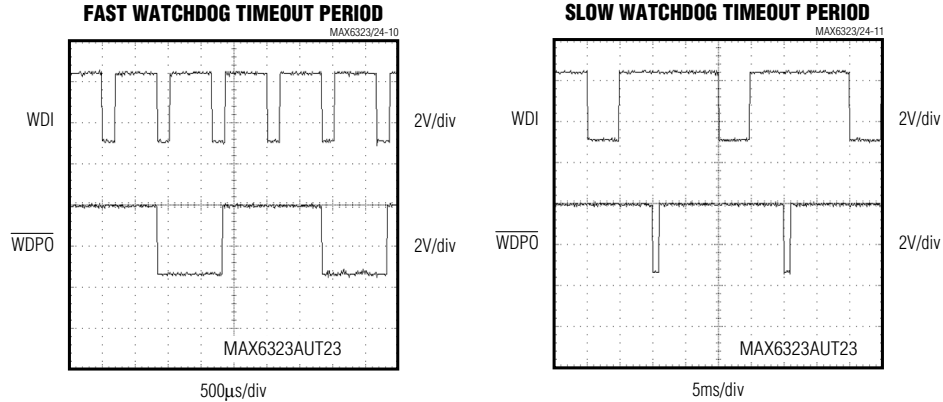
(V<sub>CC</sub> = full range, T<sub>A</sub> = +25°C, unless otherwise noted.)



# μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

## Typical Operating Characteristics (continued)

(V<sub>CC</sub> = full range, T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{MR}}$	Active-Low, Manual Reset Input. When $\overline{\text{MR}}$ is asserted low, $\overline{\text{RESET}}$ is asserted low, the internal watchdog timer is reset to zero, and $\overline{\text{WDPO}}$ is reset to high impedance (open drain). After the rising edge of $\overline{\text{MR}}$ , $\overline{\text{RESET}}$ is asserted for at least 100ms. Leave $\overline{\text{MR}}$ unconnected or connect to V <sub>CC</sub> if unused.
2	GND	Ground
3	WDI	Watchdog Input. The internal watchdog timer clears to zero on the falling edge of WDI or when $\overline{\text{RESET}}$ goes high. If WDI sees another falling edge within the factory-trimmed watchdog window, $\overline{\text{WDPO}}$ will remain unasserted. Transitions outside this window, either faster or slower, will cause $\overline{\text{WDPO}}$ to pulse low for 1ms (typ).
4	V <sub>CC</sub>	Supply Voltage for the Device. Input for V <sub>CC</sub> reset monitor. For noisy systems, bypass V <sub>CC</sub> with a 500pF (min) capacitor.
5	$\overline{\text{WDPO}}$	Watchdog Pulse Output. The open-drain $\overline{\text{WDPO}}$ output is pulsed low for 1ms (typ) upon detection of a fast or slow watchdog fault. $\overline{\text{WDPO}}$ is only active when $\overline{\text{RESET}}$ is high.
6	$\overline{\text{RESET}}$	Active-Low. Reset is asserted when V <sub>CC</sub> drops below V <sub>TH</sub> and remains asserted until V <sub>CC</sub> rises above V <sub>TH</sub> for the duration of the reset timeout period. The MAX6323 has a push-pull output and the MAX6324 has an open-drain output. Connect a pullup resistor from $\overline{\text{RESET}}$ to any supply voltage up to +6V.

# **$\mu$ P Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset**

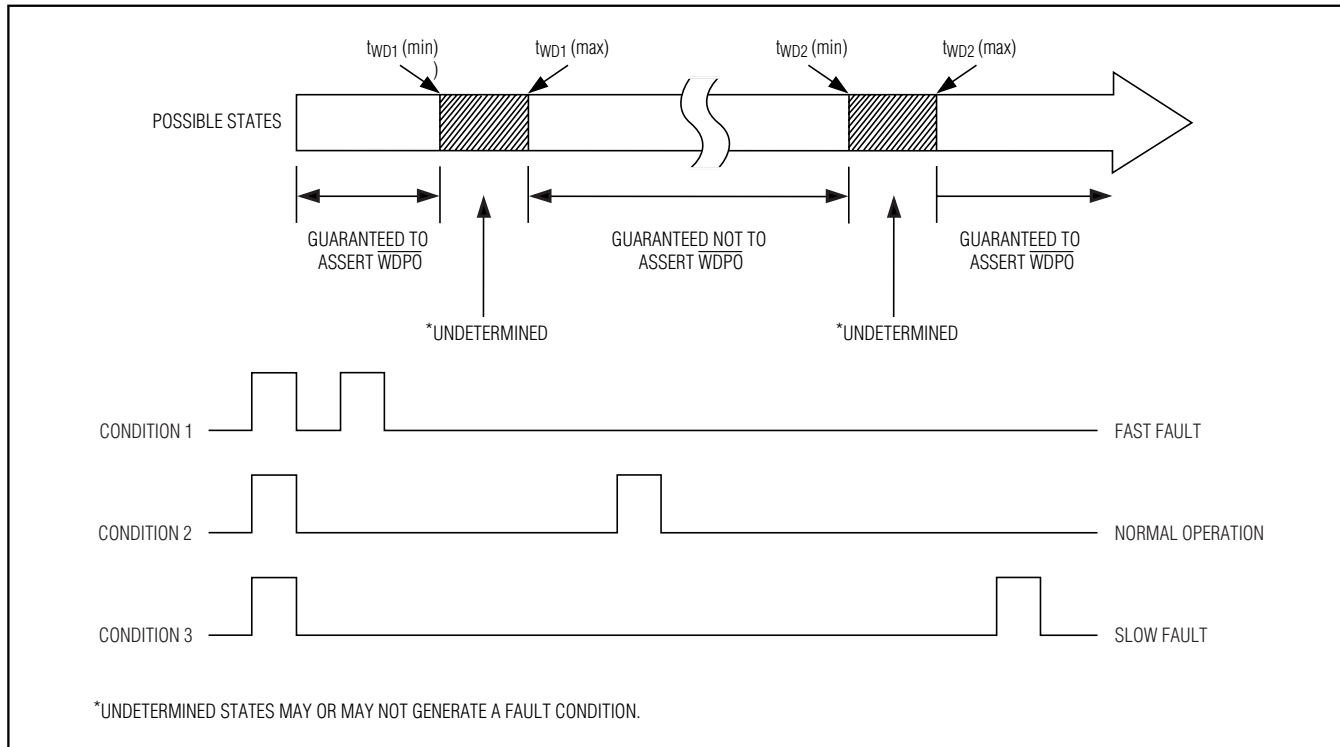


Figure 1. Detailed Watchdog Input Timing Relationship

## **Detailed Description**

The MAX6323/MAX6324  $\mu$ P supervisory circuits maintain system integrity by alerting the  $\mu$ P to fault conditions. In addition to a standard  $V_{CC}$  monitor (for power-on reset, brownout detect, and power-down reset), the devices include a sophisticated watchdog timer that detects when the processor is running outside an expected window of operation for a specific application. The watchdog signals a fault when the input pulses arrive too early (faster than the selected  $t_{WD1}$  timeout period) or too late (slower than the selected  $t_{WD2}$  timeout period) (Figure 1). Incorrect timing can lead to poor or dangerous system performance in tightly controlled operating environments. Incorrect timing could be the result of improper  $\mu$ P clocking or code execution errors. If a timing error occurs, the MAX6323/MAX6324 issue a watchdog pulse output, independent from the reset output, indicating that system maintenance may be required.

### **Watchdog Function**

A pulse on the watchdog output WDPO can be triggered by a fast fault or a slow fault. If the watchdog input (WDI) has two falling edges too close to each

other (faster than  $t_{WD1}$ ) (Figure 2) or falling edges that are too far apart (slower than  $t_{WD2}$ ) (Figure 3),  $\overline{WDPO}$  is pulsed low. Normal watchdog operation is displayed in Figure 4 ( $\overline{WDPO}$  is not asserted). The internal watchdog timer is cleared when a WDI falling edge is detected within the valid watchdog window or when the device's  $\overline{RESET}$  or  $\overline{WDPO}$  outputs are deasserted. All WDI input pulses are ignored while either  $\overline{RESET}$  or  $\overline{WDPO}$  is asserted. Figure 1 identifies the input timing regions where  $\overline{WDPO}$  fault outputs will be observed with respect to  $t_{WD1}$  and  $t_{WD2}$ . After  $\overline{RESET}$  or  $\overline{WDPO}$  deasserts, the first WDI falling edge is ignored for the fast fault condition (Figure 2).

Upon detecting a watchdog fault, the  $\overline{WDPO}$  output will pulse low for 1ms.  $\overline{WDPO}$  is an open-drain output. Connect a pullup resistor on  $\overline{WDPO}$  to any supply up to +6V.

### **VCC Reset**

The MAX6323/MAX6324 also include a standard  $V_{CC}$  reset monitor to ensure that the  $\mu$ P is started in a known state and to prevent code execution errors during power-up, power-down, or brownout conditions.  $\overline{RESET}$  is asserted whenever the  $V_{CC}$  supply voltage

# **$\mu$ P Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset**

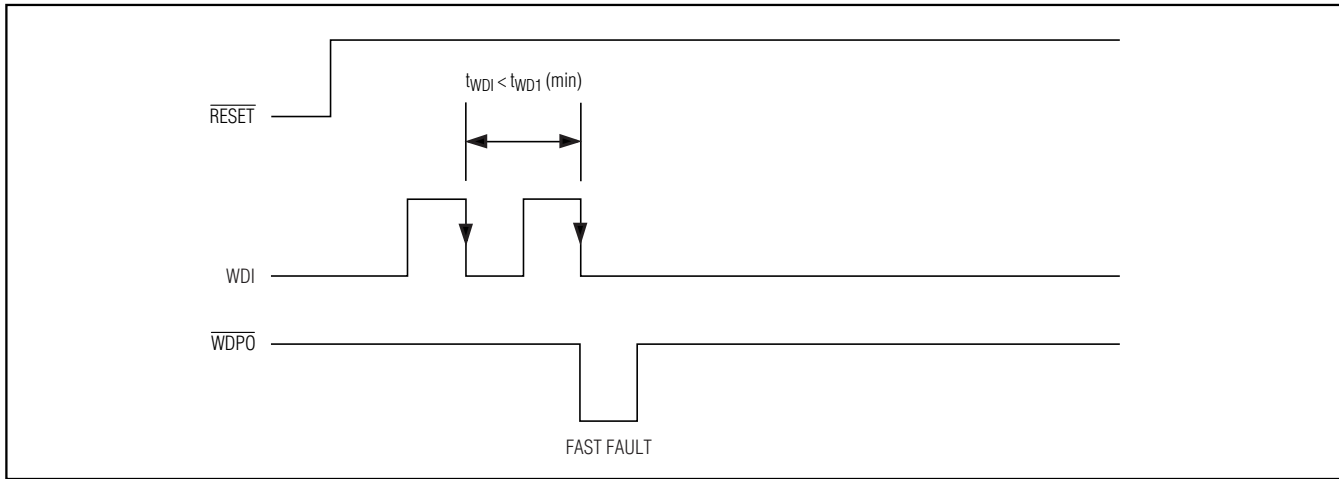


Figure 2. Fast Fault Timing

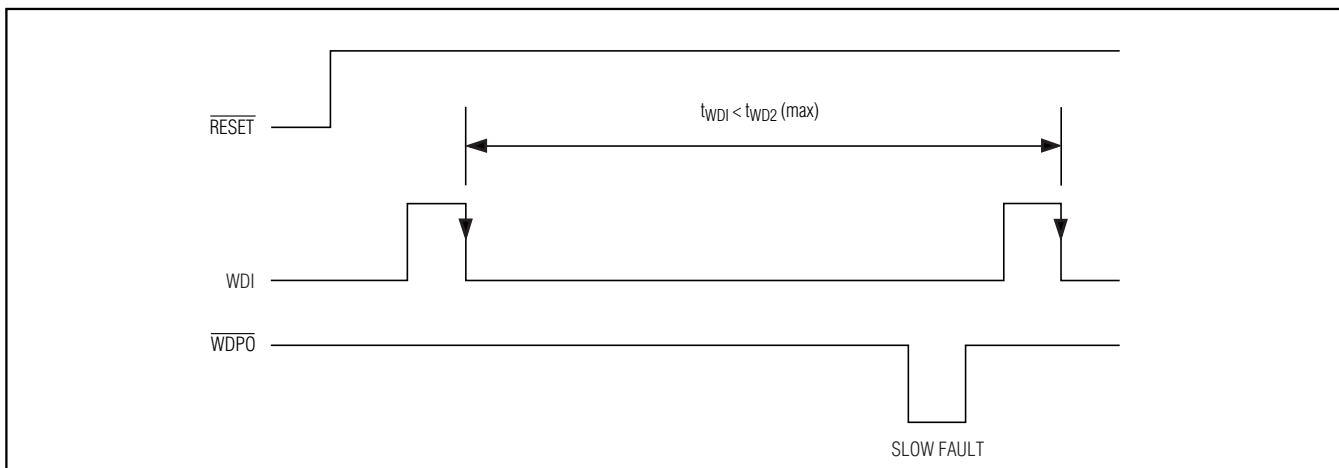
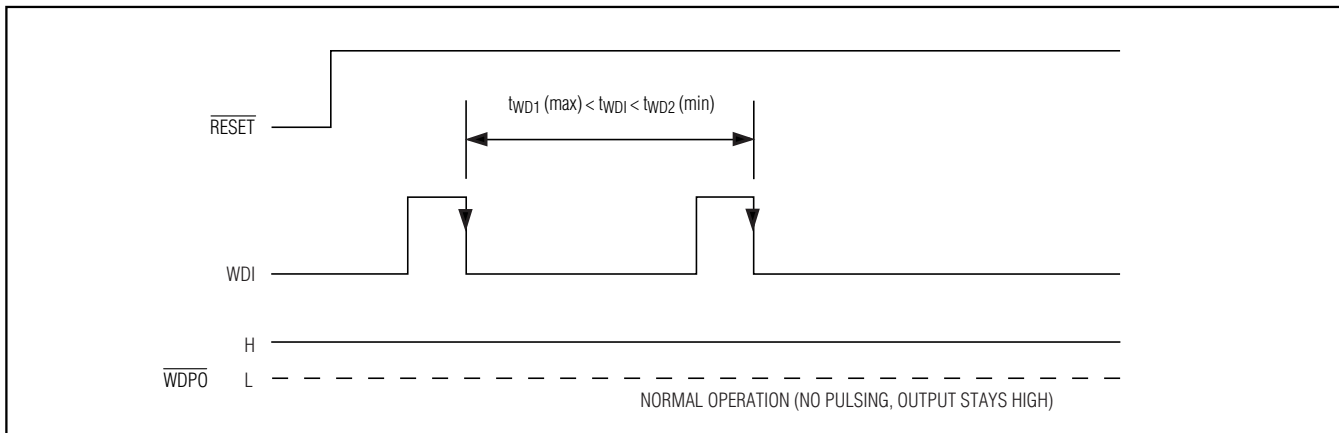


Figure 3. Slow Fault Timing

Figure 4. Normal Operation,  $\overline{\text{WDPO}}$  Not Asserted

# **μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset**

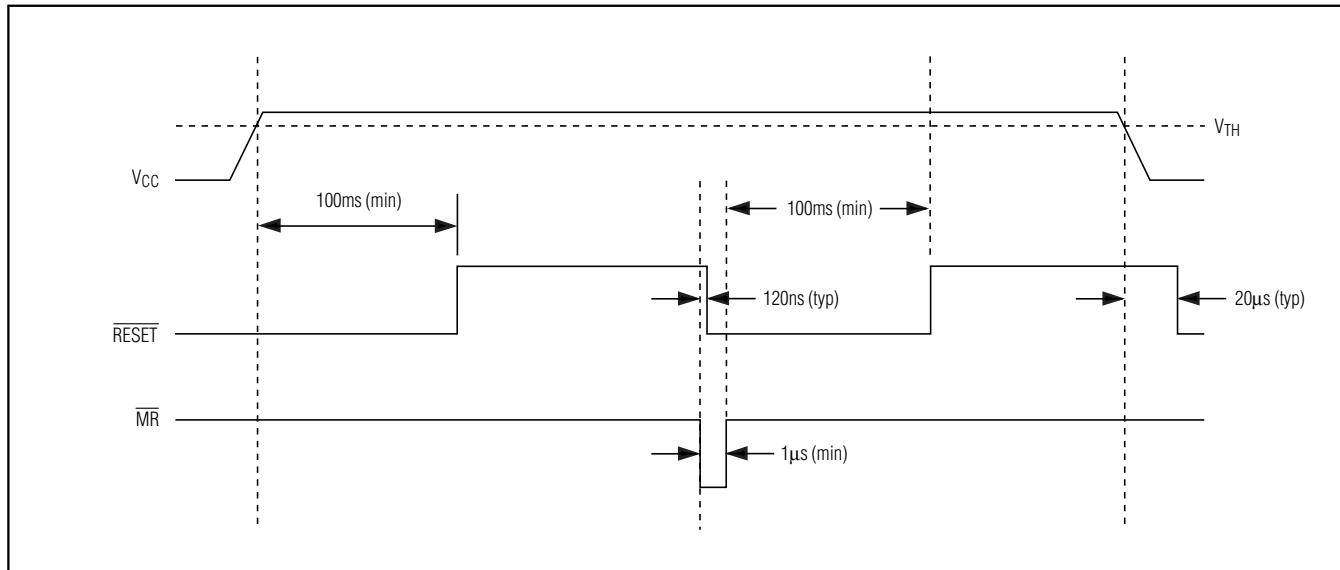


Figure 5.  $\overline{\text{RESET}}$  Timing Relationship

falls below the preset threshold or when the manual reset input ( $\overline{\text{MR}}$ ) is asserted. The  $\overline{\text{RESET}}$  output remains asserted for at least 100ms after  $V_{CC}$  has risen above the reset threshold and  $\overline{\text{MR}}$  is deasserted (Figure 5). For noisy environments, bypass  $V_{CC}$  with a 500pF (min) capacitor to ensure correct operation.

The MAX6323 has a push-pull output stage, and the MAX6324 utilizes an open-drain output. Connect a pull-up resistor on the  $\overline{\text{RESET}}$  output of the MAX6324 to any supply up to +6V. Select a resistor value large enough to register a logic low (see *Electrical Characteristics*) and small enough to register a logic high while supplying all input leakage currents and leakage paths connected to the  $\overline{\text{RESET}}$  line. A 10k $\Omega$  pullup is sufficient in most applications.

## **Manual Reset Input**

Many  $\mu\text{P}$ -based products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input ( $\overline{\text{MR}}$ ) can connect directly to a switch without an external pullup resistor or debouncing network.  $\overline{\text{MR}}$  is internally pulled up to  $V_{CC}$  and, therefore, can be left unconnected if unused.  $\overline{\text{MR}}$  is designed to reject fast, negative-going transients (typically 100ns pulses), and it must be held low for a minimum of 1 $\mu\text{s}$  to assert the reset output (Figure 5). A 0.1 $\mu\text{F}$  capacitor from  $\overline{\text{MR}}$  to ground provides additional noise immunity. After  $\overline{\text{MR}}$  transitions from low to high, reset will remain asserted for the duration of the reset timeout period, at least 100ms.

## **Applications Information**

### **Negative-Going $V_{CC}$ Transients**

The MAX6323/MAX6324 are relatively immune to short-duration negative-going  $V_{CC}$  transients (glitches), which usually do not require the entire system to shut down. Typically, 200ns large-amplitude pulses (from ground to  $V_{CC}$ ) on the supply will not cause a reset. Lower amplitude pulses result in greater immunity. Typically, a  $V_{CC}$  transient that falls 100mV below the reset threshold and lasts less than 20 $\mu\text{s}$  will not trigger a reset (see *Typical Operating Characteristics*). An optional 0.1 $\mu\text{F}$  bypass capacitor mounted close to  $V_{CC}$  provides additional transient immunity.

### **Ensuring a Valid Reset Output Down to $V_{CC} = 0$**

When  $V_{CC}$  falls below +1.2V, the MAX6323  $\overline{\text{RESET}}$  output no longer sinks current; it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to  $\overline{\text{RESET}}$  can drift to undetermined voltages. This does not present a problem in most applications, since most  $\mu\text{Ps}$  and other circuitry are inoperative with  $V_{CC}$  below +1.2V. However, in applications where  $\overline{\text{RESET}}$  must be valid down to 0, adding a pulldown resistor to  $\overline{\text{RESET}}$  causes any stray leakage currents to flow to ground, holding  $\overline{\text{RESET}}$  low (Figure 6). R1's value is not critical; 100k $\Omega$  is large enough not to load  $\overline{\text{RESET}}$  and small enough to pull  $\overline{\text{RESET}}$  to ground. This scheme does not work with the open-drain output of the MAX6324.



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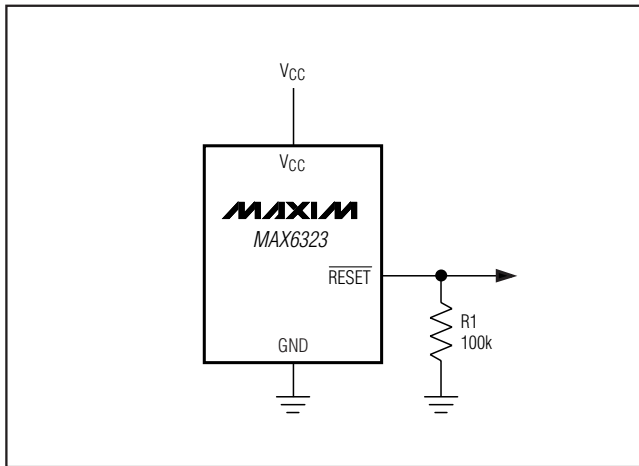


Figure 6.  $\overline{\text{RESET}}$  Valid to  $V_{CC}$  = Ground Circuit

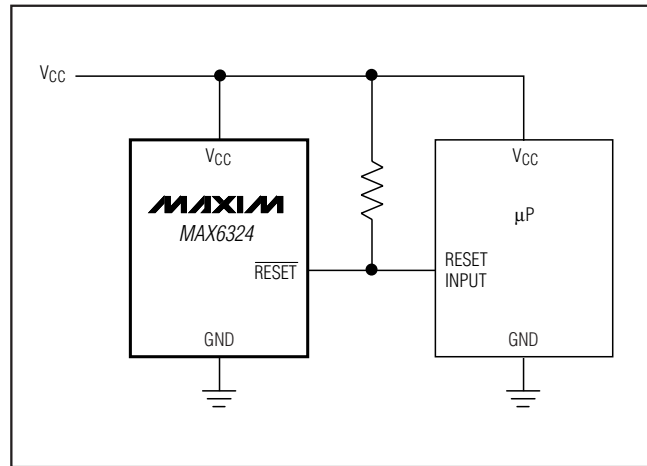


Figure 7. Interfacing to  $\mu\text{Ps}$  with Bidirectional Reset Pins

## Interfacing to $\mu\text{Ps}$ with Bidirectional Reset Pins

Since the  $\overline{\text{RESET}}$  output on the MAX6324 is open-drain, this device easily interfaces with  $\mu\text{Ps}$  that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the  $\mu\text{P}$  supervisor's  $\overline{\text{RESET}}$  output directly to the microcontroller's ( $\mu\text{C}$ 's)  $\overline{\text{RESET}}$  pin with a single pullup resistor allows either device to assert reset (Figure 7).

### MAX6324 Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Generally, the pullup resistor connected to the MAX6324 will connect to the supply voltage that is being monitored at the IC's  $V_{CC}$  pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 8). Keep in mind that as the MAX6324's  $V_{CC}$  decreases below +1.2V, so does the IC's ability to sink current at  $\overline{\text{RESET}}$ . Also, with any pull-up resistor,  $\overline{\text{RESET}}$  will be pulled high as  $V_{CC}$  decays toward 0. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

### Watchdog Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This

technique avoids a "stuck" loop in which the watchdog time would continue to be reset within the loop, keeping the watchdog from timing out.

Figure 9 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog time is allowed to time out, causing a reset or interrupt to be issued.

### $\overline{\text{WDPO}}$ to $\overline{\text{MR}}$ Loopback

An error detected by the watchdog often indicates that a problem has occurred in the  $\mu\text{P}$  code execution. This could be a stalled instruction or a loop from which the processor cannot free itself. If the  $\mu\text{P}$  will still respond to a nonmaskable input (NMI), the processor can be redirected to the proper code sequence by connecting the  $\overline{\text{WDPO}}$  output to an NMI input. Internal RAM data should not be lost, but it may have been contaminated by the same error that caused the watchdog to time out.

If the processor will not recognize NMI inputs, or if the internal data is considered potentially corrupted when a watchdog error occurs, the processor should be restarted with a reset function. To obtain proper reset timing characteristics, the  $\overline{\text{WDPO}}$  output should be connected to the  $\overline{\text{MR}}$  input, and the  $\overline{\text{RESET}}$  output should

# μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

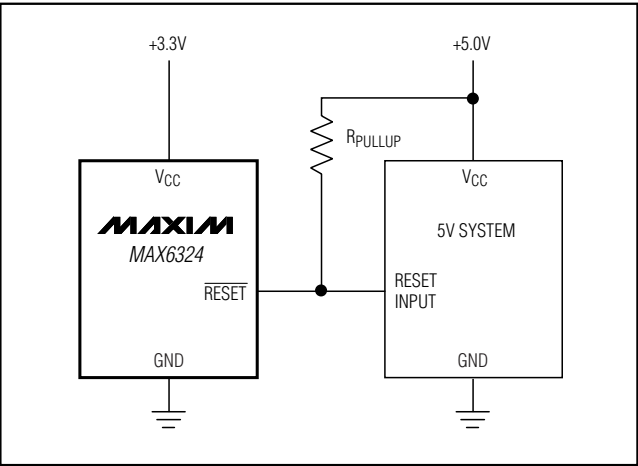


Figure 8. MAX6324 Open-Drain  $\overline{\text{RESET}}$  Output Allows Use with Multiple Supplies

drive the  $\mu\text{P}$   $\overline{\text{RESET}}$  input (Figure 10). The short 1ms  $\overline{\text{WDPO}}$  pulse output will assert the manual reset input and force the  $\overline{\text{RESET}}$  output to assert for the full reset timeout period (100ms min). All internal RAM data is lost during the reset period, but the processor is guaranteed to begin in the proper operating state.

### Standard Versions

MAX6323AUT29	MAX6324AUT29
MAX6323AUT46	MAX6324AUT46
MAX6323CUT29	MAX6324BUT29
MAX6323CUT46	MAX6324BUT46
MAX6323DUT29	MAX6324EUT29
MAX6323DUT46	MAX6324EUT46
MAX6323HUT29	MAX6324HUT29
MAX6323HUT46	MAX6324HUT46

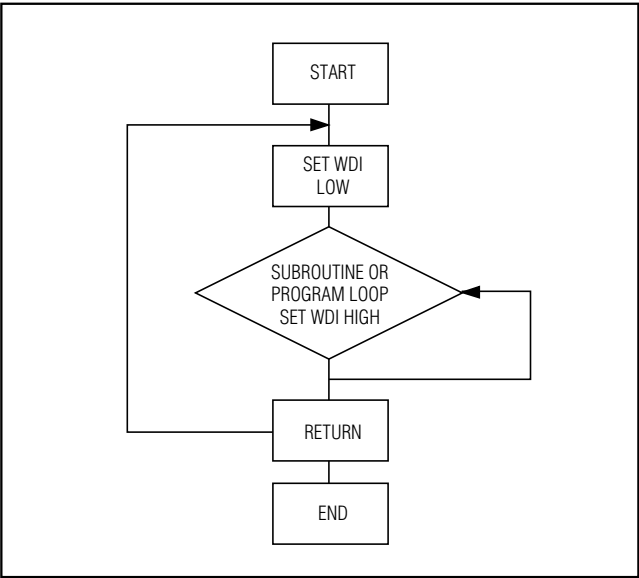


Figure 9. Watchdog Flow Diagram

### Reset Threshold Range (-40°C to +125°C)

SUFFIX	MIN	TYP	MAX	UNITS
46	4.50	4.63	4.75	V
44	4.25	4.38	4.50	
31	3.00	3.08	3.15	
29	2.85	2.93	3.00	
26	2.55	2.63	2.70	
23	2.25	2.32	2.38	

### Chip Information

TRANSISTOR COUNT: 1371  
PROCESS: BiCMOS

# **μP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset**

**MAX6323/MAX6324**

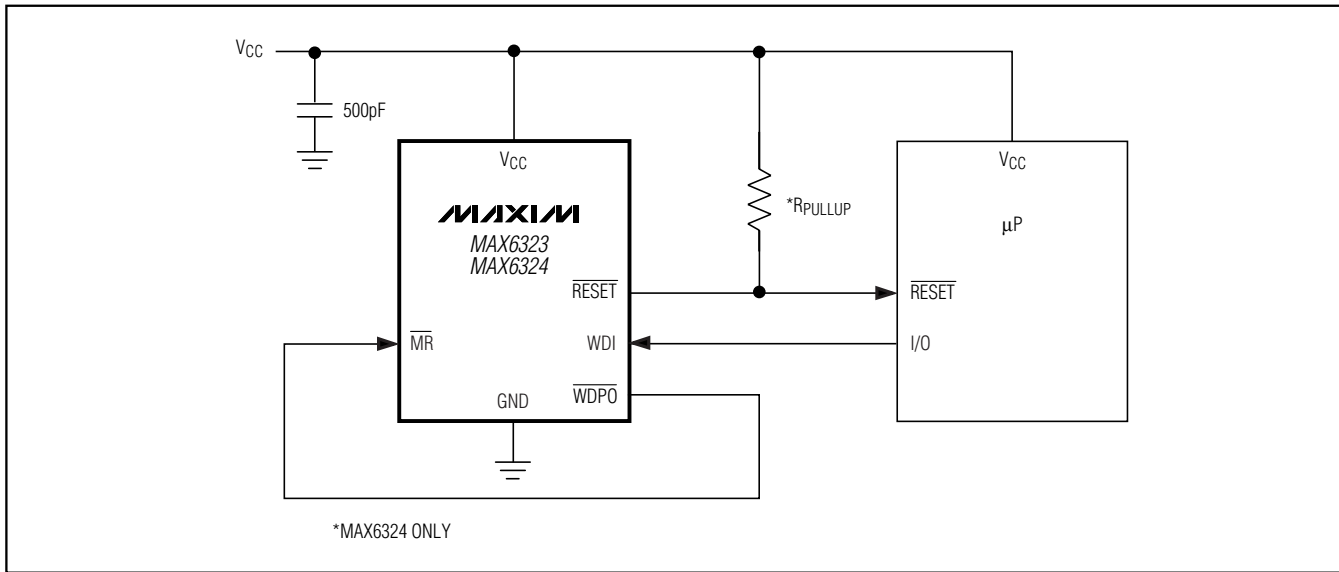
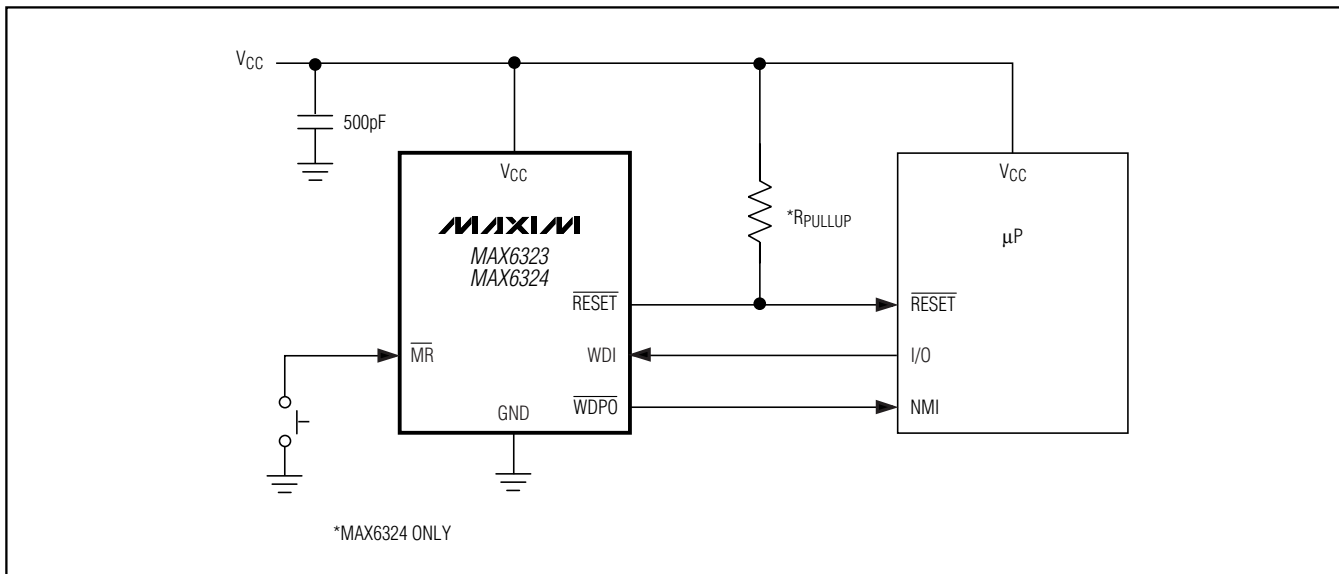


Figure 10.  $\overline{WDPO}$  to  $\overline{MR}$  Loopback Circuit

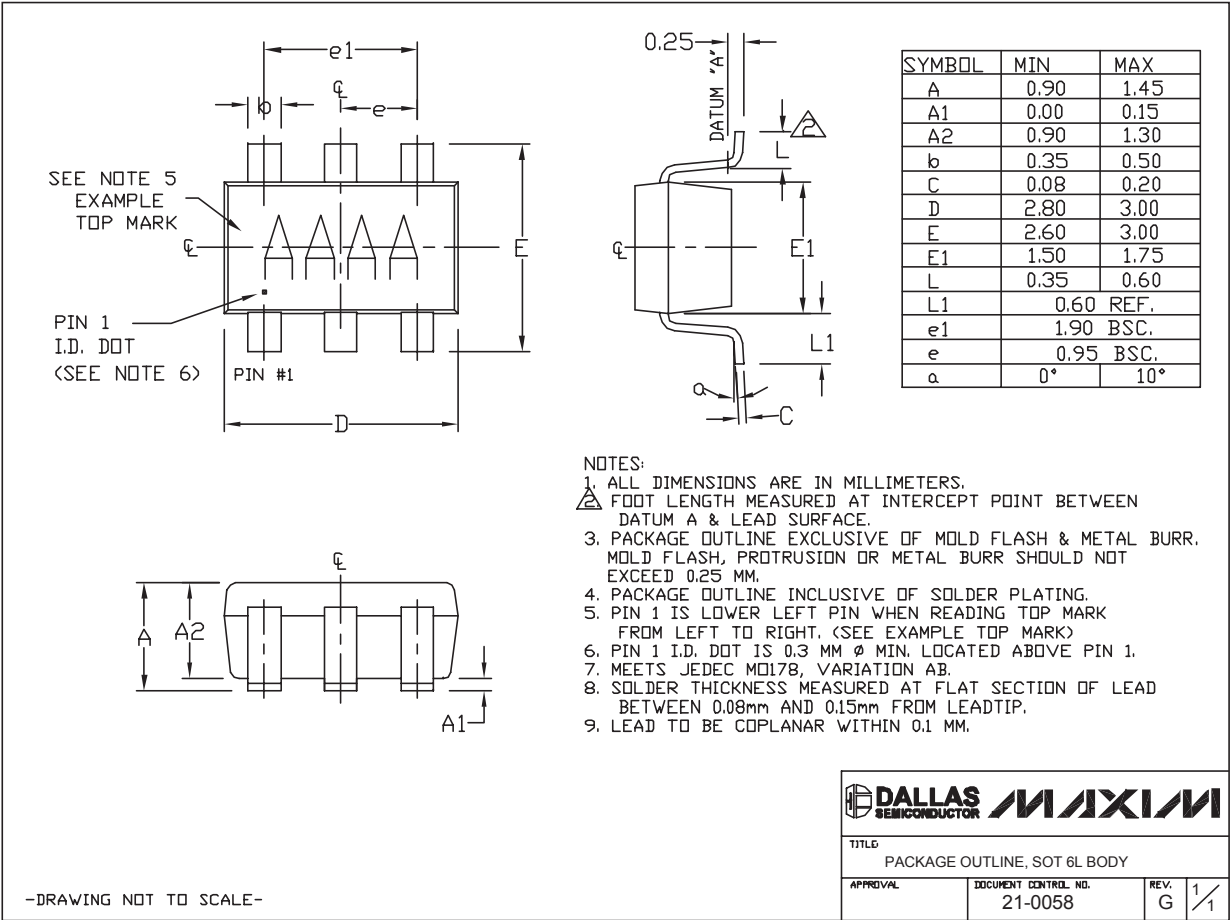
## **Typical Operating Circuit**



# µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-integrated.com/packages](http://www.maxim-integrated.com/packages).)



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