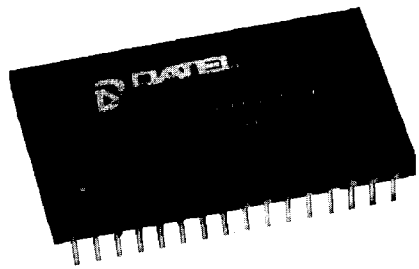
ADC-HC12B
12-Bit, Low-Power A/D Converter

FEATURES

- **Single supply operation**
- **Automatic standby mode control**
- **Low power consumption**
- **Six input ranges**
- **MIL temperature ranges available**



GENERAL DESCRIPTION

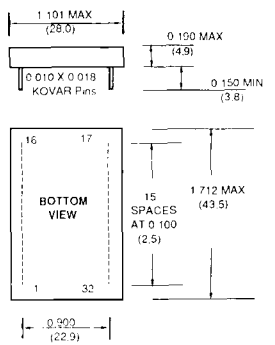
The ADC-HC is a complete, 12-bit, low-power, analog-to-digital converter utilizing CMOS technology. This hybrid IC incorporates active laser trimming of highly stable thin-film resistors to provide module performance with IC price, size and reliability.

The device is ideal for portable and remote applications such as seismology, oceanography, meteorology, and pollution monitoring. Other key applications include military and aerospace, requiring wide operating temperature ranges and high reliability.

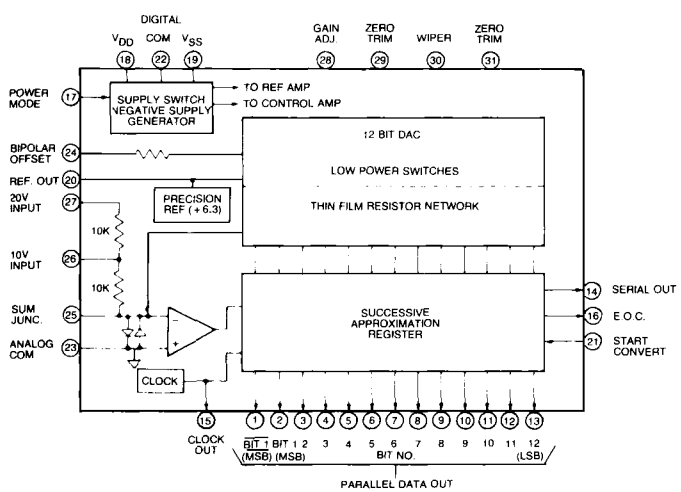
The ADC-HC converter can operate from either a single +9V dc to +15V dc power source (interrupt power mode) or from a ±9V dc to ±15V dc power source (continuous power mode) at a maximum conversion rate of 3.3 KHz.

A key feature of this unit when operating in the interrupt power mode is the extremely low quiescent power consumption (less than 10 μA at 12V, 25°C).

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE. ±0.01



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	17	POWER MODE
2	BIT 1 (MSB)	18	V_{DD}
3	BIT 2	19	V_{SS}
4	BIT 3	20	REF OUT
5	BIT 4	21	START CONVERT
6	BIT 5	22	DIGITAL COM
7	BIT 6	23	ANALOG COM
8	BIT 7	24	BIPOLAR OFFSET
9	BIT 8	25	SUM. JUNC
10	BIT 9	26	10V INPUT
11	BIT 10	27	20V INPUT
12	BIT 11	28	GAIN ADJ.
13	BIT 12 (LSB)	29	ZERO TRIM
14	SERIAL OUT	30	ZERO ADJ (WIPER)
15	CLOCK OUT	31	ZERO TRIM
16	E.O.C. (STATUS)	32	N.C.

ABSOLUTE MAXIMUM RATINGS	
Positive Supply (V_{DD})	+18V
Negative Supply (V_{SS})	−18V
Analog Inputs	±25V
Digital Inputs	0 to V_{DD}

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0 °C to +70 °C (BMC) -55 °C to +125 °C (BMM, BMM-QL)
Storage Temperature Range	−65 °C to +150 °C
Package Type	Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 g.)

FUNCTIONAL SPECIFICATIONS

Typical at 25 °C, ±12V, unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V, 0 to +20V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance	5K (0 to +5V, ±2.5V) 10K (0 to +10V, ±5V) 20K (0 to +20V, ±10V)
Start Convert, Interrupt Mode	Positive Pulse with duration of 50 microseconds minimum
Start Convert, Continuous Mode	Positive Pulse with duration of 5 microseconds minimum
V_{IL} (Logic "0")	0.3 V_{DD} maximum
V_{IH} (Logic "1")	0.7 V_{DD} minimum
Input Current	30 pA
Input Capacitance	15 pF

OUTPUTS	
Parallel Output Data	12 parallel lines of data, held until next conversion command
V_{OL} (Logic "0")	0V, −2.0 mA
V_{OH} (Logic "1")	V_{DD}, +4.0 mA
All Digital Outputs	CMOS Compatible
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary, 2's Complement
Serial Output	NRZ successive decision pulses out MSB first, Straight Binary or Offset Binary
Clock Output	Train of positive going (V_{DD}) 25 microseconds pulses, 40 kHz
E.O.C. (Status)	Conversion Status Signal, Logic "1" during reset and conversion, Logic "0" when conversion complete (data valid)

PERFORMANCE	
Resolution	12 Bits
Nonlinearity	±½ LSB maximum
Differential Nonlinearity	±½ LSB maximum
Gain Error	Adjust to zero
Offset or Zero Error	Adjust to zero
Gain Tempco	±30 ppm/°C maximum
Offset Tempco	±20 ppm/°C of FSR maximum
Zero Tempco	±10 ppm/°C of FSR
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR
No Missing Codes	Guaranteed over operating temperature range
Conversion Time	300 microseconds maximum
Throughput Time	305 microseconds maximum continuous power mode 350 microseconds maximum interrupt power mode
Power Supply Rejection	003%/% Supply

POWER REQUIREMENTS	
Continuous Power Mode	
V_{DD}	+9.0V to +15.0V
V_{SS}	−9.0V to −15.0V
Interrupt Power Mode V_{DD}	+9V to +15.0V
Power Consumption, Continuous Mode	165 mW typical, 200 mW maximum
Quiescent Mode	150 µW maximum, 15 µW typical

TECHNICAL NOTES

1. The ADC-HC contains CMOS components and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive foam or shorting all pins together with aluminum foil. Do not connect in circuit under "power on" conditions. Digital signals should be applied after the converter's power has been turned on.
2. For single supply (+12V nominal) or dual supply (±12V nominal) operation, bypass the power input pins to ground with a 0.1 µF ceramic capacitor. It is not critical that the supplies be balanced.
3. Analog and digital grounds should be kept separate whenever possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Common (Pin 23) and Digital Ground (Pin 22) are not connected internally and must be tied together externally.
4. The ADC-HC can operate from either a single or dual supply. When using dual supplies, tie POWER MODE (Pin 17) to V_{DD} (Pin 18). In this continuous power mode, an A/D conversion will take place when a 5 microseconds or greater positive going pulse is applied to START CONVERT (Pin 21). For single supply operation (interrupt power mode), tie Power Mode (Pin 17) to E.O.C. (Pin 16). When EOC goes low, the converter is switched to standby mode (power is disconnected to analog circuitry) and digital output data becomes valid and remains valid until next start pulse is applied. Upon receipt of a 50 microseconds minimum, 500 microseconds maximum pulse on START CONVERT (Pin 21), the converter will stabilize, make a complete conversion and return to standby mode.
5. Digital output codes are listed in coding tables. Parallel data is valid when EOC is in low state. This data can be transferred into latches during a logic "1" to logic "0" transition of the EOC line. Serial data out (Pin 14) is in NRZ (non-return to zero) format. This data is guaranteed valid in a 50 nanoseconds to 300 nanoseconds time frame after the positive edge of the clock. All digital inputs and outputs are CMOS compatible. See application notes for CMOS-TTL interface.
6. REF OUT (Pin 20) is a 6.3V ±5% internal reference pin connection.
7. For zero or offset and gain adjustment, refer to connections and calibration notes. The trim pots should be located as close as possible to the converter to avoid noise pickup. Zero point is always adjusted first, followed by gain, the adjustment with analog input at the most positive end of analog range. The range of the OFFSET (ZERO) ADJ. is ±15 mV. The range of GAIN ADJ. is 0.1% of full scale range can also be increased by decreasing the value of the series resistor (3.9 MΩ nominal). Potentiometer values are 10K and should be 100 ppm/°C ceramic type.

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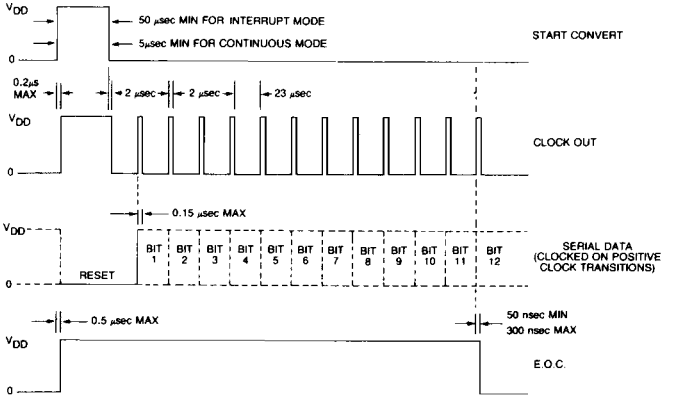
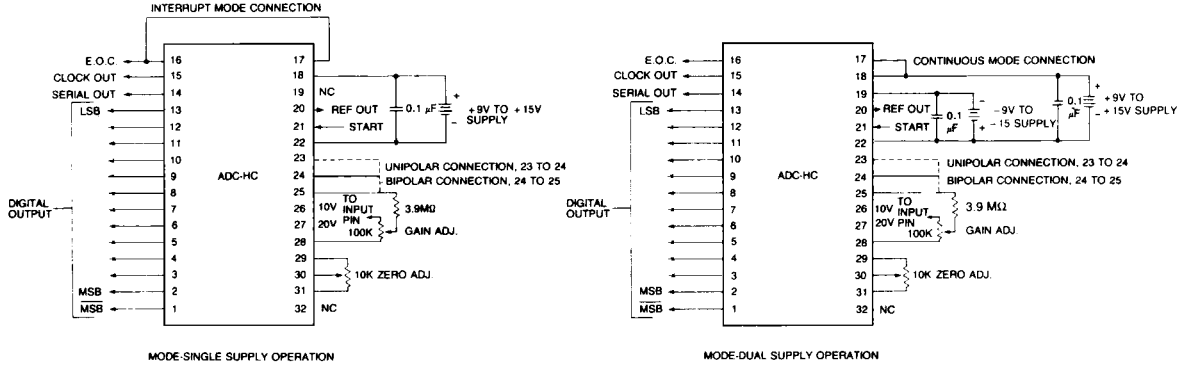
CONNECTIONS AND CALIBRATION

ADC-HC TIMING DIAGRAM



CONNECTIONS DIAGRAM



OUTPUT CODING

INPUT VOLTAGE RANGE				CODING	
	UNIPOLAR			STRAIGHT BINARY	
	0 to +20V	0 to +10V	0 to +5V	MSB	LSB
+FS – 1 LSB	+19.9951	+9.9976	+4.9988	1111	1111 1111
+½FS	+10.0000	+5.0000	+2.5000	1000	0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	0000	0000 0001
ZERO	0.0000	0.0000	0.0000	0000	0000 0000

	BIPOLAR			OFFSET BINARY*	
	±10V	±5V	±2.5V	MSB	LSB
+FS – 1 LSB	+9.9951	+4.9976	+2.4988	1111	1111 1111
+½FS	+5.0000	+2.5000	+1.2500	1100	0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000	0000 0001
ZERO	0.0000	0.0000	0.0000	1000	0000 0000
–FS – 1 LSB	–9.9951	–4.9976	–2.4988	0000	0000 0001
–FS	–10.0000	–5.0000	–2.5000	0000	0000 0000

*For 2's COMPLEMENT, MSB is inverted, use $\overline{\text{MSB}}$ (pin 1)

INPUT PIN CONNECTIONS

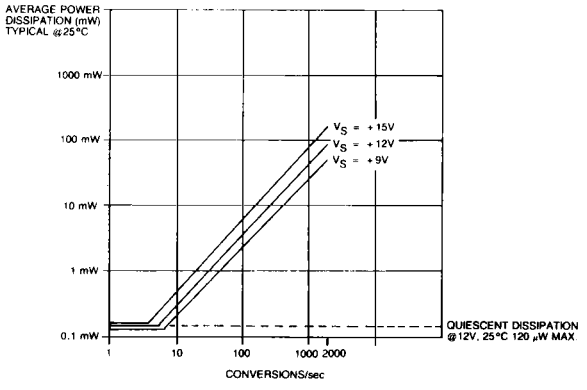
INPUT VOLTAGE RANGE	INPUT PIN	CONNECT THESE PINS TOGETHER
0 to +5V	26	23 to 24, 25 to 27
0 to +10V	26	23 to 24
0 to +20V	27	23 to 24
±2.5V	26	24 to 25, 25 to 27
±5V	26	24 to 25
±10V	27	24 to 25

CALIBRATION PROCEDURE

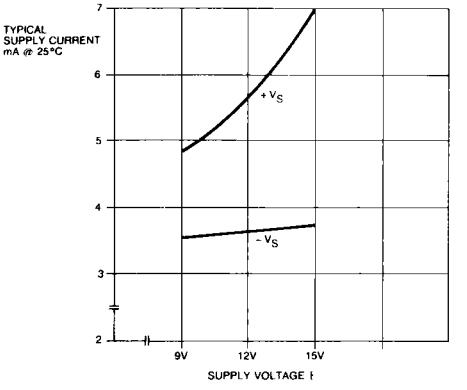
1. Connect the converter as shown in the Connection Diagram. Use the Input Pin Connections table for the desired input voltage range. Apply start conversion pulses to start pin.
2. **Zero and Offset Adjustment**
   Apply a precision voltage reference source between the selected analog input range and ground. Adjust the output of the reference source to +½ LSB. Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 for unipolar and 1000 0000 0000 and 1000 0000 0001 for bipolar mode.
3. **Full Scale Adjustment**
   Change the output of the precision reference source for +FS – 1½ LSB. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.
4. For bipolar operation, the offset and Full Scale Adjustment are interactive. Repeat the offset and Full Scale Adjustment procedure as necessary until both points are set.

APPLICATIONS

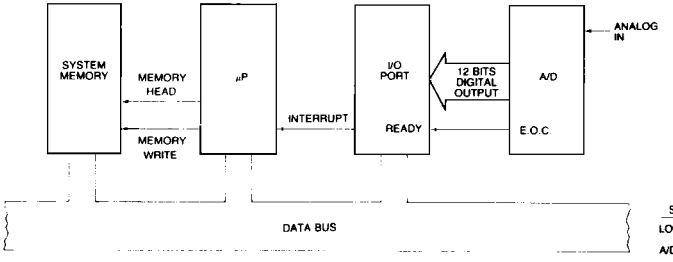
ADC-HC INTERRUPT POWER MODE



ADC-HC CONTINUOUS POWER MODE

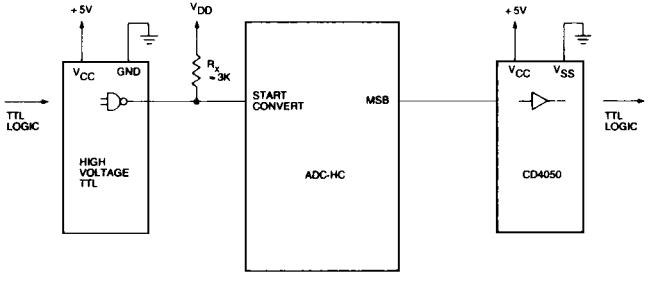


LOW POWER MICRO-PROCESSOR INTERFACE



SYSTEMS COMPONENTS	MANUFACTURE	MODEL	DATA BITS	TYPE
LOW POWER MICROPROCESSOR	RCA	CDP1802	8	CMOS
	INTERSIL	IM6100	12	CMOS
A/D CONVERTER	DATEL	ADC-HC	12	CMOS

TTL-CMOS INTERFACE



CMOS and TTL logic are not compatible due to different threshold levels. They can, however, be interfaced by simple techniques.

The START CONVERT (Pin 21) can be driven directly from an open collector, high voltage TTL gate. Resistor Rx is used to source current and bring the TTL output up to the CMOS threshold level. Typical values of Rx are 3.3K to 10K ohms.

CMOS to TTL interface requires sufficient sink current in the low state. The CD4049 (inverting) and CD4050 (noninverting) buffers, powered from +5V logic supply can accept input voltage swings of +5 to +15V from the CMOS system. Each buffer gate can drive at least one input from any TTL family.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HC12BMC	0 to +70 °C	Hermetic
ADC-HC12BMM	-55 to +125 °C	Hermetic
ADC-HC12BMM-QL	-55 to +125 °C	Hermetic

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