DS0141

Datasheet

PolarFire FPGA

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed (see page 26) and HSIO Maximum Output Buffer Speed (see page 28) .
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications (see page 21).
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics (see page 56).
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times (see page 11).

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

This datasheet describes PolarFire™ FPGA device characteristics with industrial temperature range (–40 °C to 100 °C T_J) and extended commercial temperature range (0 °C to 100 °C T_J). The devices are provided with a standard speed grade (STD) and a –1 speed grade with higher performance. The FPGA core supply V_{DD} can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply V_{DDA} can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the project.

3 References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- UG0722: PolarFire FPGA Packaging and Pin Descriptions Users Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

4 Device Offering

The following table lists the PolarFire FPGA device options.

Table 1 • PolarFire FPGA Device Options

Device Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C–100 °C	STD	–1	Transceivers T	Lower Static Power "L"	Data Security "S"
MPF300T	Yes	Yes	Yes	Yes	Yes		
MPF300TL	Yes	Yes	Yes		Yes	Yes	
MPF300TS		Yes	Yes	Yes	Yes		Yes
MPF300TLS		Yes	Yes		Yes	Yes	Yes

5 Silicon Status

There are three silicon status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production silicon data

The following table shows the status of the PolarFire FPGA device.

Table 2 • PolarFire FPGA Silicon Status

Device	Silicon Status
MPF100T, TL, TS, TLS	Advanced
MPF200T, TL, TS, TLS	Advanced
MPF300T, TL, TS, TLS	Advanced
MPF500T, TL, TS, TLS	Advanced

6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for the PolarFire device.

Table 3 • Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Core power supply	V_{DD}	–0.5	1.13	V
Transceiver core power supply	V_{DDA}	–0.5	1.13	V
Must connect to 1.8 V	V_{DD18}	–0.5	2.0	V
Must connect to 2.5 V	V_{DD25}	–0.5	2.7	V
Must connect to 2.5 V	V_{DDA25}	–0.5	2.7	V
GPIO auxiliary power supply for I/O bank 2	V_{DDAUX2}	–0.5	3.6	V
GPIO auxiliary power supply for I/O bank 4	V_{DDAUX4}	–0.5	3.6	V
GPIO auxiliary power supply for I/O bank 5	V_{DDAUX5}	–0.5	3.6	V
Transceiver reference clock input buffer power supply	$V_{DD\_XCVR\_CLK}$	–0.5	3.6	V
Transceiver reference clock input buffer comparator voltage reference	$XCVR_{VREF}$	–0.5	3.6	V
DC I/O supply voltage for HSIO	V_{DDIx}	–0.5	2.0	V
DC I/O supply voltage for GPIO	V_{DDIx}	–0.5	3.6	V
DC I/O supply voltage for JTAG	V_{DDI3}	–0.5	3.6	V
DC I/O supply voltage for SPI	V_{DDI3}	–0.5	3.6	V
Receiver absolute input voltage	Transceiver V_{IN}	–0.5	1.26	V
Reference clock absolute input voltage	Transceiver REFCLK V_{IN}	–0.5	3.6	V
Storage temperature (ambient)[1]	T_{STG}	–65	150	°C
Junction temperature	T_J	–55	135	°C
Maximum soldering temperature RoHS	$T_{SOLROHS}$		260	°C
Maximum soldering temperature leaded	T_{SOLPB}		220	°C
Maximum DC input voltage on GPIO	V_{IN}	–0.5	3.8	V
Maximum DC input voltage on HSIO	V_{IN}	–0.5	2.2	V

1. See FPGA Programming Cycles vs Retention Characteristics (see page 56) for retention time vs. temperature. The total time used in calculating the device retention includes storage time and the device stored temperature.

6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 4 • Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core supply at 1.0 V mode[1]	V_{DD}	0.97	1.00	1.03	V
FPGA core supply at 1.05 V mode[1]	V_{DD}	1.02	1.05	1.08	V

Parameter	Symbol	Min	Typ	Max	Unit
Transceiver core supply at 1.0 V mode[1]	V_{DDA}	0.97	1.00	1.03	V
Transceiver core supply at 1.05 V mode[1]	V_{DDA}	1.02	1.05	1.08	V
Must connect to 1.8 V	V_{DD18}	1.71	1.80	1.89	V
FPGA core and core PLL high-voltage supply	V_{DD25}	2.425	2.50	2.575	V
Transceiver PLL high-voltage supply	V_{DDA25}	2.425	2.50	2.575	V
HSIO allow 1.2 V, 1.5 V, and 1.8 V nominal options	V_{DDIx}	1.14	Various	1.89	V
GPIO allow 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V nominal options[2]	V_{DDIx}	1.14	Various	3.465	V
Bank 3 dedicated I/O buffers allow 1.8 V, 2.5 V, and 3.3 V nominal options (GPIO)[2]	V_{DDI3}	1.71	Various	3.465	V
GPIO with V_{DDI2} = 3.3 V nominal[2]	V_{DDAUX2}	3.135	3.3	3.465	V
GPIO with V_{DDI4} = 3.3 V nominal[2]	V_{DDAUX4}	3.135	3.3	3.465	V
GPIO with V_{DDI5} = 3.3 V nominal[2]	V_{DDAUX5}	3.135	3.3	3.465	V
GPIO with V_{DDI2} = 2.5 V nominal or lower[2]	V_{DDAUX2}	2.375	2.5	2.625	V
GPIO with V_{DDI2} = 2.5 V nominal or lower[2]	V_{DDAUX4}	2.375	2.5	2.625	V
GPIO with V_{DDI2} = 2.5 V nominal or lower[2]	V_{DDAUX5}	2.375	2.5	2.625	V
Transceiver reference clock supply –3.3 V nominal	$V_{DD\_XCVR\_CLK}$	3.135	3.3	3.465	V
Transceiver reference clock supply –2.5 V nominal	$V_{DD\_XCVR\_CLK}$	2.375	2.5	2.625	V
Global V_{REF} for transceiver reference clocks[3]	$XCVR_{VREF}$	Ground		$V_{DD\_XCVR\_CLK}$	V
Extended commercial temperature range	T_J	0		100	°C
Industrial temperature range		–40		100	°C
Extended commercial programming temperature range	T_{PRG}	0		100	°C
Industrial programming temperature range		–40		100	°C

1. V_{DD} and V_{DDA} can independently operate at 1.0 V or 1.05 V nominal. These are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank #, if V_{DDIx} is 2.5 V nominal or 3.3 V nominal, V_{DDAUXx} must be connected to the V_{DDIx} supply for that bank. If V_{DDIx} for a given GPIO bank is < 2.5 V nominal, V_{DDAUXx} per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}$/2 V but is allowed in the specified range.

6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 5 • DC Characteristics over Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Condition
Input pin capacitance[1]	C_{IN} (dedicated GPIO)		5.6	pf	
	C_{IN} (GPIO)		5.6	pf	
	C_{IN} (HSIO)		2.8	pf	
Input or output leakage current per pin	I_L (GPIO)		0.1	µA	I/O disabled, high – Z
	I_L (HSIO)		0.1	µA	I/O disabled, high – Z
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]	T_{RISE}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input rise time (10%–90% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]	T_{FALL}	0.66	2.64	ns	V_{DDIx} = 3.3 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.50	2.00	ns	V_{DDIx} = 2.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.36	1.44	ns	V_{DDIx} = 1.8 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.30	1.20	ns	V_{DDIx} = 1.5 V
Input fall time (90%–10% of V_{DDIx})[2, 3, 4]		0.24	0.96	ns	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[5]	I_{PU}	150	216	µA	V_{DDIx} = 3.3 V
Pad pull-up when V_{IN} = 0[5]		111	161	µA	V_{DDIx} = 2.5 V
Pad pull-up when V_{IN} = 0		72	111	µA	V_{DDIx} = 1.8 V
Pad pull-up when V_{IN} = 0		51	88	µA	V_{DDIx} = 1.5 V
Pad pull-up when V_{IN} = 0[6]		29	73	µA	V_{DDIx} = 1.35 V
Pad pull-up when V_{IN} = 0		16	46	µA	V_{DDIx} = 1.2 V
Pad pull-up when V_{IN} = 0[6]		8	25	µA	V_{DDIx} = 1.1 V
Pad pull-down when V_{IN} = 3.3 V[5]	I_{PD}	65	187	µA	V_{DDIx} = 3.3 V
Pad pull-down when V_{IN} = 2.5 V[5]		63	160	µA	V_{DDIx} = 2.5 V
Pad pull-down when V_{IN} = 1.8 V		60	117	µA	V_{DDIx} = 1.8 V
Pad pull-down when V_{IN} = 1.5 V		57	95	µA	V_{DDIx} = 1.5 V
Pad pull-down when V_{IN} = 1.35 V[6]		52	86	µA	V_{DDIx} = 1.35 V
Pad pull-down when V_{IN} = 1.2 V		49	77	µA	V_{DDIx} = 1.2 V
Pad pull-down when V_{IN} = 1.1 V[6]		45	71	µA	V_{DDIx} = 1.1 V

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. Numbers based on rail-to-rail input signal swing and minimum 1 V/ns and maximum 4 V/ns. These are to be used for input delay measurement consistency.
4. I/O signal standards with smaller than rail-to-rail input swings can use a nominal value of 200 ps 20–80% of swing and maximum value of 500 ps 20–80% of swing.
5. GPIO only.
6. HSIO only.

6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for HSIO.

Table 6 • Maximum Overshoot During Transitions for HSIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	1.8
100	1.85
100	1.9
100	1.95
100	2
100	2.05
100	2.1
100	2.15
100	2.2
90	2.25
30	2.3
7.5	2.35
1.9	2.4

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for HSIO.

Table 7 • Maximum Undershoot During Transitions for HSIO

AC (V_{IN}) Undershoot[1] Duration as % at T_J = 100 °C	Condition (V)
100	–0.05
100	–0.1
100	–0.15
100	–0.2
100	–0.25
100	–0.3
100	–0.35
100	–0.4
44	–0.45
14	–0.5
4.8	–0.55
1.6	–0.6

1. Undershoot level is regarding 1.8 V V_{DDI}.

The following table shows the maximum AC input voltage (V_{IN}) overshoot duration for GPIO.

Table 8 • Maximum Overshoot During Transitions for GPIO

AC (V_{IN}) Overshoot Duration as % at T_J = 100 °C	Condition (V)
100	3.8
100	3.85
100	3.9
100	3.95
70	4
50	4.05
33	4.1
22	4.15
14	4.2
9.8	4.25
6.5	4.3
4.4	4.35
3	4.4
2	4.45
1.4	4.5
0.9	4.55
0.6	4.6

The following table shows the maximum AC input voltage (V_{IN}) undershoot duration for GPIO.

Table 9 • Maximum Undershoot During Transitions for GPIO

AC (V_{IN}) Undershoot[1] Duration as % at T_J = 100 °C	Condition (V)
100	–0.5
100	–0.55
100	–0.6
100	–0.65
100	–0.7
100	–0.75
100	–0.8
100	–0.85
100	–0.9
100	–0.95
100	–1
100	–1.05
100	–1.1
100	–1.15
100	–1.2
69	–1.25
45	–1.3

1. Undershoot level is with reference to 3.3 V V_{DDI}.

6.2.2.1 Power-Supply Ramp Times

The following table shows the power-up ramp times. All supplies must rise and fall monotonically. There are no power-supply sequencing requirements for PolarFire devices.

Table 10 • Power-Supply Ramp Times

Parameter	Symbol	Min	Max	Unit
FPGA core supply	V_{DD}	0.2	100	ms
Transceiver core supply	V_{DDA}	0.2	100	ms
Must connect to 1.8 V supply	V_{DD18}	0.2	100	ms
Must connect to 2.5 V supply	V_{DD25}	0.2	100	ms
Must connect to 2.5 V supply	V_{DDA25}	0.2	100	ms
HSIO bank I/O power supplies	$V_{DDI[0,1,6,7]}$	0.2	100	ms
GPIO bank I/O power supplies	$V_{DDI[2,4,5]}$	0.2	100	ms
Bank 3 dedicated I/O buffers (GPIO)	V_{DDI3}	0.2	100	ms
GPIO bank auxiliary power supplies	$V_{DDAUX[2,4,5]}$	0.2	100	ms
Transceiver reference clock supply –3.3 V nominal	$V_{DD\_XCVR\_CLK}$	0.2	100	ms
Global V_{REF} for transceiver reference clocks	$XCVR_{VREF}$	0.2	100	ms

Note: Power-supply ramp must be monotonic.

Note: For proper operation of programming recovery mode, if a Vdd supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10ms or longer by using programmable regulator or on-board capacitors.

6.2.2.2 Hot Socketing

The following table lists the hot-socketing DC characteristics over recommended operating conditions.

Table 11 • DC Characteristics Over Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Current per transceiver Rx input pin (P or N single-ended)[1, 2]	I_{XCVRRX_HS}			±4	mA	V_{DDA} = 0 V
Current per transceiver Tx output pin (P or N single-ended)[3]	I_{XCVRTX_HS}			±10	mA	V_{DDA} = 0 V
Current per transceiver reference clock input pin (P or N single-ended)[4]	$I_{XCVRREF\_HS}$			±1	mA	$V_{DD\_XCVR\_CLK}$ = 0 V
Current per GPIO pin (P or N single-ended)[5]	I_{GPIO_HS}			±1	mA	V_{DDIx} = 0 V
Current per HSIO pin (P or N single-ended)[6]						

1. Assumes that the device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS 2^7 data.
2. Each P and N transceiver input has less than the specified maximum input current.
3. Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage (V_{DDAmax} + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no socket current will be seen.
4. $V_{DD\_XCVR\_CLK}$ is powered down and the device is driven to $–0.5\ V < V_{IN} < V_{DD\_XCVR\_CLK}$.

5. V_{DDIx} is powered down and the device is driven to –0.5 V < V_{IN} < GPIO V_{DDImax}.
6. Not supported.

6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

6.3.1 DC Input and Output Levels

The following table lists the DC I/O levels.

Table 12 • DC Input and Output Levels

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{IL} Min	V_{IL} Max	V_{IH} Min	V_{IH} Max[1]	V_{OL} Min	V_{OL} Max	V_{OH} Min	V_{OH} Max	I_{OL} mA	I_{OH} mA
PCI[2]	3.15	3.3	3.45	–0.3	0.3 × V_{DDI}	0.5 × V_{DDI}	3.45		0.1 × V_{DDI}	0.9 × V_{DDI}		1.5	0.5
LVTTL[3]	3.15	3.3	3.45	–0.3	0.8	2	3.45		0.4	2.4			
LVCMOS33[3]	3.15	3.3	3.45	–0.3	0.8	2	3.45		0.4	V_{DDI} – 0.4			
LVCMOS25[3]	2.375	2.5	2.625	–0.3	0.7	1.7	2.625		0.4	V_{DDI} – 0.4			
LVCMOS18[4]	1.71	1.8	1.89	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.89		0.45	V_{DDI} – 0.45			
LVCMOS15[5]	1.425	1.5	1.575	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.575		0.25 × V_{DDI}	0.75 × V_{DDI}			
LVCMOS12[6]	1.14	1.2	1.26	–0.3	0.35 × V_{DDI}	0.65 × V_{DDI}	1.26		0.25 × V_{DDI}	0.75 × V_{DDI}			
SSTL25I[7]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625		V_{TT} – 0.608	V_{TT} + 0.608		8.1	8.1
SSTL25II[7]	2.375	2.5	2.625	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	2.625		V_{TT} – 0.810	V_{TT} + 0.810		16.2	16.2
SSTL18I[7]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89		V_{TT} – 0.603	V_{TT} + 0.603		6.7	6.7
SSTL18II[7]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89		V_{TT} – 0.603	V_{TT} + 0.603		13.4	13.4
SSTL15I[8]	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH})/40
SSTL15II[8]	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH})/34

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{IL} Min	V_{IL} Max	V_{IH} Min	V_{IH} Max[1]	V_{OL} Min	V_{OL} Max	V_{OH} Min	V_{OH} Max	I_{OL} mA	I_{OH} mA
SSTL135I[8]	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH})/40
SSTL135II[8]	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH})/34
HSTL15I	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575		0.4	V_{DDI}-0.4		8	8
HSTL15II	1.425	1.5	1.575	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575		0.4	V_{DDI}-0.4		16	16
HSTL135I[8]	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH})/50
HSTL135II[8]	1.283	1.35	1.418	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	1.418		0.2 × V_{DDI}	0.8 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH})/25
HSTL12I[8]	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/50	(V_{DDI} – V_{OH})/50
HSTL12II[8]	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF}+ 0.1	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH})/25
HSUL18I[8]	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/55	(V_{DDI} – V_{OH})/55
HSUL18II[8]	1.71	1.8	1.89	–0.3	0.3 × V_{DDI}	0.7 × V_{DDI}	1.89		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/25	(V_{DDI} – V_{OH})/25
HSUL12I[8]	1.14	1.2	1.26	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.26		0.1 × V_{DDI}	0.9 × V_{DDI}		V_{OL}/40	(V_{DDI} – V_{OH})/40
POD12I[8, 9]	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26		0.5 × V_{DDI}			V_{OL}/48	(V_{DDI} – V_{OH})/48
POD12II[8, 9]	1.14	1.2	1.26	–0.3	V_{REF} – 0.08	V_{REF} + 0.08	1.26		0.5 × V_{DDI}			V_{OL}/34	(V_{DDI} – V_{OH})/34
LVSTL11I[8]	1.045	1.1	1.155	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.155		0.1 × V_{DDI}	V_{DDI}/3		V_{OL}/40	(V_{DDI} – V_{OH})/80
LVSTL11II[8]	1.045	1.1	1.155	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.155		0.1 × V_{DDI}	V_{DDI}/2.5		V_{OL}/40	(V_{DDI} – V_{OH})/60

1. GPIO V_{IH} max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. Drive strengths per PCI specification V/I curves.
3. Drive strengths of 2, 4, 8, 12, 16, 20 mA.
4. Drive strengths of 2, 4, 6, 8, 12, 16 mA.
5. Drive strengths of 2, 4, 6, 8, 12 mA.
6. Drive strengths of 2, 4, 6, 8 mA.
7. For external stub-series resistance. This resistance is on-die for GPIO.

8. I_{OL}/I_{OH} Units for impedance standards in Amps (not mA).
9. VOH_MAX based on external pull-up termination (pseudo-open drain).

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

6.3.2 Differential DC Input and Output Levels

The follow table lists the differential DC I/O levels.

Table 13 • Differential DC Input and Output Levels

I/O Standard	Bank Type	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max[5]	V_{ID}[2] Min	V_{ID} Typ	V_{ID} Max	V_{OCM}[3] Min	V_{OCM} Typ	V_{OCM} Max	V_{OD}[4] Min	V_{OD} Typ	V_{OD} Max
LVDS33	GPIO	0.05	1.25	2.35	0.1	0.35	0.6	1.125	1.2	1.375	0.25	0.35	0.45
LVDS25	GPIO	0.05	1.25	2.35	0.1	0.35	0.6	1.125	1.2	1.375	0.25	0.35	0.45
LVDS18	GPIO	0.05	1.25	2.35	0.1	0.35	0.6						
LVDS18[6]	HSIO	0.05	1.25	1.65	0.1	0.35	0.6						
RSDS33	GPIO	0.05	1.25	2.35	0.1	0.2	0.6	1.19	1.2	1.31	0.17	0.2	0.23
RSDS25	GPIO	0.05	1.25	2.35	0.1	0.2	0.6	1.19	1.2	1.31	0.17	0.2	0.23
RSDS18[7]	HSIO	0.05	1.25	1.65	0.1	0.2	0.6						
MiniLVDS33	GPIO	0.05	1.25	2.35	0.1	0.3	0.6	1.125	1.2	2.375	0.3	0.4	0.6
MiniLVDS25	GPIO	0.05	1.25	2.35	0.1	0.3	0.6	1.125	1.2	2.375	0.3	0.4	0.6
MiniLVDS18[7]	HSIO	0.05	1.25	1.65	0.1	0.3	0.6						
SubLVDS33	GPIO	0.05	0.9	2.35	0.1	0.15	0.3	0.8	0.9	1	0.1	0.15	0.3
SubLVDS25	GPIO	0.05	0.9	2.35	0.1	0.15	0.3	0.8	0.9	1	0.1	0.15	0.3
SubLVDS18[7]	HSIO	0.05	0.9	1.65	0.1	0.15	0.3						
PPDS33	GPIO	0.05	0.8	2.35	0.1	0.2	0.6	0.5	0.8	1.4	0.17	0.2	0.23
PPDS25	GPIO	0.05	0.8	2.35	0.1	0.2	0.6	0.5	0.8	1.4	0.17	0.2	0.23
PPDS18[7]	HSIO	0.05	0.8	1.65	0.1	0.2	0.6						
SLVS33[8]	GPIO	0.05	0.2	2.35	0.1	0.2	0.3						
SLVS25[8]	GPIO	0.05	0.2	2.35	0.1	0.2	0.3						
SLVS18[7]	HSIO	0.05	0.2	1.65	0.1	0.2	0.3						
SLVSE15[9]	GPIO, HSIO							0.1	0.2	0.3	0.12	0.135	0.15
HCSL33[8]	GPIO	0.05	0.35	2.35	0.1	0.55	1.1						
HCSL25[8]	GPIO	0.05	0.35	2.35	0.1	0.55	1.1						
HCSL18[7]	HSIO	0.05	0.35	1.65	0.1	0.55	1.1						

I/O Standard	Bank Type	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max[5]	V_{ID}[2] Min	V_{ID} Typ	V_{ID} Max	V_{OCM}[3] Min	V_{OCM} Typ	V_{OCM} Max	V_{OD}[4] Min	V_{OD} Typ	V_{OD} Max
BUSLVDSE25[9]	GPIO	0.05	1.25	2.35	0.05	0.1	V_{DDIn}	1.15	1.25	1.31	0.24	0.262	0.272
MLVDSE25[9]	GPIO	0.05	1.25	2.35	0.05	0.35	2.4	1.15	1.25	1.31	0.396	0.442	0.453
LVPECL33[9]	GPIO	0.05	1.65	2.35	0.05	0.8	2.4	1.51	1.65	1.74	0.664	0.722	0.755
LVPECLE33[9]	GPIO	0.05	1.65	2.35	0.05	0.8	2.4	1.51	1.65	1.74	0.664	0.722	0.755
MIPIE25[9]	GPIO	0.05	0.2	2.35	0.05	0.2	0.3	0.15	0.25	0.35	0.1	0.22	0.3
MIPI12 (high-speed)	GPIO	0.05	0.2	2.35	0.05	0.2	0.3						

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage.
5. V_{ICM} must be less than V_{DDI} – .3 V.
6. HSIO receiver only, for AC transient purposes, V_{ICM} cannot exceed 0.95 V.
7. HSIO receiver only.
8. GPIO receiver only.
9. Emulated output only.

6.3.3 Complementary Differential DC Input and Output Levels

The following tables lists the complementary differential DC I/O levels.

Table 14 • Complementary Differential DC Input and Output Levels

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max	V_{ID}[2] Min	V_{ID} Max	V_{OL}[3] Min	V_{OL} Max	V_{OH}[3] Min	I_{OL} Max (mA)	I_{OH} Min (mA)
SSTL25_DI	2.375	2.5	2.625	1.164	1.250	1.339	0.1			V_{TT} – 0.608	V_{TT} + 0.608	8.1	8.1
SSTL25_DII	2.375	2.5	2.625	1.164	1.250	1.339	0.1			V_{TT} – 0.810	V_{TT} + 0.810	16.2	16.2
SSTL18_DI	1.71	1.8	1.89	0.838	0.900	0.964	0.1			V_{TT} – 0.603	V_{TT} + 0.603	6.7	6.7
SSTL18_DII	1.71	1.8	1.89	0.838	0.900	0.964	0.1			V_{TT} – 0.603	V_{TT} + 0.603	13.4	13.4
SSTL15_DI[4]	1.425	1.5	1.575	0.698	0.750	0.803	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max	V_{ID}[2] Min	V_{ID} Max	V_{OL}[3] Min	V_{OL} Max	V_{OH}[3] Min	I_{OL} Max (mA)	I_{OH} Min (mA)
SSTL15_DII[4]	1.425	1.5	1.575	0.698	0.750	0.803	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/34	(V_{DDI} – V_{OH})/34
SSTL135_DI[4]	1.283	1.35	1.418	0.629	0.675	0.723	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40
SSTL135_DII[4]	1.283	1.35	1.418	0.629	0.675	0.723	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/34	(V_{DDI} – V_{OH})/34
HSTL15_DI	1.425	1.5	1.575	0.698	0.750	0.803	0.1			0.4	V_{DDI} – 0.4	8	8
HSTL15_DII	1.425	1.5	1.575	0.698	0.750	0.803	0.1			0.4	V_{DDI} – 0.4	16	16
HSTL135_DI[4]	1.283	1.35	1.418	0.629	0.675	0.723	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/50	(V_{DDI} – V_{OH})/50
HSTL135_DII[4]	1.283	1.35	1.418	0.629	0.675	0.723	0.1			0.2 × V_{DDI}	0.8 × V_{DDI}	V_{OL}/25	(V_{DDI} – V_{OH})/25
HSTL12_DI[4]	1.14	1.2	1.26	0.559	0.600	0.643	0.1			0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/50	(V_{DDI} – V_{OH})/50
HSUL18_DI[4]	1.71	1.8	1.89	0.838	0.900	0.964	0.1			0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/55	(V_{DDI} – V_{OH})/55
HSUL18_DII[4]	1.71	1.8	1.89	0.838	0.900	0.964	0.1			0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/25	(V_{DDI} – V_{OH})/25
HSUL12_DI[4]	1.14	1.2	1.26	0.559	0.600	0.643	0.1			0.1 × V_{DDI}	0.9 × V_{DDI}	V_{OL}/40	(V_{DDI} – V_{OH})/40
POD12_DI[4, 5]	1.14	1.2	1.26	0.787	0.840	0.895	0.1			0.5 × V_{DDI}		V_{OL}/48	(V_{DDI} – V_{OH})/48
POD12_DII[4, 5]	1.14	1.2	1.26	0.787	0.840	0.895	0.1			0.5 × V_{DDI}		V_{OL}/34	(V_{DDI} – V_{OH})/34

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max	V_{ID}[2] Min	V_{ID} Max	V_{OL}[3] Min	V_{OL} Max	V_{OH}[3] Min	I_{OL} Max (mA)	I_{OH} Min (mA)
LVSTL11_DI[4]	1.045	1.1	1.155	0.172	0.183	0.194	0.1			0.1 × V_{DDI}	V_{DDI}/3	V_{OL}/40	(V_{DDI} – V_{OH})/80
LVSTL11_DII[4]	1.045	1.1	1.155	0.207	0.220	0.233	0.1			0.1 × V_{DDI}	V_{DDI}/2.5	V_{OL}/40	(V_{DDI} – V_{OH})/60

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – Q).
3. V_{OH} is the single-ended high-output voltage.
4. I_{OL}/I_{OH} Units for impedance standards in Amps (not mA).
5. V_{OH_MAX} based on external pull-up termination (pseudo-open drain).

6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

Table 15 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

Min (%)	Typ	Max (%)	Unit	Condition
–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V/1.35 V/1.2 V
–40	75	20	Ω	V_{DDI} = 1.8 V
–40	150	20	Ω	V_{DDI} = 1.8 V
–20	20	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	30	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	40	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	120	20	Ω	V_{DDI} = 1.5 V/1.35 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Note: The venin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

Table 16 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	34	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.2 V
–20	48	20	Ω	V_{DDI} = 1.2 V
–20	60	20	Ω	V_{DDI} = 1.2 V
–20	80	20	Ω	V_{DDI} = 1.2 V
–20	120	20	Ω	V_{DDI} = 1.2 V

Min (%)	Typ	Max (%)	Unit	Condition
–20	240	20	Ω	V_{DDI} = 1.2 V

Note: Measured at 50% of V_{DDI}.

Table 17 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)

Min (%)	Typ	Max (%)	Unit	Condition
–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
–20	120	20	Ω	V_{DDI} = 1.2 V
–20	240	20	Ω	V_{DDI} = 1.2 V
–20	40	20	Ω	V_{DDI} = 1.1 V
–20	48	20	Ω	V_{DDI} = 1.1 V
–20	60	20	Ω	V_{DDI} = 1.1 V
–20	80	20	Ω	V_{DDI} = 1.1 V
–20	120	20	Ω	V_{DDI} = 1.1 V
–20	240	20	Ω	V_{DDI} = 1.1 V

Note: Measured at 50% of V_{DDI}.

6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

Table 18 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
Differential termination[1]	Internal differential termination	–20	100	25	Ω	V_{CM} < 0.7 V
		–20	100	25	Ω	0.7 V < V_{CM} < 0.9 V
		–20	100	25	Ω	0.9 V < V_{CM}
Single-ended thevenin termination[2,3]	Internal parallel thevenin termination	–40	50	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–40	75	20	Ω	V_{DDI} = 1.8 V
		–40	150	20	Ω	V_{DDI} = 1.8 V
		–20	20	20	Ω	V_{DDI} = 1.5 V
		–20	30	20	Ω	V_{DDI} = 1.5 V
		–20	40	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.5 V
		–20	120	20	Ω	V_{DDI} = 1.5 V
		–20	60	20	Ω	V_{DDI} = 1.2 V
		–20	120	20	Ω	V_{DDI} = 1.2 V
Single-ended termination to V_{DDI}[4]	Internal parallel termination to V_{DDI}	–20	120	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–20	240	20	Ω	V_{DDI} = 1.8 V/1.5 V
		–20	120	20	Ω	V_{DDI} = 1.2 V
		–20	240	20	Ω	V_{DDI} = 1.2 V
Single-ended termination to V_{SS}[4]	Internal parallel termination to V_{SS}	–20	240	20	Ω	V_{DDI} = 3.3 V

Parameter	Description	Min (%)	Typ	Max (%)	Unit	Condition
		–20	120	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V /1.2 V
		–20	240	20	Ω	V_{DDI} = 2.5 V/1.8 V/1.5 V /1.2 V

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of V_{DDI}.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of V_{DDI}.

6.3.6 LVDS

LVDS operation is supported in GPIO banks. The following tables provide DC specifications with various I/O bank voltage supplies of 3.3 V, 2.5 V, and 1.8 V.

Table 19 • GPIO 3.3 V LVDS DC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage[1]	V_{DDI}	3.135	3.300	3.465	V	
Output high-voltage for P and N	V_{OH}			1.675	V	RT = 100 Ω across P and N signals
Output low-voltage for P and N	V_{OL}	0.700			V	RT = 100 Ω across P and N signals
Differential output voltage	V_{ODIFF}	247	350	600	mV	RT = 100 Ω across P and N signals
Output common mode	V_{OCM}	1.000	1.250	1.425	V	RT = 100 Ω across P and N signals
Differential input voltage	V_{IDIFF}	100	350	600	mV	
Input common mode	V_{ICM}	0.050	1.200	2.350	V	

1. Differential inputs can be placed in I/O banks with a different V_{DDI} from the required level for outputs. For more information, see UG0686: PolarFire FPGA User I/O User Guide.

Table 20 • GPIO 2.5 V LVDS DC Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage[1]	V_{DDI}	2.375	2.500	2.625	V	
Output high-voltage for P and N	V_{OH}			1.675	V	RT = 100 Ω across P and N signals
Output low-voltage for P and N	V_{OL}	0.700			V	RT = 100 Ω across P and N signals
Differential output voltage	V_{ODIFF}	247	350	600	mV	RT = 100 Ω across P and N signals
Output common mode	V_{OCM}	1.000	1.250	1.425	V	RT = 100 Ω across P and N signals
Differential input voltage	V_{IDIFF}	100	350	600	mV	
Input common mode[2]	V_{ICM}	0.050	1.200	2.350	V	

1. Differential inputs can be placed in I/O banks with a different V_{DDI} from the required level for outputs. For more information, see UG0686: PolarFire FPGA I/O User Guide.
2. V_{ICM} max must be less than V_{DDI} – .3 V.

Table 21 • GPIO 1.8 V LVDS Receiver DC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage[1]	V_{DDI}	1.710	1.800	1.890	V
Differential input voltage	V_{IDIFF}	0.100	0.350	0.600	V
Input common mode[2]	V_{ICM}	0.050	0.800	1.650	V

1. Differential inputs can be placed in I/O banks with a different V_{DDI} from the required level for outputs. For more information, see UG0686: PolarFire FPGA I/O User Guide.
2. For LVDS18, AC transient purposes, V_{ICM} cannot exceed 0.95 V.

7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire devices.

7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

7.1.1 Input Delay Measurement Methodology

The following table provides information about the methodology for input delay measurement.

Table 22 • Input Delay Measurement Methodology

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
PCI33	PCIE 3.3 V	0.1	3.2			1.32		V
LVTTL33	LVTTL 3.3 V	0.1	3.2			1.75		V
LVCMOS33	LVCMOS 3.3 V	0.1	3.2			1.75		V
LVCMOS25	LVCMOS 2.5 V	0.1	2.4			1.25		V
LVCMOS18	LVCMOS 1.8 V	0.1	1.7			0.90		V
LVCMOS15	LVCMOS 1.5 V	0.1	1.4			0.75		V
LVCMOS12	LVCMOS 1.2 V	0.1	1.1			0.60		V
SSTL25_I	SSTL 2.5 V Class I	V_{REF} – 1.15	V_{REF} + 1.15			V_{REF}	1.25	V
SSTL25_II	SSTL 2.5 V Class II	V_{REF} – 1.15	V_{REF} + 1.15			V_{REF}	1.25	V
SSTL18_I	SSTL 1.8 V Class I	V_{REF} – 0.8	V_{REF} + 0.8			V_{REF}	0.90	V
SSTL18_II	SSTL 1.8 V Class II	V_{REF} – 0.8	V_{REF} + 0.8			V_{REF}	0.90	V
SSTL15_I	SSTL 1.5 V Class I	V_{REF} – .65	V_{REF} + .65			V_{REF}	0.75	V
SSTL15_II	SSTL 1.5 V Class II	V_{REF} – .65	V_{REF} + .65			V_{REF}	0.75	V
SSTL135_I	SSTL 1.35 V Class I	V_{REF} – 575	V_{REF} + .575			V_{REF}	0.675	V
SSTL135_II	SSTL 1.35 V Class II	V_{REF} – .575	V_{REF} + .575			V_{REF}	0.675	V
HSTL15_I	HSTL 1.5 V Class I	V_{REF} – .65	V_{REF} + .65			V_{REF}	0.75	V
HSTL15_II	HSTL 1.5 V Class II	V_{REF} – .65	V_{REF} + .65			V_{REF}	0.75	V
HSTL135_I	HSTL 1.35 V Class I	V_{REF} – 575	V_{REF} + .575			V_{REF}	0.675	V
HSTL135_II	HSTL 1.35 V Class II	V_{REF} – .575	V_{REF} + .575			V_{REF}	0.675	V
HSTL12	HSTL 1.2 V	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.60	V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSUL18_I	HSUL 1.8 V Class I	V_{REF} – 0.8	V_{REF} + 0.8			V_{REF}	0.90	V
HSUL18_II	HSUL 1.8 V Class II	V_{REF} – 0.8	V_{REF} + 0.8			V_{REF}	0.90	V
HSUL12	HSUL 1.2 V	V_{REF} – .5	V_{REF} + .5			V_{REF}	0.60	V
POD12_I	Pseudo open drain (POD) logic 1.2 V Class I	V_{REF} – .16	V_{REF} + .65			V_{REF}	0.84	V
POD12_II	POD 1.2 V Class II	V_{REF} – .16	V_{REF} + .65			V_{REF}	0.84	V
LVSTL11_I	Low-voltage swing terminated (LVSTL) logic 1.1 V Class I	V_{REF} – .083	V_{REF} + .083			V_{REF}	0.183	V
LVSTL11_II	LVSTL 1.1 V Class II	V_{REF} – .12	V_{REF} + .12			V_{REF}	0.22	V
LVDS33	Low-voltage differential signaling (LVDS) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS25	LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVDS18[6]	LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
RSDS33	RSDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS25	RSDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
RSDS18	RSDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MiniLVDS33	Mini-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MiniLVDS25	Mini-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MiniLVDS18	Mini-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SubLVDS33	Sub-LVDS 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SubLVDS25	Sub-LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SubLVDS18	Sub-LVDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
PPDS33	Point-to-point differential signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS25	PPDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
PPDS18	PPDS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.800	0		V
SLVS33	Scalable low-voltage signaling 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V

Standard	Description	V_{IL}[1]	V_{IH}[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
SLVS25	SLVS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SLVS18	SLVS 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
HCSL33	High-speed current steering logic (HCSL) 3.3 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL25	HCSL 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
HCSL18	HCSL 1.8 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.350	0		V
BLVDSE25[7]	Bus LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
MLVDSE25[7]	Multipoint LVDS 2.5 V	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
LVPECL33	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
LVPECLE33[7]	Low-voltage positive emitter coupled logic	V_{ICM} – .125	V_{ICM} + .125	0.250	1.650	0		V
MIPI12 (high-speed)	Mobile industry processor interface	V_{ICM} – .125	V_{ICM} + .125	0.250	0.200	0		V
SSTL25D_I	Differential SSTL 2.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL25D_II	Differential SSTL 2.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	1.250	0		V
SSTL18D_I	Differential SSTL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL18D_II	Differential SSTL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
SSTL15	Differential SSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
SSTL135	Differential SSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15D_I	Differential HSTL 1.5 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL15D_II	Differential HSTL 1.5 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.750	0		V
HSTL135D_I	Differential HSTL 1.35 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V

Standard	Description	V_L[1]	V_H[1]	V_{ID}[2]	V_{ICM}[2]	V_{MEAS}[3, 4]	V_{REF}[1, 5]	Unit
HSTL135D_II	Differential HSTL 1.35 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.675	0		V
HSTL12	Differential HSTL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
HSUL18D_I	Differential HSUL 1.8 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL18D_II	Differential HSUL 1.8 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.900	0		V
HSUL12	Differential HSUL 1.2 V	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12D_I	Differential POD 1.2 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
POD12D_II	Differential POD 1.2 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.600	0		V
LVSTLD_I	Differential LVSTL 1.1 V Class I	V_{ICM} – .125	V_{ICM} + .125	0.250	0.550	0		V
LVSTLD_II	Differential LVSTL 1.1 V Class II	V_{ICM} – .125	V_{ICM} + .125	0.250	0.550	0		V

1. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst-case of these measurements. V_{REF} values listed are typical. Input waveform switches between V_L and V_H. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV V_{ID} for timing. V_{CM} is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 26).
6. V_{ICM} cannot exceed 0.95 V.
7. Emulated bi-directional interface.

7.1.2 Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

Table 23 • Output Delay Measurement Methodology

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI33	PCIE 3.3 V	25	10	1.65	
LVTTL33	LVTTL 3.3 V	1M	0	1.65	
LVCMOS33	LVCMOS 3.3 V	1M	0	1.65	
LVCMOS25	LVCMOS 2.5 V	1M	0	1.25	
LVCMOS18	LVCMOS 1.8 V	1M	0	0.90	
LVCMOS15	LVCMOS 1.5 V	1M	0	0.75	
LVCMOS12	LVCMOS 1.2 V	1M	0	0.60	

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL25_I	Stub-series terminated logic (SSTL) 2.5 V Class I	50	0	V_{REF}	1.25
SSTL25_II	SSTL 2.5 V Class II	50	0	V_{REF}	1.25
SSTL18_I	SSTL 1.8 V Class I	50	0	V_{REF}	0.9
SSTL18_II	SSTL 1.8 V Class II	50	0	V_{REF}	0.9
SSTL15_I	SSTL 1.5 V Class I	50	0	V_{REF}	0.75
SSTL15_II	SSTL 1.5 V Class II	50	0	V_{REF}	0.75
SSTL135_I	SSTL 1.35 V Class I	50	0	V_{REF}	0.675
SSTL135_II	SSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL15_I	High-speed transceiver logic (HSTL) 1.5 V Class I	50	0	V_{REF}	0.75
HSTL15_II	HSTL 1.5 V Class II	50	0	V_{REF}	0.75
HSTL135_I	HSTL 1.35 V Class I	50	0	V_{REF}	0.675
HSTL135_II	HSTL 1.35 V Class II	50	0	V_{REF}	0.675
HSTL12	HSTL 1.2 V	50	0	V_{REF}	0.6
HSUL18_I	High-speed unterminated logic (HSUL) 1.8 V Class I	50	0	V_{REF}	0.9
HSUL18_II	HSUL 1.8 V Class II	50	0	V_{REF}	0.9
HSUL12	HSUL 1.2 V	50	0	V_{REF}	0.6
POD12_I	Pseudo open drain (POD) logic 1.2 V Class I	50	0	V_{REF}	0.84
POD12_II	POD 1.2 V Class II	50	0	V_{REF}	0.84
LVSTL11_I	LVSTL 1.1 V Class I	50	0	V_{REF}	0.183
LVSTL11_II	LVSTL 1.1 V Class II	50	0	V_{REF}	0.22
LVDS33	LVDS 3.3 V	100	0	0[1]	0
LVDS25	LVDS 2.5 V	100	0	0[1]	0
LVDS18	LVDS 1.8 V	100	0	0[1]	0
RSDS33	Reduced swing differential signaling (RSDS) 3.3 V	100	0	0[1]	0
RSDS25	RSDS 2.5 V	100	0	0[1]	0
RSDS18	RSDS 1.8 V	100	0	0[1]	0
MiniLVDS33	Mini-LVDS 3.3 V	100	0	0[1]	0
MiniLVDS25	Mini-LVDS 2.5 V	100	0	0[1]	0
MiniLVDS18	Mini-LVDS 1.8 V	100	0	0[1]	0
SubLVDS33	Sub-LVDS 3.3 V	100	0	0[1]	0
SubLVDS25	Sub-LVDS 2.5 V	100	0	0[1]	0
SubLVDS18	Sub-LVDS 1.8 V	100	0	0[1]	0
PPDS33	Point-to-point differential signaling 3.3 V	100	0	0[1]	0
PPDS25	PPDS 2.5 V	100	0	0[1]	0
PPDS18	PPDS 1.8 V	100	0	0[1]	0
SLVS33	Scalable low-voltage signaling 3.3 V	100	0	0[1]	0
SLVS25	SLVS 2.5 V	100	0	0[1]	0
SLVS18	SLVS 1.8 V	100	0	0[1]	0

Standard	Description	R_{REF} (Ω)	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
HCSL33	High-speed current steering logic 3.3 V	100	0	0[1]	0
HCSL25	HCSL 2.5 V	100	0	0[1]	0
HCSL18	HCSL 1.8 V	100	0	0[1]	0
BUSLVDSE25	Bus LVDS	100	0	0[1]	0
MLVDSE25	Multipoint LVDS 2.5 V	100	0	0[1]	0
LVPECLE33	Low-voltage positive emitter-coupled logic	100	0	0[1]	0
MIPIE25	Mobile industry processor interface 2.5 V	100	0	0[1]	0

1. The value given is the differential output voltage.

Figure 1 • Output Delay Measurement—Single-Ended Test Setup

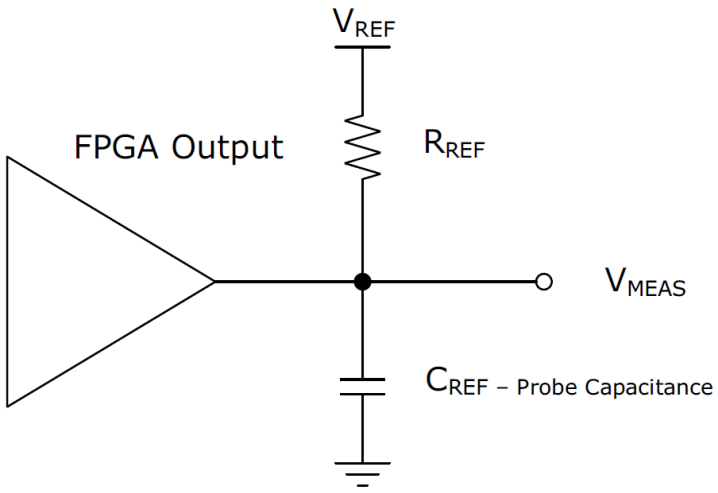
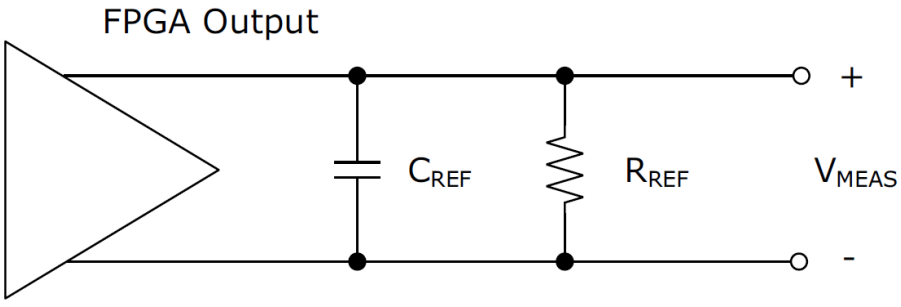


Figure 2 • Output Delay Measurement—Differential Test Setup



7.1.3 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 24 • HSIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS18	800	1250	Mbps
RSDS18	800	800	Mbps

Standard	STD	–1	Unit
MiniLVDS18	800	800	Mbps
SUBLVDS18	800	800	Mbps
PPDS18	800	800	Mbps
SLVS18	800	800	Mbps
SSTL18_I	800	1066	Mbps
SSTL18_II	800	1066	Mbps
SSTL15_I	1066	1333	Mbps
SSTL15_II	1066	1333	Mbps
SSTL135_I	1066	1333	Mbps
SSTL135_II	1066	1333	Mbps
HSTL15_I	900	1100	Mbps
HSTL15_II	900	1100	Mbps
HSTL135_I	1066	1066	Mbps
HSTL135_II	1066	1066	Mbps
HSUL18_I	400	400	Mbps
HSUL18_II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSTL12	1066	1266	Mbps
POD12_I	1333	1600	Mbps
POD12_II	1333	1600	Mbps
LVSTL11_I	1333	1600	Mbps
LVSTL11_II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps

Table 25 • GPIO Maximum Input Buffer Speed

Standard	STD	–1	Unit
LVDS25/LVDS33	800	1250	Mbps
RSDS25/RSDS33	800	800	Mbps
MINILVDS25/MINILVDS33	800	800	Mbps
SUBLVDS25/SUBLVDS33	800	800	Mbps
PPDS25/PPDS33	800	800	Mbps
SLVS25/SLVS33	800	800	Mbps
SLVSE15	800	800	Mbps
HCSL25/HCSL33	800	800	Mbps
BUSLVDSE25	800	800	Mbps
MLVDSE25	800	800	Mbps
LVPECL33	800	800	Mbps
MIPI25/MIPI33	800	800	Mbps
SSTL25_I	800	800	Mbps
SSTL25_II	800	800	Mbps

Standard	STD	–1	Unit
SSTL18_I	800	800	Mbps
SSTL18_II	800	800	Mbps
SSTL15_I	800	1066	Mbps
SSTL15_II	800	1066	Mbps
HSTL15_I	900	900	Mbps
HSTL15_II	900	900	Mbps
HSUL18_I	400	400	Mbps
HSUL18_II	400	400	Mbps
PCI33	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	300	300	Mbps

Note: All SSTLD/HSTLD/HSULD/LVSTLD/PODD type receivers use the LVDS differential receiver.

7.1.4 Output Buffer Speed

The following tables provide information about output buffer speed.

Table 26 • HSIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
SSTL18_I	800	1066	Mbps
SSTL18_II	800	1066	Mbps
SSTL18D_I	800	1066	Mbps
SSTL18D_II	800	1066	Mbps
SSTL15_I	1066	1333	Mbps
SSTL15_II	1066	1333	Mbps
SSTL15D_I	1066	1333	Mbps
SSTL15D_II	1066	1333	Mbps
SSTL135_I	1066	1333	Mbps
SSTL135_II	1066	1333	Mbps
SSTL135D_I	1066	1333	Mbps
SSTL135D_II	1066	1333	Mbps
HSTL15_I	900	1100	Mbps
HSTL15_II	900	1100	Mbps
HSTL15D_I	900	1100	Mbps
HSTL15D_II	900	1100	Mbps
HSTL135_I	1066	1066	Mbps
HSTL135_II	1066	1066	Mbps
HSTL135D_I	1066	1066	Mbps
HSTL135D_II	1066	1066	Mbps

Standard	STD	–1	Unit
HSUL18_I	400	400	Mbps
HSUL18_II	400	400	Mbps
HSUL18D_II	400	400	Mbps
HSUL12	1066	1333	Mbps
HSUL12D_I	1066	1333	Mbps
HSTL12	1066	1266	Mbps
HSTL12D_I	1066	1266	Mbps
POD12_I	1333	1600	Mbps
POD12_II	1333	1600	Mbps
LVSTL11_I	1333	1600	Mbps
LVSTL11_II	1333	1600	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps

Table 27 • GPIO Maximum Output Buffer Speed

Standard	STD	–1	Unit
LVDS25	800	1250	Mbps
RSDS25	800	800	Mbps
MINILVDS25	800	800	Mbps
SUBLVDS25	800	800	Mbps
PPDS25	800	800	Mbps
SLVSE15	500	500	Mbps
BUSLVDSE25	500	500	Mbps
MLVDSE25	500	500	Mbps
LVPECLE33	500	500	Mbps
MIPIE25	500	500	Mbps
SSTL25_I	800	800	Mbps
SSTL25_II	800	800	Mbps
SSTL25D_I	800	800	Mbps
SSTL25D_II	800	800	Mbps
SSTL18_I	800	800	Mbps
SSTL18_II	800	800	Mbps
SSTL18D_I	800	800	Mbps
SSTL18D_II	800	800	Mbps
SSTL15_I	800	1066	Mbps
SSTL15_II	800	1066	Mbps
SSTL15D_I	800	1066	Mbps
SSTL15D_II	800	1066	Mbps
HSTL15_I	900	900	Mbps
HSTL15_II	900	900	Mbps
HSTL15D_I	900	900	Mbps

Standard	STD	–1	Unit
HSTL15D_II	900	900	Mbps
HSUL18_I	400	400	Mbps
HSUL18_II	400	400	Mbps
HSUL18D_I	400	400	Mbps
HSUL18D_II	400	400	Mbps
PCI33	500	500	Mbps
LVTTL33 (20 mA)	500	500	Mbps
LVCMOS33 (20 mA)	500	500	Mbps
LVCMOS25 (16 mA)	500	500	Mbps
LVCMOS18 (12 mA)	500	500	Mbps
LVCMOS15 (10 mA)	500	500	Mbps
LVCMOS12 (8 mA)	250	300	Mbps

7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 28 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4[1]	8:1	1.8 V	1.2 V	1333	1600	167	200
DDR3	8:1	1.8 V	1.5 V	1067	1333	133	167
DDR3L	8:1	1.8 V	1.35 V	1067	1333	133	167
LPDDR3	8:1	1.8 V	1.2 V	1067	1333	133	167
LPDDR2	8:1	1.8 V	1.2 V	1067	1067	133	133
LPDDR2	4:1	1.8 V	1.2 V	600	600	150	150
QDRII+	8:1	1.8 V	1.5 V	900	1100	113	138
RLDRAM3[2]	8:1	1.8 V	1.35 V	1067	1067	133	133
RLDRAM3[2]	4:1	1.8 V	1.35 V	667	800	167	200
RLDRAM3[2]	2:1	1.8 V	1.35 V	333	400	167	200
RLDRAM2[2]	8:1	1.8 V	1.8 V	800	1067	100	133
RLDRAM2[2]	4:1	1.8 V	1.8 V	667	800	167	200
RLDRAM2[2]	2:1	1.8 V	1.8 V	333	400	167	200

1. Table represents DDR4 in the FC1152 package for all data widths without ECC and CRC enabled. DDR4 in the FCG484 and FCVG484 packages are limited to 16-bit interfaces for 1600 Mbps support.
2. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 29 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V	800	1067	100	133
QDRII+	8:1	2.5 V	1.5 V	900	900	113	113
RLDRAM2[1]	4:1	2.5 V	1.8 V	800	800	200	200

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
RLDRAM2[1]	2:1	2.5 V	1.8 V	400	400	200	200

1. RLDRAM2 is not supported with a soft IP controller currently.

7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching.

For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

Table 30 • I/O Digital Receive Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F_{MAX}	RX_SDR_G	Rx SDR							MHz	From a global clock source, aligned
F_{MAX}	RX_SDR_R	Rx SDR							MHz	From a regional clock source, aligned
F_{MAX}	RX_SDR_G_DLL	Rx SDR							MHz	From a global clock source aligned with DLL CID[1]
F_{MAX}	RX_SDR_R_DLL	Rx SDR							MHz	From a regional clock source aligned with DLL CID[1]

1. Allows the use of customer defined input delay static values to achieve timing constraints. The value of an input delay that uses the same delay step size as the DLL is specified in PLL Electrical Characteristics. (see page 40)

Table 31 • I/O Digital Receive Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
F_{MAX}	RX_DDR_G_A	Rx DDR							MHz	From a global clock source, aligned with DLL delay

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX	RX_DDR_R_A	Rx DDR							MHz	From a regional clock source, aligned with DLL delay
FMAX	RX_DDR_L_A	Rx DDR							MHz	From a Lane clock source, aligned with DLL delay
FMAX	RX_DDR_G_C	Rx DDR							MHz	From a global clock source, centered
FMAX	RX_DDR_R_C	Rx DDR							MHz	From a regional clock source, centered
FMAX	RX_DDR_L_C	Rx DDR							MHz	From a Lane clock source, centered
FMAX 2:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned with DLL delay
FMAX 4:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	
FMAX 8:1	RX_DDRX_B_A	Rx DDR digital mode							MHz	
Data valid window	RX_DDRX_B_DYN	Rx DDR digital mode							ns	From a HS_IO_CLK clock source, dynamic delay
FMAX 2:1	RX_DDRX_B_DYN	Rx DDR digital mode							MHz	
FMAX 4:1	RX_DDRX_B_DYN	Rx DDR digital mode							MHz	

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
FMAX 8:1	RX_DDRX_B_DYN	Rx DDR digital mode							MHz	

Table 32 • I/O Digital Transmit Single-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output data skew	TX_SDR_G	Tx SDR							ns	From a global clock source, aligned[1]
Output FMAX	TX_SDR_G	Tx SDR							MHz	From a global clock source, aligned[1]
Output data skew	TX_SDR_R	Tx SDR							ns	From a regional clock source, aligned[1]
Output maximum frequency	TX_SDR_R	Tx SDR							MHz	From a regional clock source, aligned[1]

1. A centered clock-to-data interface can be created with a negedge launch of the data.

Table 33 • I/O Digital Transmit Double-Data Rate Switching Characteristics

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output data skew	TX_DDR_G_A	Tx DDR							ns	From a global clock source, aligned
Output FMAX	TX_DDR_G_A	Tx DDR							MHz	From a global clock source, aligned
Output data skew	TX_DDR_R_A	Tx DDR							ns	From a regional clock source, aligned
Output FMAX	TX_DDR_R_A	Tx DDR							MHz	From a regional clock source, aligned
Output data skew	TX_DDRX_B_A	Tx DDR digital mode							ns	From a HS_IO_CLK clock source, aligned with PLL

Parameter	Interface Name	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Forwarded Clock-to-Data Skew
Output F_{MAX} 2:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned with PLL
Output F_{MAX} 4:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned with PLL
Output F_{MAX} 8:1	TX_DDRX_B_A	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, aligned with PLL
Output data skew	TX_DDRX_B_DYN	Tx DDR digital mode							ns	From a HS_IO_CLK clock source, dynamic with PLL
Output F_{MAX} 2:1	TX_DDRX_B_DYN	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, dynamic with PLL
Output F_{MAX} 4:1	TX_DDRX_B_DYN	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, dynamic with PLL
Output F_{MAX} 8:1	TX_DDRX_B_DYN	Tx DDR digital mode							MHz	From a HS_IO_CLK clock source, dynamic with PLL
In delay, out delay, DLL delay step sizes									ns	

7.1.7 I/O Digital Latency

The following table provides information about I/O digital receive double-data rate latency from pad to fabric. UI is referenced to the high-speed pin side clock period. RX latency measured from pad-to-fabric interface.

Table 34 • I/O Digital Receive Double-Data Rate Latency Characteristics

Interface Name	Gear Ratio	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
RX_SDR_G	1	Rx SDR mode		1			1		UI	From SCLK, static delay
RX_SDR_R	1	Rx SDR mode		1			1		UI	From SCLK, static delay
RX_DDR_G_A	1	Rx DDR digital mode		1			1		UI	From SCLK, static delay
RX_DDR_R_A	1	Rx DDR digital mode		1			1		UI	From SCLK, static delay
RX_DDR_L_A	1	RGMII		1			1		UI	From lane clock (DQS), static delay
RX_DDR_B_A	1	Rx DDR digital mode		1			1		UI	From a HS_IO_CLK clock source, static delay
RX_DDR_G_C	1	Rx DDR digital mode		1			1		UI	From SCLK, static delay
RX_DDR_R_C	1	Rx DDR digital mode		1			1		UI	From SCLK, static delay
RX_DDR_L_C	1	Rx DDR digital mode		1			1		UI	From lane clock (DQS), static delay
RX_DDR_B_C	1	Rx DDR digital mode		1			1		UI	From a HS_IO_CLK clock source, static delay
RX_DDRX_B_A	2	Rx DDR digital mode		4			4		UI	From a HS_IO_CLK clock source, static delay
RX_DDRX_B_A	3.5	Rx Video7		6			6		UI	From a HS_IO_CLK clock source, static delay
RX_DDRX_B_A	4	Rx DDR digital mode		7			7		UI	From a HS_IO_CLK clock source, static delay
RX_DDRX_B_A_DYN	2	Rx DDR digital mode (trained)		9			9		UI	From a HS_IO_CLK clock source, dynamic delay
RX_DDRX_B_A_DYN	3.5	Rx Video7		6			6		UI	From a HS_IO_CLK clock source, dynamic delay
RX_DDRX_B_A_DYN	4	Rx DDR digital mode (trained)		7			7		UI	From a HS_IO_CLK clock source, dynamic delay

Interface Name	Gear Ratio	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
IOD_CDR_TX	5	Rx SGMII		9			9		UI	Clock recovered from data, lane clock, dynamic delay

The following table provides information about I/O digital transmit double-data rate latency from fabric to pad. UI is referenced to the high-speed pin side clock period.

Table 35 • I/O Digital Transmit Double-Data Rate Latency Characteristics

Interface Name	Gear Ratio	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
TX_SDR_G	1	Tx SDR digital mode		1.0			1.0		UI	From a SCLK, static delay
TX_SDR_R	1	Tx SDR digital mode		1.0			1.0		UI	From a SCLK, static delay
TX_DDR_G_A	1	Tx SDR digital mode		2.5			2.5		UI	From a SCLK, static delay
TX_DDR_R_A	1	Tx DDR digital mode		2.5			2.5		UI	From a SCLK, static delay
TX_DDR_G_C	1	Tx DDR digital mode		2.5			2.5		UI	From a SCLK, static delay
TX_DDR_R_C	1	Tx DDR digital mode		2.5			2.5		UI	From a SCLK, static delay
TX_DDR_B_A	2	Tx DDR digital mode		5.5			5.5		UI	From a HS_IO_CLK clock source, static delay, with PLL
TX_DDR_B_A	3.5	Tx Video7		6.0			6.0		UI	From a HS_IO_CLK clock source, static delay, with PLL
TX_DDR_B_A	4	Tx DDR digital mode		10.5			10.5		UI	From a HS_IO_CLK clock source, static delay, with PLL

Interface Name	Gear Ratio	Topology	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit	Clock-to-Data Condition
TX_DDR_B_A	5	Tx SGMII		13.5			13.5		UI	From a HS_IO_CLK clock source, static delay
TX_DDRX_B_A_DYN	2	Tx DDR digital mode (trained)		5.5			5.5		UI	From a HS_IO_CLK clock source, dynamic delay, with PLL
TX_DDRX_B_A_DYN	4	Tx DDR digital mode (trained)		10.5			10.5		UI	From a HS_IO_CLK clock source, dynamic delay, with PLL

7.1.8 I/O Digital Training Calibration

The following tables provide information about I/O digital training calibration.

Table 36 • I/O Digital Training Calibration

Parameter	I/O Type	STD Min	STD Max	–1 Min	–1 Max	Unit
User initiated I/O calibration	GPIO		2.2		2.2	ns
	HSIO		2.2		2.2	ns

Table 37 • I/O Digital Training Timing

Parameter	I/O Type	STD Min	STD Max	–1 Min	–1 Max	Unit
User initiated I/O training	RX_SDR_G					ns
	RX_SDR_R					ns
	RX_DDR_G_A					ns
	RX_DDR_R_A					ns
	RX_DDR_L_A					ns
	RX_DDR_B_A					ns
	RX_DDR_G_C					ns
	RX_DDR_R_C					ns
	RX_DDR_L_C					ns
	RX_DDR_B_C					ns
	RX_DDRX_B_A					ns
	RX_DDRX_B_A					ns
	RX_DDRX_B_A					ns
	RX_DDRX_B_A_DYN					ns
	RX_DDRX_B_A_DYN					ns
	RX_DDRX_B_A_DYN					ns
	IOD_CDR_TX					ns
	TX_SDR_G					ns
	TX_SDR_R					ns
	TX_DDR_G_A					ns
	TX_DDR_R_A					ns
	TX_DDR_G_C					ns
	TX_DDR_R_C					ns
	TX_DDRX_B_A					ns
	TX_DDRX_B_A					ns
	TX_DDRX_B_A					ns
	TX_DDRX_B_A					ns
	TX_DDRX_B_DYN					ns
	TX_DDRX_B_DYN					ns

7.2 Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

7.2.1 Clocking

The following table provides clocking specifications from 0 °C to 100 °C.

Table 38 • Global and Regional Clock Characteristics (0 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Global clock F_{MAX}	F_{MAXG}					MHz	

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Regional clock F_{MAX}	F_{MAXR}					MHz	
Global clock skew	F_{SKEWG}					ps	
Regional clock skew	F_{SKEWR}					ps	
Global clock duty cycle distortion	T_{DCD}					ps	
Regional clock duty cycle distortion	T_{DCD}					ps	

The following table provides clocking specifications from –40 °C to 100 °C.

Table 39 • Global and Regional Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Global clock F_{MAX}	F_{MAXG}					MHz	
Regional clock F_{MAX}	F_{MAXR}					MHz	
Global clock skew	F_{SKEWG}					ps	
Regional clock skew	F_{SKEWR}					ps	
Global clock duty cycle distortion	T_{DCD}					ps	
Regional clock duty cycle distortion	T_{DCD}					ps	

The following table provides clocking specifications from 0 °C to 100 °C.

Table 40 • High-Speed I/O Clock Characteristics (0 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F_{MAX}	F_{MAXB}	1000	1250	1000	1250	MHz	HSIO without bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	HSIO with bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	GPIO without bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	GPIO with bridging
High-speed I/O clock skew	F_{SKEWB}	40	30	40	30	ps	HSIO without bridging
	F_{SKEWB}	900	700	800	600	ps	HSIO with bridging
	F_{SKEWB}	60	60	60	60	ps	GPIO without bridging
	F_{SKEWB}	900	700	800	600	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion	T_{DCB}	1000	1250	1000	1250	MHz	HSIO without bridging
	T_{DCB}	1000	1250	1000	1250	MHz	HSIO with bridging
	T_{DCB}	1000	1250	1000	1250	MHz	GPIO without bridging
	T_{DCB}	1000	1250	1000	1250	MHz	GPIO with bridging

The following table provides clocking specifications from –40 °C to 100 °C.

Table 41 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
High-speed I/O clock F_{MAX}	F_{MAXB}	1000	1250	1000	1250	MHz	HSIO without bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	HSIO with bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	GPIO without bridging
	F_{MAXB}	1000	1250	1000	1250	MHz	GPIO with bridging
High-speed I/O clock skew	F_{SKEWB}	40	30	40	30	ps	HSIO without bridging
	F_{SKEWB}	1000	700	800	600	ps	HSIO with bridging
	F_{SKEWB}	60	60	60	60	ps	GPIO without bridging
	F_{SKEWB}	1000	700	800	600	ps	GPIO with bridging
High-speed I/O clock duty cycle distortion	T_{DCB}	60	60	60	60	ps	HSIO without bridging
	T_{DCB}	60	60	60	60	ps	HSIO with bridging
	T_{DCB}	60	60	60	60	ps	GPIO without bridging
	T_{DCB}	60	60	60	60	ps	GPIO with bridging

7.2.2 PLL

The following table provides information about PLL.

Table 42 • PLL Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input clock frequency (integer mode)	F_{INI}	1		1250	MHz
Input clock frequency (fractional mode)	F_{INF}	10		1250	MHz
Minimum reference or feedback pulse width[1]	$F_{INPULSE}$	200			ps
Frequency at the Frequency Phase Detector (PFD) (integer mode)	F_{PHDETI}	1		312	MHz
Frequency at the PFD (fractional mode)	F_{PHDETF}	10		250	MHz
Allowable input duty cycle	F_{INDUTY}	25		75	%
Maximum input period clock jitter (reference and feedback clocks)[2]	F_{MAXINJ}		120	1000	ps
PLL VCO frequency	F_{VCO}	800		5000	MHz
Low PLL bandwith	F_{BW}	F_{PHDET}/25		F_{PHDET}/15	MHz

Parameter	Symbol	Min	Typ	Max	Unit
High PLL bandwith[3]	F_{BW}	F_{PHDET}/50		F_{PHDET}/25	MHz
Static phase offset of the PLL outputs[4]	T_{SPO}	–60		60	ps
	$T_{OUTJITTER}$				ps
PLL output duty cycle precision	$T_{OUTDUTY}$	48.5		51.5	%
PLL lock time[5]	T_{LOCK}		375	625	Cycles
PLL unlock time[6]	T_{UNLOCK}	2		LOCKCOUNT/4	PFD cycles
PLL output frequency	FOUT	0.050		1250	MHz
Minimum reset pulse width	T_{MRPW}				uS
Maximum delay in the feedback path[7]	F_{MAXDFB}			1.5	PFD cycles
Spread spectrum modulation spread[8]	Mod_Spread	0.1		3.1	%
Spread spectrum modulation frequency[9]	Mod_Freq	F_{PHDETF}/(128)	32	F_{PHDETF}/(128 × 63)	KHz

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Medium PLL bandwidth keeps the rest of the line blank.
4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F_{REF}. For example, F_{REF} = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.2.3 DLL

The following table provides information about DLL.

Table 43 • DLL Electrical Characteristics

Parameter[1]	Symbol	Min	Typ	Max	Unit
Input reference clock frequency	F_{INF}	133		800	MHz
Input feedback clock frequency	F_{INFDBF}	133		800	MHz
Primary output clock frequency	F_{OUTPF}	133		800	MHz
Secondary output clock frequency[2]	F_{OUTSF}	33.3		800	MHz
Input clock jitter[3]	F_{INJ}			200	ps
Output clock period jitter (w/clean input)[3]	$T_{OUTJITTERP}$			300	ps
Output clock-to-clock skew between two outputs with the same phase settings	T_{SKEW}			200	ps
DLL lock time[4]	T_{LOCK}	16		16K	cycles
Minimum reset pulse width	T_{MRPW}	3			ns
Minimum input pulse width[5]	T_{MIPW}	20			ns
Minimum clock pulse width high[6]	T_{MPWH}	400			ps
Minimum clock pulse width low[6]	T_{MPWL}	400			ps
Delay step size	T_{DEL}	14	25	36	ps
Maximum delay block delay[7]	T_{DELMAX}	2.3	4	6.1	ns
Output clock duty cycle (w/ 50% duty cycle input)[8]	T_{DUTY}	40		60	%

Parameter[1]	Symbol	Min	Typ	Max	Unit
Output clock duty cycle (in phase reference mode)[8]	T_{DUTY50}	45		55	%

1. For all DLL modes.
2. CLKOS divided by four option.
3. Cycle-to-cycle jitter.
4. Number of reference clock cycles.
5. On load, direction, move, hold, and update input signals.
6. On clock input.
7. 128 delay taps in one delay block.
8. Without duty cycle correction enabled.

7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

Table 44 • 2 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{2FREQ}		2		MHz
Accuracy	RC_{2FACC}	–4		4	%
Duty cycle	RC_{2DC}	48		51	%
Peak-to-peak output period jitter	RC_{2PJIT}	600		900	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{2CJIT}	100		250	ps
Operating current (V_{DD25})	RC_{2IVPPA}			48	µA
Operating current (V_{DD18})	RC_{2IVPP}			0	µA
Operating current (V_{DD})	RC_{2IVDD}			2.6	µA

Table 45 • 160 MHz RC Oscillator Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating frequency	RC_{SCFREQ}		160		MHz
Accuracy	RC_{SCFACC}	–4		4	%
Duty cycle	RC_{SCDC}	47		52	%
Peak-to-peak output period jitter	RC_{SCPJIT}	130		600	ps
Peak-to-peak output cycle-to-cycle jitter	RC_{SCCJIT}	60		172	ps
Operating current (V_{DD25})	RC_{SCVPPA}			599	µA
Operating current (V_{DD18})	RC_{SCVPP}			0.1	µA
Operating current (V_{DD})	RC_{SCVDD}			60.7	µA

7.3 Fabric Specifications

The following section describes specifications for the fabric.

7.3.1 Math Blocks

The following tables describe math block performance.

Table 46 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	370	470	440	545
	F_{MAX}	18 × 18 multiplication summed with 48-bit input	370	470	440	545
	F_{MAX}	18 × 19 multiplier pre-adder ROM mode	365	465	435	540
	F_{MAX}	Two 9 × 9 multiplication	370	470	440	545
	F_{MAX}	9 × 9 dot product (DOTP)	370	470	440	545
	F_{MAX}	Complex 18 × 19 multiplication	360	455	430	530

Table 47 • Math Block Performance Industrial Range (–40 °C to 100 °C)

Parameter	Symbol	Modes	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1
Maximum operating frequency	F_{MAX}	18 × 18 multiplication	365	465	435	545
	F_{MAX}	18 × 18 multiplication summed with 48-bit input	365	465	435	545
	F_{MAX}	18 × 19 multiplier pre-adder ROM mode	355	460	430	540
	F_{MAX}	Two 9 × 9 multiplication	365	465	435	545
	F_{MAX}	9 × 9 DOTP	365	465	435	545
	F_{MAX}	Complex 18 × 19 multiplication	350	450	425	530

7.3.2 LSRAM Blocks

The following tables describe the LSRAM blocks' performance.

Table 48 • LSRAM Performance Extended Commercial Temperature Range (0 °C to 100 °C)

Parameter	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Operating frequency	342	428	342	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple- write, and write-feed-through
	342	428	342	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple- write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple- write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple- write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read- before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read- before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read- before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 49 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)

Parameter	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Operating frequency	342	428	342	428	MHz	Two-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	342	428	342	428	MHz	Dual-port, all supported widths, pipelined, simple-write, and write-feed-through
	309	428	309	428	MHz	Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through
	279	295	279	295	MHz	Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through
	343	428	343	428	MHz	Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	196	285	196	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through
	274	285	274	285	MHz	Two-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, pipelined, and read-before-write
	274	285	274	285	MHz	Dual-port, all supported widths, non-pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port non-pipelined ECC mode, pipelined, and read-before-write
	274	285	274	285	MHz	Two-port pipelined ECC mode, non-pipelined, and read-before-write
	193	285	193	285	MHz	Two-port non-pipelined ECC mode, non-pipelined, and read-before-write

Table 50 • µSRAM Performance

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit	Condition
Operating frequency	F_{MAX}	400	415	450	480	MHz	Write-port
Read access time	Tac		2		2	ns	Read-port

Table 51 • µPROM Performance

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit
Read access time	Tac	10	10	10	10	ns

7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

7.4.1 Transceiver Performance

The following table describes transceiver performance.

Table 52 • PolarFire Transceiver and TXPLL Performance

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Tx data rate[1]	F_{TXRate}	0.25		10.3125	0.25		12.7	Gbps
Tx OOB (serializer bypass) data rate	$F_{TXRateOOB}$	DC		1.5	DC		1.5	Gbps
Rx data rate when AC coupled	$F_{RxRateAC}$	0.25		10.3125	0.25		12.7	Gbps
Rx data rate when DC coupled	$F_{RxRateDC}$	0.25		3.2	0.25		3.2	Gbps
Rx OOB (deserializer bypass) data rate	$F_{TXRateOOB}$	DC		1.25	DC		1.25	Gbps
TXPLL output frequency[2]	F_{TXPLL}	1.6		6.35	1.6		6.35	GHz

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. The Tx PLL rate is between 0.5x to 5.5x. The Tx data rate depends on per XCVR lane Tx post-divider settings.

7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

Table 53 • PolarFire Transceiver Reference Clock AC Requirements

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
Reference clock input rate[1, 2]	$F_{TXREFCLK}$	20		800	20		800	MHz
Reference clock input rate[1, 2, 3]	$F_{XCVRREFCLKMAX\ CASCADE}$	20			20			MHz
Reference clock rate at the PFD[4]	$F_{TXREFCLKPFD}$	20		156	20		156	MHz
Reference clock rate recommended at the	$F_{TXREFCLKPFD10G}$	75		156	75		156	MHz

Parameter	Symbol	STD Min	STD Typ	STD Max	–1 Min	–1 Typ	–1 Max	Unit
PFD for Tx rates 10 Gbps and above[4]								
Tx reference clock phase noise requirements to meet jitter specifications (622 MHz clock at reference clock input)[5]	$F_{TXREFPN}$							
Phase noise at 1 KHz	$F_{TXREFPN}$			–105			–105	dBc/Hz
Phase noise at 10 KHz	$F_{TXREFPN}$			–110			–110	dBc/Hz
Phase noise at 100 KHz	$F_{TXREFPN}$			–115			–115	dBc/Hz
Phase noise at 1 MHz	$F_{TXREFPN}$			–135			–135	dBc/Hz
Reference clock input rise time (10%–90%)	$T_{REFRISE}$		200	500		200	500	ps
Reference clock input fall time (90%–10%)	$T_{REFFALL}$		200	500		200	500	ps
Reference clock duty cycle	$T_{REFDUTY}$	40		60	40		60	%
Spread spectrum modulation spread[6]	Mod_Spread	0.1		3.1	0.1		3.1	%
Spread spectrum modulation frequency[7]	Mod_Freq	F_{PHDETF}/ (128)	32	F_{PHDETF}/ (128 × 63)	F_{PHDETF}/ (128)	32	F_{PHDETF}/ (128 × 63)	KHz

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClk}$ value by 20 × log10 (TxRefClk/622 MHz).
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

7.4.3 Transceiver Reference Clock I/O Standards

The following table describes the differential DC input levels.

Table 54 • Transceiver Differential Reference Clock I/O Standards

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{ICM}[1] Min	V_{ICM} Typ	V_{ICM} Max[3]	V_{ID}[2] Min	V_{ID} Typ	V_{ID} Max	Unit
LVDS25	2.375	2.500	2.625	0.05	1.25	2.35	0.1	0.35	0.6	V
HCSL25 (for PCIe)	2.375	2.500	2.625	0.05	0.35	2.35	0.1	0.55	1.1	V

1. V_{ICM} is the input common mode.
2. V_{ID} is the input differential voltage.
3. V_{ICM} must be less than $V_{DD\_XCVR\_CLK}$ – .3 V.

Note: The transceiver reference clock differential receiver supports V_{CM} common mode.

Note: The maximum signal range into the reference clock input buffer for optimal performance is defined as $V_{IHMAX} = V_{CM} + 0.5\ V_{ID} < V_{DD\_XCVR\_CLK}$ and V_{ILMIN} must be >0 V.

7.4.4 Transceiver Interface Performance

The following table describes transceiver interface performance.

Table 55 • Transceiver Single-Ended Reference Clock I/O Standards

I/O Standard	V_{DDI} Min	V_{DDI} Typ	V_{DDI} Max	V_{ICM}[1] Min	V_{ICM}[1] Max	V_{ID}[2] Min	V_{ID}[2] Max	Unit
SSTL18I[1]	1.71	1.8	1.89	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	1.89	V
LVCMOS25	2.375	2.5	2.625	–0.3	0.7	1.7	2.625	V

7.4.5 Transmitter Performance

The following tables describe performance of the transmitter.

Table 56 • Transceiver Reference Clock Input Termination

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended termination	RefTerm		50		Ω
Single-ended termination	RefTerm		75		Ω
Single-ended termination	RefTerm		150		Ω
Differential termination	RefDiffTerm		100		Ω
Power-up termination			>50K		Ω

Table 57 • PolarFire Transceiver User Interface Clocks

Parameter	Modes[1]	STD Min	STD Max	–1 Min	–1 Max	Unit
Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 12.7 Gbps				320	MHz
	64-bit, max data rate = 12.7 Gbps				200	MHz
	80-bit, max data rate = 12.7 Gbps				162.5	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 12.7 Gbps				320	MHz
	64-bit, max data rate = 12.7 Gbps				200	MHz
	80-bit, max data rate = 12.7 Gbps				162.5	MHz
	Fabric pipe mode 32-bit, max data rate = 6.0 Gbps		150		150	MHz
Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 12.7 Gbps				320	MHz
	64-bit, max data rate = 12.7 Gbps				200	MHz
	80-bit, max data rate = 12.7 Gbps				160	MHz
Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks)	8-bit, max data rate = 1.6 Gbps		200		200	MHz
	10-bit, max data rate = 1.6 Gbps		160		160	MHz
	16-bit, max data rate = 4.8 Gbps		300		300	MHz
	20-bit, max data rate = 6.0 Gbps		300		300	MHz
	32-bit, max data rate = 10.3125 Gbps		325		325	MHz
	40-bit, max data rate = 12.7 Gbps				320	MHz
	64-bit, max data rate = 12.7 Gbps				200	MHz
	80-bit, max data rate = 12.7 Gbps				160	MHz

1. Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

Table 58 • PolarFire Transceiver Transmitter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Differential termination	V_{OTERM}	68	85	102	Ω	50K Ω power-up
	V_{OTERM}	80	100	120	Ω	
	V_{OTERM}	120	150	180	Ω	
Common mode voltage[1]	V_{OCM}		0.525 × V_{DDA}		V	DC coupled 50% setting
	V_{OCM}		0.6 × V_{DDA}		V	DC coupled 60% setting
	V_{OCM}		0.7 × V_{DDA}		V	DC coupled 70% setting
	V_{OCM}		0.8 × V_{DDA}		V	DC coupled 80% setting
Rise time[2]	T_{TxRF}	20		40	ps	20% to 80%
Fall time[2]		20		40	ps	80% to 20%
Differential peak-to-peak amplitude[3]	V_{ODPP}	100		1350	mV	Minimum to maximum settings
	V_{ODPP}		1000		mV	1000 mV setting
	V_{ODPP}		800		mV	800 mV setting
	V_{ODPP}		600		mV	600 mV setting
	V_{ODPP}		500		mV	500 mV setting
	V_{ODPP}		400		mV	400 mV setting
	V_{ODPP}		300		mV	300 mV setting
	V_{ODPP}		200		mV	200 mV setting
	V_{ODPP}		100		mV	100 mV setting
Transmit lane P to N skew[4]	T_{OSKEW}			20	ps	
Lane to lane transmit skew [5, 6, 7]	T_{LLSKEW}			200	ps	Single PLL
	T_{LLSKEW}				ps	Multiple PLL
Electrical idle transition entry time[8]	$T_{TxEITrEntry}$				ns	
Electrical idle transition exit time[8]	$T_{TxEITrExit}$				ns	
Electrical idle amplitude	V_{TxEIpp}			15	mV	
TXPLL lock time	T_{Lock}				REFCLK UIs	
Digital PLL lock time[9]	$T_{DPLLLock}$			15K	REFCLK UIs	For Tx jitter cleaner applications
Total jitter[10, 11, 12]	T_J				UI	Rate ≥8.5 Gbps to 12.7 Gbps
Deterministic jitter[10, 11, 12]	T_{DJ}				UI	Tx V_{CO} rate 4.25 GHz to 6.35 GHz
Total jitter[10, 11, 12]	T_J				UI	Rate ≥3.2 Gbps to 8.5 Gbps
Deterministic jitter[10, 11, 12]	T_{DJ}				UI	Tx V_{CO} rate 2.5 GHz to 5.0 GHz
Total jitter[10, 11, 12]	T_J				UI	Rate ≥1.6 Gbps to 3.2 Gbps
Deterministic jitter[10, 11, 12]	T_{DJ}				UI	Tx V_{CO} rate 2.5 GHz to 5.0 GHz
Total jitter[10, 11, 12]	T_J				UI	Rate ≥ 800 Mbps to 1.6 Gbps
Deterministic jitter[10, 11, 12]	T_{DJ}				UI	Tx V_{CO} rate 2.5 GHz to 5.0 GHz
Total jitter[10, 11, 12]	T_J				UI	Rate = 250 Mbps to 800 Mbps
Deterministic jitter[10, 11, 12]	T_{DJ}				UI	Tx V_{CO} rate 2.5 GHz to 5.0 GHz
Additional Total jitter in Frac mode[13]	T_{JFRAC}				UI	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Additional deterministic jitter in Frac mode[13]	T_{DJFRAC}				UI	

1. Increased DC common mode settings above 50% reduce allowed V_{OD} output swing capabilities.
2. Adjustable through transmit emphasis.
3. V_{DDA} = 1.0 V ±30 mV.
4. With estimated package differences.
5. Single PLL applies to all four lanes in the same quad location with the same TxPLL.
6. Multiple PLL applies to N lanes using multiple TxPLLs from different quad locations.
7. For more information about how to transmit align multiple lanes from different quad locations, see *UG0677: PolarFire FPGA Transceiver User Guide*.
8. From the PMA mode, the TX_ELEC_IDLE port to the XCVR TXP/N pins.
9. FTxRefClk = 75 MHz with typical settings.
10. Jitter measurements are obtained using the TXPL_SSC and/or TXPLL in integer mode with the slowest possible V_{CO} rate with a reference clock of at least 100 MHz that meets the input phase noise specifications.
11. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher V_{CO} rate used.
12. Tx jitter is specified with all transmitters on the device enabled, a 10-12 bit error rate (BER) and Tx data pattern of PRBS2[7].
13. Additional T_J when Fractional-N mode is enabled.

7.4.6 Receiver Performance

The following table describes performance of the receiver.

Table 59 • PolarFire Transceiver Receiver Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input voltage range	V_{IN}	0		V_{DDA} + 0.3	V	
Differential peak-to-peak amplitude	V_{IDPP}	140		1250	mV	
Differential termination	V_{ITERM}	68	85	102	Ω	50K Ω power-up
	V_{ITERM}	80	100	120	Ω	50K Ω power-up
	V_{ITERM}	120	150	180	Ω	50K Ω power-up
Common mode voltage	V_{ICMAC}		1.0 × V_{DDA}		V	AC coupled
Common mode voltage	V_{ICMDC}[1]	0.7 × V_{DDA}		0.9 × V_{DDA}	V	DC coupled
Electrical idle detect threshold (differential)	V_{EIDET}	60		300	mV	
Exit electrical idle detection time	T_{EIDET}		50	100	ns	
Run length of consecutive identical digits (CID)	C_{ID}			85	UI	
CDR PPM tolerance[2]	C_{DRPPM}			1.15	% UI	
CDR lock-to-data time	T_{LTD}		512		CDR_{REFCLK} UIs	
CDR lock-to-ref time	T_{LTF}	512		1024	CDR_{REFCLK} UIs	
Loss-of-signal detect threshold-low	V_{DETLOW}			65[3]	mV	Setting = PCIe
	V_{DETLOW}			75[4]	mV	Setting = SATA
	V_{DETLOW}					Setting = 1
	V_{DETLOW}					Setting = 2
	V_{DETLOW}					Setting = 3
	V_{DETLOW}					Setting = 4
	V_{DETLOW}					Setting = 5
	V_{DETLOW}					Setting = 6
	V_{DETLOW}					Setting = 7
Loss-of-signal detect threshold-high	$V_{DETHIGH}$	175[4]			mV	Setting = PCIe
	$V_{DETHIGH}$	200[4]			mV	Setting = SATA
	$V_{DETHIGH}$					Setting = 1
	$V_{DETHIGH}$					Setting = 2
	$V_{DETHIGH}$					Setting = 3
	$V_{DETHIGH}$					Setting = 4
	$V_{DETHIGH}$					Setting = 5
	$V_{DETHIGH}$					Setting = 6
	$V_{DETHIGH}$					Setting = 7
Sinusoidal jitter tolerance	T_{SJTOL}				UI	>8.5–12.7 Gbps[4]
					UI	>3.2–8.5 Gbps[5]
					UI	>1.6 to 3.2 Gbps[5]
					UI	>0.8 to 1.6 Gbps[6]
					UI	250 to 800 Mpbs[6]
	$T_{TJTOLSE}$				UI	3.125 Gbps[5]

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Total jitter tolerance with stressed eye					UI	6.25 Gbps[5]
					UI	10.3125 Gbps[5]
					UI	12.5 Gbps[5]
Sinusoidal jitter tolerance with stressed eye	$T_{SJTOLSE}$				UI	3.125 Gbps[5]
					UI	6.25 Gbps[5]
					UI	10.3125 Gbps[5]
					UI	12.5 Gbps[5]
CTLE DC gain (all stages, max settings)				10	dB	
CTLE AC gain (all stages, max settings)				16	dB	
DFE AC gain (per 5 stages, max settings)				14	dB	
CTLE auto adaptive calibration time					us	
CTLE + DFE auto adaptive calibration time					us	

1. Valid at 3.2 Gbps and below.
2. Data vs. Rx reference clock frequency.
3. Achieves compliance with PCIe electrical idle detection.
4. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV V_{ID}, single stage of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
5. Rx jitter values based on BER of 10–12, AC coupled input with 400 mV V_{ID}, Rx CTLE disabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.

7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

7.5.1 PCI Express

The following tables describes the PCI express.

Table 60 • PCI Express Gen1

	Data Rate	Min	Max	Unit
Total transmit jitter	2.5 Gbps			UI
Receiver jitter tolerance	2.5 Gbps			UI

Table 61 • PCI Express Gen2

	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps			UI
Receiver jitter tolerance	5.0 Gbps			UI

7.5.2 10GbE (XAUI, RXAUI, 10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (XAUI).

Table 62 • 10GbE (XAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps			UI
Receiver jitter tolerance	3.125 Gbps			UI

The following table describes 10GbE (RXAUI).

Table 63 • 10GbE (RXAUI)

	Data Rate	Min	Max	Unit
Total transmit jitter	6.25 Gbps			UI
Receiver jitter tolerance	6.25 Gbps			UI

The following table describes 10GbE (10GBASE-R).

Table 64 • 10GbE (10GBASE-R)

	Data Rate	Min	Max	Unit
Total transmit jitter	10.3125 Gbps			UI
Receiver jitter tolerance	10.3125 Gbps			UI

The following table describes 10GbE (10GBASE-KR).

Table 65 • 10GbE (10GBASE-KR)

	Data Rate	Min	Max	Unit
Total transmit jitter	12.5 Gbps			UI
Receiver jitter tolerance	12.5 Gbps			UI

7.5.3 1GbE (SGMII, 1000BASE-T, 1000BASE-X, and QSGMII)

The following table describes 1GbE (SGMII).

Table 66 • 1GbE (SGMII)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-T).

Table 67 • 1GbE (1000BASE-T)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (1000BASE-X).

Table 68 • 1GbE (1000BASE-X)

	Data Rate	Min	Max	Unit
Total transmit jitter	1.25 Gbps			UI
Receiver jitter tolerance	1.25 Gbps			UI

The following table describes 1GbE (QSGMII).

Table 69 • 1GbE (QSGMII)

	Data Rate	Min	Max	Unit
Total transmit jitter	5.0 Gbps			UI
Receiver jitter tolerance	5.0 Gbps			UI

7.5.4 CPRI

The following table describes CPRI.

Table 70 • CPRI

	Data Rate	Min	Max	Unit
Total transmit jitter	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps			UI
Receive jitter tolerance	0.6144 Gbps			UI
	1.2288 Gbps			UI
	2.4576 Gbps			UI
	3.0720 Gbps			UI
	4.9152 Gbps			UI
	6.1440 Gbps			UI
	9.8304 Gbps			UI
	10.1376 Gbps			UI
	12.16512 Gbps			UI

7.5.5 JESD204B

The following table describes JESD204B.

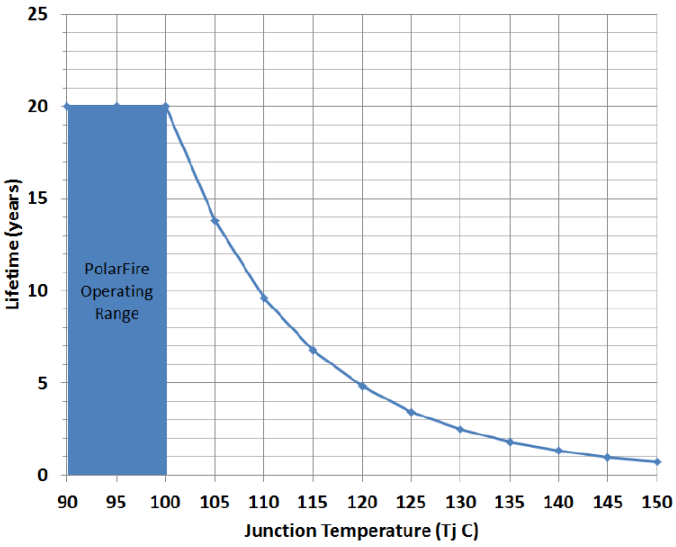
Table 71 • JESD204B

	Data Rate	Min	Max	Unit
Total transmit jitter	3.125 Gbps			UI
	6.25 Gbps			UI
	12.5 Gbps			UI
Receive jitter tolerance	3.125 Gbps			UI
	6.25 Gbps			UI
	12.5 Gbps			UI

7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

Figure 3 • High-Temperature Retention (HTR) Curve



7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

Table 72 • FPGA Programming Cycles vs Retention Characteristics

Programming T J	Programming Cycles, Max	Retention Years	Retention Years at T J
0 °C to 85 °C	1000	20	85 °C
0 °C to 100 °C	500	20	100 °C
–20 °C to 100 °C	500	20	100 °C
–40 °C to 100 °C	500	20	100 °C
–40 °C to 85 °C	1000	16	100 °C
–40 °C to 55 °C	2000	12	100 °C

Note: Power supplied to the device must be valid during programming operations such as programming, verify, zeroization, and digest checks. Programming recovery mode is available only for in-application programming mode and requires an external SPI flash. A Zeroization operation is counted as one programming cycle.

7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

Table 73 • Master SPI Programming Time (IAP)

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	30		s
		MPF300T, TL, TS, TLS	50		s
		MPF500T, TL, TS, TLS	55		s

Table 74 • Slave SPI Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	35		s
		MPF300T, TL, TS, TLS	58		s
		MPF500T, TL, TS, TLS	63		s

Table 75 • JTAG Programming Time

Parameter	Symbol	Devices	Typ	Max	Unit
Programming time	T_{PROG}	MPF100T, TL, TS, TLS			s
		MPF200T, TL, TS, TLS	35		s
		MPF300T, TL, TS, TLS	58		s
		MPF500T, TL, TS, TLS	63		s

7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

Table 76 • Bitstream Sizes

Devices	.SPI File Size	.STPL File Size	Unit
MPF100T, TL, TS, TLS	3.41	5.44	MB
MPF200T, TL, TS, TLS	5.9	9.4	MB
MPF300T, TL, TS, TLS	9.1	14.4	MB
MPF500T, TL, TS, TLS	14.4	22.8	MB

7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

Table 77 • Maximum Number of Digest Cycles

		Retention Since Programmed. N = Number Digests During that Time[1]								
Digest T_J	**Storage and Operating T_J**	**N ≤300**	**N = 500**	**N = 1000**	**N = 1500**	**N = 2000**	**N = 4000**	**N = 6000**	**Unit**	**Retention**
–40 to 100	–40 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 100	0 to 100	20 × LF	17 × LF	12 × LF	10 × LF	8 × LF	4 × LF	2 × LF	°C	Years
–40 to 85	–40 to 85	20 × LF	20 × LF	20 × LF	20 × LF	16 × LF	8 × LF	4 × LF	°C	Years
–40 to 55	–40 to 55	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	20 × LF	°C	Years

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

Table 78 • FPGA Programming Cycles Lifetime Factor

Programming T_J	Programming Cycles	LF
–40 °C to 100 °C	500	1
–40 °C to 85 °C	1000	0.8
–40 °C to 55 °C	2000	0.6

Note: The maximum number of device digest cycles is 100K.

Note: Digests are operational only over the –40 °C to 100 °C temperature range.

Note: After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.

Note: Retention is specified for total device storage and operating temperature.

Note: All temperatures are junction temperatures (T_J).

Note: Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C T_J. 501 programming cycles are occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.

Note: Example 2—programming cycle has occurred, N = 1500 digest cycles are occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

7.6.5 Digest Time

The following table describes digest time.

Table 79 • Digest Times

Parameter	Devices	Typ	Max	Unit
Setup time	All	2		us
Fabric digest run time	MPF100T, TL,TS, TLS			ms
	MPF200T, TL,TS, TLS	957		ms
	MPF300T, TL,TS, TLS	1451		ms
	MPF500T, TL,TS, TLS	1876		ms

Parameter	Devices	Typ	Max	Unit
UFS CC digest run time	MPF100T, TL, TS, TLS			us
	MPF200T, TL, TS, TLS	28		us
	MPF300T, TL, TS, TLS	28		us
	MPF500T, TL, TS, TLS	28		us
sNVM digest run time[1]	MPF100T, TL, TS, TLS			ms
	MPF200T, TL, TS, TLS			ms
	MPF300T, TL, TS, TLS			ms
	MPF500T, TL, TS, TLS			ms
UFS UL digest run time	MPF100T, TL, TS, TLS			us
	MPF200T, TL, TS, TLS	41		us
	MPF300T, TL, TS, TLS	41		us
	MPF500T, TL, TS, TLS	41		us
User key digest run time[2]	MPF100T, TL, TS, TLS			us
	MPF200T, TL, TS, TLS	564		us
	MPF300T, TL, TS, TLS	564		us
	MPF500T, TL, TS, TLS	564		us
UFS UPERM digest run time	MPF100T, TL, TS, TLS			us
	MPF200T, TL, TS, TLS	28		us
	MPF300T, TL, TS, TLS	28		us
	MPF500T, TL, TS, TLS	28		us
Factory digest run time	MPF100T, TL, TS, TLS			us
	MPF200T, TL, TS, TLS	461		us
	MPF300T, TL, TS, TLS	461		us
	MPF500T, TL, TS, TLS	461		us

1. The entire sNVM is used as ROM.
2. Valid for User key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 80 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			seconds	Full scrubbing

Parameter	Typ	Max	Unit	Conditions
Time to scrub the pNVM data (like new)[1, 2]			seconds	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			seconds	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]			seconds	Full scrubbing
Time to verify[5]			seconds	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 81 • Zeroization Times for MPF200T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization			ms	Zip flag set
Time to destroy the fabric data[1]			ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]			ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]			ms	One iteration of scrubbing
Time to scrub the fabric data[1]			seconds	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]			seconds	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]			seconds	Full scrubbing
Time to scrub the fabric data PNVM data (non-recoverable)[1, 4]			seconds	Full scrubbing
Time to verify[5]			seconds	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 82 • Zeroization Times for MPF300T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization	8.7		ms	Zip flag set
Time to destroy the Fabric data[1]	34.3		ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]	801		ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]	860		ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non- recoverable)[1, 4]	909.9		ms	One iteration of scrubbing
Time to scrub the fabric data[1]	1.151		seconds	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]	2.4		seconds	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]	2.58		seconds	Full scrubbing

Parameter	Typ	Max	Unit	Conditions
Time to scrub the fabric data pNVM data (non-recoverable)[1, 4]	2.73		seconds	Full scrubbing
Time to verify[5]	1.57		seconds	

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

Table 83 • Zeroization Times for MPF500T, TL, TS, and TLS Devices

Parameter	Typ	Max	Unit	Conditions
Time to enter zeroization	8.7		ms	Zip flag set
Time to destroy the fabric data[1]	34.3		ms	Data erased
Time to destroy data in non-volatile memory (like new)[1, 2]	801		ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (recoverable)[1, 3]	860		ms	One iteration of scrubbing
Time to destroy data in non-volatile memory (non-recoverable)[1, 4]	909.9		ms	One iteration of scrubbing
Time to scrub the fabric data[1]	1.151		seconds	Full scrubbing
Time to scrub the pNVM data (like new)[1, 2]	2.4		seconds	Full scrubbing
Time to scrub the pNVM data (recoverable)[1, 3]	2.58		seconds	Full scrubbing
Time to scrub the fabric data pNVM data (non-recoverable)[1,	2.73		seconds	Full scrubbing
Time to verify[5]	1.74		seconds	

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

7.6.7 Verify Time

The following tables describe verify time.

Table 84 • Standalone Fabric Verify Times

Parameter	Devices	Typ	Max	Unit
Standalone verification over JTAG	MPF100T, TL, TS, TLS			s
	MPF200T, TL, TS, TLS			s
	MPF300T, TL, TS, TLS			s
	MPF500T, TL, TS, TLS			s
Standalone verification over SPI	MPF100T, TL, TS, TLS			s
	MPF200T, TL, TS, TLS			s
	MPF300T, TL, TS, TLS			s
	MPF500T, TL, TS, TLS			s

Note: Standalone verify is limited to 2000 total device hours over the industrial –40 °C to 100 °C temperature.

Note: Use the digest system service, for verify device time more than 2000 hours.

Note: Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.

Note: Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2000 hour verify time specification.

Table 85 • Verify Time by Programming Hardware

Devices	IAP	FlashPro4	FlashPro5	BP	Silicon Sculptor
MPF100T, TL, TS, TLS					
MPF200T, TL, TS, TLS					
MPF300T, TL, TS, TLS		1 min 50 sec	1 min 36 sec		
MPF500T, TL, TS, TLS		2 min 40 sec	2 min 20 sec		

Note: FlashPro4 verification time collected based on 4 MHz TCK.
Note: FlashPro5 verification time collected based on 10 MHz TCK.

7.6.8 Secure NVM Performance

The following table describes secure NVM performance.

Table 86 • sNVM Read/Write Characteristics

Parameter	Min	Typ	Max	Unit	Conditions
Plain text programming				ms	
Authenticated text programming				ms	
Authenticated and encrypted text programming				ms	
Authentication R/W 1st access from power-up overhead				ms	
Plain text read				ms	
Authenticated text read					
Authenticated and decrypted text read				ms	

Note: Page size= 252 Bytes (non-authenticated), 236 Bytes (authenticated).

Note: Only page reads and writes allowed.

Note: $T_{KEYOVHD}$ is an additional time that occurs on the first R/W to sNVM using authenticated or authenticated and encrypted text.

7.6.9 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

Table 87 • sNVM Programming Cycles vs. Retention Characteristics

Programming Temperature	Programming Cycles Per Page, Max	Programming Cycles Per Block, Max	Retention Years
–40 °C to 100 °C	10,000	100,000	20
–40 °C to 85 °C	10,000	100,000	20
–40 °C to 55 °C	10,000	100,000	20

Note: Page size = 128 Bytes

Note: Block size = 56 KBytes

7.7 System Services

This section describes system switching and throughput characteristics.

7.7.1 System Services Throughput Characteristics

The following table describes system services throughput characteristics.

Table 88 • System Services Throughput Characteristics

Parameter	Symbol	Service ID	Typ	Max	Conditions
Serial number	T_{Serial}	00H			
User code	T_{User}	01H			
Design information	T_{Design}	02H			
Device certificate	T_{Cert}	03H			
Read digests	T_{digest_read}	04H			
Query security locks	T_{sec_Query}	05H			
Read debug information	T_{Rd_debug}	06H			
Reserved		07H–0FH			
Secure NVM write plain text[1]	$T_{SNVM\_Wr\_Plain}$	10H			
Secure NVM write authenticated plain text[1]	$T_{SNVM\_Wr\_Auth}$	11H			
Secure NVM write authenticated cipher text[1]	$T_{SNVM\_Wr\_Cipher}$	12H			
Reserved		13H–17H			
Secure NVM read[1]	T_{SNVM_Rd}	18H			
Digital signature service raw	T_{SIG_RAW}	19H			
Digital signature service DER	T_{SIG_DER}	1AH			
Reserved		1BH–1FH			
PUF emulation	$T_{Challenge}$	20H			
Nonce service	T_{Nonce}	21H			
Bitstream authentication	T_{BIT_AUTH}	22H			SPI F_{MAX}
IAP Image authentication	T_{IAP_AUTH}	23H			SPI F_{MAX} + Optional INIT data
Reserved		26H–3FH			
Flash*Freeze service[2]	T_{FF}	40H			
Flash*Freeze service with time out[2]	T_{FF_TOUT}	41H			
In application programming by index[3]	$T_{IAP\_Prg\_Index}$	42H			
In application programming by SPI address[3]	$T_{IAP\_Prg\_Addr}$	43H			
In application verify by index[3]	$T_{IAP\_Ver\_Index}$	44H			
In application verify by SPI address[3]	$T_{IAP\_Ver\_Addr}$	45H			
Auto update[3]	$T_{AutoUpdate}$	46H			
Digest check[4]	T_{digest_chk}	47H			

1. See sNVM Read/Write Characteristics (see page 62).
2. See LSRAM and µSRAM Initialization Time (see page 78).

3. See FPGA Programming Time (see page 57).
4. See Digest Times (see page 58).

7.8 User Crypto

The following section describes user crypto.

7.8.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

Table 89 • TeraFire F5200B Switching Characteristics

Parameter	Symbol	VDD = 1.0 V STD	VDD = 1.0 V –1	VDD = 1.05 V STD	VDD = 1.05 V –1	Unit	Condition
Operating frequency	F_{MAX}	189		189		MHz	–40 °C to 100 °C

7.8.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

Note: Clock-cycles indicate total clock-cycles from Cortex-M1 driver to Athena TeraFire core completion and return. 100 MHz Cortex-M1 and Athena TeraFire core.

Table 90 • AES

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
AES-ECB-128 encrypt[1]	128	515	4523
	64K	52157	56148
AES-ECB-128 decrypt[1]	128	561	4558
	64K	52433	56428
AES-ECB-256 encrypt[1]	128	531	4730
	64K	60349	64545
AES-ECB-256 decrypt[1]	128	593	4800
	64K	60721	64930
AES-CBC-256 encrypt[1]	128	592	5366
	64K	62739	67526
AES-CBC-256 decrypt[1]	128	621	5401
	64K	60901	65671
AES-GCM-128 encrypt[1], 128-bit tag, 128-bit authtag before plaintext (full message encrypted /authenticated)	128	2506	6857
	64K	82188	86517
AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	1960	6280
	64K	81642	85975
AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated)	128	2008	6557
	64K	81674	86217

1. With DPA counter measures.

Table 91 • GMAC

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
AES-GCM-256[1],128-bit tag, (message is only authenticated)	128	2008	6557
	64K	81674	86217

1. With DPA counter measures.

Table 92 • HMAC

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
HMAC-SHA-256[1], 256-bit key	512	7477	9577
	64K	88367	90462
HMAC-SHA-384[1], 384-bit key	1024	11731	14042
	64K	106111	108402

1. With DPA counter measures.

Table 93 • CMAC

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
AES-CMAC-256[1] (message is only authenticated)	128	223	14924
	64K	223	159942

1. With DPA counter measures.

Table 94 • KEY TREE

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
128-bit nonce + 8-bit optype	NA	102511	105413
256-bit nonce + 8-bit optype	NA	103272	106454

Table 95 • SHA

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
SHA-1[1]	512	2386	3683
	64K	77576	78863
SHA-256[1]	512	2516	3823
	64K	84752	86038
SHA-384[1]	1024	4162	5468
	64K	51274	101543
SHA-512[1]	1024	4162	5468
	64K	51274	101543

1. With DPA counter measures.

Table 96 • ECC

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
ECDSA SigGen, P-384/SHA-384 [1]	1024	12530673	12538712
	8K	12545812	12553842
ECDSA SigGen, P-384/SHA-384	1024	5502580	5510607
ECDSA SigVer, P-384/SHA-384	1024	6329349	6336684
	8K	6374140	6381484
Key agreement (KAS), P-384[1]		5037644	5043464
Point multiply, P-256[1]		5176445	5182129
Point multiply, P-384[1]		12048196	12055249
Point multiply, P-521[1]		26886848	26895584
Point addition, P-384		5049697	5056192
KeyGen (PKG), P-384[1]		12059342	12067938
KeyVer (PKV), P-384[1]			
Point verification, P-384		5185	8214

1. With DPA counter measures.

Table 97 • IFC (RSA)

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
Encrypt, RSA-2048, e=65537	2048	1694898	1707983
	3072	3734115	3752628
Decrypt, RSA-2048[1], CRT	2048		
Decrypt, RSA-3072[1], CRT	3072		
Decrypt, RSA-4096[1], CRT	4096		
Decrypt, RSA-8192[1], CRT	8192		
Decrypt, RSA-3072, CRT	3072	38135488	38160269
SigGen, RSA-3072/SHA-384[1], PKCS #1 V 1.5	1024		
	8K		
SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5	1024	13199641	147436351
	8K	13210656	147447376
SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5	1024	21574887	88701666
	8K	21583957	88710731
SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5	1024	26916920	26929701
	8K	26931018	26943806
SigGen, RSA-3072/SHA-384, ANSI X9.31	1024	13148583	147385003
	8K	13156661	147393088
SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31	1024	21614156	88740653
	8K	21632391	88758888

1. With DPA counter measures.

Table 98 • FFC (DH)

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
SigGen, DSA-3072 /SHA-3842	1024	27948851	27966136
	8K	27961233	27978526
SigGen, DSA-3072 /SHA-384	1024	11951377	11967172
SigVer, DSA-3072 /SHA-384	1024	24484509	24504278
	8K	24950598	24970373
SigVer, DSA-2048 /SHA-256	1024	10016686	10031188
	8K	10008257	10022753
Key Agreement (KAS), DH-3072 (p= 3072, security= 256)		12207595	12225892
Key Agreement (KAS), DH-3072 (p= 3072, security= 56)[1]		40537984	241882971

1. With DPA counter measures.

Table 99 • NRBG

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
Instantiate: strength, s = 256, 384-bit nonce, 384-bit personalization string		0	757
Reseed: no additional input, s = 256		769	4630
Reseed: 384-bit additional input, s = 256		1490	6271
Generate: (no add'l input, no prediction resistance), s = 256	128	1909	3640
Generate: (no add'l input, no prediction resistance), s = 256	8K	12808	27125
Generate: (no add'l input), prediction resistance enabled, s = 256	128	6078	7817
Generate: (no add'l input), prediction resistance enabled, s = 256	8K	16977	31337
Generate: 384-bit add'l input, (no prediction resistance), s = 256	128	6064	8539
Generate: 384-bit add'l input, (no prediction resistance), s = 256	8K	16963	32024
Generate: (no add'l input, no prediction resistance), s = 256	128	7719	10196
	8K	18618	33681

Modes	Message Size (Bits)	Athena TeraFire Crypto Core Clock-Cycles Per Message	Clock-Cycles
Generate: (no add'l input, no prediction resistance), s = 256			
Un-instantiate		761	1613

1. With DPA counter measures.

7.9 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.

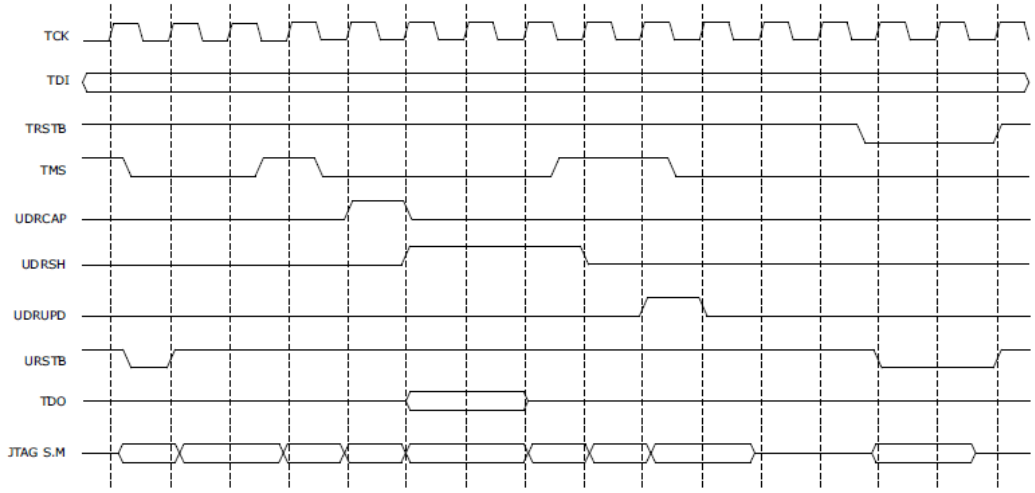
7.9.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

Table 100 • UJTAG Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F_{TCK}			50	MHz	

Figure 4 • UJTAG Timing Diagram



7.9.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

Table 101 • UJTAG Security Performance Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
TCK frequency	F_{TCK}				MHz	

7.9.3 USPI Switching Characteristics

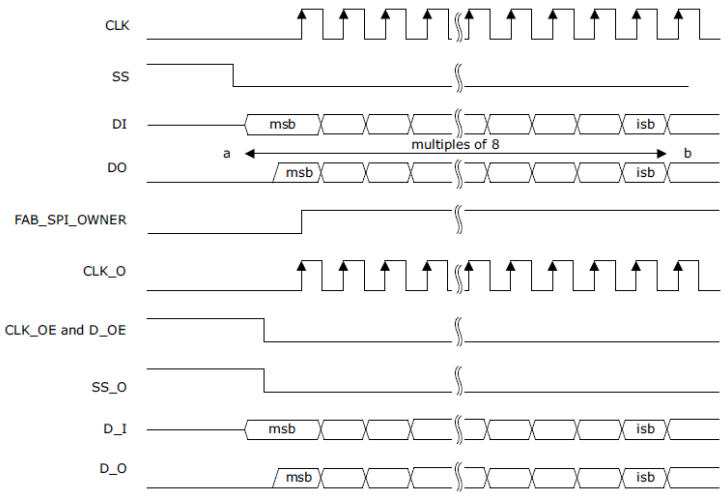
The following section describes characteristics of USPI switching.

Table 102 • SPI Macro Interface Timing Characteristics

Parameter	Symbol	V_{DDI} = 3.3 V Max	V_{DDI} = 2.5 V Max	V_{DDI} = 1.8 V Max	V_{DDI} = 1.5 V Max	V_{DDI} = 1.2 V Max	Unit
Propagation delay from the fabric to pins[1]	TPD_MOSI	0.8	1	1.2	1.4	1.6	ns
	TPD_MISO	3.5	3.75	4	4.25	4.5	ns
	TPD_SS	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK	3.5	3.75	4	4.25	4.5	ns
	TPD_MOSI_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SS_OE	3.5	3.75	4	4.25	4.5	ns
	TPD_SCK_OE	3.5	3.75	4	4.25	4.5	ns

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

Figure 5 • USPI Switching Characteristics



7.9.4 Tamper Detectors

The following section describes tamper detectors.

Table 103 • ADC Conversion Rate

Parameter	Description	Min	Typ[1]	Max
T_{CONV1}	Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0	420 us		470 us
T_{CONVN}	Time between subsequent channel conversion's		480 us	
T_{SETUP}	Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 us.	0 ns		
T_{VALID}[2]	Width of the valid pulse.	1.625 us		2 us
T_{RATE}	Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter.	480 us	Rate × 32 us	8128 us

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started, that is if channel 0 has just completed and only channels 0 and 3 are enabled; the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed; the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted) then no further conversions will be started.

Figure 6 • ADC Switching Characteristics

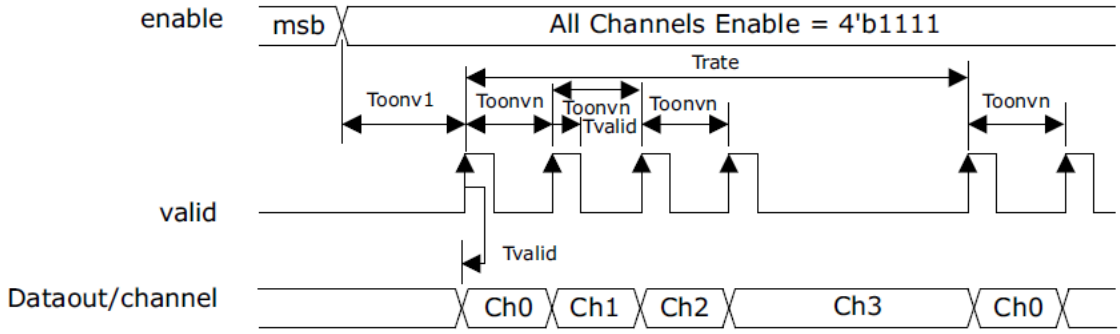


Figure 7 • ADC Switching Characteristics Timing Diagram

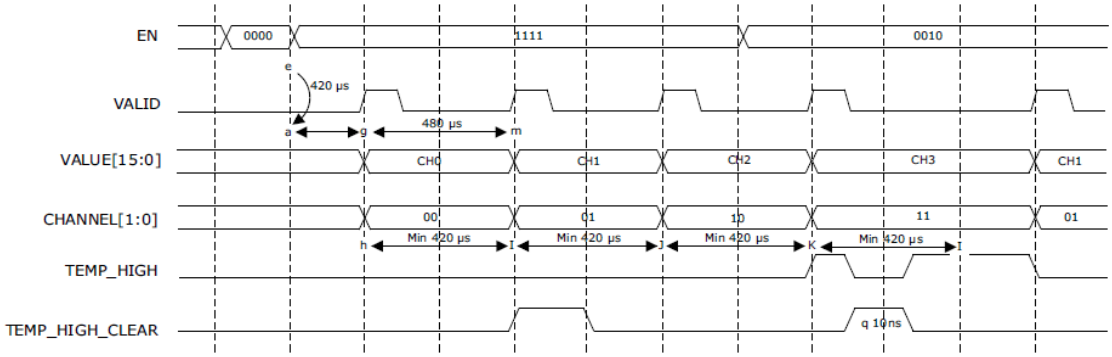


Table 104 • Temperature and Voltage Sensor Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Temperature sensing range	–40		125	°C	
Temperature sensing accuracy	–10		10	°C	
Voltage sensing range	0.9		2.8	V	
Voltage sensing accuracy	–1.5		1.5	%	

Table 105 • Tamper Macro Timing Characteristics—Flags and Clearing

Parameter	Symbol	Typ	Max	Unit
From event detection to flag generation	T_{JTAG_ACTIVE}[1, 2]		5	ns
	T_{MESH_ERR}[2]	0.1	6.5	us
	T_{CLK_GLITCH}[1, 2]		50	ns
	T_{CLK_FREQ}[1, 2]		4	us
	T_{LOW_1P05}[2]		44	us
	T_{HIGH_1P8}[2]		44	us
	T_{HIGH_2P5}[2]		44	us
	T_{GLITCH_1P05}[2]		20	ns
	T_{SECDEC}[1, 2]		5	ns
	T_{SCB_ERR}[2]		50	ns
	T_{WDOG}[1, 2]		5	ns
	T_{LOCK_ERR}[2]		5	ns
Time from system controller instruction execution to flag generation	$T_{INST\_BUF\_ACCESS}$[2, 3]			
	T_{INST_DEBUG}[2, 3]			
	$T_{INST\_CHK\_DIGEST}$[2, 3]			
	$T_{INST\_EC\_SETUP}$[2, 3]			
	$T_{INST\_FACT\_PRIV}$[2, 3]			
	$T_{INST\_KEY\_VAL}$[2, 3]			
	T_{INST_MISC}[2, 3]			
	$T_{INST\_PASSCODE\_MATCH}$[2, 3]			
	$T_{INST\_PASSCODE\_SETUP}$[2, 3]			
	T_{INST_PROG}[2, 3]			
	$T_{INST\_PUB\_INFO}$[2, 3]			
	$T_{INST\_ZERO\_RECO}$[2, 3]			
	$T_{INST\_PASSCODE\_FAIL}$[2, 3]			
	$T_{INST\_KEY\_VAL\_FAIL}$[2, 3]			
	T_{INST_UNUSED}[2, 3]			
Time from sending the CLEAR to deassertion on FLAG	T_{CLEAR_FLAG}		3	ns

1. Not available during Flash*Freeze.
2. The timing does not impact the user design, however it is useful for Security Analysis.
3. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.

Table 106 • Tamper Macro Response Timing Characteristics

Parameter	Symbol	Typ	Max	Unit
Time from triggering the response to all I/Os disabled	$T_{IO\_DISABLE}$		150	ns
Time from negation of RESPONSE to all I/Os re-enabled	$T_{CLR\_IO\_DISABLE}$		10	us
Time from triggering the response to security locked	$T_{LOCKDOWN}$		20	ns
Time from negation of RESPONSE to earlier security unlock condition	$T_{CLR\_LOCKDOWN}$		20	ns
Time from triggering the response to device enters RESET	T_{tr_RESET}			
Time from triggering the response to start of zeroization	$T_{tr\_ZEROLISE}$			

7.9.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

Table 107 • System Controller Suspend Entry and Exit Characteristics

Parameter	Symbol	Definition	Typ	Max	Unit
Time from TRSTb falling edge to SUSPEND_EN signal assertion	$T_{suspend\_Tr}$[1, 2]	Suspend entry time from TRST_N assertion	1		µs
Time from TRSTb rising edge to ACTIVE signal assertion	$T_{suspend\_exit}$	Suspend exit time from TRST_N negation	360		µs

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

7.9.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

Table 108 • Dynamic Reconfiguration Interface Timing Characteristics

Parameter	Symbol	Max	Unit
PCLK frequency	F_{PD_PCLK}	200	MHz

Figure 8 • Write Transfer Without Wait States

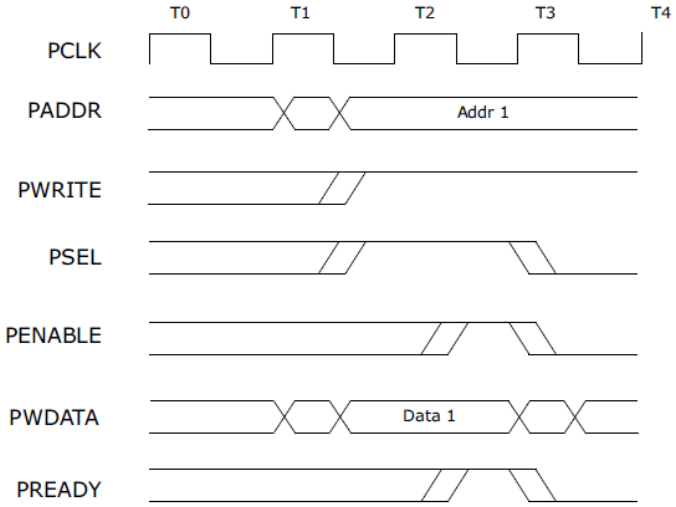


Figure 9 • Write Transfer With Wait States

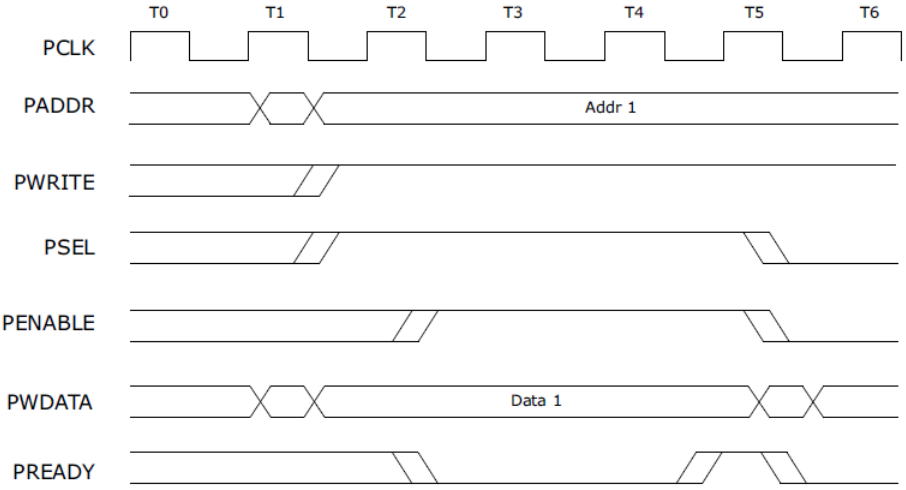


Figure 10 • Read Transfer Without Wait States

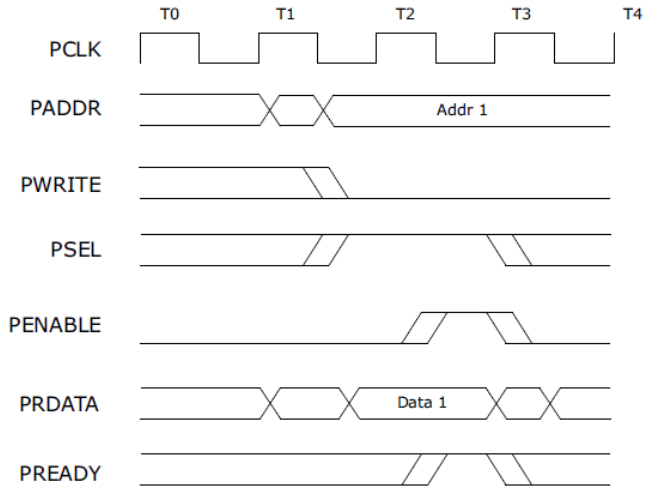
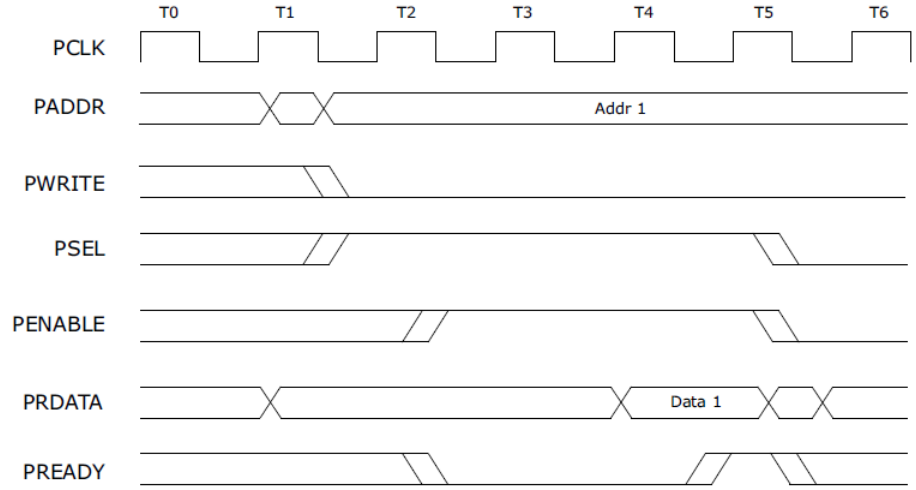


Figure 11 • Read Transfer With Wait States



7.10 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin) timing. The power-up diagrams assume all power supplies to the device are stable.

Table 109 • Cold-Boot Power-Up to Functional Times

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power-on reset circuit trip point	T_{POR_START}				µs	POR start = V_{DD} at 0.91 V, V_{DD18} at 1.6 V, V_{DDA} at 2.19 V
System controller start[1]	T_{BOOT_START} (COLD)		100		µs	

1. V_{DDI3} and V_{DDAUX3} must be valid 50 usec before T_{BOOT_START} complete to avoid additional delay. V_{DDI3} = 0.85 V V_{DDAUX3} = 1.6 V.

Table 110 • Warm-Boot Power-Up to Functional Times

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Warm reset	$T_{WARM\_RESET\_START}$					
The time from warm reset assertion to I/Os disabled	$T_{IO\_DISABLED}$		1		µs	
DEVRST_N assertion time	$T_{DEVRSTN}$	1			µs	
Time from DEVRST_N negation to T_{BOOT} (WARM) if DEVRSTN asserted for less than 1000 us			1000–$T_{DEVRSTN}$		µs	
Time from DEVRST_N negation to T_{BOOT} (WARM) if DEVRSTN asserted for greater than 1000 us			0		µs	

Table 111 • Cold and Warm Boot

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T_{BOOT_START} to the FPGA fabric operational	T_{FABRIC_UP}		550		µs	2 MHz and 160 MHz RC oscillators are available at this time
The time from FPGA fabric operational to FPGA inputs operational[1]	T_{IN_ACTIVE}		25		µs	
The time from T_{BOOT_START} to FPGA fabric POR negation[1]	$T_{FAB\_POR\_DELAY}$		600		µs	FABRIC_POR_N asserted to indicate to user design POR is complete
The time from T_{FAB_READY} to FPGA outputs operational[2]	T_{OUT_ACTIVE}		200		µs	GPIO_ACTIVE and HSIO_ACTIVE indicate that I/O calibration is complete.
The time from T_{FAB_READY} to FPGA pull-up /pull-down operational	$T_{PU\_PD\_ACTIVE}$		200		µs	
IO bank controller calibration time period (HSIO/GPIO) assumes bank supplies are valid			200		µs	
The time from T_{BOOT_START} to ready to program through JTAG/SPI-Slave			800		ms	
The time from T_{BOOT_START} to autoupdate start			800		ms	
The time from T_{BOOT_START} to programming recovery start			800		ms	
The time from TFAB_READY to transceivers PCIe initialization complete	$T_{PCIE\_XCVR\_ACTIVE}$				µs	
The time from TFAB_READY to DEVICE_INIT_DONE assertion	$T_{DEVICE\_INIT\_DONE}$				ms	Dependent on the number of LSRAMs, µSRAMs, and transceivers initialized
The time from DEVICE_INIT_DONE assertion to SUSPEND_EN signal assertion	$T_{SUSPEND}$		10		µs	Valid at T_{FABRIC_UP}
The time from $T_{PORDELAY}$ to PLL/DLL initialization complete	T_{PLL_INIT}		200		µs	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from T_{FAB_READY} to PLL lock	T_{PLL_LOCK}		200			See PLL Electrical Characteristics (see page 40)
The time from T_{FAB_READY} to the PUF available for a system service call	T_{PUF_READY}		200		µs	Covered in System Service PUF dependent functions
The time from T_{FAB_READY} to the NRBG available (for S devices only)	T_{NRBG_READY}		200		µs	Covered in System Service PUF dependent functions
The time from T_{FAB_READY} to the tamper flags being available	T_{TAMPER_READY}		200		µs	Valid at T_{FABRIC_UP}
The time from T_{FAB_READY} to the Athena Crypto-co-processor being available (for S devices only)	T_{CRYPTO_READY}		200		µs	Valid at T_{FABRIC_UP}

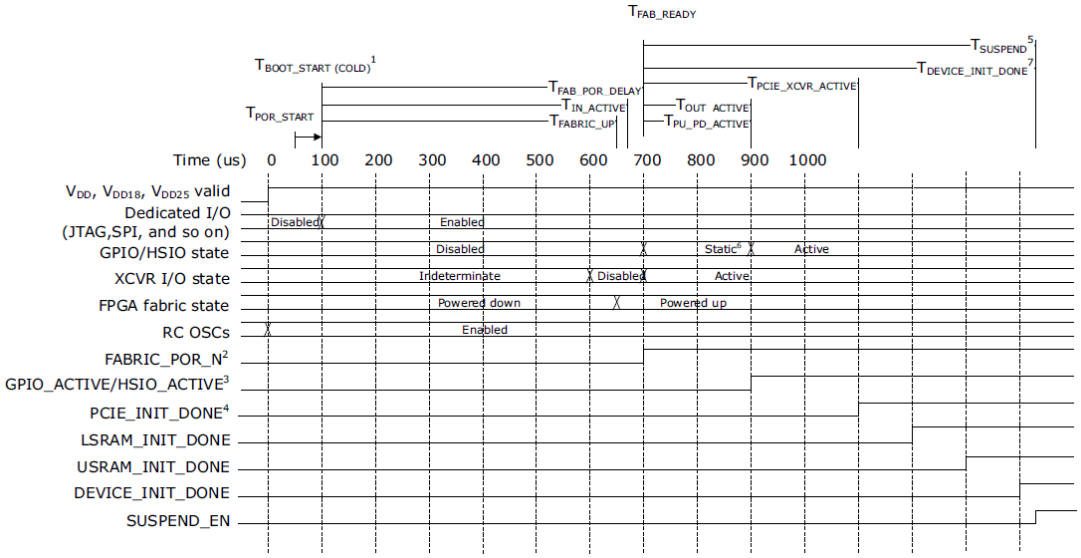
1. GPIO V_{DDIn} and V_{DDAUXn} must reach target 50 usec before T_{FABRIC_UP} to avoid delay. HSIO V_{DDIn} and V_{DD18} must reach target before T_{FABRIC_UP}. V_{DDIn} = 0.85 V, V_{DDAUXn} = 1.6 V, V_{DD18}= 1.6 V.
2. Inputs are ready 200 usec before T_{OUTPUT_ACTIVE}. I/Os can be configured to output a static state 1/0 before calibration is complete. Need to determined by user/Libero.

Table 112 • Flash*Freeze

Parameter	Symbol	Min	Typ	Max	Unit	Condition
The time from Flash*Freeze entry command to the Flash*Freeze state	T_{FF_ENTRY}		59		µs	
The time from Flash*Freeze exit pin assertion to fabric operational state	$T_{FF\_FABRIC\_UP}$		133		µs	
The time from Flash*Freeze exit pin assertion to I/Os operational	$T_{FF\_IO\_ACTIVE}$		143		µs	

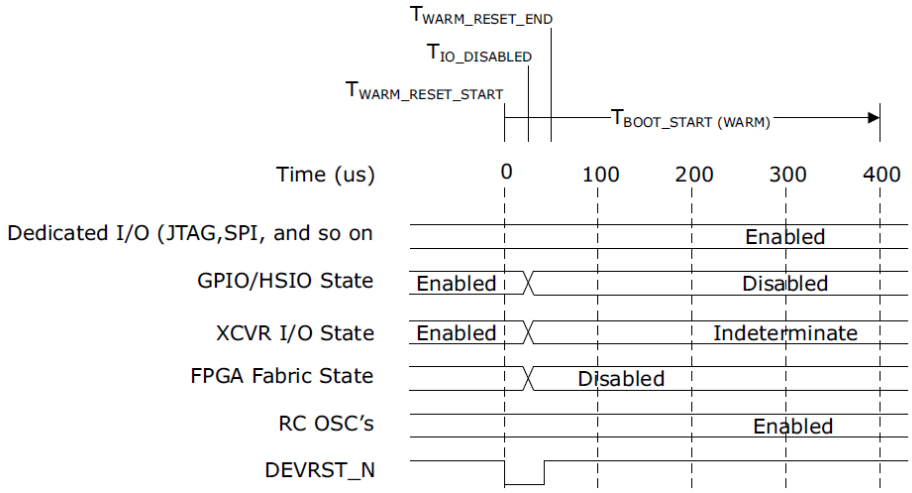
Note: Asserting reset from the tamper macro has the same power-up to functional timings starting from T_{BOOT}.

Figure 12 • Cold-Boot Power-Up to Functional Times



1. System controller boots.
2. Device initialization starts here. For PCIe, the termination value of XCVR I/O must be set to 50 Ω and 70 ms before PVPERL after start of POR.
3. For PCIe. PERST# or WAKE# must be operational before 50 ms after start of POR.
4. For PCIe, device configuration space must be accessible by host within 1 sec of negation of PERST#.
5. SUSPEND_EN asserts only after cold boot and DEVICE_INIT_DONE asserts.
6. I/O's can be configured to output a static state 1/0 before calibration is complete.
7. User design dependent times dependent on the number of LSRAMs, uSRAMs, and transceivers initialized.
8. Any delay in I/O supplies becoming valid will delay the I/O active times.
9. V_{DDI3} and V_{DDAUX3} must be valid 50 usec before T_{BOOT_START} completes to avoid additional delay. V_{DDI3} = 0.85 V, V_{DDAUX3} = 1.6 V.

Figure 13 • Warm-Boot Power-Up to Functional Times



Note: At time T_{BOOT_START} (WARM), the FPGA boot process follows the cold start boot process at time T_{BOOT_START} (COLD). For more information, see previous illustration.

7.10.1 LSRAM and µSRAM Initialization Time

The following table describes initialization time for LSRAM and µSRAM.

Table 113 • Ram Initialization Characteristics

Parameter	Symbol	Typ	Max	Unit	Formula
INIT time of 1 LSRAM	T_{UPROM_LSRAM}				T1
INIT time of 1 µSRAM	T_{UPROM_USRAM}				T2
INIT time of n LSRAM/LSRAMs in normal mode	$T_{UPROM\_LSRAM\_n}$				n × T1
INIT time of n µSRAM/µSRAM in normal mode	$T_{UPROM\_USRAM\_n}$				n × T2
INIT time of n LSRAM in broadcast mode	$T_{UPROM\_LSRAM\_Br}$				T1
INIT time of n µSRAM in broadcast mode	$T_{UPROM\_USRAM\_Br}$				T2
INIT time of 1 LSRAM	T_{SNVM_LSRAM}				T4
INIT time of 1 µSRAM	T_{SNVM_USRAM}				T5
INIT time of n LSRAM/LSRAMs in normal mode	$T_{SNVM\_LSRAM\_n}$				n × T4
INIT time of n µSRAM/µSRAM in normal mode	$T_{SNVM\_USRAM\_n}$				n × T5
INIT time of n LSRAM in broadcast mode	$T_{SNVM\_LSRAM\_Br}$				T4
INIT time of n µSRAM in broadcast mode	$T_{SNVM\_USRAM\_Br}$				T5
INIT time of 1 LSRAM	$T_{SPI\_PLAIN\_LSRAM}$				T7
INIT time of 1 µSRAM	$T_{SPI\_PLAIN\_USRAM}$				T8
INIT time of n LSRAMs in normal mode	$T_{SPI\_PLAIN\_LSRAM\_n}$				n × T7
INIT time of n µSRAMs in normal mode	$T_{SPI\_PLAIN\_USRAM\_n}$				n × T8
INIT time of n LSRAM in broadcast mode	$T_{SPI\_PLAIN\_LSRAM\_Br}$				T7
INIT time of n µSRAM in broadcast mode	$T_{SPI\_PLAIN\_USRAM\_Br}$				T8
INIT time of 1 LSRAM	$T_{SPI\_AUTH\_LSRAM}$				T10
INIT time of 1 µSRAM	$T_{SPI\_AUTH\_USRAM}$				T11
INIT time of n LSRAMs in normal mode	$T_{SPI\_AUTH\_LSRAM\_n}$				n × T10
INIT time of n µSRAMs in normal mode	$T_{SPI\_AUTH\_USRAM\_n}$				n × T11
INIT time of n LSRAM in broadcast mode	$T_{SPI\_AUTH\_LSRAM\_Br}$				T10
INIT time of n µSRAM in broadcast mode	$T_{SPI\_AUTH\_USRAM\_Br}$				T11
INIT time of 1 LSRAM	$T_{SPI\_ENCRYPT\_LSRAM}$				T13
INIT time of 1 µSRAM	$T_{SPI\_ENCRYPT\_USRAM}$				T14
INIT time of n LSRAMs in normal mode	$T_{SPI\_ENCRYPT\_LSRAM\_n}$				n × T13
INIT time of n µSRAMs in normal mode	$T_{SPI\_ENCRYPT\_USRAM\_n}$				n × T14
INIT time of n LSRAM in broadcast mode	$T_{SPI\_ENCRYPT\_LSRAM\_Br}$				T13
INIT time of n µSRAM in broadcast mode	$T_{SPI\_ENCRYPT\_USRAM\_Br}$				T14

7.11 Dedicated Pins

The following section describes the dedicated pins.

7.11.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

Table 114 • JTAG Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
T_{DISU}	TDI input setup time	0.0			ns	
T_{DIHD}	TDI input hold time			2.0	ns	
T_{TMSSU}	TMS input setup time	1.5			ns	
T_{TMSHD}	TMS input hold time			1.5	ns	
F_{TCK}	TCK frequency			25	MHz	
T_{TCKDC}	TCK duty cycle	40		60	%	
T_{TDOCQ}	TDO clock to Q out			7	ns	C_{LOAD} = 40 pf
T_{RSTBCQ}	TRSTB clock to Q out			23.5	ns	C_{LOAD} = 40 pf
T_{RSTBPW}	TRSTB min pulse width	50			ns	
$T_{RSTBREM}$	TRSTB removal time			0.0	ns	
$T_{RSTBREC}$	TRSTB recovery time	12.0			ns	
CIN_{TDI}	TDI input pin capacitance			5.3	pf	
CIN_{TMS}	TMS input pin capacitance			5.3	pf	
CIN_{TCK}	TCK input pin capacitance			5.3	pf	
CIN_{TRSTB}	TRSTB input pin capacitance			5.3	pf	

7.11.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

Table 115 • SPI Master Mode (PolarFire master) During Programming

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			20	MHz	
SCK minimum clock period	T_{MSCKMP}	50			ns	
SCK minimum pulse width high	$T_{MSCKPWH}$	20			ns	
SCK minimum pulse width low	$T_{MSCKPWL}$	20			ns	
SDO clock to out	T_{SDOCO}			10	ns	
SDI setup time	T_{SDISU}	10			ns	
SDI hold time	T_{SDIHD}	10			ns	

Table 116 • SPI Master Mode (PolarFire master) During Device Initialization

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{MSCK}			40	MHz	
SCK minimum clock period	T_{MSCKMP}	25			ns	
SCK minimum pulse width high	$T_{MSCKPWH}$	10			ns	
SCK minimum pulse width low	$T_{MSCKPWL}$	10			ns	
SDO clock to out	T_{SDOCO}				ns	
SDI setup time	T_{SDISU}	5			ns	
SDI hold time	T_{SDIHD}	5			ns	

Table 117 • SPI Slave Mode (PolarFire slave)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SCK frequency	F_{SSCK}			80	MHz	
SCK minimum clock period	T_{SSCKMP}	13			ns	
SCK minimum pulse width high	$T_{SSCKPWH}$	5			ns	
SCK minimum pulse width low	$T_{SSCKPWL}$	5			ns	
SDO clock to out	T_{SDOCO}			2.5	ns	
SDI setup time	T_{SDISU}	2.5			ns	
SDI hold time	T_{SDIHD}	2.5			ns	

7.11.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

Table 118 • SmartDebug Probe Performance Characteristics

Parameter	Symbol	V_{DD} = 1.0 V STD	V_{DD} = 1.0 V –1	V_{DD} = 1.05 V STD	V_{DD} = 1.05 V –1	Unit
Maximum frequency of probe signal	F_{MAX}	250	250	250	250	MHz
Minimum delay of probe signal	T_{Min_delay}	13	12	13	12	ns
Maximum delay of probe signal	T_{Max_delay}	13	12	13	12	ns

7.11.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

Table 119 • DEVRST_N Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DEVRST_N ramp rate	DR_{RAMP}		10		us	It must be a normal clean digital signal, with typical rise and fall times
Minimum DEVRST_N assert time	DR_{ASSERT}		1		us	The minimum time for DEVRST_N to be recognized
Minimum DEVRST_N de-assert time	$DR_{DEASSERT}$		1		us	The minimum time DEVRST_N needs to be de-asserted before assertion

7.11.5 FF_EXIT Switching Characteristics

The following table describes characteristics of FF_EXIT switching.

Table 120 • FF_EXIT Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
FF_EXIT_N ramp rate	FF_{RAMP}		10		µs	
Minimum FF_EXIT_N assert time	FF_{ASSERT}		1		µs	The minimum time for FF_EXIT_N to be recognized
Minimum FF_EXIT_N de-assert time	$FF_{DEASSERT}$		1		µs	The minimum time FF_EXIT_N needs to be de-asserted before assertion

7.11.6 IO_CFG Switching Characteristics

The following table describes characteristics of IO_CFG switching.

Table 121 • IO_CFG Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
IO_CFG_N ramp rate	$IOCFG_{RAMP}$		10		µs	
Minimum IO_CFG_N assert time	$IOCFG_{ASSERT}$		1		µs	The minimum time for IO_CFG_N to be recognized
Minimum IO_CFG_N de-assert time	$IOCFG_{DEASSERT}$		1		µs	The minimum time IO_CFG_N needs to be de-asserted before assertion
IO_CFG_N to SPI Tristate	$IOCFG_{TRISTATE}$		20		ns	The time from IO_CFG_N changing to SPI pins going tri-state

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