



# UM10839

## LPC112x User manual

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User manual

### Document information

Info	Content
<b>Keywords</b>	ARM Cortex-M0, LPC1125, LPC1124.
<b>Abstract</b>	LPC112x User manual



**Revision history**

Rev	Date	Description
1	20150212	Initial revision. LPC1125 User manual.

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### 1.1 Introduction

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The LPC1125 is a ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC1125 operates at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC1125 includes 64 kB of flash memory, 8 kB of data memory, one Fast-mode Plus I<sup>2</sup>C-bus interface, three RS-485/EIA-485 UARTs, two SSP interfaces, four general purpose counter/timers, a 12-bit ADC, and up to 38 general purpose I/O pins.

### 1.2 Features

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- System:
  - ARM Cortex-M0 processor running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-Maskable Interrupt (NMI) input selectable from several input sources.
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 64 kB on-chip flash programming memory.
  - 256 byte page erase function.
  - 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip boot loader software.
- Digital peripherals:
  - Up to 38 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. A configurable open-drain mode is supported.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I<sup>2</sup>C-bus pins in Fast-mode Plus.
  - Four general purpose counter/timers with up to six capture inputs and up to 13 match outputs.
  - Programmable windowed WDT.
- Analog peripherals:
  - 12-bit ADC with 2 MSamples/s and eight channels.
- Serial interfaces:

- Three UARTs with fractional baud rate generation, internal FIFO, and RS-485 support. One UART with modem control.
- Two SSP controllers with FIFO and multi-protocol capabilities.
- I<sup>2</sup>C-bus interface supporting full I<sup>2</sup>C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Available as LQFP48 package.

## 1.3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1125JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1124JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	I <sup>2</sup> C/ Fast+	SSP	ADC channels	GPIO	Package
LPC1125JBD48/303	64 kB	8 kB	3	1	2	8	38	LQFP48
LPC1124JBD48/303	32 kB	8 kB	3	1	2	8	38	LQFP48

## 1.4 Block diagram

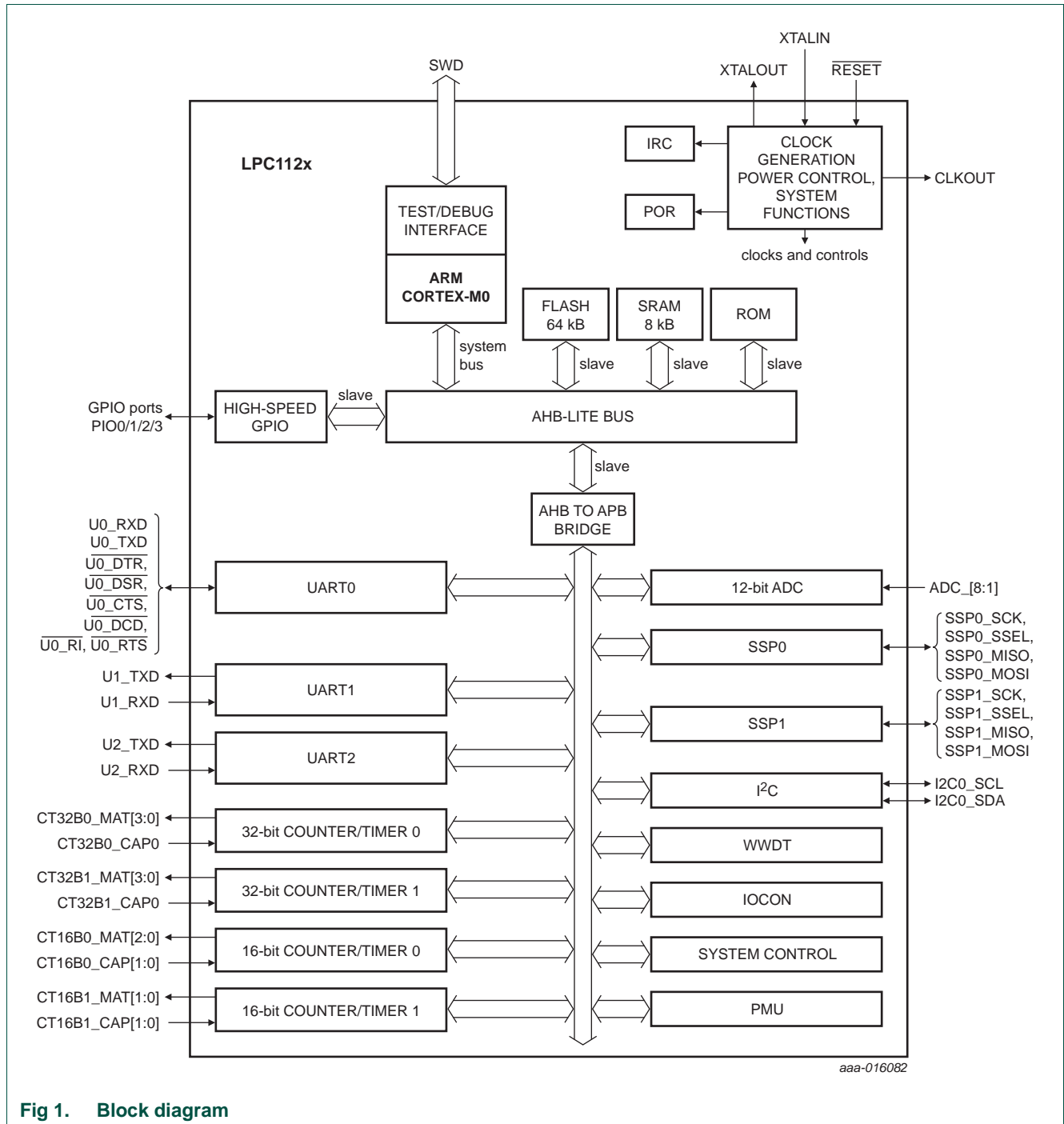


Fig 1. Block diagram

### 2.1 Memory map

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The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The GPIO ports are the only AHB peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

All peripheral register addresses are 32-bit word aligned regardless of their size. An implication of this is that word and half-word registers must be accessed all at once. For example, it is not possible to read or write the upper byte of a word register separately.

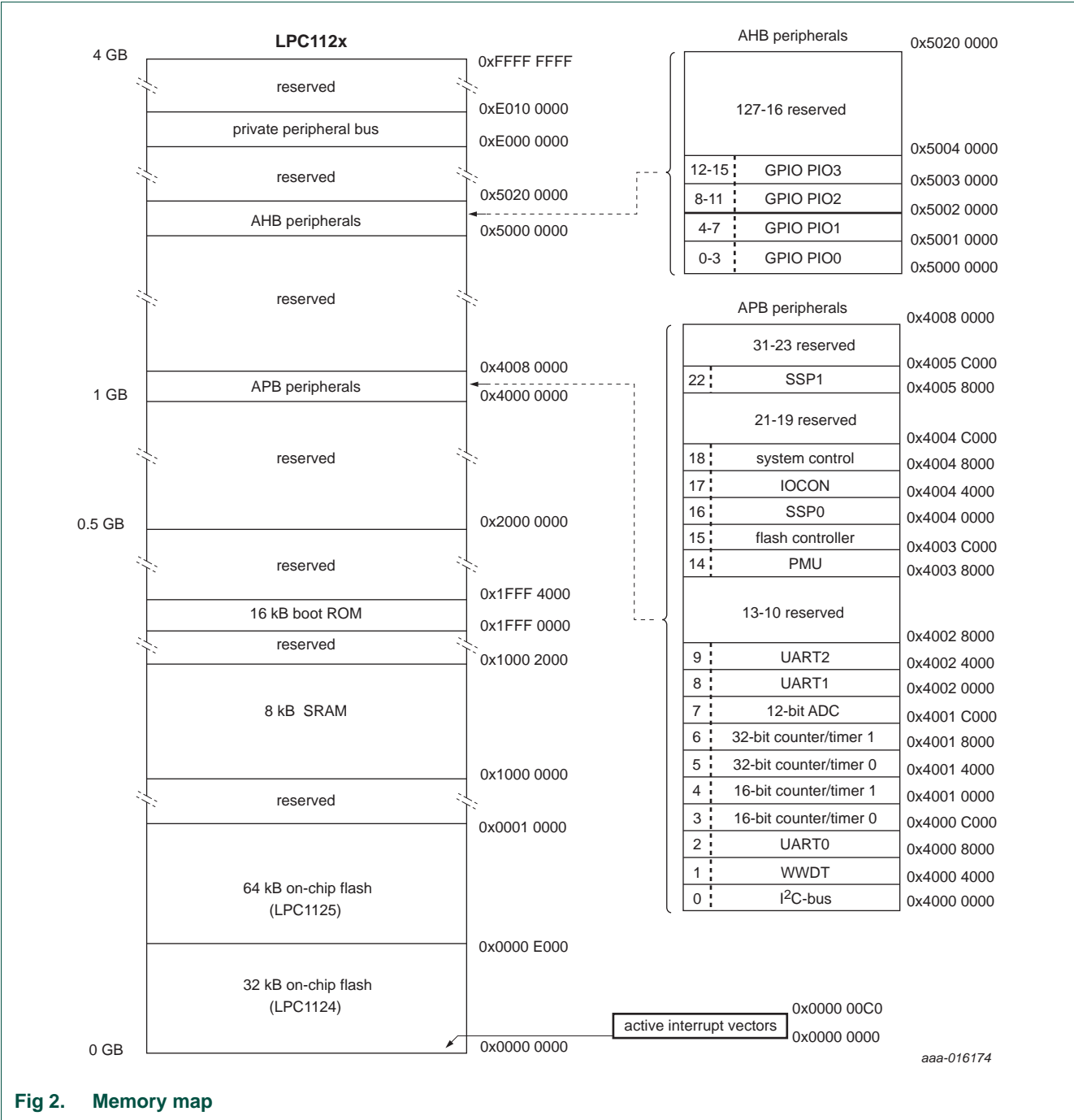


Fig 2. Memory map

### 3.1 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M0.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- The NVIC supports 32 vectored interrupts.
- 4 programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

### 3.2 General description

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

#### 3.2.1 Interrupt sources

Each peripheral device may have one or more interrupt lines to the Vectored Interrupt Controller. Each line may represent more than one interrupt source. There is no significance or priority about what line is connected where, except for certain standards from ARM.

See [Section 21.5.2](#) for the NVIC register bit descriptions.

**Table 3. Connection of interrupt sources to the Vectored Interrupt Controller**

Interrupt number	Name	Description	Flag(s)
12 to 0	PIO0_0 to PIO0_11; PIO1_0	start logic wake-up interrupts	Each interrupt is connected to a PIO input pin serving as wake-up pin from Deep-sleep mode; Interrupt 0 to 11 correspond to PIO0_0 to PIO0_11 and interrupt 12 corresponds to PIO1_0; see <a href="#">Table 37</a> .
13	ADC_B	ADC interrupt B interrupt	Combined interrupt of conversion complete sequence B interrupt and data overrun interrupt
14	SSP1	SPI/SSP1 interrupt	Tx FIFO half empty Rx FIFO half full Rx Timeout Rx Overrun
15	I2C	I2C interrupt	SI (state change)
16	CT16B0	16-bit timer 0 interrupt	Match 0 - 2 Capture 0



Table 3. Connection of interrupt sources to the Vectored Interrupt Controller

Interrupt number	Name	Description	Flag(s)
17	CT16B1	16-bit timer 1 interrupt	Match 0 - 1 Capture 0
18	CT32B0	32-bit timer 0 interrupt	Match 0 - 3 Capture 0
19	CT32B1	32-bit timer 1 interrupt	Match 0 - 3 Capture 0
20	SSP0	SPI/SSP0 interrupt	Tx FIFO half empty Rx FIFO half full Rx Timeout Rx Overrun
21	UART0	UART0 interrupt	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) End of Auto-Baud (ABEO) Auto-Baud Time-Out (ABTO)
22	UART1	UART1 interrupt	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) End of Auto-Baud (ABEO) Auto-Baud Time-Out (ABTO)
23	UART2	UART2 interrupt	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) End of Auto-Baud (ABEO) Auto-Baud Time-Out (ABTO)
24	ADC_A	ADC interrupt A	Combined interrupt of conversion complete sequence A interrupt and threshold compare out-of-range interrupt
25	WDT	WWDT interrupt	Watchdog interrupt (WDINT)
26	BOD	BOD interrupt	Brown-out detect interrupt depending on BOD voltage level
27		-	Reserved
28	GPIO3	GPIO3 port interrupt	GPIO interrupt status of port 3
29	GPIO2	GPIO2 port interrupt	GPIO interrupt status of port 2
30	GPIO1	GPIO1 port interrupt	GPIO interrupt status of port 1
31	GPIO0	GPIO0 port interrupt	GPIO interrupt status of port 0

### 4.1 Features

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- Clock generation and control.
- PLL control.
- Power and reset control for individual peripherals.
- Memory mapping.
- Power-down and wake-up configuration.

### 4.2 General description

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The system configuration block controls oscillators, start logic, and clock generation of the part. Also included in this block is a register for remapping flash, SRAM, and ROM memory areas.

#### 4.2.1 Clock generation

See [Figure 3](#) for an overview of the Clock Generation Unit (CGU).

The CGU includes three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the part will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency.

The SYSAHBCLKCTRL register gates the system clock to the various peripherals and memories. UART, the WDT, and SSP0/1 have individual clock dividers to derive peripheral clocks from the main clock.

The main clock and the clock outputs from the IRC, the system oscillator, and the watchdog oscillator can be observed directly on the CLKOUT pin.

For details on power control see [Section 5.4.1](#).

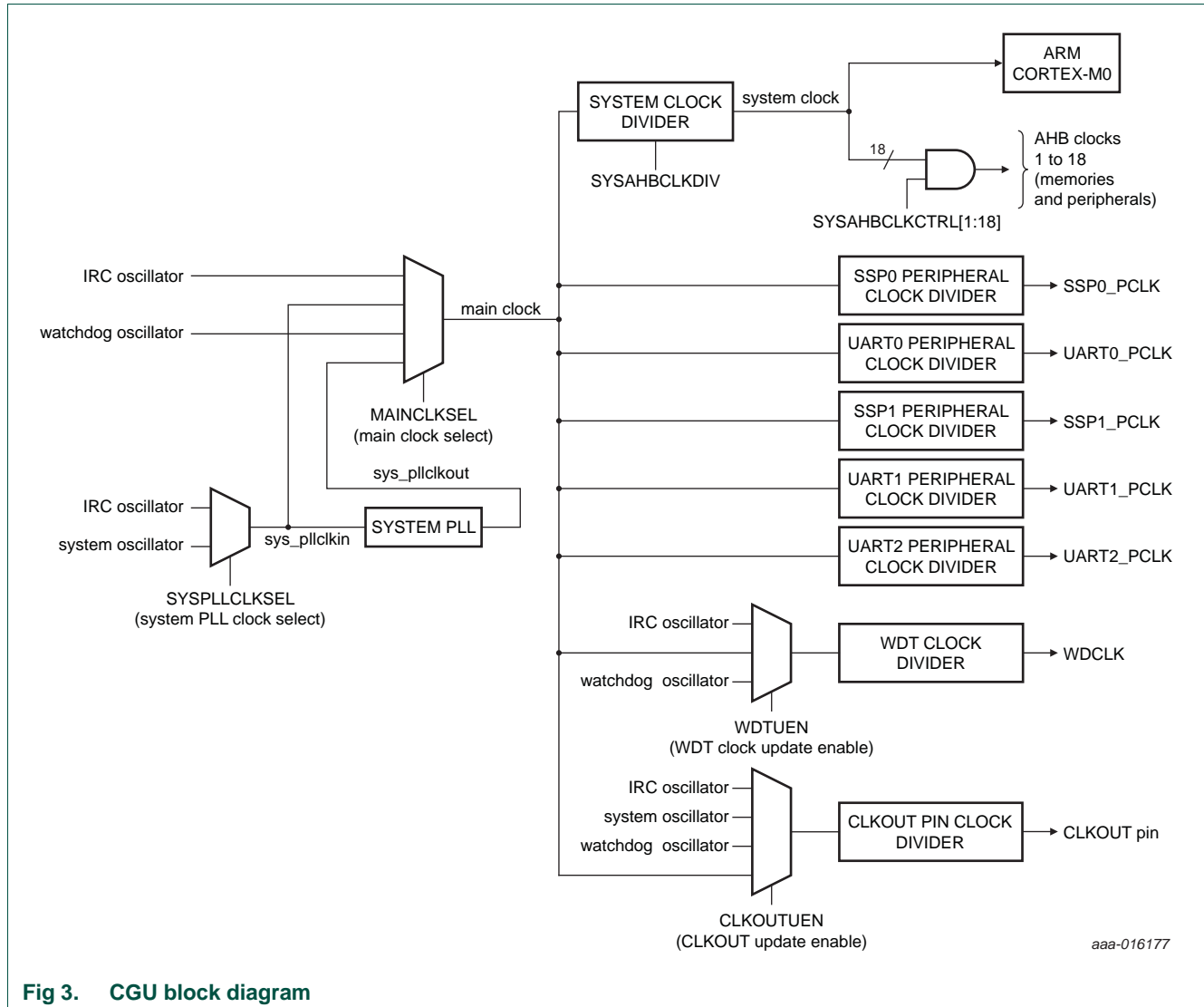


Fig 3. CGU block diagram

## 4.3 Pin description

Table 4 shows pins that are associated with system control block functions.

Table 4. Pin summary

Pin name	Pin direction	Pin description
CLKOUT	O	Clockout pin
PIO0_0 to PIO0_11	I	Start logic wake-up pins port 0
PIO1_0	I	Start logic wake-up pin port 1

## 4.4 Register description

All registers, regardless of size, are on word address boundaries. Details of the registers appear in the description of each function.

See [Section 4.5.5](#) for the flash access timing register, which can be re-configured as part the system setup. This register is not part of the system configuration block.

**Table 5. Register overview: system control block (base address 0x4004 8000)**

Name	Access	Address offset	Description	Reset value	Reference
SYSMEMREMAP	R/W	0x000	System memory remap	0x002	<a href="#">Table 6</a>
PRESETCTRL	R/W	0x004	Peripheral reset control	0x000	<a href="#">Table 7</a>
SYSPLLCTRL	R/W	0x008	System PLL control	0x000	<a href="#">Table 8</a>
SYSPLLSTAT	R	0x00C	System PLL status	0x000	<a href="#">Table 9</a>
-	-	0x010 - 0x01C	Reserved	-	-
SYSOSCCTRL	R/W	0x020	System oscillator control	0x000	<a href="#">Table 10</a>
WDTOSCCTRL	R/W	0x024	Watchdog oscillator control	0x000	<a href="#">Table 11</a>
IRCCTRL	R/W	0x028	IRC control	0x080	<a href="#">Table 12</a>
-	-	0x02C	Reserved	-	-
SYSRSTSTAT	R/W	0x030	System reset status register	0x000	<a href="#">Table 13</a>
-	-	0x034 - 0x03C	Reserved	-	-
SYSPLLCLKSEL	R/W	0x040	System PLL clock source select	0x000	<a href="#">Table 14</a>
SYSPLLCLKUEN	R/W	0x044	System PLL clock source update enable	0x000	<a href="#">Table 15</a>
-	-	0x048 - 0x06C	Reserved	-	-
MAINCLKSEL	R/W	0x070	Main clock source select	0x000	<a href="#">Table 16</a>
MAINCLKUEN	R/W	0x074	Main clock source update enable	0x000	<a href="#">Table 17</a>
SYSAHBCLKDIV	R/W	0x078	System AHB clock divider	0x001	<a href="#">Table 18</a>
-	-	0x07C	Reserved	-	-
SYSAHBCLKCTRL	R/W	0x080	System AHB clock control	0x85F	<a href="#">Table 19</a>
-	-	0x084 - 0x090	Reserved	-	-
SSP0CLKDIV	R/W	0x094	SSP0 clock divider	0x000	<a href="#">Table 20</a>
UART0CLKDIV	R/W	0x098	UART0 clock divider	0x000	<a href="#">Table 21</a>
SSP1CLKDIV	R/W	0x09C	SSP1 clock divider	0x000	<a href="#">Table 22</a>
UART1CLKDIV	R/W	0x0A0	UART1 clock divider	0x000	<a href="#">Table 23</a>
UART2CLKDIV	R/W	0x0A4	UART2 clock divider	0x000	<a href="#">Table 24</a>
-	-	0x0A8-0x0CC	Reserved	-	-
WDTCLKSEL	R/W	0x0D0	WDT clock source select	0x000	<a href="#">Table 25</a>
WDTCLKUEN	R/W	0x0D4	WDT clock source update enable	0x000	<a href="#">Table 26</a>
WDTCLKDIV	R/W	0x0D8	WDT clock divider	0x000	<a href="#">Table 27</a>
-	-	0x0DC	Reserved	-	-
CLKOUTCLKSEL	R/W	0x0E0	CLKOUT clock source select	0x000	<a href="#">Table 28</a>
CLKOUTUEN	R/W	0x0E4	CLKOUT clock source update enable	0x000	<a href="#">Table 29</a>
CLKOUTCLKDIV	R/W	0x0E8	CLKOUT clock divider	0x000	<a href="#">Table 30</a>
-	-	0x0EC - 0x0FC	Reserved	-	-
PIOPORCAP0	R	0x100	POR captured PIO status 0	user dependent	<a href="#">Table 31</a>
PIOPORCAP1	R	0x104	POR captured PIO status 1	user dependent	<a href="#">Table 32</a>

Table 5. Register overview: system control block (base address 0x4004 8000) ...continued

Name	Access	Address offset	Description	Reset value	Reference
-	R	0x108 - 0x14C	Reserved	-	-
BODCTRL	R/W	0x150	BOD control	0x000	<a href="#">Table 33</a>
SYSTCKCAL	R/W	0x154	System tick counter calibration	0x004	<a href="#">Table 34</a>
-	-	0x158 - 0x16C	Reserved	-	-
IRQLATENCY	R/W	0x170	IQR delay. Allows trade-off between interrupt latency and determinism.	0x10	<a href="#">Table 35</a>
NMISRC	R/W	0x174	NMI source selection	0x000	<a href="#">Table 36</a>
-	-	0x178 - 0x1FC	Reserved	-	-
STARTAPRP0	R/W	0x200	Start logic edge control register 0		<a href="#">Table 37</a>
STARTERP0	R/W	0x204	Start logic signal enable register 0		<a href="#">Table 38</a>
STARTSRP0CLR	W	0x208	Start logic reset register 0	n/a	<a href="#">Table 39</a>
STARTSRP0	R	0x20C	Start logic status register 0	n/a	<a href="#">Table 40</a>
-	-	0x210 - 0x22C	Reserved	-	-
PDSLEEP_CFG	R/W	0x230	Power-down states in Deep-sleep mode	0x0000 0000	<a href="#">Table 42</a>
PDAWAKE_CFG	R/W	0x234	Power-down states after wake-up from Deep-sleep mode	0x0000 EDF0	<a href="#">Table 43</a>
PDRUN_CFG	R/W	0x238	Power-down configuration register	0x0000 EDF0	<a href="#">Table 44</a>
-	-	0x23C - 0x3F0	Reserved	-	-

#### 4.4.1 System memory remap register

The system memory remap register selects whether the ARM interrupt vectors are read from the boot ROM, the flash, or the SRAM. By default, the flash memory is mapped to address 0x0000 0000. When the MAP bits in the SYSMEMREMAP register are set to 0x0 or 0x1, the boot ROM or RAM respectively are mapped to the bottom 512 bytes of the memory map (addresses 0x0000 0000 to 0x0000 0200).

Table 6. System memory remap register (SYSMEMREMAP, address 0x4004 8000) bit description

Bit	Symbol	Value	Description	Reset value
1:0	MAP		System memory remap	10
		0x0	Boot Loader Mode. Interrupt vectors are re-mapped to Boot ROM.	
		0x1	User RAM Mode. Interrupt vectors are re-mapped to Static RAM.	
		0x2	User Flash Mode. Interrupt vectors are not re-mapped and reside in Flash.	
31:2	-	-	Reserved	0x00

### 4.4.2 Peripheral reset control register

This register allows software to reset the SSP and I2C peripherals. Writing a zero to the SSP0/1\_RST\_N or I2C\_RST\_N bits resets the SSP0/1 or I2C peripheral. Writing a one de-asserts the reset.

**Remark:** Before accessing the SSP and I2C peripherals, write a one to this register to ensure that the reset signals to the SSP and I2C are de-asserted.

**Table 7. Peripheral reset control register (PRESETCTRL, address 0x4004 8004) bit description**

Bit	Symbol	Value	Description	Reset value
0	SSP0_RST_N		SSP0 reset control	0
		0	Resets the SSP0 peripheral.	
		1	SSP0 reset de-asserted.	
1	I2C_RST_N		I2C reset control	0
		0	Resets the I2C peripheral.	
		1	I2C reset de-asserted.	
2	SSP1_RST_N		SSP1 reset control	0
		0	Resets the SSP1 peripheral.	
		1	SSP1 reset de-asserted.	
31:3	-	-	Reserved	0x00

### 4.4.3 System PLL control register

This register connects and enables the system PLL and configures the PLL multiplier and divider values. The PLL accepts an input frequency from 10 MHz to 25 MHz from various clock sources. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU, peripherals, and memories. The PLL can produce a clock up to the maximum allowed for the CPU.

**Table 8. System PLL control register (SYSPLLCTRL, address 0x4004 8008) bit description**

Bit	Symbol	Value	Description	Reset value
4:0	MSEL		Feedback divider value. The division value M is the programmed MSEL value + 1. 00000: Division ratio M = 1 to 11111: Division ratio M = 32.	0x000
6:5	PSEL		Post divider ratio P. The division ratio is $2 \times P$ .	0x00
		0x0	P = 1	
		0x1	P = 2	
		0x2	P = 4	
		0x3	P = 8	
31:7	-	-	Reserved. Do not write ones to reserved bits.	0x0

#### 4.4.4 System PLL status register

This register is a Read-only register and supplies the PLL lock status (see [Section 4.5.4.1](#)).

**Table 9. System PLL status register (SYSPLLSTAT, address 0x4004 800C) bit description**

Bit	Symbol	Value	Description	Reset value
0	LOCK		PLL lock status	0x0
		0	PLL not locked	
		1	PLL locked	
31:1	-	-	Reserved	0x00

#### 4.4.5 System oscillator control register

This register configures the frequency range for the system oscillator.

**Table 10. System oscillator control register (SYSOSCCTRL, address 0x4004 8020) bit description**

Bit	Symbol	Value	Description	Reset value
0	BYPASS		Bypass system oscillator	0x0
		0	Oscillator is not bypassed.	
		1	Bypass enabled. PLL input (sys_osc_clk) is fed directly from the XTALIN pin bypassing the oscillator. Use this mode when using an external clock source instead of the crystal oscillator.	
1	FREQRANGE		Determines frequency range for Low-power oscillator.	0x0
		0	Low. 1 - 20 MHz frequency range.	
		1	High. 15 - 25 MHz frequency range	
31:2	-	-	Reserved	0x00

#### 4.4.6 Watchdog oscillator control register

This register configures the watchdog oscillator. The oscillator consists of an analog and a digital part. The analog part contains the oscillator function and generates an analog clock (Fclkana). With the digital part, the analog output clock (Fclkana) can be divided to the required output clock frequency wdt\_osc\_clk. The analog output frequency (Fclkana) can be adjusted with the FREQSEL bits between 600 kHz and 4.6 MHz. With the digital part Fclkana will be divided (divider ratios = 2, 4,...,64) to wdt\_osc\_clk using the DIVSEL bits.

The output clock frequency of the watchdog oscillator can be calculated as  

$$\text{wdt\_osc\_clk} = \text{Fclkana} / (2 \times (1 + \text{DIVSEL})) = 9.3 \text{ kHz to } 2.3 \text{ MHz (nominal values)}.$$

**Remark:** Any setting of the FREQSEL bits will yield a Fclkana value within  $\pm 40\%$  of the listed frequency value. The watchdog oscillator is the clock source with the lowest power consumption. If accurate timing is required, use the IRC or system oscillator.

**Remark:** The frequency of the watchdog oscillator is undefined after reset. The watchdog oscillator frequency must be programmed by writing to the WDTOSCCTRL register before using the watchdog oscillator.

**Table 11. Watchdog oscillator control register (WDTOSCCTRL, address 0x4004 8024) bit description**

Bit	Symbol	Value	Description	Reset value
4:0	DIVSEL		Select divider for Fclkana. $\text{wdt\_osc\_clk} = \text{Fclkana} / (2 \times (1 + \text{DIVSEL}))$ 00000: $2 \times (1 + \text{DIVSEL}) = 2$ 00001: $2 \times (1 + \text{DIVSEL}) = 4$ to 11111: $2 \times (1 + \text{DIVSEL}) = 64$	0
8:5	FREQSEL		Select watchdog oscillator analog output frequency (Fclkana).	0x00
		0x1	0.6 MHz	
		0x2	1.05 MHz	
		0x3	1.4 MHz	
		0x4	1.75 MHz	
		0x5	2.1 MHz	
		0x6	2.4 MHz	
		0x7	2.7 MHz	
		0x8	3.0 MHz	
		0x9	3.25 MHz	
		0xA	3.5 MHz	
		0xB	3.75 MHz	
		0xC	4.0 MHz	
		0xD	4.2 MHz	
		0xE	4.4 MHz	
		0xF	4.6 MHz	
31:9	-	-	Reserved	0x00

#### 4.4.7 Internal resonant crystal control register

This register is used to trim the on-chip 12 MHz oscillator. The trim value is factory-preset and written by the boot code on start-up.

**Table 12. Internal resonant crystal control register (IRCCTRL, address 0x4004 8028) bit description**

Bit	Symbol	Description	Reset value
7:0	TRIM	Trim value	0x1000 0000, then flash will reprogram
31:8	-	Reserved	0x00

#### 4.4.8 System reset status register

The SYSRSTSTAT register shows the source of the latest reset event. Write a one to clear the reset.

The POR event clears all other bits in this register. If any reset signal - for example EXTRST - remains asserted after the POR signal is negated, then its bit is set to detected in this register.



The reset value given in [Table 13](#) applies to the POR reset.

**Table 13. System reset status register (SYSRSTSTAT, address 0x4004 8030) bit description**

Bit	Symbol	Value	Description	Reset value
0	POR		POR reset status	0x0
		0	No POR detected.	
		1	POR detected. Writing a one clears this reset.	
1	EXTRST		Status of the external $\overline{\text{RESET}}$ pin.	0x0
		0	No $\overline{\text{RESET}}$ event detected.	
		1	$\overline{\text{RESET}}$ detected. Writing a one clears this reset.	
2	WDT		Status of the Watchdog reset	0x0
		0	No WDT reset detected.	
		1	WDT reset detected. Writing a one clears this reset.	
3	BOD		Status of the Brown-out detect reset	0x0
		0	No BOD reset detected.	
		1	BOD reset detected. Writing a one clears this reset.	
4	SYSRST		Status of the software system reset	0x0
		0	No System reset detected.	
		1	System reset detected. Writing a one clears this reset.	
31:5	-	-	Reserved	0x0

#### 4.4.9 System PLL clock source select register

This register selects the clock source for the system PLL. The SYSPLLCLKUEN register (see [Section 4.4.10](#)) must be toggled from LOW to HIGH for the update to take effect.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 14. System PLL clock source select register (SYSPLLCLKSEL, address 0x4004 8040) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	SEL		System PLL clock source	0x00
		0x0	IRC oscillator	
		0x1	System oscillator	
		0x2	Reserved	
		0x3	Reserved	
31:2	-	-	Reserved	0x00

#### 4.4.10 System PLL clock source update enable register

This register updates the clock source of the system PLL with the new input clock after the SYSPLLCLKSEL register has been written to. In order for the update to take effect, first write a zero to the SYSPLLUEN register and then write a one to SYSPLLUEN.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 15. System PLL clock source update enable register (SYSPLLCLKUEN, address 0x4004 8044) bit description**

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable system PLL clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

#### 4.4.11 Main clock source select register

This register selects the main system clock which can be either any input to the system PLL, the output from the system PLL (sys\_pllclkout), or the watchdog or IRC oscillators directly. The main system clock clocks the core, the peripherals, and the memories.

The MAINCLKUEN register (see [Section 4.4.12](#)) must be toggled from LOW to HIGH for the update to take effect.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 16. Main clock source select register (MAINCLKSEL, address 0x4004 8070) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	SEL		Clock source for main clock	0x00
		0x0	IRC oscillator	
		0x1	PLL input. Input clock to system PLL	
		0x2	WDT oscillator	
		0x3	PLL output. System PLL clock out	
31:2	-	-	Reserved	0x00

#### 4.4.12 Main clock source update enable register

This register updates the clock source of the main clock with the new input clock after the MAINCLKSEL register has been written to. In order for the update to take effect, first write a zero to the MAINCLKUEN register and then write a one to MAINCLKUEN.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 17. Main clock source update enable register (MAINCLKUEN, address 0x4004 8074) bit description**

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable main clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

#### 4.4.13 System AHB clock divider register

This register divides the main clock to provide the system clock to the core, memories, and the peripherals. The system clock can be shut down completely by setting the DIV bits to 0x0.

**Table 18. System AHB clock divider register (SYSAHBCLKDIV, address 0x4004 8078) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	System AHB clock divider values 0: System clock disabled. 1: Divide by 1. to 255: Divide by 255.	0x01
31:8	-	Reserved	0x00

#### 4.4.14 System AHB clock control register

The AHBCLKCTRL register enables the clocks to individual system and peripheral blocks. The system clock (sys\_ahb\_clk[0], bit 0 in the AHBCLKCTRL register) provides the clock for the AHB to APB bridge, the AHB matrix, the ARM Cortex-M0, the Syscon block, and the PMU. This clock cannot be disabled.

**Table 19. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description**

Bit	Symbol	Value	Description	Reset value
0	SYS		Enables clock for AHB to APB bridge, to the AHB matrix, to the Cortex-M0 FCLK and HCLK, to the SysCon, and to the PMU. This bit is read only.	1
		0	Reserved	
		1	Enable	
1	ROM		Enables clock for ROM.	1
		0	Disable	
		1	Enable	
2	RAM		Enables clock for RAM.	1
		0	Disable	
		1	Enable	
3	FLASHREG		Enables clock for flash register interface.	1
		0	Disabled	
		1	Enabled	

**Table 19. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description ...continued**

Bit	Symbol	Value	Description	Reset value
4	FLASHARRAY		Enables clock for flash array access.	1
		0	Disabled	
		1	Enabled	
5	I2C		Enables clock for I2C.	0
		0	Disable	
		1	Enable	
6	GPIO		Enables clock for GPIO.	1
		0	Disable	
		1	Enable	
7	CT16B0		Enables clock for 16-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
8	CT16B1		Enables clock for 16-bit counter/timer 1.	0
		0	Disable	
		1	Enable	
9	CT32B0		Enables clock for 32-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
10	CT32B1		Enables clock for 32-bit counter/timer 1.	0
		0	Disable	
		1	Enable	
11	SSP0		Enables clock for SSP0.	1
		0	Disable	
		1	Enable	
12	UART0		Enables clock for UART0.	0
		0	Disable	
		1	Enable	
13	ADC		Enables clock for 12-bit ADC.	0
		0	Disable	
		1	Enable	
14	-		Reserved	0
15	WDT		Enables clock for WWDT.	0
		0	Disable	
		1	Enable	
16	IOCON		Enables clock for I/O configuration block.	0
		0	Disable	
		1	Enable	

**Table 19. System AHB clock control register (SYSAHBCLKCTRL, address 0x4004 8080) bit description ...continued**

Bit	Symbol	Value	Description	Reset value
17	-		Reserved.	0
		0	Disable	
		1	Enable	
18	SSP1		Enables clock for SSP1.	0
		0	Disable	
		1	Enable	
19	UART1		Enables clock for UART1.	0
		0	Disable	
		1	Enable	
20	UART2		Enables clock for UART2.	0
		0	Disable	
		1	Enable	
31:21	-	-	Reserved	0x00

#### 4.4.15 SSP0 clock divider register

This register configures the SSP0 peripheral clock SSP0\_PCLK. The SSP0\_PCLK can be shut down by setting the DIV bits to 0x0.

**Table 20. SSP0 clock divider register (SSP0CLKDIV, address 0x4004 8094) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	SSP0_PCLK clock divider values 0: Disable SSP0_PCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.16 UART0 clock divider register

This register configures the UART peripheral clock UART\_PCLK. The UART\_PCLK can be shut down by setting the DIV bits to 0x0.

**Table 21. UART0 clock divider register (UART0CLKDIV, address 0x4004 8098) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	UART0_PCLK clock divider values 0: Disable UART0_PCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.17 SSP1 clock divider register

This register configures the SSP1 peripheral clock SSP1\_PCLK. The SSP1\_PCLK can be shut down by setting the DIV bits to 0x0.

**Table 22. SSP1 clock divider register (SSP1CLKDIV, address 0x4004 809C) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	SSP1_PCLK clock divider values 0: Disable SSP1_PCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.18 UART1 clock divider register

This register configures the UART1 peripheral clock UART1\_PCLK. The UART1\_PCLK can be shut down by setting the DIV bits to 0x0.

**Table 23. UART1 clock divider register (UART1CLKDIV, address 0x4004 80A0) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	UART1_PCLK clock divider values 0: Disable UART1_PCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.19 UART2 clock divider register

This register configures the UART2 peripheral clock UART2\_PCLK. The UART2\_PCLK can be shut down by setting the DIV bits to 0x0.

**Table 24. UART2 clock divider register (UART2CLKDIV, address 0x4004 80A4) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	UART2_PCLK clock divider values 0: Disable UART2_PCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.20 WDT clock source select register

This register selects the clock source for the watchdog timer. The WDTCLKUEN register (see [Section 4.4.21](#)) must be toggled from LOW to HIGH for the update to take effect.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 25. WDT clock source select register (WDTCLKSEL, address 0x4004 80D0) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	SEL		WDT clock source	0x00
		0x0	IRC oscillator	
		0x1	Main clock	
		0x2	Watchdog oscillator	
		0x3	Reserved	
31:2	-	-	Reserved	0x00

#### 4.4.21 WDT clock source update enable register

This register updates the clock source of the watchdog timer with the new input clock after the WDTCLKSEL register has been written to. In order for the update to take effect at the input of the watchdog timer, first write a zero to the WDTCLKUEN register and then write a one to WDTCLKUEN.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 26. WDT clock source update enable register (WDTCLKUEN, address 0x4004 80D4) bit description**

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable WDT clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

#### 4.4.22 WDT clock divider register

This register determines the divider values for the watchdog clock wdt\_clk.

**Table 27. WDT clock divider register (WDTCLKDIV, address 0x4004 80D8) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	WDT clock divider values 0: Disable WDCLK. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.23 CLKOUT clock source select register

This register configures the clkout\_clk signal to be output on the CLKOUT pin. All three oscillators and the main clock can be selected for the clkout\_clk clock.

The CLKOUTCLKUEN register (see [Section 4.4.24](#)) must be toggled from LOW to HIGH for the update to take effect.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 28. CLKOUT clock source select register (CLKOUTCLKSEL, address 0x4004 80E0) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	SEL		CLKOUT clock source	0x00
		0x0	IRC oscillator	
		0x1	System oscillator	
		0x2	Watchdog oscillator	
		0x3	Main clock	
31:2	-	-	Reserved	0x00

#### 4.4.24 CLKOUT clock source update enable register

This register updates the clock source of the CLKOUT pin with the new clock after the CLKOUTCLKSEL register has been written to. In order for the update to take effect at the input of the CLKOUT pin, first write a zero to the CLKCLKUEN register and then write a one to CLKCLKUEN.

**Remark:** When switching clock sources, both clocks must be running before the clock source is updated.

**Table 29. CLKOUT clock source update enable register (CLKOUTUEN, address 0x4004 80E4) bit description**

Bit	Symbol	Value	Description	Reset value
0	ENA		Enable CLKOUT clock source update	0x0
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	0x00

#### 4.4.25 CLKOUT clock divider register

This register determines the divider value for the clock output signal on the CLKOUT pin.

**Table 30. CLKOUT clock divider registers (CLKOUTCLKDIV, address 0x4004 80E8) bit description**

Bit	Symbol	Description	Reset value
7:0	DIV	Clock output divider values 0: Disable CLKOUT. 1: Divide by 1. to 255: Divide by 255.	0x00
31:8	-	Reserved	0x00

#### 4.4.26 POR captured PIO status register 0

The PIOPORCAP0 register captures the state (HIGH or LOW) of the PIO pins of ports 0, 1, and 2 (pins PIO2\_0 to PIO2\_7) at power-on-reset. Each bit represents the reset state of one GPIO pin. This register is a read-only status register.



**Table 31. POR captured PIO status registers 0 (PIOPORCAP0, address 0x4004 8100) bit description**

Bit	Symbol	Description	Reset value
11:0	CAPPIO0_n	Raw reset status input PIO0_n: PIO0_11 to PIO0_0	User implementation dependent
23:12	CAPPIO1_n	Raw reset status input PIO1_n: PIO1_11 to PIO1_0	User implementation dependent
31:24	CAPPIO2_n	Raw reset status input PIO2_n: PIO2_7 to PIO2_0	User implementation dependent

#### 4.4.27 POR captured PIO status register 1

The PIOPORCAP1 register captures the state (HIGH or LOW) of the PIO pins of port 2 (PIO2\_8 to PIO2\_11) and port 3 at power-on-reset. Each bit represents the reset state of one PIO pin. This register is a read-only status register.

**Table 32. POR captured PIO status registers 1 (PIOPORCAP1, address 0x4004 8104) bit description**

Bit	Symbol	Description	Reset value
0	CAPPIO2_8	Raw reset status input PIO2_8	User implementation dependent
1	CAPPIO2_9	Raw reset status input PIO2_9	User implementation dependent
2	CAPPIO2_10	Raw reset status input PIO2_10	User implementation dependent
3	CAPPIO2_11	Raw reset status input PIO2_11	User implementation dependent
4	CAPPIO3_0	Raw reset status input PIO3_0	User implementation dependent
5	CAPPIO3_1	Raw reset status input PIO3_1	User implementation dependent
6	CAPPIO3_2	Raw reset status input PIO3_2	User implementation dependent
7	CAPPIO3_3	Raw reset status input PIO3_3	User implementation dependent
8	CAPPIO3_4	Raw reset status input PIO3_4	User implementation dependent
9	CAPPIO3_5	Raw reset status input PIO3_5	User implementation dependent
31:10	-	Reserved	-

#### 4.4.28 BOD control register

The BOD control register selects up to four separate threshold values for sending a BOD interrupt to the NVIC and for forced reset. Reset and interrupt threshold values listed are typical values.

**Table 33. BOD control register (BODCTRL, address 0x4004 8150) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	BODRSTLEV		BOD reset level	00
		0x0	Level 0: The reset assertion threshold voltage is 1.46 V; the reset de-assertion threshold voltage is 1.63 V.	
		0x1	Level 1: The reset assertion threshold voltage is 2.06 V; the reset de-assertion threshold voltage is 2.15 V.	
		0x2	Level 2: The reset assertion threshold voltage is 2.35 V; the reset de-assertion threshold voltage is 2.43 V.	
		0x3	Level 3: The reset assertion threshold voltage is 2.63 V; the reset de-assertion threshold voltage is 2.71 V.	

Table 33. BOD control register (BODCTRL, address 0x4004 8150) bit description

Bit	Symbol	Value	Description	Reset value
3:2	BODINTVAL		BOD interrupt level	00
		0x0	Level 0: Reserved.	
		0x1	Level 1: The interrupt assertion threshold voltage is 2.22 V; the interrupt de-assertion threshold voltage is 2.35 V.	
		0x2	Level 2: The interrupt assertion threshold voltage is 2.52 V; the interrupt de-assertion threshold voltage is 2.66 V.	
		0x3	Level 3: The interrupt assertion threshold voltage is 2.80 V; the interrupt de-assertion threshold voltage is 2.90 V.	
4	BODRSTENA		BOD reset enable	0
		0	Disable reset function.	
		1	Enable reset function.	
31:5	-	-	Reserved	0x00

#### 4.4.29 System tick counter calibration register

This register determines the value of the SYST\_CALIB register (see [Table 223](#)).

Table 34. System tick timer calibration register (SYSTCKCAL, address 0x4004 8154) bit description

Bit	Symbol	Description	Reset value
25:0	CAL	System tick timer calibration value	0x04
31:26	-	Reserved	0x00

#### 4.4.30 IRQ latency register

The IRQLATENCY register is an eight-bit register which specifies the minimum number of cycles (0-255) permitted for the system to respond to an interrupt request. The intent of this register is to allow the user to select a trade-off between interrupt response time and determinism.

Setting this parameter to a very low value (e.g. zero) will guarantee the best possible interrupt performance but will also introduce a significant degree of uncertainty and jitter. Requiring the system to always take a larger number of cycles (whether it needs it or not) will reduce the amount of uncertainty but may not necessarily eliminate it.

Theoretically, the ARM Cortex-M0 core should always be able to service an interrupt request within 15 cycles. System factors external to the cpu, however, bus latencies, peripheral response times, etc. can increase the time required to complete a previous instruction before an interrupt can be serviced. Therefore, accurately specifying a minimum number of cycles that will ensure determinism will depend on the application.

The default setting for this register is 0x010.

**Table 35. IRQ latency register (IRQLATENCY, address 0x4004 8170) bit description**

Bit	Symbol	Description	Reset value
7:0	LATENCY	8-bit latency value	0x010
31:8	-	Reserved	-

#### 4.4.31 NMI source selection register

The NMI source selection register selects a peripheral interrupts as source for the NMI interrupt of the ARM Cortex-M0 core. For a list of all peripheral interrupts and their IRQ numbers see [Table 3](#). For a description of the NMI functionality, see [Section 21.3.3.2](#).

**Table 36. NMI source selection register (NMISRC, address 0x4004 8174) bit description**

Bit	Symbol	Description	Reset value
4:0	IRQNO	The IRQ number of the interrupt that acts as the Non-Maskable Interrupt (NMI) if bit 31 in this register is 1.	0
30:5	-	Reserved	-
31	NMIEN	Write a 1 to this bit to enable the Non-Maskable Interrupt (NMI) source selected by bits 4:0.	0

Note: If the NMISRC register is used to select an interrupt as the source of Non-Maskable interrupts, and the selected interrupt is enabled, one interrupt request can result in both a Non-Maskable and a normal interrupt. Avoid this situation by disabling the normal interrupt in the NVIC, as described in [Section 21.5.2](#).

#### 4.4.32 Start logic edge control register 0

The STARTAPRP0 register controls the start logic inputs of ports 0 (PIO0\_0 to PIO0\_11) and 1 (PIO1\_0). This register selects a falling or rising edge on the corresponding PIO input to produce a falling or rising clock edge, respectively, for the start logic (see [Section 5.4.2.2](#)).

Every bit in the STARTAPRP0 register controls one port input and is connected to one wake-up interrupt in the NVIC. Bit 0 in the STARTAPRP0 register corresponds to interrupt 0, bit 1 to interrupt 1, etc. (see [Table 3](#)), up to a total of 13 interrupts.

**Remark:** Each interrupt connected to a start logic input must be enabled in the NVIC if the corresponding PIO pin is used to wake up the chip from Deep-sleep mode.

**Table 37. Start logic edge control register 0 (STARTAPRP0, address 0x4004 8200) bit description**

Bit	Symbol	Description	Reset value
11:0	APRPIO0	Edge select for start logic input PIO0_n: PIO0_11 to PIO0_0 0 = Falling edge 1 = Rising edge	0x0
12	APRPIO1	Edge select for start logic input PIO1_0 0 = Falling edge 1 = Rising edge	0x0
31:13	-	Reserved. Do not write a 1 to reserved bits in this register.	0x0

#### 4.4.33 Start logic signal enable register 0

This STARTERP0 register enables or disables the start signal bits in the start logic. The bit assignment is identical to [Table 37](#).

**Table 38. Start logic signal enable register 0 (STARTERP0, address 0x4004 8204) bit description**

Bit	Symbol	Description	Reset value
11:0	ERPIO0	Enable start signal for start logic input PIO0_n: PIO0_11 to PIO0_0 0 = Disabled 1 = Enabled	0x0
12	ERPIO1	Enable start signal for start logic input PIO1_0 0 = Disabled 1 = Enabled	0x0
31:13	-	Reserved. Do not write a 1 to reserved bits in this register.	0x0

#### 4.4.34 Start logic reset register 0

Writing a one to a bit in the STARTRSRP0CLR register resets the start logic state. The bit assignment is identical to [Table 37](#). The start-up logic uses the input signals to generate a clock edge for registering a start signal. This clock edge (falling or rising) sets the interrupt for waking up from Deep-sleep mode. Therefore, the start-up logic states must be cleared before being used.

**Table 39. Start logic reset register 0 (STARTRSRP0CLR, address 0x4004 8208) bit description**

Bit	Symbol	Description	Reset value
11:0	RSRPIO0	Start signal reset for start logic input PIO0_n:PIO0_11 to PIO0_0 0 = Do nothing. 1 = Writing 1 resets the start signal.	n/a
12	RSRPIO1	Start signal reset for start logic input PIO1_0 0 = Do nothing. 1 = Writing 1 resets the start signal.	n/a
31:13	-	Reserved. Do not write a 1 to reserved bits in this register.	n/a

#### 4.4.35 Start logic status register 0

This register reflects the status of the enabled start signal bits. The bit assignment is identical to [Table 37](#). Each bit (if enabled) reflects the state of the start logic, i.e. whether or not a wake-up signal has been received for a given pin.

**Table 40. Start logic status register 0 (STARTSRP0, address 0x4004 820C) bit description**

Bit	Symbol	Description	Reset value
11:0	SRPIO0	Start signal status for start logic input PIO0_n: PIO0_11 to PIO0_0 0 = No start signal received. 1 = Start signal pending.	n/a
12	SRPIO1	Start signal status for start logic input PIO1_0 0 = No start signal received. 1 = Start signal pending.	n/a
31:13	-	Reserved	n/a

#### 4.4.36 Deep-sleep mode configuration register

This register controls the behavior of the WatchDog (WD) oscillator and the BOD circuit when the device enters Deep-sleep mode.

This register **must be initialized at least once before entering Deep-sleep mode** with one of the four values shown in [Table 41](#):

**Table 41. Allowed values for PDSLEEPCFG register**

Configuration	WD oscillator on	WD oscillator off
<b>BOD on</b>	PDSLEEPCFG = 0x0000 18B7	PDSLEEPCFG = 0x0000 18F7
<b>BOD off</b>	PDSLEEPCFG = 0x0000 18BF	PDSLEEPCFG = 0x0000 18FF

**Remark:** Failure to initialize and program this register correctly may result in undefined behavior of the microcontroller. The values listed in [Table 41](#) are the only values allowed for PDSLEEPCFG register.

To select the appropriate power configuration for Deep-sleep mode, consider the following:

- **BOD:** Leaving the BOD circuit enabled will protect the part from a low voltage event occurring while the part is in Deep-sleep mode. However, the BOD circuit causes an additional current drain in Deep-sleep mode.
- **WD oscillator:** The watchdog oscillator can be left running in Deep-sleep mode to provide a clock for the watchdog timer or a general purpose timer if they are needed for timing a wake-up event (see [Section 5.4.2.3](#) for details). In this case, the watchdog oscillator analog output frequency must be set to its lowest value (bits FREQSEL in the WDTOSCCTRL = 0001, see [Table 11](#)) and all peripheral clocks other than the timer clock must be disabled in the SYSAHBCLKCTRL register (see [Table 19](#)) before entering Deep-sleep mode.

The watchdog oscillator, if running, contributes an additional current drain in Deep-sleep mode.

**Remark:** Reserved bits in this register must always be written as indicated. This register must be initialized correctly before entering Deep-sleep mode.

**Table 42. Deep-sleep configuration register (PDSLEEPCFG, address 0x4004 8230) bit description**

Bit	Symbol	Value	Description	Reset value
2:0	NOTUSED0		Reserved. Always write these bits as 111.	0
3	BOD_PD		BOD power-down control in Deep-sleep mode, see <a href="#">Table 41</a> .	0
		0	Powered	
		1	Powered down	
5:4	NOTUSED1		Reserved. Always write these bits as 11.	0
6	WDTOSC_PD		Watchdog oscillator power control in Deep-sleep mode, see <a href="#">Table 41</a> .	0
		0	Powered	
		1	Powered down	
7	NOTUSED2		Reserved. Always write this bit as 1.	0
10:8	NOTUSED3		Reserved. <b>Always write these bits as 000.</b>	0
12:11	NOTUSED4		Reserved. Always write these bits as 11.	0
31:13	-	0	Reserved	0

#### 4.4.37 Wake-up configuration register

The bits in this register determine the state the chip enters when it is waking up from Deep-sleep mode.

By default, the IRC and flash memory are powered and running and the BOD circuit is enabled when the chip wakes up from Deep-sleep mode.

**Remark:** Reserved bits must be always written as indicated.

**Table 43. Wake-up configuration register (PDAWAKECFG, address 0x4004 8234) bit description**

Bit	Symbol	Value	Description	Reset value
0	IRCOUT_PD		IRC oscillator output wake-up configuration	0
		0	Powered	
		1	Powered down	
1	IRC_PD		IRC oscillator power-down wake-up configuration	0
		0	Powered	
		1	Powered down	
2	FLASH_PD		Flash wake-up configuration	0
		0	Powered	
		1	Powered down	
3	BOD_PD		BOD wake-up configuration	0
		0	Powered	
		1	Powered down	

**Table 43. Wake-up configuration register (PDAWAKECFG, address 0x4004 8234) bit description ...continued**

Bit	Symbol	Value	Description	Reset value
4	ADC_PD		ADC wake-up configuration	1
		0	Powered	
		1	Powered down	
5	SYSOSC_PD		System oscillator wake-up configuration	1
		0	Powered	
		1	Powered down	
6	WDTOSC_PD		Watchdog oscillator wake-up configuration	1
		0	Powered	
		1	Powered down	
7	SYSPLL_PD		System PLL wake-up configuration	1
		0	Powered	
		1	Powered down	
8	NOTUSED0		Reserved. Always write this bit as 1.	1
9	NOTUSED1		Reserved. <b>Always write this bit as 0.</b>	0
10	NOTUSED2		Reserved. Always write this bit as 1.	1
11	NOTUSED3		Reserved. <b>Always write this bit as 1.</b>	1
12	NOTUSED4		Reserved. <b>Always write this bit as 0.</b>	0
15:13	NOTUSED5		Reserved. Always write these bits as 111.	111
31:16	-	-	Reserved	-

#### 4.4.38 Power-down configuration register

The bits in the PDRUNCFG register control the power to the various analog blocks. This register can be written to at any time while the chip is running, and a write will take effect immediately with the exception of the power-down signal to the IRC.

To avoid glitches when powering down the IRC, the IRC clock is automatically switched off at a clean point. Therefore, for the IRC a delay is possible before the power-down state takes effect.

By default, the IRC and flash memory are powered and running and the BOD circuit is enabled.

**Remark:** Reserved bits must be always written as indicated.

**Table 44. Power-down configuration register (PDRUNCFG, address 0x4004 8238) bit description**

Bit	Symbol	Value	Description	Reset value
0	IRCOUT_PD		IRC oscillator output power-down	0
		0	Powered	
		1	Powered down	

Table 44. Power-down configuration register (PDRUNCFG, address 0x4004 8238) bit description ...continued

Bit	Symbol	Value	Description	Reset value
1	IRC_PD		IRC oscillator power-down	0
		0	Powered	
		1	Powered down	
2	FLASH_PD		Flash power-down	0
		0	Powered	
		1	Powered down	
3	BOD_PD		BOD power-down	0
		0	Powered	
		1	Powered down	
4	ADC_PD		ADC power-down	1
		0	Powered	
		1	Powered down	
5	SYSOSC_PD		System oscillator power-down	1
		0	Powered	
		1	Powered down	
6	WDTOSC_PD		Watchdog oscillator power-down	1
		0	Powered	
		1	Powered down	
7	SYSPLL_PD		System PLL power-down	1
		0	Powered	
		1	Powered down	
8	NOTUSED0		Reserved. Always write this bit as 1.	1
9	NOTUSED1		Reserved. <b>Always write this bit as 0.</b>	0
10	NOTUSED2		Reserved. Always write this bit as 1.	1
11	NOTUSED3		Reserved. <b>Always write this bit as 1.</b>	1
12	NOTUSED4		Reserved. <b>Always write this bit as 0.</b>	0
15:13	NOTUSED5		Reserved. Always write these bits as 111.	111
31:16	-	-	Reserved	-

## 4.5 Functional description

### 4.5.1 Reset

Reset has four sources on this part: the  $\overline{\text{RESET}}$  pin, Watchdog Reset, Power-On Reset (POR), and Brown Out Detect (BOD). In addition, there is an ARM software reset.

The  $\overline{\text{RESET}}$  pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the IRC causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, and the flash controller has completed its initialization.



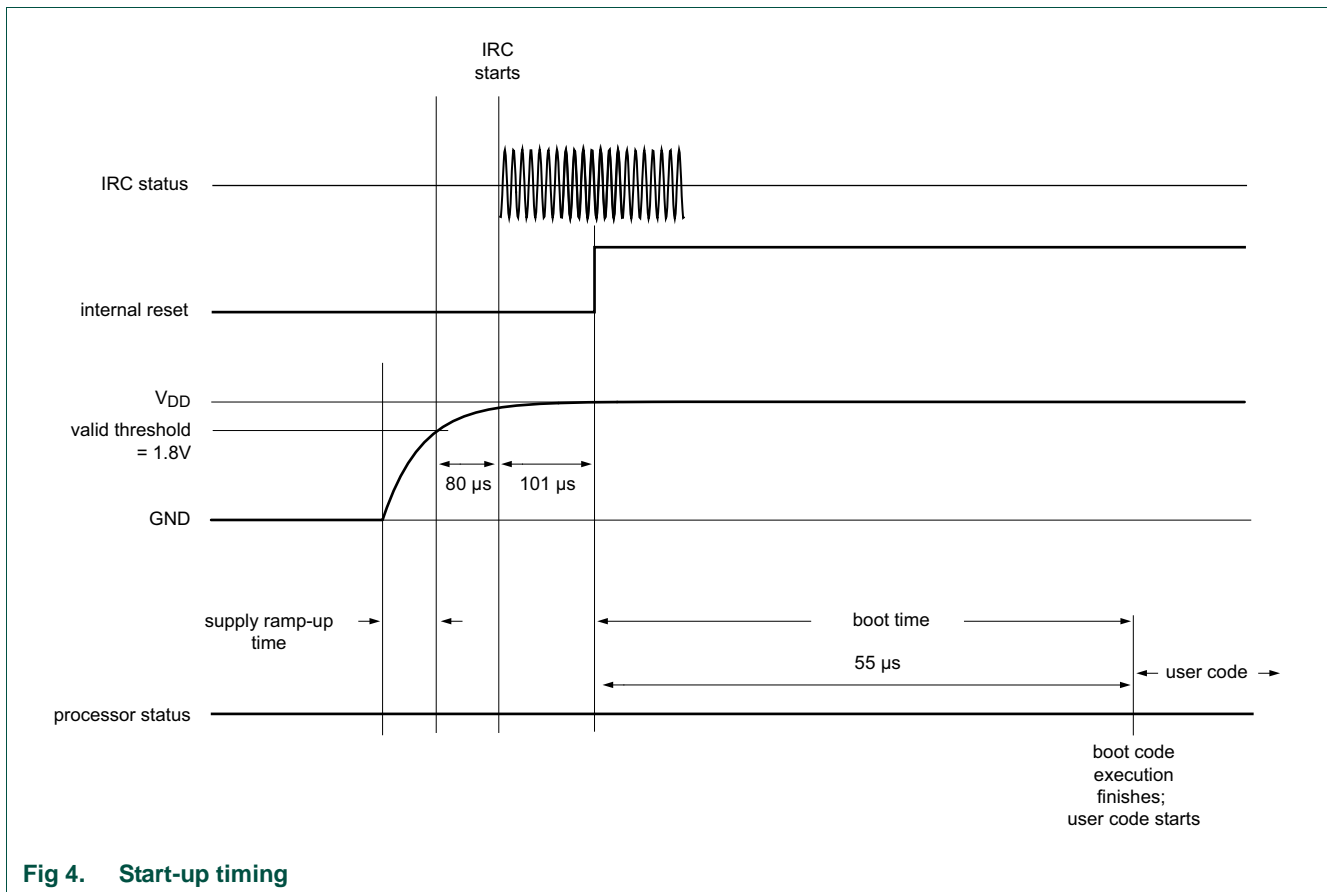
On the assertion of any reset source (ARM software reset, POR, BOD reset, External reset, and Watchdog reset), the following processes are initiated:

1. The IRC starts up. After the IRC-start-up time (maximum of 6  $\mu\text{s}$  on power-up), the IRC provides a stable clock output.
2. The flash is powered up. This takes approximately 100  $\mu\text{s}$ . Then the flash initialization sequence is started.
3. The boot code in the ROM starts. The boot code performs the boot tasks and may jump to the flash.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

### 4.5.2 Start-up behavior

See [Figure 4](#) for the start-up timing after reset. The IRC is the default clock at Reset and provides a clean system clock shortly after the supply voltage reaches the threshold value of 1.8 V.



**Fig 4. Start-up timing**

### 4.5.3 Brown-out detection

This part includes up to four levels for monitoring the voltage on the  $V_{DD}$  pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading the NVIC status register (see [Table 3](#)). Four threshold levels can be selected to cause a forced reset of the chip (see [Table 33](#)).

### 4.5.4 System PLL functional description

This part uses the system PLL to create the clocks for the core and peripherals.

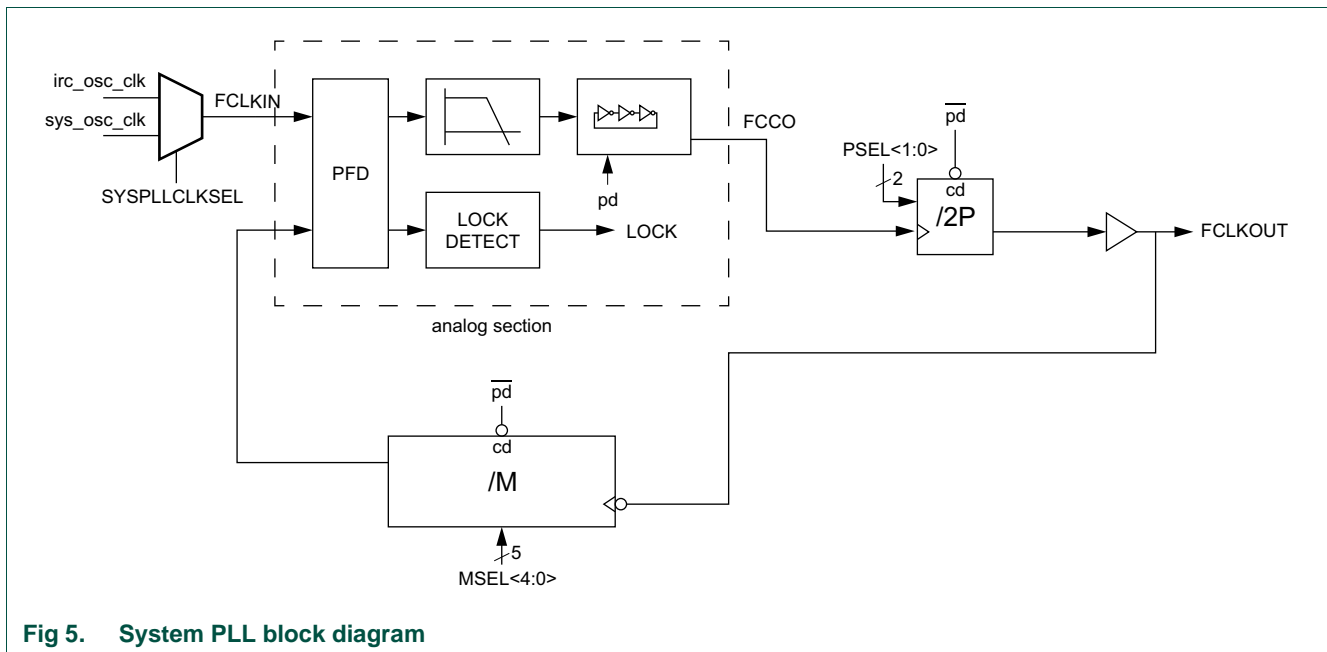


Fig 5. System PLL block diagram

The block diagram of this PLL is shown in [Figure 5](#). The input frequency range is 10 MHz to 25 MHz. The input clock is fed directly to the Phase-Frequency Detector (PFD). This block compares the phase and frequency of its inputs, and generates a control signal when phase and/ or frequency do not match. The loop filter filters these control signals and drives the current controlled oscillator (CCO), which generates the main clock and optionally two additional phases. The CCO frequency range is 156 MHz to 320 MHz. These clocks are either divided by  $2^P$  by the programmable post divider to create the output clock(s), or are sent directly to the output(s). The main output clock is then divided by  $M$  by the programmable feedback divider to generate the feedback clock. The output signal of the phase-frequency detector is also monitored by the lock detector, to signal when the PLL has locked on to the input clock.

**Remark:** The divider values for  $P$  and  $M$  must be selected so that the PLL output clock frequency `FCLKOUT` is lower than 100 MHz.

#### 4.5.4.1 Lock detector

The lock detector measures the phase difference between the rising edges of the input and feedback clocks. Only when this difference is smaller than the so called “lock criterion” for more than eight consecutive input clock periods, the lock output switches

from low to high. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was high). Requiring eight phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

#### 4.5.4.2 Power-down control

To reduce the power consumption when the PLL clock is not needed, a Power-down mode has been incorporated. This mode is enabled by setting the SYSPLL\_PD bits to one in the Power-down configuration register ([Table 44](#)). In this mode, the internal current reference will be turned off, the oscillator and the phase-frequency detector will be stopped and the dividers will enter a reset state. While in Power-down mode, the lock output will be low to indicate that the PLL is not in lock. When the Power-down mode is terminated by setting the SYSPLL\_PD bits to zero, the PLL will resume its normal operation and will make the lock signal high once it has regained lock on the input clock.

#### 4.5.4.3 Divider ratio programming

##### Post divider

The division ratio of the post divider is controlled by the PSEL bits. The division ratio is two times the value of P selected by PSEL bits as shown in [Table 8](#). This guarantees an output clock with a 50% duty cycle.

##### Feedback divider

The feedback divider's division ratio is controlled by the MSEL bits. The division ratio between the PLL's output clock and the input clock is the decimal value on MSEL bits plus one, as specified in [Table 8](#).

##### Changing the divider values

Changing the divider ratio while the PLL is running is not recommended. As there is no way to synchronize the change of the MSEL and PSEL values with the dividers, the risk exists that the counter will read in an undefined value, which could lead to unwanted spikes or drops in the frequency of the output clock. The recommended way of changing between divider settings is to power down the PLL, adjust the divider settings and then let the PLL start up again.

#### 4.5.4.4 Frequency selection

The PLL frequency equations use the following parameters (also see [Figure 3](#)):

**Table 45. PLL frequency parameters**

Parameter	System PLL
FCLKIN	Frequency of sys_pllclk (input clock to the system PLL) from the SYSPLLCLKSEL multiplexer (see <a href="#">Section 4.4.9</a> ).
FCCO	Frequency of the Current Controlled Oscillator (CCO); 156 to 320 MHz.
FCLKOUT	Frequency of sys_pllclkout. FCLKOUT must be < 100 MHz.
P	System PLL post divider ratio; PSEL bits in SYSPLLCTRL (see <a href="#">Section 4.4.3</a> ).
M	System PLL feedback divider register; MSEL bits in SYSPLLCTRL (see <a href="#">Section 4.4.3</a> ).

#### 4.5.4.4.1 Normal mode

In normal mode the post divider is enabled, giving a 50% duty cycle clock with the following frequency relations:

(1)

$$FCLKOUT = M \times FCLKIN = (FCCO)/(2 \times P)$$

To select the appropriate values for M and P, it is recommended to follow these steps:

1. Specify the input clock frequency FCLKIN.
2. Calculate M to obtain the desired output frequency FCLKOUT with  
 $M = FCLKOUT / FCLKIN$ .
3. Find a value so that  $FCCO = 2 \times P \times FCLKOUT$ .
4. Verify that all frequencies and divider values conform to the limits specified in [Table 8](#).
5. Ensure that  $FCLKOUT < 100$  MHz.

[Table 46](#) shows how to configure the PLL for a 12 MHz crystal oscillator using the SYSPLLCTRL register ([Table 8](#)). The main clock is equivalent to the system clock if the system clock divider SYSAHBCLKDIV is set to one (see [Table 18](#)).

**Table 46. PLL configuration examples**

PLL input clock sys_pllclk (FCLKIN)	Main clock (FCLKOUT)	MSEL bits <a href="#">Table 8</a>	M divider value	PSEL bits <a href="#">Table 8</a>	P divider value	FCCO frequency
12 MHz	48 MHz	00011	4	01	2	192 MHz
12 MHz	36 MHz	00010	3	10	4	288 MHz
12 MHz	24 MHz	00001	2	10	4	192 MHz

#### 4.5.4.4.2 Power-down mode

In this mode, the internal current reference is turned off, the oscillator and the phase-frequency detector are stopped, and the dividers enter a reset state. While in Power-down mode, the lock output is be LOW to indicate that the PLL is not in lock. When the Power-down mode is terminated by setting the SYSPLL\_PD bit to zero in the Power-down configuration register ([Table 44](#)), the PLL resumes its normal operation and asserts the lock signal HIGH once it has regained lock on the input clock.

### 4.5.5 Flash memory access

Depending on the system clock frequency, access to the flash memory can be configured with various access times by writing to the FLASHCFG register at address 0x4003 C010. This register is part of the flash configuration block.

**Remark:** Improper setting of this register may result in incorrect operation of the flash memory.

Table 47. Flash configuration register (FLASHCFG, address 0x4003 C010) bit description

Bit	Symbol	Value	Description	Reset value
1:0	FLASHTIM		Flash memory access time. FLASHTIM +1 is equal to the number of system clocks used for flash access.	10
		00	1 system clock flash access time (for system clock frequencies of up to 20 MHz).	
		01	2 system clocks flash access time (for system clock frequencies of up to 40 MHz).	
		10	3 system clocks flash access time (for system clock frequencies of up to 50 MHz).	
		11	Reserved.	
31:2	-	-	Reserved. <b>User software must not change the value of these bits. Bits 31:2 must be written back exactly as read.</b>	-

### 5.1 Features

- Control of active and power-down modes.
- General Purpose back-up registers in Deep power-down mode.

### 5.2 General description

The PMU controls the Deep power-down mode. Four general purpose register in the PMU can be used to retain data during Deep power-down mode.

### 5.3 Register description

**Table 48. Register overview: PMU (base address 0x4003 8000)**

Name	Access	Address offset	Description	Reset value
PCON	R/W	0x000	Power control register	0x0
GPREG0	R/W	0x004	General purpose register 0	0x0
GPREG1	R/W	0x008	General purpose register 1	0x0
GPREG2	R/W	0x00C	General purpose register 2	0x0
GPREG3	R/W	0x010	General purpose register 3	0x0
GPREG4	R/W	0x014	General purpose register 4	0x0

#### 5.3.1 Power control register

The power control register selects whether one of the ARM Cortex-M0 controlled power-down modes (Sleep mode or Deep-sleep mode) or the Deep power-down mode is entered and provides the flags for Sleep or Deep-sleep modes and Deep power-down modes respectively. See [Section 5.4.1](#) for details on how to enter the power-down modes.

**Table 49. Power control register (PCON, address 0x4003 8000) bit description**

Bit	Symbol	Value	Description	Reset value
0	-	-	Reserved. Do not write 1 to this bit.	0x0
1	DPDEN		Deep power-down mode enable	0
		0	Sleep Deep-sleep mode. ARM WFI will enter Sleep or Deep-sleep mode (clock to ARM Cortex-M0 core turned off).	
		1	Deep-power down mode. ARM WFI will enter Deep-power down mode (ARM Cortex-M0 core powered-down).	
7:2	-	-	Reserved. Do not write ones to this bit.	0x0

Table 49. Power control register (PCON, address 0x4003 8000) bit description ...continued

Bit	Symbol	Value	Description	Reset value
8	SLEEPFLAG		Sleep mode flag	0
		0	Active mode. Read: No power-down mode entered. The part is in Active mode. Write: No effect.	
		1	Sleep Deep-sleep mode. Read: Sleep/Deep-sleep or Deep power-down mode entered. Write: Writing a 1 clears the SLEEPFLAG bit to 0.	
10:9	-	-	Reserved. Do not write ones to this bit.	0x0
11	DPDFLAG		Deep power-down flag	0x0
		0	No Deep power-down mode. Read: Deep power-down mode <b>not</b> entered. Write: No effect.	0x0
		1	Deep power-down mode. Read: Deep power-down mode entered. Write: Clear the Deep power-down flag.	0x0
31:12	-	-	Reserved. Do not write ones to this bit.	0x0

### 5.3.2 General purpose registers 0 to 3

The general purpose registers retain data through the Deep power-down mode when power is still applied to the  $V_{DD}$  pin but the chip has entered Deep power-down mode. Only a “cold” boot when all power has been completely removed from the chip will reset the general purpose registers.

Table 50. General purpose registers 0 to 3 (GPREG[0:3], address 0x4003 8004 (GPREG0) to 0x4003 8010 (GPREG3)) bit description

Bit	Symbol	Description	Reset value
31:0	GPDATA	Data retained during Deep power-down mode.	0x0

### 5.3.3 General purpose register 4

The general purpose register 4 retains data through the Deep power-down mode when power is still applied to the  $V_{DD}$  pin but the chip has entered Deep power-down mode. Only a “cold” boot, when all power has been completely removed from the chip, will reset the general purpose registers.

**Remark:** If there is a possibility that the external voltage applied on pin  $V_{DD}$  drops below 2.2 V during Deep power-down, the hysteresis of the WAKEUP input pin has to be disabled in this register before entering Deep power-down mode in order for the chip to wake up.

Table 51. General purpose register 4 (GPREG4, address 0x4003 8014) bit description

Bit	Symbol	Value	Description	Reset value
9:0	-	-	Reserved. Do not write ones to this bit.	0x0

Table 51. General purpose register 4 (GPREG4, address 0x4003 8014) bit description

Bit	Symbol	Value	Description	Reset value
10	WAKEUPHYS		WAKEUP pin hysteresis enable	0x0
		0	Disabled. Hysteresis for WAKEUP pin disabled.	
		1	Enabled. Hysteresis for WAKEUP pin enabled.	
31:11	GPDATA		Data retained during Deep power-down mode.	0x0

## 5.4 Functional description

### 5.4.1 Power management

This part supports a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be optimized for power consumption. In addition, there are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode.

**Remark:** The Debug mode is not supported in Sleep, Deep-sleep, or Deep power-down modes.

#### 5.4.1.1 Active mode

In Active mode, the ARM Cortex-M0 core and memories are clocked by the system clock, and peripherals are clocked by the system clock or a dedicated peripheral clock.

The chip is in Active mode after reset and the default power configuration is determined by the reset values of the PDRUNCFG and SYSAHBCLKCTRL registers. The power configuration can be changed during run time.

##### 5.4.1.1.1 Power configuration in Active mode

Power consumption in Active mode is determined by the following configuration choices:

- The SYSAHBCLKCTRL register controls which memories and peripherals are running ([Table 19](#)).
- The power to various analog blocks (PLL, oscillators, the ADC, the BOD circuit, and the flash block) can be controlled at any time individually through the PDRUNCFG register ([Table 44](#)).
- The clock source for the system clock can be selected from the IRC (default), the system oscillator, or the watchdog oscillator (see [Figure 3](#) and related registers).
- The system clock frequency can be selected by the SYSPLLCTRL ([Table 8](#)) and the SYSAHBCLKDIV register ([Table 18](#)).
- Selected peripherals (UART, SSP0/1, WDT) use individual peripheral clocks with their own clock dividers. The peripheral clocks can be shut down through the corresponding clock divider registers ([Table 20](#) to [Table 22](#)).

#### 5.4.1.2 Sleep mode

In Sleep mode, the system clock to the ARM Cortex-M0 core is stopped, and execution of instructions is suspended until either a reset or an enabled interrupt occurs.



Peripheral functions, if selected to be clocked in the SYSAHBCLKCTRL register, continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and their related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

#### 5.4.1.2.1 Power configuration in Sleep mode

Power consumption in Sleep mode is configured by the same settings as in Active mode:

- The clock remains running.
- The system clock frequency remains the same as in Active mode, but the processor is not clocked.
- Analog and digital peripherals are selected as in Active mode.

#### 5.4.1.2.2 Programming Sleep mode

The following steps must be performed to enter Sleep mode:

1. The DPDEN bit in the PCON register must be set to zero ([Table 49](#)).
2. The SLEEPDEEP bit in the ARM Cortex-M0 SCR register must be set to zero, see ([Table 331](#)).
3. Use the ARM Cortex-M0 Wait-For-Interrupt (WFI) instruction.

#### 5.4.1.2.3 Wake-up from Sleep mode

Sleep mode is exited automatically when an interrupt enabled by the NVIC arrives at the processor or a reset occurs. After wake-up due to an interrupt, the microcontroller returns to its original power configuration defined by the contents of the PDRUNCFG and the SYSAHBCLKDIV registers. If a reset occurs, the microcontroller enters the default configuration in Active mode.

#### 5.4.1.3 Deep-sleep mode

In Deep-sleep mode, the system clock to the processor is disabled as in Sleep mode. All analog blocks are powered down, except for the BOD circuit and the watchdog oscillator, which must be selected or deselected during Deep-sleep mode in the PDSLEEPCFG register.

Deep-sleep mode eliminates all power used by the flash and analog peripherals and all dynamic power used by the processor itself, memory systems and their related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

#### 5.4.1.3.1 Power configuration in Deep-sleep mode

Power consumption in Deep-sleep mode is determined by the Deep-sleep power configuration setting in the PDSLEEPCFG ([Table 42](#)) register:

- The only clock source available in Deep-sleep mode is the watchdog oscillator. The watchdog oscillator can be left running in Deep-sleep mode if required for timer-controlled wake-up (see [Section 5.4.2.3](#)). All other clock sources (the IRC and

system oscillator) and the system PLL are shut down. The watchdog oscillator analog output frequency must be set to the lowest value of its analog clock output (bits FREQSEL in the WDTOSCCTRL = 0001, see [Table 11](#)).

- The BOD circuit can be left running in Deep-sleep mode if required by the application.
- If the watchdog oscillator is running in Deep-sleep mode, only the watchdog timer or one of the general-purpose timers should be enabled in SYSAHBCLKCTRL register to minimize power consumption.

#### 5.4.1.3.2 Programming Deep-sleep mode

The following steps must be performed to enter Deep-sleep mode:

1. The DPDEN bit in the PCON register must be set to zero ([Table 49](#)).
2. Select the power configuration in Deep-sleep mode in the PDSLEEPCFG ([Table 42](#)) register.
  - a. If a timer-controlled wake-up is needed, ensure that the watchdog oscillator is powered in the PDRUNCFG register and switch the clock source to WD oscillator in the MAINCLKSEL register ([Table 16](#)).
  - b. If no timer-controlled wake-up is needed and the watchdog oscillator is shut down, ensure that the IRC is powered in the PDRUNCFG register and switch the clock source to IRC in the MAINCLKSEL register ([Table 16](#)). This ensures that the system clock is shut down glitch-free.
3. Select the power configuration after wake-up in the PDAWAKECFG ([Table 43](#)) register.
4. If an external pin is used for wake-up, enable and clear the wake-up pin in the start logic registers ([Table 37](#) to [Table 40](#)), and enable the start logic interrupt in the NVIC.
5. In the SYSAHBCLKCTRL register ([Table 19](#)), disable all peripherals except counter/timer or WDT if needed.
6. Write one to the SLEEPDEEP bit in the ARM Cortex-M0 SCR register ([Table 331](#)).
7. Use the ARM WFI instruction.

#### 5.4.1.3.3 Wake-up from Deep-sleep mode

The microcontroller can wake up from Deep-sleep mode in the following ways:

- Signal on an external pin. For this purpose, pins PIO0\_0 to PIO0\_11 and PIO1\_0 can be enabled as inputs to the start logic. The start logic does not require any clocks and generates the interrupt if enabled in the NVIC to wake up from Deep-sleep mode.
- Input signal to the start logic created by a match event on one of the general purpose timer external match outputs. The pin holding the timer match function must be enabled as start logic input in the NVIC, the corresponding timer must be enabled in the SYSAHBCLKCTRL register, and the watchdog oscillator must be running in Deep-sleep mode (for details see [Section 5.4.2.3](#)).
- Reset from the BOD circuit. In this case, the BOD circuit must be enabled in the PDSLEEPCFG register, and the BOD reset must be enabled in the BODCTRL register ([Table 33](#)).
- Reset from the watchdog timer. In this case, the watchdog oscillator must be running in Deep-sleep mode (see PDSLEEPCFG register), and the WDT must be enabled in the SYSAHBCLKCTRL register.

- A reset signal from the external  $\overline{\text{RESET}}$  pin.

**Remark:** If the watchdog oscillator is running in Deep-sleep mode, its frequency determines the wake-up time causing the wake-up time to be longer than waking up with the IRC.

#### 5.4.1.4 Deep power-down mode

In Deep power-down mode, power and clocks are shut off to the entire chip with the exception of the WAKEUP pin.

During Deep power-down mode, the contents of the SRAM and registers are not retained except for a small amount of data which can be stored in the five 32-bit general purpose registers of the PMU block.

All functional pins are tri-stated in Deep power-down mode except for the WAKEUP pin.

##### 5.4.1.4.1 Power configuration in Deep power-down mode

Deep power-down mode has no configuration options. All clocks, the core, and all peripherals are powered down. Only the WAKEUP pin is powered.

##### 5.4.1.4.2 Programming Deep power-down mode

The following steps must be performed to enter Deep power-down mode:

1. Write one to the DPDEN bit in the PCON register (see [Table 49](#)).
2. Store data to be retained in the general purpose registers ([Table 50](#)).
3. Write one to the SLEEPDEEP bit in the ARM Cortex-M0 SCR register ([Table 331](#)).
4. Use the ARM WFI instruction.

**Remark:** The WAKEUP pin must be pulled HIGH externally before entering Deep power-down mode.

##### 5.4.1.4.3 Wake-up from Deep power-down mode

Pulling the WAKEUP pin LOW wakes up the part from Deep power-down, and the chip goes through the entire reset process ([Section 4.5.1](#)). The minimum pulse width for the HIGH-to-LOW transition on the WAKEUP pin is 50 ns.

Follow these steps to wake up the chip from Deep power-down mode:

1. A wake-up signal is generated when a HIGH-to-LOW transition occurs externally on the WAKEUP pin with a pulse length of at least 50 ns while the part is in Deep power-down mode.
  - The PMU will turn on the on-chip voltage regulator. When the core voltage reaches the power-on-reset (POR) trip point, a system reset will be triggered and the chip re-boots.
  - All registers except the GPREG0 to GPREG4 and PCON will be in their reset state.
2. Once the chip has booted, read the deep power-down flag in the PCON register ([Table 49](#)) to verify that the reset was caused by a wake-up event from Deep power-down.
3. Clear the deep power-down flag in the PCON register ([Table 49](#)).

4. (Optional) Read the stored data in the general purpose registers ([Table 50](#) and [Table 51](#)).
5. Set up the PMU for the next Deep power-down cycle.

**Remark:** The  $\overline{\text{RESET}}$  pin has no functionality in Deep power-down mode.

## 5.4.2 Deep-sleep mode details

### 5.4.2.1 IRC oscillator

The IRC is the only oscillator that can always shut down glitch-free. Therefore it is recommended that the user switches the clock source to IRC before the chip enters Deep-sleep mode.

### 5.4.2.2 Start logic

The Deep-sleep mode is exited when the start logic indicates an interrupt to the ARM core. The port pins PIO0\_0 to PIO0\_11 and PIO1\_0 are connected to the start logic and serve as wake-up pins. The user must program the start logic registers for each input to set the appropriate edge polarity for the corresponding wake-up event. Furthermore, the interrupts corresponding to each input must be enabled in the NVIC. Interrupts 0 to 12 in the NVIC correspond to 13 PIO pins (see [Section 4.4.32](#)).

The start logic does not require a clock to run because it uses the input signals on the enabled pins to generate a clock edge when enabled. Therefore, the start logic signals should be cleared (see [Table 39](#)) before use.

The start logic can also be used in Active mode to provide a vectored interrupt using the LPC111x/LPC11Cxx's input pins.

### 5.4.2.3 Using the general purpose counter/timers to create a self-wake-up event

If enabled in Deep-sleep mode through the SYSAHBCLKCFG register, the counter/timers can count clock cycles of the watchdog oscillator and create a match event when the number of cycles equals a preset match value. The match event causes the corresponding match output pin to go HIGH, LOW, or toggle. The state of the match output pin is also monitored by the start logic and can trigger a wake-up interrupt if that pin is enabled in the NVIC and the start logic trigger is configured accordingly in the start logic edge control register (see [Table 37](#)).

The following steps must be performed to configure the counter/timer and create a timed Deep-sleep self-wake-up event:

1. Configure the port pin as match output in the IOCON block. Select from pins PIO0\_1 or PIO0\_8 to PIO0\_11, which are inputs to the start logic and also hold a match output function.
2. In the corresponding counter/timer, set the match value, and configure the match output for the selected pin.
3. Select the watchdog oscillator to run in Deep-sleep mode in the PDSLEEPCFG register.
4. Switch the clock source to the watchdog oscillator in the MAINCLKSEL register ([Table 16](#)) and ensure the watchdog oscillator is powered in the PDRUNCFG register.

5. Enable the pin, configure its edge detect function, and reset the start logic in the start logic registers ([Table 37](#) to [Table 40](#)), and enable the interrupt in the NVIC.
6. Disable all other peripherals in the SYSAHBCLKCTRL register.
7. Ensure that the DPDEN bit in the PCON register is set to zero ([Table 49](#)).
8. Write one to the SLEEPDEEP bit in the ARM Cortex-M0 SCR register ([Table 331](#)).
9. Start the counter/timer.
10. Use the ARM WFI instruction to enter Deep-sleep mode.

### 6.1 How to read this chapter

See [Table 52](#) for available pin registers:

Table 52. GPIO configuration

Package	GPIO port 0	GPIO port 1	GPIO port 2	GPIO port 3	Total GPIO pins
LQFP48JFBD48	PIO0_0 to PIO0_11	PIO1_0 to PIO1_11	PIO2_0 to PIO2_9	PIO3_0; PIO3_3 to PIO3_5	38

### 6.2 Features

The I/O configuration registers control the electrical characteristics of the pads. The following features are programmable:

- Pin function.
- Internal pull-up/pull-down resistor or bus keeper function.
- Hysteresis.
- Analog input or digital mode for pads hosting the ADC inputs.
- I<sup>2</sup>C mode for pads hosting the I<sup>2</sup>C-bus function.
- Pseudo open-drain mode for non-I<sup>2</sup>C pins.

### 6.3 General description

The IOCON registers control the function (GPIO or peripheral function), the input mode, and the hysteresis of all PION<sub>m</sub> pins. In addition, the I<sup>2</sup>C-bus pins can be configured for different I<sup>2</sup>C-bus modes. An analog input mode can be selected for the ADC inputs.

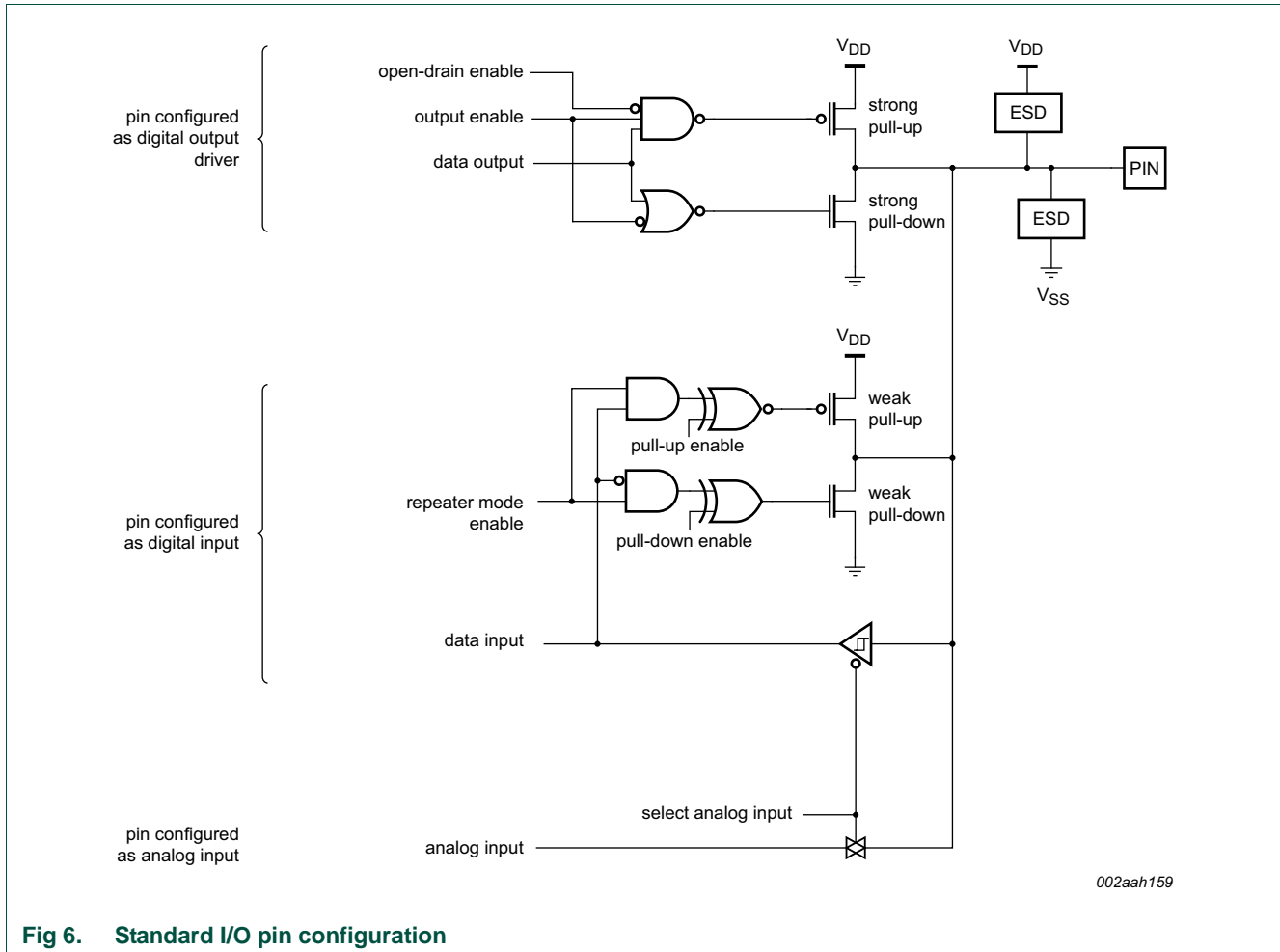


Fig 6. Standard I/O pin configuration

### 6.3.1 Pin function

The FUNC bits in the IOCON registers can be set to GPIO (FUNC = 000) or to a peripheral function. If the pins are GPIO pins, the GPIO DIR registers determine whether the pin is configured as an input or output. For any peripheral function, the pin direction is controlled automatically depending on the pin's functionality. The GPIO DIR registers have no effect for peripheral functions.

### 6.3.2 Pin mode

The MODE bits in the IOCON register allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is pull-up enabled. If the pull-up resistor is enabled (default), all non-I2C pins are pulled up to 3.3 V ( $V_{DD} = 3.3$  V).

The repeater mode enables the pull-up resistor if the pin is at a logic HIGH and enables the pull-down resistor if the pin is at a logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is

not applicable to the Deep power-down mode. Repeater mode may typically be used to prevent a pin from floating (and potentially using significant power if it floats to an indeterminate state) if it is temporarily not driven.

### 6.3.3 Hysteresis

The input buffer for digital functions can be configured with hysteresis or as plain buffer through the IOCON registers.

If the external pad supply voltage  $V_{DD}$  is between 2.5 V and 3.6 V, the hysteresis buffer can be enabled or disabled. If  $V_{DD}$  is below 2.5 V, the hysteresis buffer must be **disabled** to use the pin in input mode.

### 6.3.4 A/D-mode

In A/D-mode, the digital receiver is disconnected to obtain an accurate input voltage for analog-to-digital conversions. This mode can be selected in those IOCON registers that control pins with an analog function. If A/D mode is selected, Hysteresis and Pin mode settings have no effect.

For pins without analog functions, the A/D-mode setting has no effect.

### 6.3.5 I<sup>2</sup>C mode

If the I<sup>2</sup>C function is selected by the FUNC bits of registers PIO0\_4 ([Table 64](#)) and PIO0\_5 ([Table 65](#)), then the I<sup>2</sup>C-bus pins can be configured for different I<sup>2</sup>C-modes:

- Standard mode/Fast-mode I<sup>2</sup>C with input glitch filter (this includes an open-drain output according to the I<sup>2</sup>C-bus specification).
- Fast-mode Plus with input glitch filter (this includes an open-drain output according to the I<sup>2</sup>C-bus specification). In this mode, the pins function as high-current sinks.
- Standard open-drain I/O functionality without input filter.

**Remark:** Either Standard mode/Fast-mode I<sup>2</sup>C or Standard I/O functionality should be selected if the pin is used as GPIO pin.

### 6.3.6 Open-drain Mode

When output is selected, either by selecting a special function in the FUNC field, or by selecting GPIO function for a pin having a 1 in its GPIODIR register, a 1 in the OD bit selects open-drain operation, that is, a 1 disables the high-drive transistor. This option has no effect on the primary I<sup>2</sup>C pins.

## 6.4 Register description

The I/O configuration registers control the PIO port pins, the inputs and outputs of all peripherals and functional blocks, the I<sup>2</sup>C-bus pins, and the ADC input pins.

Each port pin PION\_m has one IOCON register assigned to control the pin's function and electrical characteristics.



Some input functions (SSP0\_SCK,  $\overline{U0\_DSR}$ ,  $\overline{U0\_DCD}$ ,  $\overline{U0\_RI}$ , SSP1\_SSEL, CT16B0\_CAP0, SSP1\_SCK, SSP1\_MISO, SSP1\_MOSI, CT32B0\_CAP0, and U0\_RXD) are multiplexed to several physical pins. The LOC registers select the pin location for each of these functions.

**Remark:** The IOCON registers are listed in order of their memory locations in [Table 53](#), which correspond to the order of their physical pin numbers in the LQFP48 package starting at the upper left corner with pin 1 (PIO2\_6). See [Table 54](#) for a listing of IOCON registers ordered by port number.

The IOCON location registers are used to select a physical pin for multiplexed functions.

**Remark:** Note that once the pin location has been selected, the function still must be configured in the corresponding IOCON registers for the function to be usable on that pin.

**Table 53. Register overview: I/O configuration (base address 0x4004 4000)**

Name	Access	Address offset	Description	Reset value	Reference
PIO2_6	R/W	0x000	I/O configuration for pin PIO2_6/ CT32B0_MAT1	0xD0	<a href="#">Table 55</a>
-	R/W	0x004	Reserved	-	-
PIO2_0	R/W	0x008	I/O configuration for pin PIO2_0/U0_DTR/SSP1_SSEL/ ADC_PIN_TRIG4	0xD0	<a href="#">Table 56</a>
RESET_PIO0_0	R/W	0x00C	I/O configuration for pin $\overline{RESET}$ /PIO0_0	0xD0	<a href="#">Table 57</a>
PIO0_1	R/W	0x010	I/O configuration for pin PIO0_1/CLKOUT/CT32B0_MAT2	0xD0	<a href="#">Table 58</a>
PIO1_8	R/W	0x018	I/O configuration for pin PIO1_8/CT16B1_CAP0/R/U2_TXD	0xD0	<a href="#">Table 59</a>
PIO0_2	R/W	0x01C	I/O configuration for pin PIO0_2/SSP0_SSEL/CT16B0_CAP0/ ADC_PIN_TRIG0	0xD0	<a href="#">Table 60</a>
PIO2_7	R/W	0x020	I/O configuration for pin PIO2_7/ CT32B0_MAT2/U0_RXD	0xD0	<a href="#">Table 61</a>
PIO2_8	R/W	0x024	I/O configuration for pin PIO2_8/ CT32B0_MAT3/U0_TXD	0xD0	<a href="#">Table 62</a>
PIO2_1	R/W	0x028	I/O configuration for pin PIO2_1/U0_DSR/SSP1_SCK	0xD0	<a href="#">Table 63</a>
PIO0_4	R/W	0x030	I/O configuration for pin PIO0_4/I2C0_SCL	0x00	<a href="#">Table 64</a>
PIO0_5	R/W	0x034	I/O configuration for pin PIO0_5/I2C0_SDA	0x00	<a href="#">Table 65</a>
PIO1_9	R/W	0x038	I/O configuration for pin PIO1_9/CT16B1_MAT0/SSP1_MOSI	0xD0	<a href="#">Table 66</a>
PIO3_4	R/W	0x03C	I/O configuration for pin PIO3_4/ CT16B0_CAP1/U0_RXD	0xD0	<a href="#">Table 67</a>
PIO2_4	R/W	0x040	I/O configuration for pin PIO2_4/ CT16B1_MAT1/ SSP1_SSEL	0xD0	<a href="#">Table 68</a>
PIO2_5	R/W	0x044	I/O configuration for pin PIO2_5/ CT32B0_MAT0	0xD0	<a href="#">Table 69</a>

Table 53. Register overview: I/O configuration (base address 0x4004 4000)

Name	Access	Address offset	Description	Reset value	Reference
PIO3_5	R/W	0x048	I/O configuration for pin PIO3_5/ CT16B1_CAP1/U0_TXD	0xD0	<a href="#">Table 70</a>
PIO2_9	R/W	0x054	I/O configuration for pin PIO2_9/ CT32B0_CAP0	0xD0	<a href="#">Table 71</a>
PIO2_10	R/W	0x058	I/O configuration for pin PIO2_10	0xD0	<a href="#">Table 72</a>
PIO2_2	R/W	0x05C	I/O configuration for pin PIO2_2/U0_DCD/SSP1_MISO	0xD0	<a href="#">Table 73</a>
PIO0_8	R/W	0x060	I/O configuration for pin PIO0_8/SSP0_MISO/CT16B0_MAT0/R/ ADC_PIN_TRIG2	0xD0	<a href="#">Table 74</a>
PIO0_9	R/W	0x064	I/O configuration for pin PIO0_9SSP0_MOSI/CT16B0_MAT1/R/ ADC_PIN_TRIG3	0xD0	<a href="#">Table 75</a>
SWCLK_PIO0_10	R/W	0x068	I/O configuration for pin SWCLK/PIO0_10/ SSP0_SCK/CT16B0_MAT2	0xD0	<a href="#">Table 76</a>
PIO1_10	R/W	0x06C	I/O configuration for pin PIO1_10/ADC_8/CT16B1_MAT1/ SSP1_MISO	0xD0	<a href="#">Table 77</a>
R_PIO0_11	R/W	0x074	I/O configuration for pin R/PIO0_11/ADC_7/CT32B0_MAT3	0xD0	<a href="#">Table 78</a>
R_PIO1_0	R/W	0x078	I/O configuration for pin R/PIO1_0/ADC_6/CT32B1_CAP0	0xD0	<a href="#">Table 79</a>
R_PIO1_1	R/W	0x07C	I/O configuration for pin R/PIO1_1/ADC_5/CT32B1_MAT0	0xD0	<a href="#">Table 80</a>
R_PIO1_2	R/W	0x080	I/O configuration for pin R/PIO1_2/ADC_4/CT32B1_MAT1	0xD0	<a href="#">Table 81</a>
PIO3_0	R/W	0x084	I/O configuration for pin PIO3_0/U0_DTR/CT16B0_MAT0/ U0_TXD	0xD0	<a href="#">Table 82</a>
PIO2_3	R/W	0x08C	I/O configuration for pin PIO2_3/U0_RI/SSP1_MOSI	0xD0	<a href="#">Table 83</a>
SWDIO_PIO1_3	R/W	0x090	I/O configuration for pin SWDIO/PIO1_3/ADC_3/CT32B1_MAT2	0xD0	<a href="#">Table 84</a>
PIO1_4	R/W	0x094	I/O configuration for pin PIO1_4/ADC_2/CT32B1_MAT3	0xD0	<a href="#">Table 85</a>
PIO1_11	R/W	0x098	I/O configuration for pin PIO1_11/ADC_1/CT32B1_CAP1	0xD0	<a href="#">Table 86</a>
PIO3_2	R/W	0x09C	I/O configuration for pin PIO3_2/U0_DCD/ CT16B0_MAT2/SSP1_SCK	0xD0	<a href="#">Table 87</a>
PIO1_5	R/W	0x0A0	I/O configuration for pin PIO1_5/U0_RTS/CT32B0_CAP0	0xD0	<a href="#">Table 88</a>
PIO1_6	R/W	0x0A4	I/O configuration for pin PIO1_6/U0_RXD/CT32B0_MAT0	0xD0	<a href="#">Table 89</a>
PIO1_7	R/W	0x0A8	I/O configuration for pin PIO1_7/U0_TXD/CT32B0_MAT1	0xD0	<a href="#">Table 90</a>

Table 53. Register overview: I/O configuration (base address 0x4004 4000)

Name	Access	Address offset	Description	Reset value	Reference
PIO3_3	R/W	0x0AC	I/O configuration for pin PIO3_3/ $\overline{U0\_RI}$ / $\overline{CT16B0\_CAP0}$	0xD0	<a href="#">Table 91</a>
SCK0_LOC	R/W	0x0B0	SCK0 pin location select register	0x00	<a href="#">Table 92</a>
DSR_LOC	R/W	0x0B4	$\overline{DSR}$ pin location select register	0x00	<a href="#">Table 93</a>
DCD_LOC	R/W	0x0B8	$\overline{DCD}$ pin location select register	0x00	<a href="#">Table 94</a>
RI_LOC	R/W	0x0BC	$\overline{RI}$ pin location select register	0x00	<a href="#">Table 95</a>
PIO0_3	R/W	0x0C0	I/O configuration for pin PIO0_3/R/R/U2_RXD	0xD0	<a href="#">Table 96</a>
PIO0_6	R/W	0x0C4	I/O configuration for pin PIO0_6/SSP0_SCK/U1_TXD	0xD0	<a href="#">Table 97</a>
PIO0_7	R/W	0x0C8	I/O configuration for pin PIO0_7/U0_CTS/ADC_PIN_TRIG1/U1_RXD	0xD0	<a href="#">Table 98</a>
SSEL1_LOC	R/W	0x0CC	SSEL1 pin location select register	0x0	<a href="#">Table 99</a>
CT16B0_CAP0_LOC	R/W	0x0D0	CT16B0_CAP0 pin location select register	0x00	<a href="#">Table 100</a>
SCK1_LOC	R/W	0x0D4	SCK1 pin location select register	0x00	<a href="#">Table 101</a>
MISO1_LOC	R/W	0x0D8	MISO1 pin location select register	0x00	<a href="#">Table 102</a>
MOSI1_LOC	R/W	0x0DC	MOSI1 pin location select register	0x00	<a href="#">Table 103</a>
CT32B0_CAP0_LOC	R/W	0x0E0	CT32B0_CAP0 pin location select register	0x00	<a href="#">Table 104</a>
RXD_LOC	R/W	0x0E4	RXD pin location select register	0x00	<a href="#">Table 105</a>

Table 54. I/O configuration registers ordered by port number

Port pin	Register name	LQFP48	Reference
PIO0_0	RESET_PIO0_0	yes	<a href="#">Table 57</a>
PIO0_1	PIO0_1	yes	<a href="#">Table 55</a>
PIO0_2	PIO0_2	yes	<a href="#">Table 60</a>
PIO0_3	PIO0_3	yes	<a href="#">Table 96</a>
PIO0_4	PIO0_4	yes	<a href="#">Table 64</a>
PIO0_5	PIO0_5	yes	<a href="#">Table 65</a>
PIO0_6	PIO0_6	yes	<a href="#">Table 97</a>
PIO0_7	PIO0_7	yes	<a href="#">Table 98</a>
PIO0_8	PIO0_8	yes	<a href="#">Table 74</a>
PIO0_9	PIO0_9	yes	<a href="#">Table 75</a>
PIO0_10	SWCLK_PIO0_10	yes	<a href="#">Table 76</a>
PIO0_11	R_PIO0_11	yes	<a href="#">Table 78</a>
PIO1_0	R_PIO1_0	yes	<a href="#">Table 79</a>
PIO1_1	R_PIO1_1	yes	<a href="#">Table 80</a>
PIO1_2	R_PIO1_2	yes	<a href="#">Table 81</a>
PIO1_3	SWDIO_PIO1_3	yes	<a href="#">Table 84</a>
PIO1_4	PIO1_4	yes	<a href="#">Table 85</a>

Table 54. I/O configuration registers ordered by port number

Port pin	Register name	LQFP48	Reference
PIO1_5	PIO1_5	yes	<a href="#">Table 88</a>
PIO1_6	PIO1_6	yes	<a href="#">Table 89</a>
PIO1_7	PIO1_7	yes	<a href="#">Table 90</a>
PIO1_8	PIO1_8	yes	<a href="#">Table 59</a>
PIO1_9	PIO1_9	yes	<a href="#">Table 66</a>
PIO1_10	PIO1_10	yes	<a href="#">Table 77</a>
PIO1_11	PIO1_11	yes	<a href="#">Table 86</a>
PIO2_0	PIO2_0	yes	<a href="#">Table 56</a>
PIO2_1	PIO2_1	yes	<a href="#">Table 63</a>
PIO2_2	PIO2_2	yes	<a href="#">Table 73</a>
PIO2_3	PIO2_3	yes	<a href="#">Table 83</a>
PIO2_4	PIO2_4	yes	<a href="#">Table 68</a>
PIO2_5	PIO2_5	yes	<a href="#">Table 69</a>
PIO2_6	PIO2_6	yes	<a href="#">Table 55</a>
PIO2_7	PIO2_7	yes	<a href="#">Table 61</a>
PIO2_8	PIO2_8	yes	<a href="#">Table 62</a>
PIO2_9	PIO2_9	yes	<a href="#">Table 71</a>
PIO2_10	PIO2_10	no	<a href="#">Table 72</a>
PIO3_0	PIO3_0	yes	<a href="#">Table 82</a>
PIO3_2	PIO3_2	no	<a href="#">Table 87</a>
PIO3_3	PIO3_3	yes	<a href="#">Table 91</a>
PIO3_4	PIO3_4	yes	<a href="#">Table 67</a>
PIO3_5	PIO3_5	yes	<a href="#">Table 70</a>

### 6.4.1 PIO2\_6 register

Table 55. PIO2\_6 register (PIO2\_6, address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_6.	
		0x1	CT32B0_MAT1.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011

Table 55. PIO2\_6 register (PIO2\_6, address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.2 PIO2\_0 register

Table 56. PIO2\_0 register (PIO2\_0, address 0x4004 4008) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_0.	
		0x1	U0_DTR.	
		0x2	SSP1_SSEL.	
		0x3	ADC_PIN_TRIG4	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.3 PIO\_RESET\_PIO0\_0 register

Table 57. RESET\_PIO0\_0 register (RESET\_PIO0\_0, address 0x4004 400C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	RESET.	
		0x1	PIO0_0.	

Table 57. RESET\_PIO0\_0 register (RESET\_PIO0\_0, address 0x4004 400C) bit description

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

#### 6.4.4 PIO0\_1 register

Table 58. PIO0\_1 register (PIO0\_1, address 0x4004 4010) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_1.	
		0x1	CLKOUT.	
		0x2	CT32B0_MAT2.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.5 PIO1\_8 register

Table 59. PIO1\_8 register (PIO1\_8, address 0x4004 4018) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_8.	
		0x1	CT16B1_CAP0.	
		0x3	U2_TXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.6 PIO0\_2 register

Table 60. PIO0\_2 register (PIO0\_2, address 0x4004 401C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_2.	
		0x1	SSP0_SSEL.	
		0x2	CT16B0_CAP0.	
		0x3	ADC_PIN_TRIG0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011

Table 60. PIO0\_2 register (PIO0\_2, address 0x4004 401C) bit description ...continued

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.7 PIO2\_7 register

Table 61. PIO2\_7 register (PIO2\_7, address 0x4004 4020) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_7.	
		0x1	CT32B0_MAT2.	
		0x2	U0_RXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.8 PIO2\_8 register

Table 62. PIO2\_8 register (PIO2\_8, address 0x4004 4024) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_8.	
		0x1	CT32B0_MAT3.	
		0x2	U0_TXD.	



Table 62. PIO2\_8 register (PIO2\_8, address 0x4004 4024) bit description

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.9 PIO2\_1 register

Table 63. PIO2\_1 register (PIO2\_1, address 0x4004 4028) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_1.	
		0x1	U0_DSR.	
		0x2	SSP1_SCK.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.10 PIO0\_4 register

Table 64. PIO0\_4 register (PIO0\_4, address 0x4004 4030) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_4 (open-drain pin).	
		0x1	I2C0_SCL (open-drain pin).	
7:3		-	Reserved.	00000
9:8	I2CMODE		Selects I2C mode. Select Standard mode (I2CMODE = 00, default) or Standard I/O functionality (I2CMODE = 01) if the pin function is GPIO (FUNC = 000).	00
		0x0	Standard mode/ Fast-mode I2C.	
		0x1	Standard I/O functionality	
		0x2	Fast-mode Plus I2C	
		0x3	Reserved.	
31:10	-	-	Reserved.	-

### 6.4.11 PIO0\_5 register

Table 65. PIO0\_5 register (PIO0\_5, address 0x4004 4034) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_5 (open-drain pin).	
		0x1	I2C0_SDA (open-drain pin).	
7:3		-	Reserved.	00000
9:8	I2CMODE		Selects I2C mode. Select Standard mode (I2CMODE = 00, default) or Standard I/O functionality (I2CMODE = 01) if the pin function is GPIO (FUNC = 000).	00
		0x0	Standard mode/ Fast-mode I2C.	
		0x1	Standard I/O functionality	
		0x2	Fast-mode Plus I2C	
		0x3	Reserved.	
31:10	-	-	Reserved.	-

### 6.4.12 PIO1\_9 register

Table 66. PIO1\_9 register (PIO1\_9, address 0x4004 4038) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_9.	
		0x1	CT16B1_MAT0.	
		0x2	SSP1_MOSI.	

Table 66. PIO1\_9 register (PIO1\_9, address 0x4004 4038) bit description ...continued

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.13 PIO3\_4 register

Table 67. PIO3\_4 register (PIO3\_4, address 0x4004 403C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO3_4.	
		0x1	CT16B0_CAP1.	
		0x2	U0_RXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.14 PIO2\_4 register

Table 68. PIO2\_4 register (PIO2\_4, address 0x4004 4040) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_4.	
		0x1	CT16B1_MAT1.	
		0x2	SSP1_SSEL.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.15 PIO2\_5 register

Table 69. PIO2\_5 register (PIO2\_5, address 0x4004 4044) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_5.	
		0x1	CT32B0_MAT0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011

Table 69. PIO2\_5 register (PIO2\_5, address 0x4004 4044) bit description

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.16 PIO3\_5 register

Table 70. PIO3\_5 register (PIO3\_5, address 0x4004 4048) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO3_5.	
		0x1	CT16B1_CAP1.	
		0x2	U0_TXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.17 PIO2\_9 register

Table 71. PIO2\_9 register (PIO2\_9, address 0x4004 4054) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_9.	
		0x1	CT32B0_CAP0.	

Table 71. PIO2\_9 register (PIO2\_9, address 0x4004 4054) bit description

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.18 PIO2\_10 register

Table 72. PIO2\_10 register (PIO2\_10, address 0x4004 4058) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_10.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.19 PIO2\_2 register

Table 73. PIO2\_2 register (PIO2\_2, address 0x4004 405C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_2.	
		0x1	U0_DCD.	
		0x2	SSP1_MISO.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.20 PIO0\_8 register

Table 74. PIO0\_8 register (PIO0\_8, address 0x4004 4060) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_8.	
		0x1	SSP0_MISO.	
		0x2	CT16B0_MAT0.	
		0x4	ADC_PIN_TRIG2	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011

Table 74. PIO0\_8 register (PIO0\_8, address 0x4004 4060) bit description ...continued

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.21 PIO0\_9 register

Table 75. PIO0\_9 register (PIO0\_9, address 0x4004 4064) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_9.	
		0x1	SSP0_MOSI.	
		0x2	CT16B0_MAT1.	
		0x4	ADC_PIN_TRIG3	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.22 SWCLK\_PIO0\_10 register

Table 76. SWCLK\_PIO0\_10 register (SWCLK\_PIO0\_10, address 0x4004 4068) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	SWCLK.	
		0x1	PIO0_10.	
		0x2	SSP0_SCK (only if pin SWCLK/PIO0_10/SSP0_SCK/CT16B0_MAT2 selected in the SCK0_LOC register).	
		0x3	CT16B0_MAT2.	



**Table 76. SWCLK\_PIO0\_10 register (SWCLK\_PIO0\_10, address 0x4004 4068) bit description ...continued**

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.23 PIO1\_10 register

**Table 77. PIO1\_10 register (PIO1\_10, address 0x4004 406C) bit description**

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_10.	
		0x1	ADC_8.	
		0x2	CT16B1_MAT1.	
		0x3	SSP1_MISO.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00

Table 77. PIO1\_10 register (PIO1\_10, address 0x4004 406C) bit description ...continued

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

#### 6.4.24 R\_PIO0\_11 register

Table 78. R\_PIO0\_11 register (R\_PIO0\_11, address 0x4004 4074) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	R. This function is reserved. Select one of the alternate functions below.	
		0x1	PIO0_11.	
		0x2	ADC_7.	
		0x3	CT32B0_MAT3.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.25 R\_PIO1\_0 register

Table 79. R\_PIO1\_0 register (R\_PIO1\_0, address 0x4004 4078) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	R. This function is reserved. Select one of the alternate functions below.	
		0x1	PIO1_0.	
		0x2	ADC_6.	
		0x3	CT32B1_CAP0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.26 R\_PIO1\_1 register

Table 80. R\_PIO1\_1 register (R\_PIO1\_1, address 0x4004 407C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	R. This function is reserved. Select one of the alternate functions below.	
		0x1	PIO1_1.	
		0x2	ADC_5.	
		0x3	CT32B1_MAT0.	

Table 80. R\_PIO1\_1 register (R\_PIO1\_1, address 0x4004 407C) bit description ...continued

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

## 6.4.27 R\_PIO1\_2 register

Table 81. R\_PIO1\_2 register (R\_PIO1\_2, address 0x4004 4080) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	R. This function is reserved. Select one of the alternate functions below.	
		0x1	PIO1_2.	
		0x2	ADC_4.	
		0x3	CT32B1_MAT1.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1

Table 81. R\_PIO1\_2 register (R\_PIO1\_2, address 0x4004 4080) bit description ...continued

Bit	Symbol	Value	Description	Reset value
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.28 PIO3\_0 register

Table 82. PIO3\_0 register (PIO3\_0, address 0x4004 4084) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO3_0.	
		0x1	U0_DTR.	
		0x2	CT16B0_MAT0.	
		0x3	U0_TXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.29 PIO2\_3 register

Table 83. PIO2\_3 register (PIO2\_3, address 0x4004 408C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO2_3.	
		0x1	U0_RI.	
		0x2	SSP1_MOSI.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.30 SWDIO\_PIO1\_3 register

Table 84. SWDIO\_PIO1\_3 register (SWDIO\_PIO1\_3, address 0x4004 4090) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	SWDIO.	
		0x1	PIO1_3.	
		0x2	ADC_3.	
		0x3	CT32B1_MAT2.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1

Table 84. SWDIO\_PIO1\_3 register (SWDIO\_PIO1\_3, address 0x4004 4090) bit description

Bit	Symbol	Value	Description	Reset value
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.31 PIO1\_4 register

Table 85. PIO1\_4 register (PIO1\_4, address 0x4004 4094) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. This pin functions as WAKEUP pin if the part is in Deep power-down mode regardless of the value of FUNC. All other values are reserved.	000
		0x0	PIO1_4.	
		0x1	ADC_2.	
		0x2	CT32B1_MAT3.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

## 6.4.32 PIO1\_11

Table 86. PIO1\_11 register (PIO1\_11, address 0x4004 4098) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_11.	
		0x1	ADC_1.	
		0x2	CT32B1_CAP1.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	-	-	Reserved	1
7	ADMODE		Selects Analog/Digital mode	1
		0	Analog input mode	
		1	Digital functional mode	
9:8	-	-	Reserved	00
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

## 6.4.33 PIO3\_2

Table 87. PIO3\_2 register (PIO3\_2, address 0x4004 409C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO3_2.	
		0x1	U0_DCD.	
		0x2	CT16B0_MAT2.	
		0x3	SSP1_SCK.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	



Table 87. PIO3\_2 register (PIO3\_2, address 0x4004 409C) bit description ...continued

Bit	Symbol	Value	Description	Reset value
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.34 PIO1\_5

Table 88. PIO1\_5 register (PIO1\_5, address 0x4004 40A0) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_5.	
		0x1	U0_RTS.	
		0x2	CT32B0_CAP0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.35 PIO1\_6

Table 89. PIO1\_6 register (PIO1\_6, address 0x4004 40A4) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_6.	
		0x1	U0_RXD.	
		0x2	CT32B0_MAT0.	

Table 89. PIO1\_6 register (PIO1\_6, address 0x4004 40A4) bit description ...continued

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

### 6.4.36 PIO1\_7

Table 90. PIO1\_7 register (PIO1\_7, address 0x4004 40A8) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO1_7.	
		0x1	U0_TXD.	
		0x2	CT32B0_MAT1.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

## 6.4.37 PIO3\_3

Table 91. PIO3\_3 register (PIO3\_3, address 0x4004 40AC) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO3_3.	
		0x1	U0_RI.	
		0x2	CT16B0_CAP0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

## 6.4.38 SCK0\_LOC

Table 92. IOCON SCK0 location register (SCK0\_LOC, address 0x4004 40B0) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SCKLOC		Selects pin location for SSP0_SCK function.	00
		0x0	PIO0_10. Selects SCK0 function in pin location SWCLK/PIO0_10.	
		0x1	Reserved.	
		0x2	PIO0_6. Selects SSP0_SCK function in pin location PIO0_6.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

## 6.4.39 DSR\_LOC

Table 93. IOCON U0\_DSR location register (DSR\_LOC, address 0x4004 40B4) bit description

Bit	Symbol	Value	Description	Reset value
1:0	DSRLOC		Selects pin location for $\overline{U0\_DSR}$ function.	00
		0x0	PIO2_1. Selects $\overline{U0\_DSR}$ function in pin location PIO2_1	
31:2	-	-	Reserved.	-

### 6.4.40 DCD\_LOC

Table 94. IOCON  $\overline{U0\_DCD}$  location register (DCD\_LOC, address 0x4004 40B8) bit description

Bit	Symbol	Value	Description	Reset value
1:0	DCDLOC		Selects pin location for $\overline{U0\_DCD}$ function.	00
		0x0	PIO2_2. Selects $\overline{U0\_DCD}$ function in pin location PIO2_2.	
		0x1	PIO3_2. Selects $\overline{U0\_DCD}$ function in pin location PIO3_2.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.41 RI\_LOC

Table 95. IOCON  $\overline{U0\_RI}$  location register (RI\_LOC, address 0x4004 40BC) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RILOC		Selects pin location for $\overline{U0\_RI}$ function.	00
		0x0	PIO2_3. Selects $\overline{U0\_RI}$ function in pin location PIO2_3.	
		0x1	PIO3_3. Selects $\overline{U0\_RI}$ function in pin location PIO3_3.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.42 PIO0\_3 register

Table 96. PIO0\_3 register (PIO0\_3, address 0x4004 40C0) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_3.	
		0x3	U2_RXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011

Table 96. PIO0\_3 register (PIO0\_3, address 0x4004 40C0) bit description ...continued

Bit	Symbol	Value	Description	Reset value
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

#### 6.4.43 PIO0\_6 register

Table 97. PIO0\_6 register (PIO0\_6, address 0x4004 40C4) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_6.	
		0x1	Reserved.	
		0x2	SSP0_SCK (only if pin PIO0_6/SSP0_SCK selected in the SCK0_LOC register).	
		0x3	U1_TXD.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

#### 6.4.44 PIO0\_7 register

Table 98. PIO0\_7 register (PIO0\_7, address 0x4004 40C8) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. All other values are reserved.	000
		0x0	PIO0_7.	
		0x1	U0_CTS.	
		0x2	ADC_PIN_TRIG1.	
		0x3	U1_RXD.	

Table 98. PIO0\_7 register (PIO0\_7, address 0x4004 40C8) bit description

Bit	Symbol	Value	Description	Reset value
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
9:6	-	-	Reserved	0011
10	OD		Selects pseudo open-drain mode.	0
		0	Standard GPIO output	
		1	Open-drain output	
31:11	-	-	Reserved	-

#### 6.4.45 SSEL1\_LOC

Table 99. IOCON SSP1\_SSEL location register (SSEL1\_LOC, address 0x4004 40CC) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SSEL1LOC		Selects pin location for SSP1_SSEL function.	00
		0x0	PIO2_0. Selects SSP1_SSEL function in pin location PIO2_0.	
		0x1	PIO2_4. Selects SSP1_SSEL function in pin location PIO2_4.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.46 CT16B0\_CAP0\_LOC

Table 100. IOCON CT16B0\_CAP0 location register (CT16B0\_CAP0\_LOC, address 0x4004 40D0) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CT16B0_CAP0LOC		Selects pin location for CT16B0_CAP0 function.	00
		0x0	PIO0_2. Selects CT16B0_CAP0 function in pin location PIO0_2.	
		0x1	PIO3_3. Selects CT16B0_CAP0 function in pin location PIO3_3.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.47 SCK1\_LOC

Table 101. IOCON SSP1\_SCK location register (SCK1\_LOC, address 0x4004 40D4) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SCK1LOC		Selects pin location for SSP1_SCK function.	00
		0x0	PIO2_1. Selects SSP1_SCK function in pin location PIO2_1.	
		0x1	PIO3_2. Selects SSP1_SCK function in pin location PIO3_2.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.48 MISO1\_LOC

Table 102. IOCON SSP1\_MISO location register (MISO1\_LOC, address 0x4004 40D8) bit description

Bit	Symbol	Value	Description	Reset value
1:0	MISO1LOC		Selects pin location for the SSP1_MISO function.	00
		0x0	PIO2_2. Selects SSP1_MISO function in pin location PIO2_2.	
		0x1	PIO1_10. Selects SSP1_MISO function in pin location PIO1_10.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.49 MOSI1\_LOC

Table 103. IOCON SSP1\_MOSI location register (MOSI1\_LOC, address 0x4004 40DC) bit description

Bit	Symbol	Value	Description	Reset value
1:0	MOSI1LOC		Selects pin location for the SSP1_MOSI function.	00
		0x0	PIO2_3. Selects SSP1_MOSI1 function in pin location PIO2_3.	
		0x1	PIO1_9. Selects SSP1_MOSI function in pin location PIO1_9.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.50 CT32B0\_CAP0\_LOC

Table 104. IOCON CT32B0\_CAP0 location register (CT32B0\_CAP0\_LOC, address 0x4004 40E0) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CT32B0_CAP0LOC		Selects pin location for the CT32B0_CAP0 function.	00
		0x0	PIO1_5. Selects CT32B0_CAP0 function in pin location PIO1_5.	
		0x1	PIO2_9. Selects CT32B0_CAP0 function in pin location PIO2_9.	
		0x2	Reserved.	
		0x3	Reserved.	
31:2	-	-	Reserved.	-

### 6.4.51 RXD\_LOC

Table 105. IOCON U0\_RXD location register (RXD\_LOC, address 0x4004 40E4) bit description

Bit	Symbol	Value	Description	Reset value
1:0	RXDLOC		Selects pin location for the U0_RXD function.	00
		0x0	PIO1_6. Selects U0_RXD function in pin location PIO1_6.	
		0x1	PIO2_7. Selects U0_RXD function in pin location PIO2_7.	
		0x2	Reserved.	
		0x3	PIO3_4. Selects U0_RXD function in pin location PIO3_4.	
31:2	-	-	Reserved.	-



## 6.4.52 IOCON function assignments

Table 106. IOCON function assignments

Symbol	Function = 0	Function = 1	Function = 2	Function = 3	Function = 4	Reference
RESET/PIO0_0	RESET	PIO0_0	-	-	-	<a href="#">Table 57</a>
PIO0_1	PIO0_1	CLKOUT	CT32B0_MAT2	-	-	<a href="#">Table 58</a>
PIO0_2	PIO0_2	SSP0_SSEL	CT16B0_CAP0	ADC_PIN_TRIG0	-	<a href="#">Table 60</a>
PIO0_3	PIO0_3	R	R	U2_RXD	-	<a href="#">Table 96</a>
PIO0_4	PIO0_4	I2C0_SCL	-	-	-	<a href="#">Table 64</a>
PIO0_5	PIO0_5	I2C0_SDA	-	-	-	<a href="#">Table 65</a>
PIO0_6	PIO0_6	R	SSP0_SCK	U1_TXD	-	<a href="#">Table 97</a>
PIO0_7	PIO0_7	U0_CTS	ADC_PIN_TRIG1	U1_RXD	-	<a href="#">Table 98</a>
PIO0_8	PIO0_8	SSP0_MISO	CT16B0_MAT0	R	ADC_PIN_TRIG2	<a href="#">Table 74</a>
PIO0_9	PIO0_9	SSP0_MOSI	CT16B0_MAT1	R	ADC_PIN_TRIG3	<a href="#">Table 75</a>
SWCLK/PIO0_10	SWCLK	PIO0_10	SSP0_SCK	CT16B0_MAT2	-	<a href="#">Table 76</a>
R/PIO0_11/ADC_7/CT32B0_MAT3	R	PIO0_11	ADC_7	CT32B0_MAT3	-	<a href="#">Table 78</a>
R/PIO1_0/ADC_6/CT32B1_CAP0	R	PIO1_0	ADC_6	CT32B1_CAP0	-	<a href="#">Table 79</a>
R/PIO1_1/ADC_5/CT32B1_MAT0	R	PIO1_1	ADC_5	CT32B1_MAT0	-	<a href="#">Table 80</a>
R/PIO1_2/ADC_4/CT32B1_MAT1	R	PIO1_2	ADC_4	CT32B1_MAT1	-	<a href="#">Table 81</a>
SWDIO/PIO1_3/ADC_3/CT32B1_MAT2	SWDIO	PIO1_3	ADC_3	CT32B1_MAT2	-	<a href="#">Table 84</a>
PIO1_4/ADC_2/CT32B1_MAT3/WAKEUP	PIO1_4	ADC_2	CT32B1_MAT3	-	-	<a href="#">Table 85</a>
PIO1_5	PIO1_5	U0_RTS	CT32B0_CAP0	-	-	<a href="#">Table 88</a>
PIO1_6	PIO1_6	U0_RXD	CT32B0_MAT0	-	-	<a href="#">Table 89</a>
PIO1_7	PIO1_7	U0_TXD	CT32B0_MAT1	-	-	<a href="#">Table 90</a>
PIO1_8	PIO1_8	CT16B1_CAP0	R	U2_TXD	-	<a href="#">Table 59</a>
PIO1_9	PIO1_9	CT16B1_MAT0	SSP1_MOSI	-	-	<a href="#">Table 66</a>
PIO1_10/ADC_8/CT16B1_MAT1/SSP1_MISO	PIO1_10	ADC_8	CT16B1_MAT1	SSP1_MISO	-	<a href="#">Table 77</a>
PIO1_11/ADC_1/CT32B1_CAP1	PIO1_11	ADC_1	CT32B1_CAP1	-	-	<a href="#">Table 86</a>
PIO2_0	PIO2_0	U0_DTR	SSP1_SSEL	ADC_PIN_TRIG4	-	<a href="#">Table 56</a>
PIO2_1	PIO2_1	U0_DSR	SSP1_SCK	-	-	<a href="#">Table 63</a>
PIO2_2	PIO2_2	U0_DCD	SSP1_MISO	-	-	<a href="#">Table 73</a>

Table 106. IOCON function assignments

Symbol	Function = 0	Function = 1	Function= 2	Function = 3	Function = 4	Reference
PIO2_3	PIO2_3	U0_RI	SSP1_MOSI	-	-	<a href="#">Table 83</a>
PIO2_4	PIO2_4	CT16B1_MAT1	SSP1_SSEL	-	-	<a href="#">Table 68</a>
PIO2_5	PIO2_5	CT32B0_MAT0	-	-	-	<a href="#">Table 69</a>
PIO2_6	PIO2_6	CT32B0_MAT1	-	-	-	<a href="#">Table 55</a>
PIO2_7	PIO2_7	CT32B0_MAT2	U0_RXD	-	-	<a href="#">Table 61</a>
PIO2_8	PIO2_8	CT32B0_MAT3	U0_TXD	-	-	<a href="#">Table 62</a>
PIO2_9	PIO2_9	CT32B0_CAP0	-	-	-	<a href="#">Table 62</a>
PIO2_10	PIO2_10	-	-	-	-	<a href="#">Table 72</a>
PIO3_0	PIO3_0	U0_DTR	CT16B0_MAT0	U0_TXD	-	<a href="#">Table 82</a>
PIO3_2	PIO3_2	U0_DCD	CT16B0_MAT2	SSP1_SCK	-	<a href="#">Table 87</a>
PIO3_3	PIO3_3	U0_RI	CT16B0_CAP0	-	-	<a href="#">Table 91</a>
PIO3_4	PIO3_4	CT16B0_CAP1	U0_RXD	-	-	<a href="#">Table 67</a>
PIO3_5	PIO3_5	CT16B1_CAP1	U0_TXD	-	-	<a href="#">Table 70</a>

### 7.1 Pin description

[Table 107](#) shows all pins and their assigned digital or analog functions ordered by GPIO port number.

**Table 107. Pin description**

Symbol	LQFP48		Reset state <a href="#">[1]</a>	Start logic wake-up pin	Type	Description
RESET/PIO0_0	3	<a href="#">[6]</a>	I; PU	yes	I	<b>RESET</b> — External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
					I/O	<b>PIO0_0</b> — General purpose port 0 input/output 0.
PIO0_1	4	<a href="#">[6]</a>	I; PU	yes	I/O	<b>PIO0_1</b> — General purpose port 0 input/output 1. A LOW level on this pin during reset starts the ISP command handler.
					O	<b>CLKOUT</b> — Clock output.
					O	<b>CT32B0_MAT2</b> — Match output 2 for 32-bit timer 0.
PIO0_2	10	<a href="#">[6]</a>	I; PU	yes	I/O	<b>PIO0_2</b> — General purpose port 0 input/output 2.
					I/O	<b>SSP0_SSEL</b> — Slave select for SSP0.
					I	<b>CT16B0_CAP0</b> — Capture input 0 for 16-bit timer 0.
					I	<b>ADC_PIN_TRIG0</b> — ADC pin trigger input 0.
PIO0_3	14	<a href="#">[6]</a>	I; PU	yes	I/O	<b>PIO0_3</b> — General purpose port 0 input/output 3.
					-	<b>R</b> — Reserved.
					-	<b>R</b> — Reserved.
					I	<b>U2_RXD</b> — Receiver input for UART2.
PIO0_4	15		I; IA	yes	I/O	<b>PIO0_4</b> — General purpose port 0 input/output 4.
					I/O	<b>I2C0_SCL</b> — I <sup>2</sup> C-bus, open-drain clock input/output. High-current sink only if I <sup>2</sup> C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5	16	<a href="#">[7]</a>	I; IA	yes	I/O	<b>PIO0_5</b> — General purpose port 0 input/output 5.
					I/O	<b>I2C0_SDA</b> — I <sup>2</sup> C-bus, open-drain data input/output. High-current sink only if I <sup>2</sup> C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6	22	<a href="#">[6]</a>	I; PU	yes	I/O	<b>PIO0_6</b> — General purpose port 0 input/output 6.
					-	<b>R</b> — Reserved.
					I/O	<b>SSP0_SCK</b> — Serial clock for SSP0.
					O	<b>U1_TXD</b> — Transmitter output for UART1.

Table 107. Pin description

Symbol	LQFP48		Reset state <a href="#">[1]</a>	Start logic wake-up pin	Type	Description
PIO0_7	23	<a href="#">[5]</a>	I; PU	yes	I/O	<b>PIO0_7</b> — General purpose port 0 input/output 7. High-current output driver.
					I	<b>U0_CTS</b> — Clear To Send input for UART0.
					I	<b>ADC_PIN_TRIG1</b> — ADC pin trigger input 1.
					I	<b>U1_RXD</b> — Receiver input for UART1.
PIO0_8	26	<a href="#">[6]</a>	I; PU	yes	I/O	<b>PIO0_8</b> — General purpose port 0 input/output 8.
					I/O	<b>SSP0_MISO</b> — Master In Slave Out for SSP0.
					O	<b>CT16B0_MAT0</b> — Match output 0 for 16-bit timer 0.
					-	<b>R</b> — Reserved.
PIO0_9	27	<a href="#">[6]</a>	I; PU	yes	I	<b>ADC_PIN_TRIG2</b> — ADC pin trigger input 2.
					I/O	<b>PIO0_9</b> — General purpose port 0 input/output 9.
					I/O	<b>SSP0_MOSI</b> — Master Out Slave In for SSP0.
					O	<b>CT16B0_MAT1</b> — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10	28	<a href="#">[6]</a>	I; PU	yes	-	<b>R</b> — Reserved.
					I	<b>ADC_PIN_TRIG3</b> — ADC pin trigger input 3.
					I/O	<b>SWCLK</b> — Serial wire clock.
					I/O	<b>PIO0_10</b> — General purpose port 0 input/output 10.
R/PIO0_11	30	<a href="#">[3]</a>	I; PU	yes	I/O	<b>SSP0_SCK</b> — Serial clock for SSP0.
					O	<b>CT16B0_MAT2</b> — Match output 2 for 16-bit timer 0.
					I	<b>R</b> — Reserved. Configure for an alternate function in the IOCON block.
					I/O	<b>PIO0_11</b> — General purpose port 0 input/output 11.
R/PIO1_0	31	<a href="#">[3]</a>	I; PU	yes	AI	<b>ADC_7</b> — A/D converter, input 7.
					O	<b>CT32B0_MAT3</b> — Match output 3 for 32-bit timer 0.
					I	<b>R</b> — Reserved. Configure for an alternate function in the IOCON block.
					I/O	<b>PIO1_0</b> — General purpose port 1 input/output 0.
R/PIO1_1	32	<a href="#">[3]</a>	O; PU	no	AI	<b>ADC_6</b> — A/D converter, input 6.
					I	<b>CT32B1_CAP0</b> — Capture input 0 for 32-bit timer 1.
					O	<b>R</b> — Reserved. Configure for an alternate function in the IOCON block.
					I/O	<b>PIO1_1</b> — General purpose port 1 input/output 1.
$\overline{\text{R}}$ /PIO1_2	35	<a href="#">[3]</a>	I; PU	no	AI	<b>ADC_5</b> — A/D converter, input 5.
					O	<b>CT32B1_MAT0</b> — Match output 0 for 32-bit timer 1.
					I	<b>R</b> — Reserved. Configure for an alternate function in the IOCON block.
					I/O	<b>PIO1_2</b> — General purpose port 1 input/output 2.
$\overline{\text{R}}$ /PIO1_2	35	<a href="#">[3]</a>	I; PU	no	AI	<b>ADC_4</b> — A/D converter, input 4.
					O	<b>CT32B1_MAT1</b> — Match output 1 for 32-bit timer 1.

Table 107. Pin description

Symbol	LQFP48		Reset state <a href="#">[1]</a>	Start logic wake-up pin	Type	Description
SWDIO/PIO1_3	38	<a href="#">[3]</a>	I; PU	no	I/O	<b>SWDIO</b> — Serial Wire Debug I/O. SWDIO is enabled by default on this pin.
					I/O	<b>PIO1_3</b> — General purpose port 1 input/output 3.
					AI	<b>ADC_3</b> — A/D converter, input 3.
					O	<b>CT32B1_MAT2</b> — Match output 2 for 32-bit timer 1.
PIO1_4/ WAKEUP	39	<a href="#">[4]</a>	I; PU	no	IO	<b>PIO1_4</b> — General purpose port 1 input/output 4. General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
					AI	<b>ADC_2</b> — A/D converter, input 2.
					O	<b>CT32B1_MAT3</b> — Match output 3 for 32-bit timer 1.
PIO1_5	45	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO1_5</b> — General purpose port 1 input/output 5.
					O	<b>U0_RTS</b> — Request To Send output for UART0.
					I	<b>CT32B0_CAP0</b> — Capture input 0 for 32-bit timer 0.
PIO1_6	46	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO1_6</b> — General purpose port 1 input/output 6.
					I	<b>U0_RXD</b> — Receiver input for UART0. In ISP mode, connect to UART.
					O	<b>CT32B0_MAT0</b> — Match output 0 for 32-bit timer 0.
PIO1_7	47	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO1_7</b> — General purpose port 1 input/output 7.
					O	<b>U0_TXD</b> — Transmitter output for UART0. In ISP mode, connect to UART.
					O	<b>CT32B0_MAT1</b> — Match output 1 for 32-bit timer 0.
PIO1_8	9	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO1_8</b> — General purpose port 1 input/output 8.
					I	<b>CT16B1_CAP0</b> — Capture input 0 for 16-bit timer 1.
					-	<b>R</b> — Reserved.
					O	<b>U2_TXD</b> — Transmitter output for U2.
PIO1_9	17	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO1_9</b> — General purpose port 1 input/output 9.
					O	<b>CT16B1_MAT0</b> — Match output 0 for 16-bit timer 1.
					I/O	<b>SSP1_MOSI</b> — Master Out Slave In for SSP1.I
PIO1_10	29	<a href="#">[3]</a>	I; PU	no	I/O	<b>PIO1_10</b> — General purpose port 1 input/output 10.
					AI	<b>ADC_8</b> — A/D converter, input 8.
					O	<b>CT16B1_MAT1</b> — Match output 1 for 16-bit timer 1.
					I/O	<b>SSP1_MISO</b> — Master In Slave Out for SSP1.
PIO1_11	42	<a href="#">[3]</a>	I; PU	no	I/O	<b>PIO1_11</b> — General purpose port 1 input/output 11.
					AI	<b>ADC_1</b> — A/D converter, input 1.
					I	<b>CT32B1_CAP1</b> — Capture input 1 for 32-bit timer 1.

Table 107. Pin description

Symbol	LQFP48		Reset state <a href="#">[1]</a>	Start logic wake-up pin	Type	Description
PIO2_0	2	<a href="#">[6]</a>	I; PU	no	IO	<b>PIO2_0</b> — General purpose port 2 input/output 0.
					O	<b>U0_DTR</b> — Data Terminal Ready output for UART0.
					I/O	<b>SSP1_SSEL</b> — Slave Select for SSP1.
					I	<b>ADC_PIN_TRIG4</b> — ADC pin trigger input 4.
PIO2_1	13	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_1</b> — General purpose port 2 input/output 1.
					I	<b>U0_DSR</b> — Data Set Ready input for UART0.
					I/O	<b>SSP1_SCK</b> — Serial clock for SSP1.
PIO2_2	25	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_2</b> — General purpose port 2 input/output 2.
					I	<b>U0_DCD</b> — Data Carrier Detect input for UART0.
					I/O	<b>SSP1_MISO</b> — Master In Slave Out for SSP1.
PIO2_3	37	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_3</b> — General purpose port 2 input/output 3.
					I	<b>U0_RI</b> — Ring Indicator input for UART0.
					I/O	<b>SSP1_MOSI</b> — Master Out Slave In for SSP1.
PIO2_4	19	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_4</b> — General purpose port 2 input/output 4.
					O	<b>CT16B1_MAT1</b> — Match output 1 for 16-bit timer 1.
					I/O	<b>SSP1_SSEL</b> — Slave Select for SSP1.
PIO2_5	20	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_5</b> — General purpose port 2 input/output 5.
					O	<b>CT32B0_MAT0</b> — Match output 0 for 32-bit timer 0.
PIO2_6	1	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_6</b> — General purpose port 2 input/output 6.
					O	<b>CT32B0_MAT1</b> — Match output 1 for 32-bit timer 0.
PIO2_7	11	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_7</b> — General purpose port 2 input/output 7.
					O	<b>CT32B0_MAT2</b> — Match output 2 for 32-bit timer 0.
					I	<b>U0_RXD</b> — Receiver input for UART0.
PIO2_8	12	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_8</b> — General purpose port 2 input/output 8.
					I	<b>CT32B0_MAT3</b> — Match output 3 for 32-bit timer 0.
					O	<b>U0_TXD</b> — Transmitter output for UART0.
PIO2_9	24	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_9</b> — General purpose port 2 input/output 9.
					I	<b>CT32B0_CAP0</b> — Capture input 0 for 32-bit timer 0.
PIO2_10	-	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO2_10</b> — General purpose port 2 input/output 10.
PIO3_0	36	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO3_0</b> — General purpose port 3 input/output 0.
					O	<b>U0_DTR</b> — Data Terminal Ready output for UART0.
					O	<b>CT16B0_MAT0</b> — Match output 0 for 16-bit timer 0.
					O	<b>U0_TXD</b> — Transmitter Output for UART0.
PIO3_2	-	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO3_2</b> — General purpose port 3 input/output 2.
					I	<b>U0_DCD</b> — Data Carrier Detect input for UART0.
					O	<b>CT16B0_MAT2</b> — Match output 2 for 16-bit timer 0.
					I/O	<b>SSP1_SCK</b> — Serial clock for SSP1.

Table 107. Pin description

Symbol	LQFP48		Reset state <a href="#">[1]</a>	Start logic wake-up pin	Type	Description
PIO3_3	48	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO3_3</b> — General purpose port 3 input/output 3.
					I	<b>U0_RI</b> — Ring Indicator input for UART0.
					I	<b>CT16B0_CAP0</b> — Capture input 0 for 16-bit timer 0.
PIO3_4	18	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO3_4</b> — General purpose port 3 input/output 4.
					I	<b>CT16B0_CAP1</b> — Capture input 1 for 16-bit timer 0.
					I	<b>U0_RXD</b> — Receiver input for UART0.
PIO3_5	21	<a href="#">[6]</a>	I; PU	no	I/O	<b>PIO3_5</b> — General purpose port 3 input/output 5.
					I	<b>CT16B1_CAP1</b> — Capture input 1 for 16-bit timer 1.
					O	<b>U0_TXD</b> — Transmitter output for UART0.
XTALIN	6	<a href="#">[2]</a>	-	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	<a href="#">[2]</a>	-	-	-	Output from the oscillator amplifier.
VREFP	33		-	-	-	Positive reference voltage for the ADC.
VREFN	34		-	-	-	Negative reference voltage for the ADC.
V <sub>DD</sub>	8; 44		-	-	-	3.3 V supply voltage to the internal regulator and the external rail.
V <sub>DDA</sub>	43		-	-	-	Analog supply voltage.
V <sub>SSA</sub>	40		-	-	-	Analog ground.
V <sub>SS</sub>	5; 41		-	-	-	Ground.

- [1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V<sub>DD</sub> level (V<sub>DD</sub> = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 6](#)).
- [4] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled (see [Figure 6](#)). In deep power-down mode, this pin serves as the wake-up pin.
- [5] High-current output driver. Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 6](#)).
- [6] Standard digital I/O pin. Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 6](#)).
- [7] I<sup>2</sup>C-bus pins compliant with the I<sup>2</sup>C-bus specification for I<sup>2</sup>C standard mode, I<sup>2</sup>C Fast-mode, and I<sup>2</sup>C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I<sup>2</sup>C lines. Open-drain configuration applies to all functions on this pin.
- [8] 5 V tolerant pad. RESET functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 6](#) for the reset pad configuration.

### 8.1 How to read this chapter

See [Table 108](#) for available GPIO pins on each GPIO port:

**Table 108. GPIO configuration**

Package	GPIO port 0	GPIO port 1	GPIO port 2	GPIO port 3	Total GPIO pins
LQFP48	PIO0_0 to PIO0_11	PIO1_0 to PIO1_11	PIO2_0 to PIO2_9	PIO3_0; PIO3_3 to PIO3_5	38

Register bits corresponding to PION\_m pins that are not available are reserved. Pins PIO2\_11 and PIO3\_1 are missing on both packages.

### 8.2 Introduction

#### 8.2.1 Features

- GPIO pins can be configured as input or output by software.
- Each individual port pin can serve as an edge or level-sensitive interrupt request.
- Interrupts can be configured on single falling or rising edges and on both edges.
- Level-sensitive interrupt pins can be HIGH or LOW-active.
- All GPIO pins are inputs by default.
- Reading and writing of data registers are masked by address bits 13:2.

### 8.3 Register description

Each GPIO register can be up to 12 bits wide and can be read or written using word or half-word operations at word addresses.

**Table 109. Register overview: GPIO (base address 0x5000 0000 (GPIO0), 0x5001 0000 (GPIO1), 0x5002 0000 (GPIO2), 0x5003 0000 (GPIO3))**

Name	Access	Address offset	Description	Reset value
DATA	R/W	0x0000 to 0x3FF8	Port n data address masking register locations for pins PION_0 to PION_11 (see <a href="#">Section 8.4.1</a> ).	n/a
DATA	R/W	0x3FFC	Port n data register for pins PION_0 to PION_11	n/a
-	-	0x4000 to 0x7FFC	reserved	-
DIR	R/W	0x8000	Data direction register for port n	0x00
IS	R/W	0x8004	Interrupt sense register for port n	0x00
IBE	R/W	0x8008	Interrupt both edges register for port n	0x00
IEV	R/W	0x800C	Interrupt event register for port n	0x00



**Table 109. Register overview: GPIO (base address 0x5000 0000 (GPIO0), 0x5001 0000 (GPIO1), 0x5002 0000 (GPIO2), 0x5003 0000 (GPIO3))**

Name	Access	Address offset	Description	Reset value
IE	R/W	0x8010	Interrupt mask register for port n	0x00
RIS	R	0x8014	Raw interrupt status register for port n	0x00
MIS	R	0x8018	Masked interrupt status register for port n	0x00
IC	W	0x801C	Interrupt clear register for port n	0x00
-	-	0x8020 - 0xFFFF	reserved	0x00

### 8.3.1 GPIO data register

The DATA register holds the current logic state of the pin (HIGH or LOW), independently of whether the pin is configured as an GPIO input or output or as another digital function. If the pin is configured as GPIO output, the current value of the GPIO DATA register is driven to the pin.

A read of the GPIO DATA register always returns the current logic level (state) of the pin independently of its configuration. Because there is a single data register for both the value of the output driver and the state of the pin's input, write operations have different effects depending on the pin's configuration:

- If a pin is configured as GPIO input, a write to the GPIO DATA register has no effect on the pin level. A read returns the current state of the pin.
- If a pin is configured as GPIO output, the current value of GPIO DATA register is driven to the pin. This value can be a result of writing to the GPIO DATA register, or it can reflect the previous state of the pin if the pin is switched to GPIO output from GPIO input or another digital function. A read returns the current state of the output latch.
- If a pin is configured as another digital function (input or output), a write to the GPIO DATA register has no effect on the pin level. A read returns the current state of the pin even if it is configured as an output. This means that by reading the GPIO DATA register, the digital output or input value of a function other than GPIO on that pin can be observed.

The following rules apply when the pins are switched from input to output:

- Pin is configured as input with a HIGH level applied:
  - Change pin to output: pin drives HIGH level.
- Pin is configured as input with a LOW level applied:
  - Change pin to output: pin drives LOW level.

The rules show that the pins mirror the current logic level. Therefore floating pins may drive an unpredictable level when switched from input to output.

**Table 110. GPIO DATA register (DATA, address 0x5000 0000 to 0x5000 3FFC (GPIO0), 0x5001 0000 to 0x5001 3FFC (GPIO1), 0x5002 0000 to 0x5002 3FFC (GPIO2), 0x5003 0000 to 0x5003 3FFC (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	DATA	Logic levels for pins PION_x to PION_11. HIGH = 1, LOW = 0.	n/a	R/W
31:12	-	Reserved	-	-

### 8.3.2 GPIO data direction register

**Table 111. GPIO DIR register (DIR, address 0x5000 8000 (GPIO0), 0x5001 8000 (GPIO1), 0x5002 8000 (GPIO2), 0x5003 8000 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	IO	Selects pin x as input or output (x = 0 to 11). 0 = Pin PION_x is configured as input. 1 = Pin PION_x is configured as output.	0x00	R/W
31:12	-	Reserved	-	-

### 8.3.3 GPIO interrupt sense register

**Table 112. GPIO IS register (IS, address 0x5000 8004 (GPIO0), 0x5001 8004 (GPIO1), 0x5002 8004 (GPIO2), 0x5003 8004 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	SENSE	Selects interrupt on pin x as level or edge sensitive (x = 0 to 11). 0 = Interrupt on pin PION_x is configured as edge sensitive. 1 = Interrupt on pin PION_x is configured as level sensitive.	0x00	R/W
31:12	-	Reserved	-	-

### 8.3.4 GPIO interrupt both edges sense register

**Table 113. GPIO IBE register (IBE, address 0x5000 8008 (GPIO0), 0x5001 8008 (GPIO1), 0x5002 8008 (GPIO2), 0x5003 8008 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	EDGE	Selects interrupt on pin x to be triggered on both edges (x = 0 to 11). 0 = Interrupt on pin PION_x is controlled through register GPIO IEV. 1 = Both edges on pin PION_x trigger an interrupt.	0x00	R/W
31:12	-	Reserved	-	-

### 8.3.5 GPIO interrupt event register

**Table 114. GPIO IEV register (IEV, address 0x5000 800C (GPIO0), address 0x5001 800C (GPIO1), address 0x5002 800C (GPIO2), address 0x5003 800C (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	EVENT	Selects interrupt on pin x to be triggered rising or falling edges (x = 0 to 11). 0 = Depending on setting in register GPIO IS (see <a href="#">Table 112</a> ), falling edges or LOW level on pin PION_x trigger an interrupt. 1 = Depending on setting in register GPIO IS (see <a href="#">Table 112</a> ), rising edges or HIGH level on pin PION_x trigger an interrupt.	0x00	R/W
31:12	-	Reserved	-	-

### 8.3.6 GPIO interrupt mask register

Bits set to HIGH in the GPIO IE register allow the corresponding pins to trigger their individual interrupts and the combined GPIO INTR line. Clearing a bit disables interrupt triggering on that pin.

**Table 115. GPIO IE register (IE, address 0x5000 8010 (GPIO0), 0x5001 8010 (GPIO1), 0x5002 8010 (GPIO2), 0x5003 8010 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	MASK	Selects interrupt on pin x to be masked (x = 0 to 11). 0 = Interrupt on pin PION_x is masked. 1 = Interrupt on pin PION_x is not masked.	0x00	R/W
31:12	-	Reserved	-	-

### 8.3.7 GPIO raw interrupt status register

Bits read HIGH in the GPIO RIS register reflect the raw (prior to masking) interrupt status of the corresponding pins indicating that all the requirements have been met before they are allowed to trigger the GPIO IE. Bits read as zero indicate that the corresponding input pins have not initiated an interrupt. The register is read-only.

**Table 116. GPIO RIS register (RIS, address 0x5000 8014 (GPIO0), 0x5001 8014 (GPIO1), 0x5002 8014 (GPIO2), 0x5003 8014 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	RAWST	Raw interrupt status (x = 0 to 11). 0 = No interrupt on pin PION_x. 1 = Interrupt requirements met on PION_x.	0x00	R
31:12	-	Reserved	-	-

### 8.3.8 GPIO masked interrupt status register

Bits read HIGH in the GPIO MIS register reflect the status of the input lines triggering an interrupt. Bits read as LOW indicate that either no interrupt on the corresponding input pins has been generated or that the interrupt is masked. GPIO MIS is the state of the interrupt after masking. The register is read-only.

**Table 117. GPIO MIS register (MIS, address 0x5000 8018 (GPIO0), 0x5001 8018 (GPIO1), 0x5002 8018 (GPIO2), 0x5003 8018 (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	MASKST	Selects interrupt on pin x to be masked (x = 0 to 11). 0 = No interrupt or interrupt masked on pin PION_x. 1 = Interrupt on PION_x.	0x00	R
31:12	-	Reserved	-	-

### 8.3.9 GPIO interrupt clear register

This register allows software to clear edge detection for port bits that are identified as edge-sensitive in the Interrupt Sense register. This register has no effect on port bits identified as level-sensitive.

**Table 118. GPIO IC register (IC, address 0x5000 801C (GPIO0), 0x5001 801C (GPIO1), 0x5002 801C (GPIO2), 0x5003 801C (GPIO3)) bit description**

Bit	Symbol	Description	Reset value	Access
11:0	CLR	Selects interrupt on pin x to be cleared (x = 0 to 11). Clears the interrupt edge detection logic. This register is write-only. <b>Remark:</b> The synchronizer between the GPIO and the NVIC blocks causes a delay of 2 clocks. It is recommended to add two NOPs after the clear of the interrupt edge detection logic before the exit of the interrupt service routine. 0 = No effect. 1 = Clears edge detection logic for pin PION_x.	0x00	W
31:12	-	Reserved	-	-

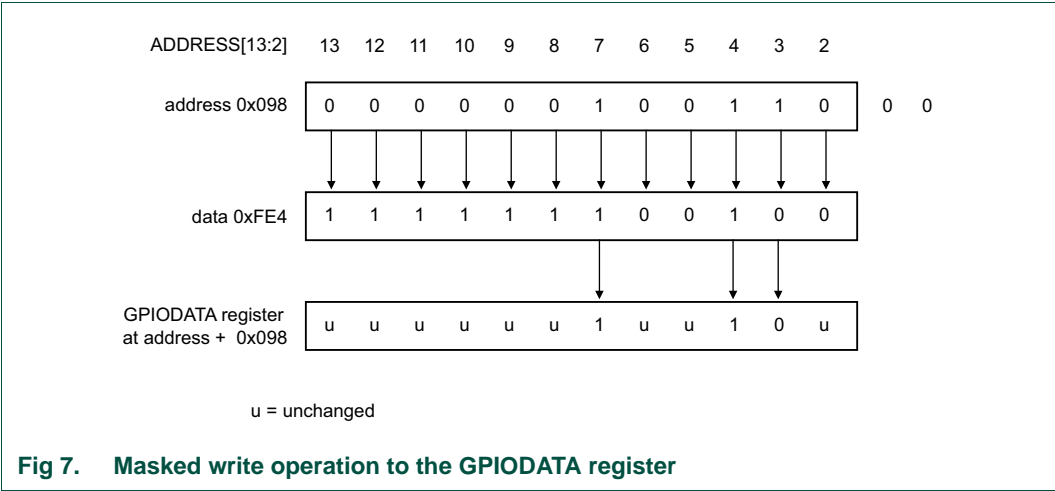
## 8.4 Functional description

### 8.4.1 Write/read data operation

In order for software to be able to set GPIO bits without affecting any other pins in a single write operation, bits [13:2] of a 14-bit wide address bus are used to create a 12-bit wide mask for write and read operations on the 12 GPIO pins for each port. Only GPIO DATA bits masked by 1 are affected by read and write operations. The masked GPIO DATA register can be located anywhere between address offsets 0x0000 to 0x3FFC in the GPIO address space. Reading and writing to the GPIO DATA register at address 0x3FFC sets all masking bits to 1.

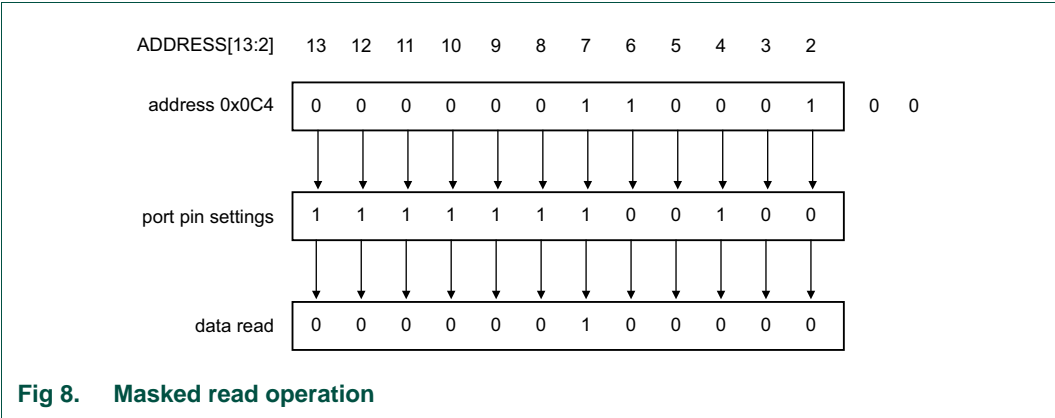
8.4.1.1 Write operation

If the address bit (i+2) associated with the GPIO port bit i (i = 0 to 11) to be written is HIGH, the value of the GPIODATA register bit i is updated. If the address bit (i+2) is LOW, the corresponding GPIODATA register bit i is left unchanged.



8.4.1.2 Read operation

If the address bit associated with the GPIO data bit is HIGH, the value is read. If the address bit is LOW, the GPIO data bit is read as 0. Reading a port DATA register yields the state of port pins 11:0 ANDed with address bits 13:2.



### 9.1 Features

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- Standard I<sup>2</sup>C-compliant bus interfaces may be configured as Master, Slave, or Master/Slave.
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I<sup>2</sup>C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.
- Supports Fast-mode Plus.
- Optional recognition of up to four distinct slave addresses.
- Monitor mode allows observing all I<sup>2</sup>C-bus traffic, regardless of slave address.
- I<sup>2</sup>C-bus can be used for test and diagnostic purposes.
- The I<sup>2</sup>C0-bus contains a standard I<sup>2</sup>C-compliant bus interface with two open-drain pins.

### 9.2 Basic configuration

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The I<sup>2</sup>C-bus interface is configured using the following registers:

1. Pins: The I2C pin functions and the I2C mode are configured in the IOCON register block ([Section 6.4](#), [Table 64](#), and [Table 65](#)).
2. Power and peripheral clock: In the SYSAHBCLKCTRL register, set bit 5 ([Table 19](#)).
3. Reset: Before accessing the I2C block, ensure that the I2C\_RST\_N bit in the PRESETCTRL register ([Table 7](#)) are set to 1. This de-asserts the reset signal to the I2C block.

### 9.3 General description

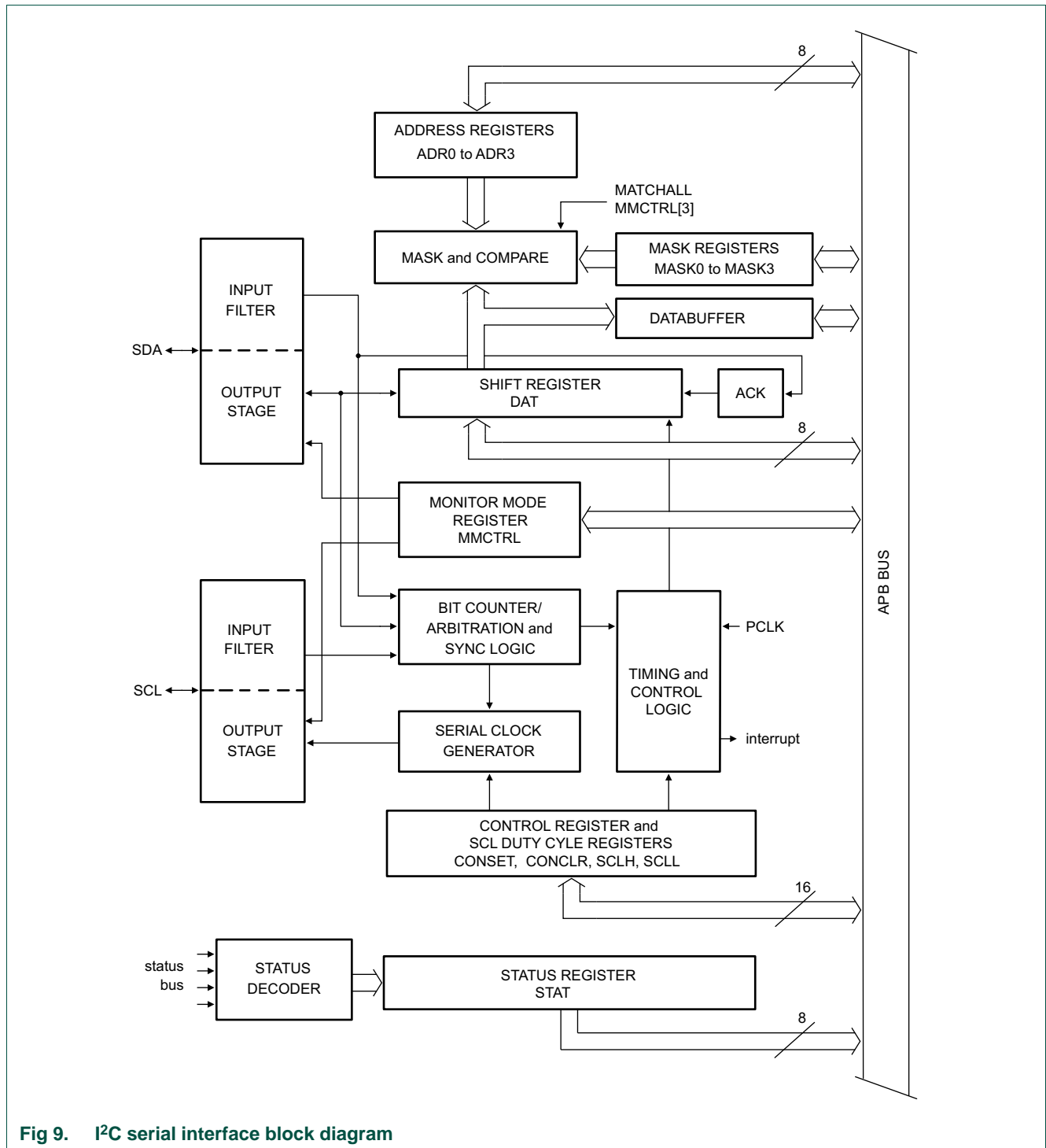


Fig 9. I2C serial interface block diagram



### 9.3.1 Address Registers, ADR0 to ADR3

These registers may be loaded with the 7-bit slave address (7 most significant bits) to which the I<sup>2</sup>C block will respond when programmed as a slave transmitter or receiver. The LSB (GC) is used to enable General Call address (0x00) recognition. When multiple slave addresses are enabled, the actual address received may be read from the DAT register at the state where the own slave address has been received.

### 9.3.2 Address mask registers, MASK0 to MASK3

The four mask registers each contain seven active bits (7:1). Any bit in these registers which is set to '1' will cause an automatic compare on the corresponding bit of the received address when it is compared to the ADR<sub>n</sub> register associated with that mask register. In other words, bits in an ADR<sub>n</sub> register which are masked are not taken into account in determining an address match.

When an address-match interrupt occurs, the processor will have to read the data register (DAT) to determine what the received address was that actually caused the match.

### 9.3.3 Comparator

The comparator compares the received 7-bit slave address with its own slave address (7 most significant bits in ADR). It also compares the first received 8-bit byte with the General Call address (0x00). If an equality is found, the appropriate status bits are set and an interrupt is requested.

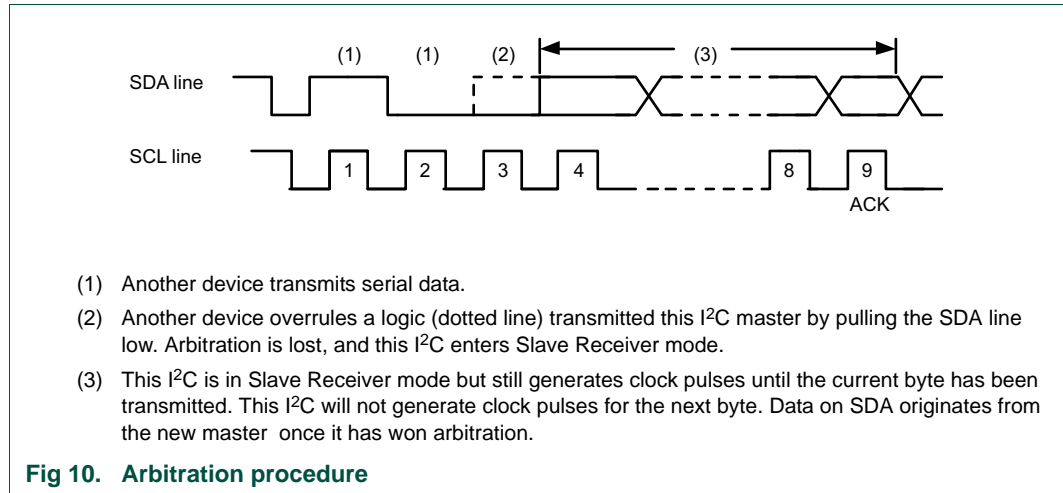
### 9.3.4 Shift register, DAT

This 8-bit register contains a byte of serial data to be transmitted or a byte which has just been received. Data in DAT is always shifted from right to left; the first bit to be transmitted is the MSB (bit 7) and, after a byte has been received, the first bit of received data is located at the MSB of DAT. While data is being shifted out, data on the bus is simultaneously being shifted in; DAT always contains the last byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in DAT.

### 9.3.5 Arbitration and synchronization logic

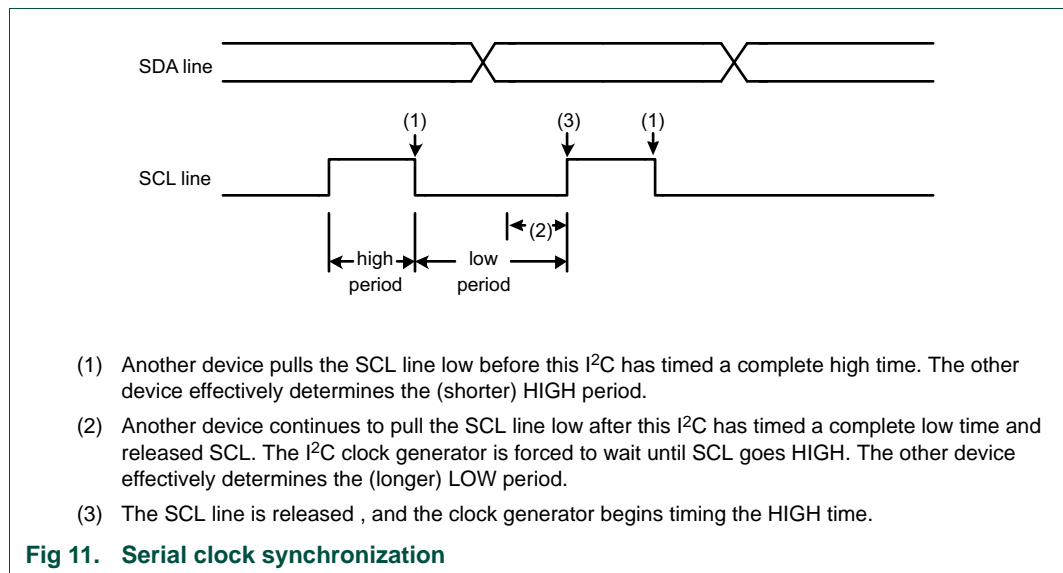
In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I<sup>2</sup>C-bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost, and the I<sup>2</sup>C block immediately changes from master transmitter to slave receiver. The I<sup>2</sup>C block will continue to output clock pulses (on SCL) until transmission of the current serial byte is complete.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode can only occur while the I<sup>2</sup>C block is returning a "not acknowledge: (logic 1) to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this can occur only at the end of a serial byte, the I<sup>2</sup>C block generates no further clock pulses. [Figure 10](#) shows the arbitration procedure.



The synchronization logic will synchronize the serial clock generator with the clock pulses on the SCL line from another device. If two or more master devices generate clock pulses, the “mark” duration is determined by the device that generates the shortest “marks,” and the “space” duration is determined by the device that generates the longest “spaces”.

[Figure 11](#) shows the synchronization procedure.



A slave may stretch the space duration to slow down the bus master. The space duration may also be stretched for handshaking purposes. This can be done after each bit or after a complete byte transfer. The I<sup>2</sup>C block will stretch the SCL space duration after a byte has been transmitted or received and the acknowledge bit has been transferred. The serial interrupt flag (SI) is set, and the stretching continues until the serial interrupt flag is cleared.

### 9.3.6 Serial clock generator

This programmable clock pulse generator provides the SCL clock pulses when the I<sup>2</sup>C block is in the master transmitter or master receiver mode. It is switched off when the I<sup>2</sup>C block is in slave mode. The I<sup>2</sup>C output clock frequency and duty cycle is programmable

via the I<sup>2</sup>C Clock Control Registers. See the description of the I2CSCLL and I2CSCLH registers for details. The output clock pulses have a duty cycle as programmed unless the bus is synchronizing with other SCL clock sources as described above.

### 9.3.7 Timing and control

The timing and control logic generates the timing and control signals for serial byte handling. This logic block provides the shift pulses for DAT, enables the comparator, generates and detects START and STOP conditions, receives and transmits acknowledge bits, controls the master and slave modes, contains interrupt request logic, and monitors the I<sup>2</sup>C-bus status.

### 9.3.8 Control register, CONSET and CONCLR

The I<sup>2</sup>C control register contains bits used to control the following I<sup>2</sup>C block functions: start and restart of a serial transfer, termination of a serial transfer, bit rate, address recognition, and acknowledgment.

The contents of the I<sup>2</sup>C control register may be read as CONSET. Writing to CONSET will set bits in the I<sup>2</sup>C control register that correspond to ones in the value written. Conversely, writing to CONCLR will clear bits in the I<sup>2</sup>C control register that correspond to ones in the value written.

### 9.3.9 Status decoder and status register

The status decoder takes all of the internal status bits and compresses them into a 5-bit code. This code is unique for each I<sup>2</sup>C-bus status. The 5-bit code may be used to generate vector addresses for fast processing of the various service routines. Each service routine processes a particular bus status. There are 26 possible bus states if all four modes of the I<sup>2</sup>C block are used. The 5-bit status code is latched into the five most significant bits of the status register when the serial interrupt flag is set (by hardware) and remains stable until the interrupt flag is cleared by software. The three least significant bits of the status register are always zero. If the status code is used as a vector to service routines, then the routines are displaced by eight address locations. Eight bytes of code is sufficient for most of the service routines (see the software example in this section).

### 9.3.10 I<sup>2</sup>C operating modes

In a given application, the I<sup>2</sup>C block may operate as a master, a slave, or both. In the slave mode, the I<sup>2</sup>C hardware looks for any one of its four slave addresses and the General Call address. If one of these addresses is detected, an interrupt is requested. If the processor wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave operation is not interrupted. If bus arbitration is lost in the master mode, the I<sup>2</sup>C block switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

#### 9.3.10.1 Master Transmitter mode

In this mode data is transmitted from master to slave. Before the master transmitter mode can be entered, the CONSET register must be initialized as shown in [Table 119](#). I2EN must be set to 1 to enable the I<sup>2</sup>C function. If the AA bit is 0, the I<sup>2</sup>C interface will not acknowledge any address when another device is master of the bus, so it can not enter

slave mode. The STA, STO and SI bits must be 0. The SI Bit is cleared by writing 1 to the SIC bit in the CONCLR register. The STA bit should be cleared after writing the slave address.

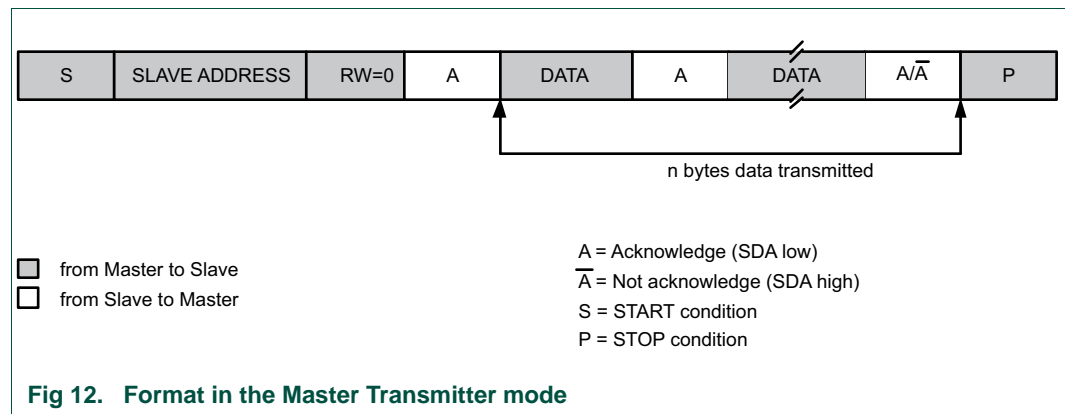
**Table 119. CONSET used to configure Master mode**

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	0	-	-

The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this mode the data direction bit (R/W) should be 0 which means Write. The first byte transmitted contains the slave address and Write bit. Data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

The I<sup>2</sup>C interface will enter master transmitter mode when software sets the STA bit. The I<sup>2</sup>C logic will send the START condition as soon as the bus is free. After the START condition is transmitted, the SI bit is set, and the status code in the STAT register is 0x08. This status code is used to vector to a state service routine which will load the slave address and Write bit to the DAT register, and then clear the SI bit. SI is cleared by writing a 1 to the SIC bit in the CONCLR register.

When the slave address and R/W bit have been transmitted and an acknowledgment bit has been received, the SI bit is set again, and the possible status codes now are 0x18, 0x20, or 0x38 for the master mode, or 0x68, 0x78, or 0xB0 if the slave mode was enabled (by setting AA to 1). The appropriate actions to be taken for each of these status codes are shown in [Table 137](#) to [Table 142](#).

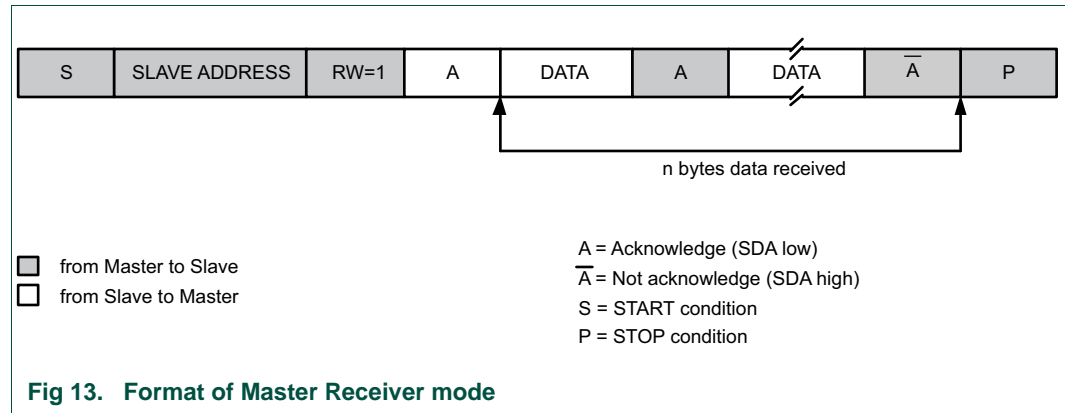


### 9.3.10.2 Master Receiver mode

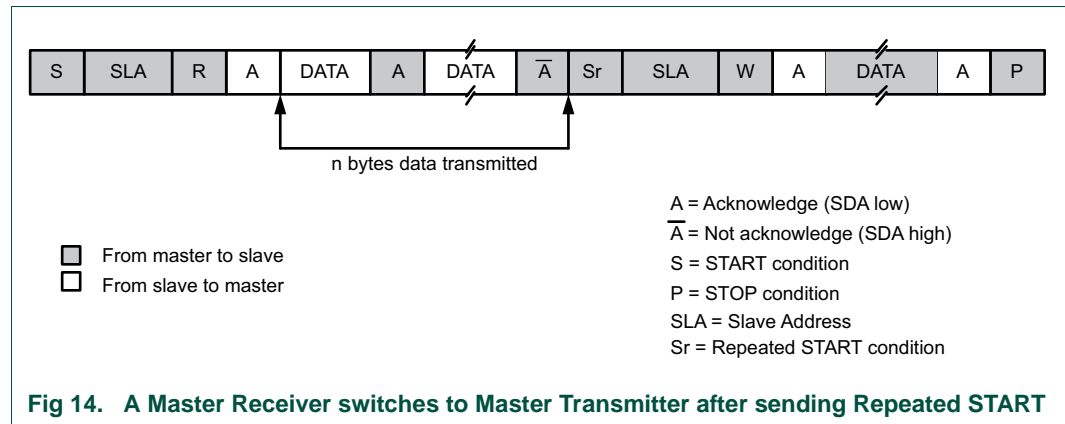
In the master receiver mode, data is received from a slave transmitter. The transfer is initiated in the same way as in the master transmitter mode. When the START condition has been transmitted, the interrupt service routine must load the slave address and the data direction bit to the I<sup>2</sup>C Data register (DAT), and then clear the SI bit. In this case, the data direction bit (R/W) should be 1 to indicate a read.

When the slave address and data direction bit have been transmitted and an acknowledge bit has been received, the SI bit is set, and the Status Register will show the status code. For master mode, the possible status codes are 0x40, 0x48, or 0x38. For

slave mode, the possible status codes are 0x68, 0x78, or 0xB0. For details, refer to [Table 138](#).



After a Repeated START condition, I<sup>2</sup>C may switch to the master transmitter mode.



### 9.3.10.3 Slave Receiver mode

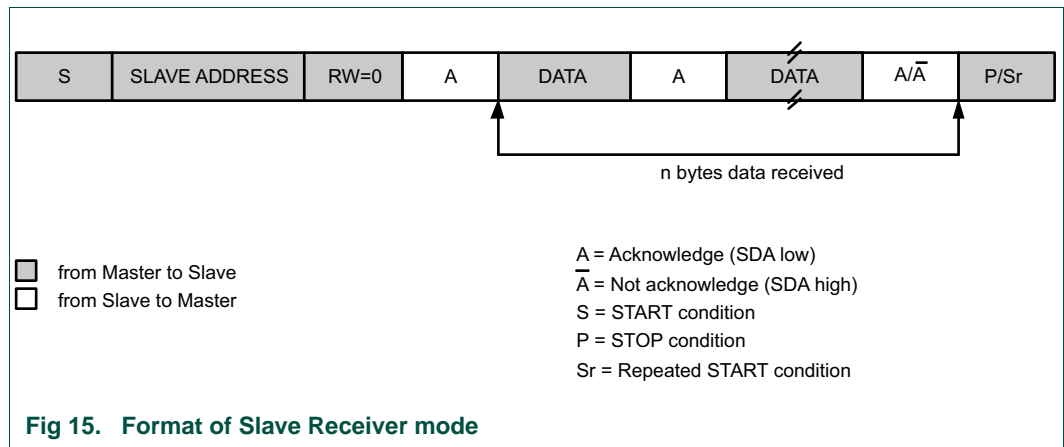
In the slave receiver mode, data bytes are received from a master transmitter. To initialize the slave receiver mode, write any of the Slave Address registers (ADR0-3) and write the I<sup>2</sup>C Control Set register (CONSET) as shown in [Table 120](#).

**Table 120. CONSET used to configure Slave mode**

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	1	-	-

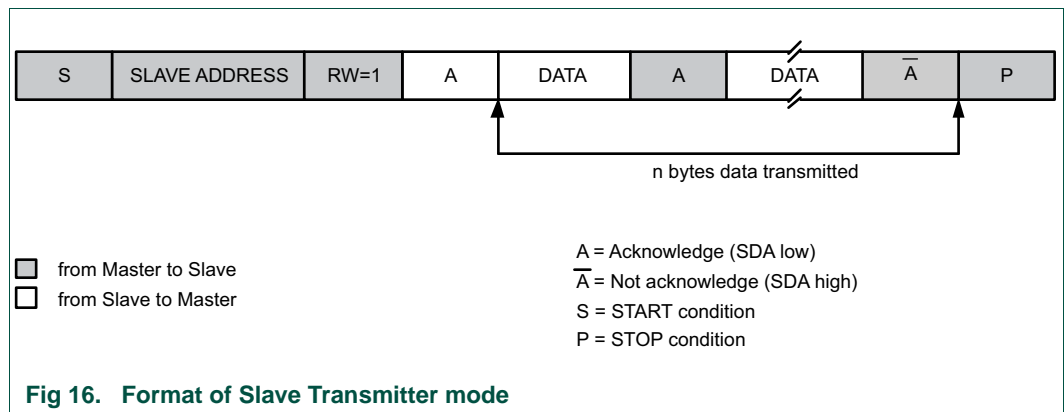
I2EN must be set to 1 to enable the I<sup>2</sup>C function. AA bit must be set to 1 to acknowledge its own slave address or the General Call address. The STA, STO and SI bits are set to 0.

After ADR and CONSET are initialized, the I<sup>2</sup>C interface waits until it is addressed by its own address or general address followed by the data direction bit. If the direction bit is 0 (W), it enters slave receiver mode. If the direction bit is 1 (R), it enters slave transmitter mode. After the address and direction bit have been received, the SI bit is set and a valid status code can be read from the Status register (STAT). Refer to [Table 141](#) for the status codes and actions.



#### 9.3.10.4 Slave Transmitter mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will be 1, indicating a read operation. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. In a given application, I<sup>2</sup>C may operate as a master and as a slave. In the slave mode, the I<sup>2</sup>C hardware looks for its own slave address and the General Call address. If one of these addresses is detected, an interrupt is requested. When the microcontrollers wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, the I<sup>2</sup>C interface switches to the slave mode immediately and can detect its own slave address in the same serial transfer.



### 9.3.11 I2C bus configuration

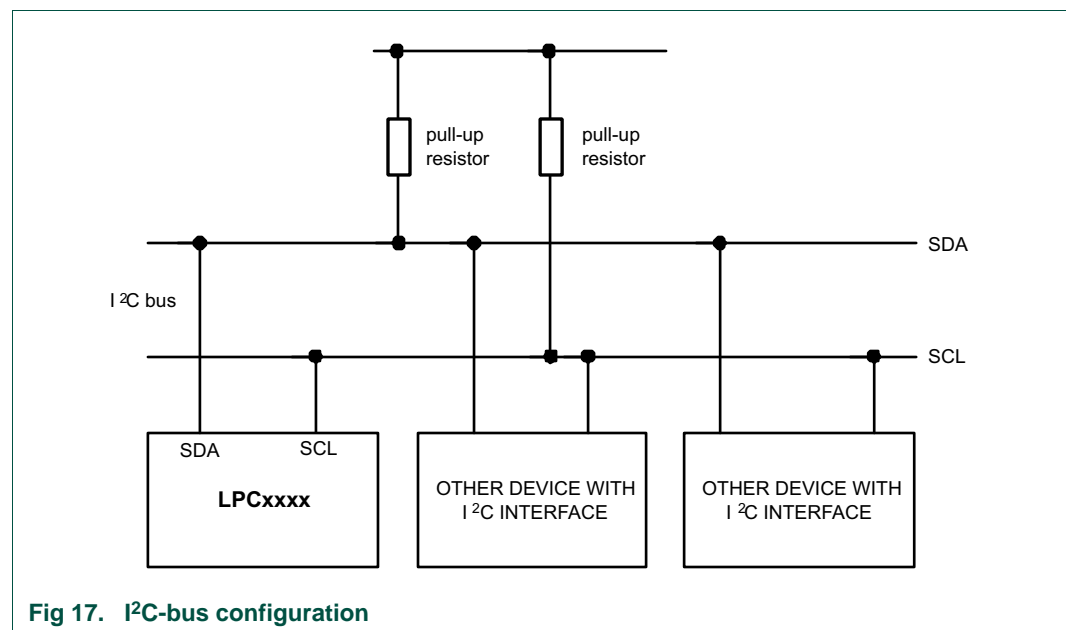
A typical I<sup>2</sup>C-bus configuration is shown in [Figure 17](#). Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I<sup>2</sup>C-bus:

- Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

- Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since a Repeated START condition is also the beginning of the next serial transfer, the I<sup>2</sup>C bus will not be released.

The I<sup>2</sup>C interface is byte oriented and has four operating modes: master transmitter mode, master receiver mode, slave transmitter mode and slave receiver mode.

The I<sup>2</sup>C interface complies with the entire I<sup>2</sup>C specification, supporting the ability to turn power off to the ARM core without interfering with other devices on the same I<sup>2</sup>C-bus.



### 9.3.12 I<sup>2</sup>C Fast-mode Plus

Fast-Mode Plus supports a 1 Mbit/sec transfer rate to communicate with the I<sup>2</sup>C-bus products which NXP Semiconductors is now providing.

### 9.3.13 Applications

Interfaces to external I<sup>2</sup>C standard parts, such as serial RAMs, LCDs, tone generators, other microcontrollers, etc.

### 9.3.14 Input filters and output stages

Input signals are synchronized with the internal clock, and spikes shorter than three clocks are filtered out.

The output for I<sup>2</sup>C is a special pad designed to conform to the I<sup>2</sup>C specification.

## 9.4 Pin description

Table 121. I<sup>2</sup>C-bus pin description

Pin	Type	Description
I2C0_SDA	Input/Output	I <sup>2</sup> C0 Serial Data. This is an open-drain pin.
I2C0_SCL	Input/Output	I <sup>2</sup> C Serial Clock. This is an open-drain pin.

The I<sup>2</sup>C0-bus pins must be configured through the PIO0\_4 and PIO0\_5 registers in the IOCON for Standard/ Fast-mode or Fast-mode Plus. In Fast-mode Plus, rates above 400 kHz and up to 1 MHz may be selected. The I<sup>2</sup>C-bus pins are open-drain outputs and fully compatible with the I<sup>2</sup>C-bus specification.

## 9.5 Register description

Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 122. Register overview: I<sup>2</sup>C (base address 0x4000 0000)

Name	Access	Address offset	Description	Reset value	Reference
CONSET	R/W	0x000	<b>I<sup>2</sup>C Control Set Register.</b> When a one is written to a bit of this register, the corresponding bit in the I <sup>2</sup> C control register is set. Writing a zero has no effect on the corresponding bit in the I <sup>2</sup> C control register.	0x00	<a href="#">Table 123</a>
STAT	RO	0x004	<b>I<sup>2</sup>C Status Register.</b> During I <sup>2</sup> C operation, this register provides detailed status codes that allow software to determine the next action needed.	0xF8	<a href="#">Table 124</a>
DAT	R/W	0x008	<b>I<sup>2</sup>C Data Register.</b> During master or slave transmit mode, data to be transmitted is written to this register. During master or slave receive mode, data that has been received may be read from this register.	0x00	<a href="#">Table 125</a>
ADR0	R/W	0x00C	<b>I<sup>2</sup>C Slave Address Register 0.</b> Contains the 7-bit slave address for operation of the I <sup>2</sup> C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00	<a href="#">Table 126</a>
SCLH	R/W	0x010	<b>SCH Duty Cycle Register High Half Word.</b> Determines the high time of the I <sup>2</sup> C clock.	0x04	<a href="#">Table 127</a>
SCLL	R/W	0x014	<b>SCL Duty Cycle Register Low Half Word.</b> Determines the low time of the I <sup>2</sup> C clock. I2nSCLL and I2nSCLH together determine the clock frequency generated by an I <sup>2</sup> C master and certain times used in slave mode.	0x04	<a href="#">Table 128</a>
CONCLR	WO	0x018	<b>I<sup>2</sup>C Control Clear Register.</b> When a one is written to a bit of this register, the corresponding bit in the I <sup>2</sup> C control register is cleared. Writing a zero has no effect on the corresponding bit in the I <sup>2</sup> C control register.	NA	<a href="#">Table 130</a>
MMCTRL	R/W	0x01C	<b>Monitor mode control register.</b>	0x00	<a href="#">Table 131</a>



Table 122. Register overview: I<sup>2</sup>C (base address 0x4000 0000) ...continued

Name	Access	Address offset	Description	Reset value	Reference
ADR1	R/W	0x020	<b>I<sup>2</sup>C Slave Address Register 1.</b> Contains the 7-bit slave address for operation of the I <sup>2</sup> C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00	<a href="#">Table 132</a>
ADR2	R/W	0x024	<b>I<sup>2</sup>C Slave Address Register 2.</b> Contains the 7-bit slave address for operation of the I <sup>2</sup> C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00	<a href="#">Table 132</a>
ADR3	R/W	0x028	<b>I<sup>2</sup>C Slave Address Register 3.</b> Contains the 7-bit slave address for operation of the I <sup>2</sup> C interface in slave mode, and is not used in master mode. The least significant bit determines whether a slave responds to the General Call address.	0x00	<a href="#">Table 132</a>
DATA_BUFFER	RO	0x02C	<b>Data buffer register.</b> The contents of the 8 MSBs of the I2DAT shift register will be transferred to the DATA_BUFFER automatically after every nine bits (8 bits of data plus ACK or NACK) has been received on the bus.	0x00	<a href="#">Table 133</a>
MASK0	R/W	0x030	<b>I<sup>2</sup>C Slave address mask register 0.</b> This mask register is associated with I2ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address ('0000000').	0x00	<a href="#">Table 134</a>
MASK1	R/W	0x034	<b>I<sup>2</sup>C Slave address mask register 1.</b> This mask register is associated with I2ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address ('0000000').	0x00	<a href="#">Table 134</a>
MASK2	R/W	0x038	<b>I<sup>2</sup>C Slave address mask register 2.</b> This mask register is associated with I2ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address ('0000000').	0x00	<a href="#">Table 134</a>
MASK3	R/W	0x03C	<b>I<sup>2</sup>C Slave address mask register 3.</b> This mask register is associated with I2ADR0 to determine an address match. The mask register has no effect when comparing to the General Call address ('0000000').	0x00	<a href="#">Table 134</a>

### 9.5.1 I<sup>2</sup>C Control Set register

The CONSET registers control setting of bits in the CON register that controls operation of the I<sup>2</sup>C interface. Writing a one to a bit of this register causes the corresponding bit in the I<sup>2</sup>C control register to be set. Writing a zero has no effect.

Table 123. I<sup>2</sup>C Control Set register (CONSET, address 0x4000 0000) bit description

Bit	Symbol	Description	Reset value
1:0	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	AA	Assert acknowledge flag.	
3	SI	I <sup>2</sup> C interrupt flag.	0
4	STO	STOP flag.	0

Table 123. I<sup>2</sup>C Control Set register (CONSET, address 0x4000 0000) bit description

Bit	Symbol	Description	Reset value
5	STA	START flag.	0
6	I2EN	I <sup>2</sup> C interface enable.	0
31:7	-	Reserved. The value read from a reserved bit is not defined.	-

**I2EN** I<sup>2</sup>C Interface Enable. When I2EN is 1, the I<sup>2</sup>C interface is enabled. I2EN can be cleared by writing 1 to the I2ENC bit in the CONCLR register. When I2EN is 0, the I<sup>2</sup>C interface is disabled.

When I2EN is “0”, the SDA and SCL input signals are ignored, the I<sup>2</sup>C block is in the “not addressed” slave state, and the STO bit is forced to “0”.

I2EN should not be used to temporarily release the I<sup>2</sup>C-bus since, when I2EN is reset, the I<sup>2</sup>C-bus status is lost. The AA flag should be used instead.

**STA** is the START flag. Setting this bit causes the I<sup>2</sup>C interface to enter master mode and transmit a START condition or transmit a Repeated START condition if it is already in master mode.

When STA is 1 and the I<sup>2</sup>C interface is not already in master mode, it enters master mode, checks the bus and generates a START condition if the bus is free. If the bus is not free, it waits for a STOP condition (which will free the bus) and generates a START condition after a delay of a half clock period of the internal clock generator. If the I<sup>2</sup>C interface is already in master mode and data has been transmitted or received, it transmits a Repeated START condition. STA may be set at any time, including when the I<sup>2</sup>C interface is in an addressed slave mode.

STA can be cleared by writing 1 to the STAC bit in the CONCLR register. When STA is 0, no START condition or Repeated START condition will be generated.

If STA and STO are both set, then a STOP condition is transmitted on the I<sup>2</sup>C-bus if the interface is in master mode, and transmits a START condition thereafter. If the I<sup>2</sup>C interface is in slave mode, an internal STOP condition is generated, but is not transmitted on the bus.

**STO** is the STOP flag. Setting this bit causes the I<sup>2</sup>C interface to transmit a STOP condition in master mode, or recover from an error condition in slave mode. When STO is 1 in master mode, a STOP condition is transmitted on the I<sup>2</sup>C-bus. When the bus detects the STOP condition, STO is cleared automatically.

In slave mode, setting this bit can recover from an error condition. In this case, no STOP condition is transmitted to the bus. The hardware behaves as if a STOP condition has been received and it switches to “not addressed” slave receiver mode. The STO flag is cleared by hardware automatically.

**SI** is the I<sup>2</sup>C Interrupt Flag. This bit is set when the I<sup>2</sup>C state changes. However, entering state F8 does not set SI since there is nothing for an interrupt service routine to do in that case.

While SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. When SCL is HIGH, it is unaffected by the state of the SI flag. SI must be reset by software, by writing a 1 to the SIC bit in the CONCLR register.

**AA** is the Assert Acknowledge Flag. When set to 1, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. The address in the Slave Address Register has been received.
2. The General Call address has been received while the General Call bit (GC) in the ADR register is set.
3. A data byte has been received while the I<sup>2</sup>C is in the master receiver mode.
4. A data byte has been received while the I<sup>2</sup>C is in the addressed slave receiver mode.

The AA bit can be cleared by writing 1 to the AAC bit in the CONCLR register. When AA is 0, a not acknowledge (HIGH level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations:

1. A data byte has been received while the I<sup>2</sup>C is in the master receiver mode.
2. A data byte has been received while the I<sup>2</sup>C is in the addressed slave receiver mode.

### 9.5.2 I<sup>2</sup>C Status register

Each I<sup>2</sup>C Status register reflects the condition of the corresponding I<sup>2</sup>C interface. The I<sup>2</sup>C Status register is Read-Only.

**Table 124. I<sup>2</sup>C Status register (STAT, address 0x4000 0004) bit description**

Bit	Symbol	Description	Reset value
2:0	-	These bits are unused and are always 0.	0
7:3	STATUS	These bits give the actual status information about the I <sup>2</sup> C interface.	0x1F
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

The three least significant bits are always 0. Taken as a byte, the status register contents represent a status code. There are 26 possible status codes. When the status code is 0xF8, there is no relevant information available and the SI bit is not set. All other 25 status codes correspond to defined I<sup>2</sup>C states. When any of these states entered, the SI bit will be set. For a complete list of status codes, refer to tables from [Table 137](#) to [Table 142](#).

### 9.5.3 I<sup>2</sup>C Data register

This register contains the data to be transmitted or the data just received. The CPU can read and write to this register only while it is not in the process of shifting a byte, when the SI bit is set. Data in DAT register remains stable as long as the SI bit is set. Data in DAT register is always shifted from right to left: the first bit to be transmitted is the MSB (bit 7), and after a byte has been received, the first bit of received data is located at the MSB of the DAT register.

**Table 125. I<sup>2</sup>C Data register (DAT, address 0x4000 0008) bit description**

Bit	Symbol	Description	Reset value
7:0	DATA	This register holds data values that have been received or are to be transmitted.	0
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

### 9.5.4 I<sup>2</sup>C Slave Address register 0

This register is readable and writable and are only used when an I<sup>2</sup>C interface is set to slave mode. In master mode, this register has no effect. The LSB of the ADR register is the General Call bit. When this bit is set, the General Call address (0x00) is recognized.

If this register contains 0x00, the I<sup>2</sup>C will not acknowledge any address on the bus. All four registers (ADR0 to ADR3) will be cleared to this disabled state on reset. See also [Table 132](#).

**Table 126. I<sup>2</sup>C Slave Address register 0 (ADR0, address 0x4000 000C) bit description**

Bit	Symbol	Description	Reset value
0	GC	General Call enable bit.	0
7:1	ADDRESS	The I <sup>2</sup> C device address for slave mode.	0x00
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

### 9.5.5 I<sup>2</sup>C SCL HIGH and LOW duty cycle registers

**Table 127. I<sup>2</sup>C SCL HIGH Duty Cycle register (SCLH, address 0x4000 0010) bit description**

Bit	Symbol	Description	Reset value
15:0	SCLH	Count for SCL HIGH time period selection.	0x0004
31:16	-	Reserved. The value read from a reserved bit is not defined.	-

**Table 128. I<sup>2</sup>C SCL Low duty cycle register (SCLL, address 0x4000 0014) bit description**

Bit	Symbol	Description	Reset value
15:0	SCLL	Count for SCL low time period selection.	0x0004
31:16	-	Reserved. The value read from a reserved bit is not defined.	-

#### 9.5.5.1 Selecting the appropriate I<sup>2</sup>C data rate and duty cycle

Software must set values for the registers SCLH and SCLL to select the appropriate data rate and duty cycle. SCLH defines the number of I2C\_PCLK cycles for the SCL HIGH time, SCLL defines the number of I2C\_PCLK cycles for the SCL low time. The frequency is determined by the following formula (I2C\_PCLK is the frequency of the peripheral I2C clock):

(2)

$$I^2C_{bitfrequency} = \frac{I2CPCLK}{SCLH + SCLL}$$

The values for SCLL and SCLH must ensure that the data rate is in the appropriate I<sup>2</sup>C data rate range. Each register value must be greater than or equal to 4. [Table 129](#) gives some examples of I<sup>2</sup>C-bus rates based on I2C\_PCLK frequency and SCLL and SCLH values.

Table 129. SCLL + SCLH values for selected I<sup>2</sup>C clock values

I <sup>2</sup> C mode	I <sup>2</sup> C bit frequency	I <sup>2</sup> C_PCLK (MHz)								
		6	8	10	12	16	20	30	40	50
		SCLH + SCLL								
Standard mode	100 kHz	60	80	100	120	160	200	300	400	500
Fast-mode	400 kHz	15	20	25	30	40	50	75	100	125
Fast-mode Plus	1 MHz	-	8	10	12	16	20	30	40	50

SCLL and SCLH values should not necessarily be the same. Software can set different duty cycles on SCL by setting these two registers. For example, the I<sup>2</sup>C-bus specification defines the SCL low time and high time at different values for a Fast-mode and Fast-mode Plus I<sup>2</sup>C.

### 9.5.6 I<sup>2</sup>C Control Clear register

The CONCLR register control clearing of bits in the CON register that controls operation of the I<sup>2</sup>C interface. Writing a one to a bit of this register causes the corresponding bit in the I<sup>2</sup>C control register to be cleared. Writing a zero has no effect.

Table 130. I<sup>2</sup>C Control Clear register (CONCLR, address 0x4000 0018) bit description

Bit	Symbol	Description	Reset value
1:0	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	AAC	Assert acknowledge Clear bit.	
3	SIC	I <sup>2</sup> C interrupt Clear bit.	0
4	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
5	STAC	START flag Clear bit.	0
6	I2ENC	I <sup>2</sup> C interface Disable bit.	0
7	-	Reserved. User software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
31:8	-	Reserved. The value read from a reserved bit is not defined.	-

**AAC** is the Assert Acknowledge Clear bit. Writing a 1 to this bit clears the AA bit in the CONSET register. Writing 0 has no effect.

**SIC** is the I<sup>2</sup>C Interrupt Clear bit. Writing a 1 to this bit clears the SI bit in the CONSET register. Writing 0 has no effect.

**STAC** is the START flag Clear bit. Writing a 1 to this bit clears the STA bit in the CONSET register. Writing 0 has no effect.

**I2ENC** is the I<sup>2</sup>C Interface Disable bit. Writing a 1 to this bit clears the I2EN bit in the CONSET register. Writing 0 has no effect.

### 9.5.7 I<sup>2</sup>C Monitor mode control register

This register controls the Monitor mode which allows the I<sup>2</sup>C module to monitor traffic on the I<sup>2</sup>C bus without actually participating in traffic or interfering with the I<sup>2</sup>C bus.

Table 131. I<sup>2</sup>C Monitor mode control register (MMCTRL, address 0x4000 001C) bit description

Bit	Symbol	Value	Description	Reset value
0	MM_ENA		Monitor mode enable.	0
		0	Disable. Monitor mode disabled.	
		1	Enabled. The I <sup>2</sup> C module will enter monitor mode. In this mode the SDA output will be forced high. This will prevent the I <sup>2</sup> C module from outputting data of any kind (including ACK) onto the I <sup>2</sup> C data bus. Depending on the state of the ENA_SCL bit, the output may be also forced high, preventing the module from having control over the I <sup>2</sup> C clock line.	
1	ENA_SCL		SCL output enable.	0
		0	High. When this bit is cleared to 0, the SCL output will be forced high when the module is in monitor mode. As described above, this will prevent the module from having any control over the I <sup>2</sup> C clock line.	
		1	Stretch. When this bit is set, the I <sup>2</sup> C module may exercise the same control over the clock line that it would in normal operation. This means that, acting as a slave peripheral, the I <sup>2</sup> C module can stretch the clock line (hold it low) until it has had time to respond to an I <sup>2</sup> C interrupt. When the ENA_SCL bit is cleared and the I <sup>2</sup> C no longer has the ability to stall the bus, interrupt response time becomes important. To give the part more time to respond to an I <sup>2</sup> C interrupt under these conditions, a DATA_BUFFER register is used to hold received data for a full 9-bit word transmission time.	
2	MATCH_ALL		Select interrupt register match.	0
		0	Match address. When this bit is cleared, an interrupt will only be generated when a match occurs to one of the (up-to) four address registers described above. That is, the module will respond as a normal slave as far as address-recognition is concerned.	
		1	Any address. When this bit is set to 1 and the I <sup>2</sup> C is in monitor mode, an interrupt will be generated on ANY address received. This will enable the part to monitor all traffic on the bus.	
31:3	-	-	Reserved. The value read from reserved bits is not defined.	

**Remark:** The ENA\_SCL and MATCH\_ALL bits have no effect if the MM\_ENA is 0 (i.e. if the module is NOT in monitor mode).

### 9.5.7.1 Interrupt in Monitor mode

All interrupts will occur as normal when the module is in monitor mode. This means that the first interrupt will occur when an address-match is detected (any address received if the MATCH\_ALL bit is set, otherwise an address matching one of the four address registers).

Subsequent to an address-match detection, interrupts will be generated after each data byte is received for a slave-write transfer, or after each byte that the module “thinks” it has transmitted for a slave-read transfer. In this second case, the data register will actually contain data transmitted by some other slave on the bus which was actually addressed by the master.

Following all of these interrupts, the processor may read the data register to see what was actually transmitted on the bus.

### 9.5.7.2 Loss of arbitration in Monitor mode

In monitor mode, the I<sup>2</sup>C module will not be able to respond to a request for information by the bus master or issue an ACK). Some other slave on the bus will respond instead. This will most probably result in a lost-arbitration state as far as our module is concerned.

Software should be aware of the fact that the module is in monitor mode and should not respond to any loss of arbitration state that is detected. In addition, hardware may be designed into the module to block some/all loss of arbitration states from occurring if those state would either prevent a desired interrupt from occurring or cause an unwanted interrupt to occur. Whether any such hardware will be added is still to be determined.

### 9.5.8 I<sup>2</sup>C Slave Address registers

These registers are readable and writable and are only used when an I<sup>2</sup>C interface is set to slave mode. In master mode, this register has no effect. The LSB of the ADR register is the General Call bit. When this bit is set, the General Call address (0x00) is recognized.

If these registers contain 0x00, the I<sup>2</sup>C will not acknowledge any address on the bus. All four registers will be cleared to this disabled state on reset (also see [Table 126](#)).

**Table 132. I<sup>2</sup>C Slave Address registers (ADR[1:3], address 0x4000 0020 (ADR1) to 0x4000 0028 (ADR3)) bit description**

Bit	Symbol	Description	Reset value
0	GC	General Call enable bit.	0
7:1	ADDRESS	The I <sup>2</sup> C device address for slave mode.	0x00
31:8	-	Reserved. The value read from a reserved bit is not defined.	0

### 9.5.9 I<sup>2</sup>C Data buffer register

In monitor mode, the I<sup>2</sup>C module may lose the ability to stretch the clock (stall the bus) if the ENA\_SCL bit is not set. This means that the processor will have a limited amount of time to read the contents of the data received on the bus. If the processor reads the DAT shift register, as it ordinarily would, it could have only one bit-time to respond to the interrupt before the received data is overwritten by new data.

To give the processor more time to respond, a new 8-bit, read-only DATA\_BUFFER register will be added. The contents of the 8 MSBs of the DAT shift register will be transferred to the DATA\_BUFFER automatically after every nine bits (8 bits of data plus ACK or NACK) has been received on the bus. This means that the processor will have nine bit transmission times to respond to the interrupt and read the data before it is overwritten.



The processor will still have the ability to read the DAT register directly, as usual, and the behavior of DAT will not be altered in any way.

Although the DATA\_BUFFER register is primarily intended for use in monitor mode with the ENA\_SCL bit = '0', it will be available for reading at any time under any mode of operation.

**Table 133. I<sup>2</sup>C Data buffer register (DATA\_BUFFER, address 0x4000 002C) bit description**

Bit	Symbol	Description	Reset value
7:0	DATA	This register holds contents of the 8 MSBs of the DAT shift register.	0
31:8	-	Reserved. The value read from a reserved bit is not defined.	0

### 9.5.10 I<sup>2</sup>C Mask registers

The four mask registers each contain seven active bits (7:1). Any bit in these registers which is set to '1' will cause an automatic compare on the corresponding bit of the received address when it is compared to the ADRn register associated with that mask register. In other words, bits in an ADRn register which are masked are not taken into account in determining an address match.

On reset, all mask register bits are cleared to '0'.

The mask register has no effect on comparison to the General Call address ("0000000").

Bits(31:8) and bit(0) of the mask registers are unused and should not be written to. These bits will always read back as zeros.

When an address-match interrupt occurs, the processor will have to read the data register (DAT) to determine what the received address was that actually caused the match.

**Table 134. I<sup>2</sup>C Mask registers (MASK[0:3], 0x4000 0030 (MASK0) to 0x4000 003C (MASK3)) bit description**

Bit	Symbol	Description	Reset value
0	-	Reserved. User software should not write ones to reserved bits. This bit reads always back as 0.	0
7:1	MASK	Mask bits.	0x00
31:8	-	Reserved. The value read from reserved bits is undefined.	0

## 9.6 Functional description

### 9.6.1 Details of I<sup>2</sup>C operating modes

The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter



Data transfers in each mode of operation are shown in [Figure 18](#), [Figure 19](#), [Figure 20](#), [Figure 21](#), and [Figure 22](#). [Table 135](#) lists abbreviations used in these figures when describing the I<sup>2</sup>C operating modes.

**Table 135. Abbreviations used to describe an I<sup>2</sup>C operation**

Abbreviation	Explanation
S	START Condition
SLA	7-bit slave address
R	Read bit (HIGH level at SDA)
W	Write bit (LOW level at SDA)
A	Acknowledge bit (LOW level at SDA)
$\bar{A}$	Not acknowledge bit (HIGH level at SDA)
Data	8-bit data byte
P	STOP condition

In [Figure 18](#) to [Figure 22](#), circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in the STAT register. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When a serial interrupt routine is entered, the status code in STAT is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in tables from [Table 137](#) to [Table 143](#).

### 9.6.1.1 Master Transmitter mode

In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see [Figure 18](#)). Before the master transmitter mode can be entered, I2CON must be initialized as follows:

**Table 136. CONSET used to initialize Master Transmitter mode**

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	x	-	-

The I<sup>2</sup>C rate must also be configured in the SCLL and SCLH registers. I2EN must be set to logic 1 to enable the I<sup>2</sup>C block. If the AA bit is reset, the I<sup>2</sup>C block will not acknowledge its own slave address or the General Call address in the event of another device becoming master of the bus. In other words, if AA is reset, the I<sup>2</sup>C interface cannot enter slave mode. STA, STO, and SI must be reset.

The master transmitter mode may now be entered by setting the STA bit. The I<sup>2</sup>C logic will now test the I<sup>2</sup>C-bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI) is set, and the status code in the status register (STAT) will be 0x08. This status code is used by the interrupt service routine to enter the appropriate state service routine that loads DAT with the slave address and the data direction bit (SLA+W). The SI bit in CON must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in STAT are possible. There are 0x18, 0x20, or 0x38 for the master mode and also 0x68, 0x78, or 0xB0 if the slave mode was enabled (AA = logic 1). The appropriate action to be taken for each of these status codes is detailed in [Table 137](#). After a Repeated START condition (state 0x10). The I<sup>2</sup>C block may switch to the master receiver mode by loading DAT with SLA+R).

Table 137. Master Transmitter mode

Status Code (I2CSTAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Load SLA+W; clear STA	X	0	0	X	SLA+W will be transmitted; ACK bit will be received.
0x10	A Repeated START condition has been transmitted.	Load SLA+W or	X	0	0	X	As above.
		Load SLA+R; Clear STA	X	0	0	X	SLA+R will be transmitted; the I <sup>2</sup> C block will be switched to MST/REC mode.
0x18	SLA+W has been transmitted; ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x20	SLA+W has been transmitted; NOT ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x28	Data byte in DAT has been transmitted; ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x30	Data byte in DAT has been transmitted; NOT ACK has been received.	Load data byte or	0	0	0	X	Data byte will be transmitted; ACK bit will be received.
		No DAT action or	1	0	0	X	Repeated START will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x38	Arbitration lost in SLA+R/W or Data bytes.	No DAT action or	0	0	0	X	I <sup>2</sup> C-bus will be released; not addressed slave will be entered.
		No DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

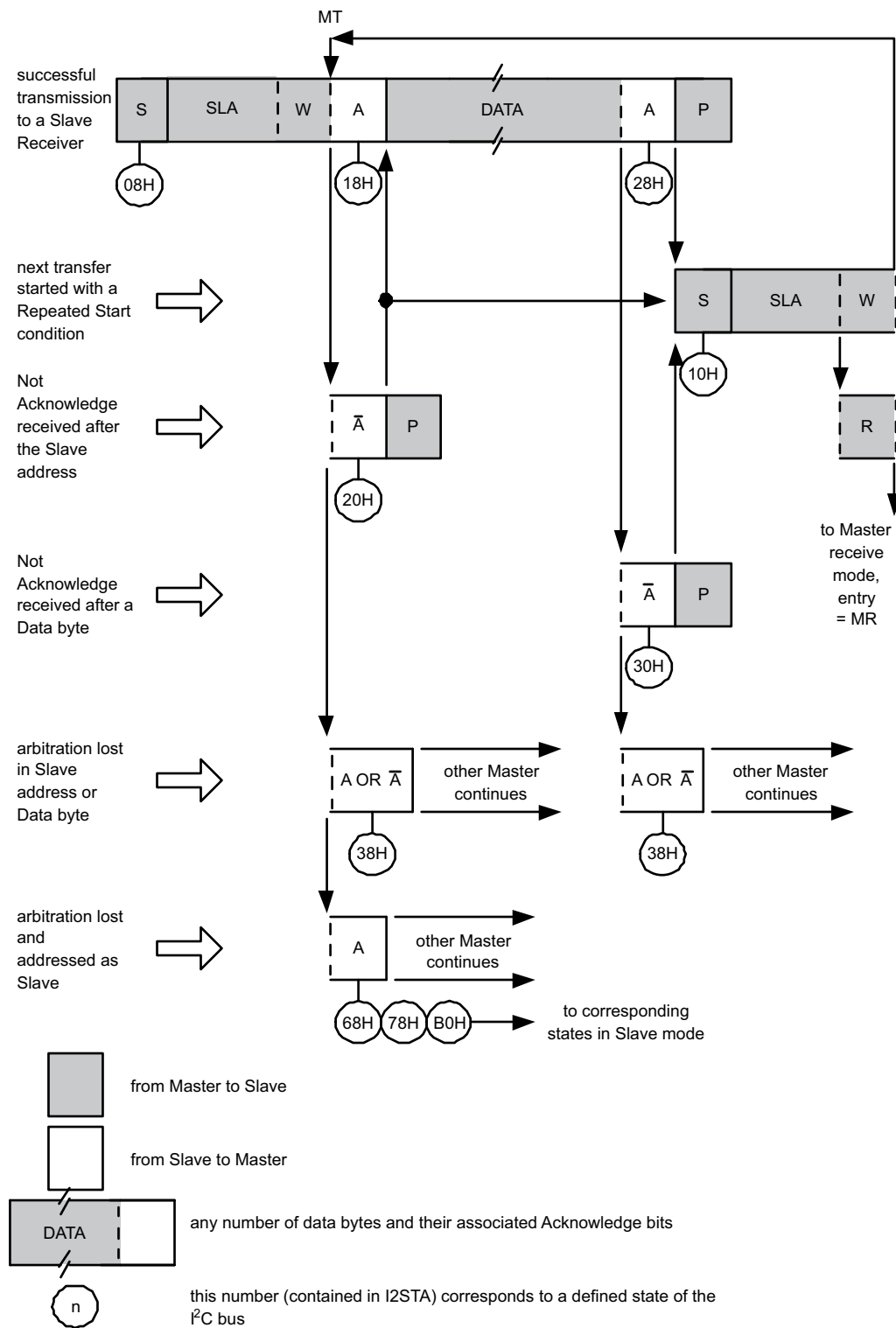


Fig 18. Format and states in the Master Transmitter mode

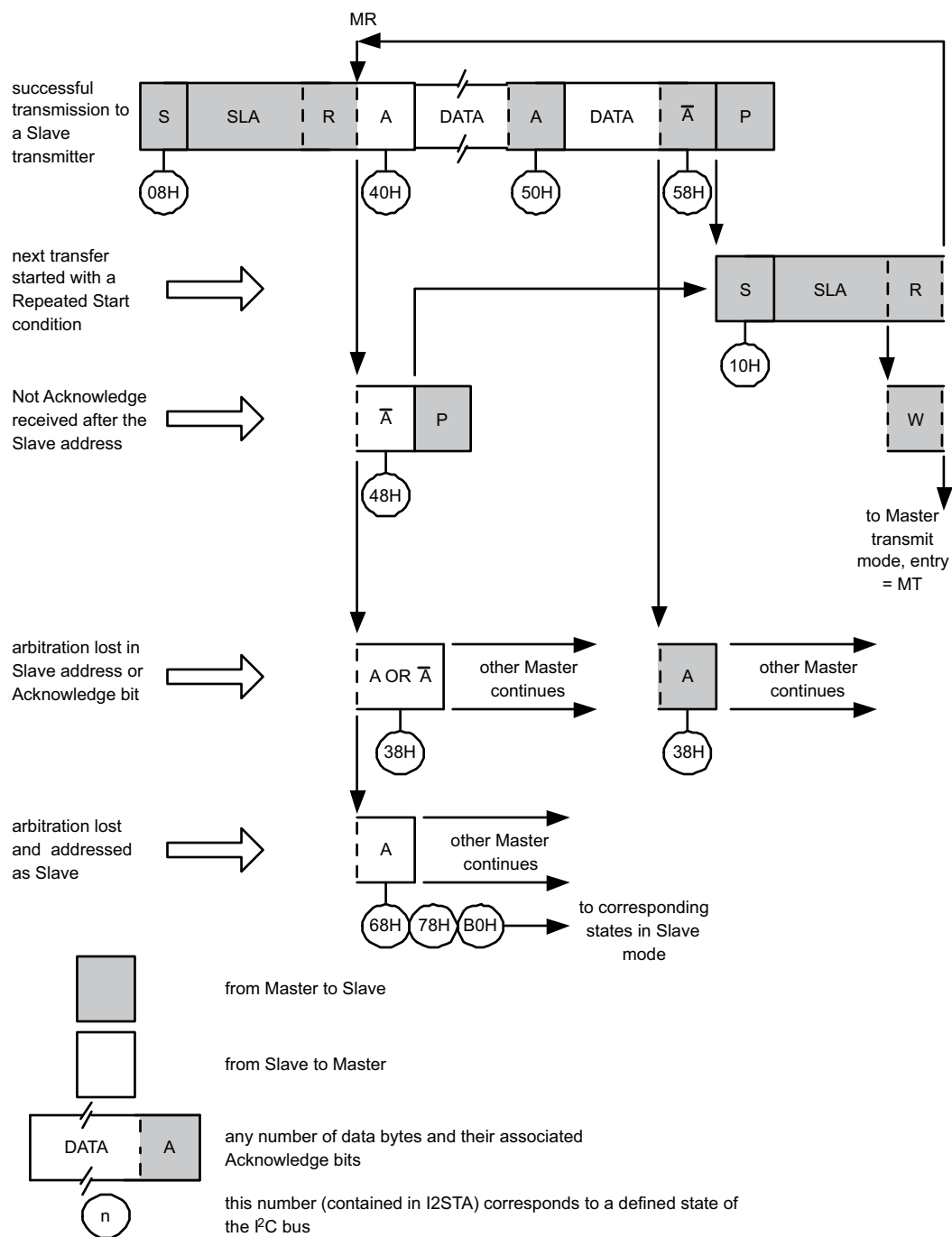
### 9.6.1.2 Master Receiver mode

In the master receiver mode, a number of data bytes are received from a slave transmitter (see [Figure 19](#)). The transfer is initialized as in the master transmitter mode. When the START condition has been transmitted, the interrupt service routine must load DAT with the 7-bit slave address and the data direction bit (SLA+R). The SI bit in CON must then be cleared before the serial transfer can continue.

When the slave address and the data direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag (SI) is set again, and a number of status codes in STAT are possible. These are 0x40, 0x48, or 0x38 for the master mode and also 0x68, 0x78, or 0xB0 if the slave mode was enabled (AA = 1). The appropriate action to be taken for each of these status codes is detailed in [Table 138](#). After a Repeated START condition (state 0x10), the I<sup>2</sup>C block may switch to the master transmitter mode by loading DAT with SLA+W.

Table 138. Master Receiver mode

Status Code (STAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Load SLA+R	X	0	0	X	SLA+R will be transmitted; ACK bit will be received.
0x10	A Repeated START condition has been transmitted.	Load SLA+R or	X	0	0	X	As above.
		Load SLA+W	X	0	0	X	SLA+W will be transmitted; the I <sup>2</sup> C block will be switched to MST/TRX mode.
0x38	Arbitration lost in NOT ACK bit.	No DAT action or	0	0	0	X	I <sup>2</sup> C-bus will be released; the I <sup>2</sup> C block will enter slave mode.
		No DAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.
0x40	SLA+R has been transmitted; ACK has been received.	No DAT action or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned.
		No DAT action	0	0	0	1	Data byte will be received; ACK bit will be returned.
0x48	SLA+R has been transmitted; NOT ACK has been received.	No DAT action or	1	0	0	X	Repeated START condition will be transmitted.
		No DAT action or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		No DAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.
0x50	Data byte has been received; ACK has been returned.	Read data byte or	0	0	0	0	Data byte will be received; NOT ACK bit will be returned.
		Read data byte	0	0	0	1	Data byte will be received; ACK bit will be returned.
0x58	Data byte has been received; NOT ACK has been returned.	Read data byte or	1	0	0	X	Repeated START condition will be transmitted.
		Read data byte or	0	1	0	X	STOP condition will be transmitted; STO flag will be reset.
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted; STO flag will be reset.



**Fig 19. Format and states in the Master Receiver mode**

### 9.6.1.3 Slave Receiver mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (see [Figure 20](#)). To initiate the slave receiver mode, ADR and CON must be loaded as follows:

**Table 139. ADR usage in Slave Receiver mode**

Bit	7	6	5	4	3	2	1	0
Symbol	own slave 7-bit address							GC

The upper 7 bits are the address to which the I<sup>2</sup>C block will respond when addressed by a master. If the LSB (GC) is set, the I<sup>2</sup>C block will respond to the General Call address (0x00); otherwise it ignores the General Call address.

**Table 140. CONSET used to initialize Slave Receiver mode**

Bit	7	6	5	4	3	2	1	0
Symbol	-	I2EN	STA	STO	SI	AA	-	-
Value	-	1	0	0	0	1	-	-

The I<sup>2</sup>C-bus rate settings do not affect the I<sup>2</sup>C block in the slave mode. I2EN must be set to logic 1 to enable the I<sup>2</sup>C block. The AA bit must be set to enable the I<sup>2</sup>C block to acknowledge its own slave address or the General Call address. STA, STO, and SI must be reset.

When ADR and CON have been initialized, the I<sup>2</sup>C block waits until it is addressed by its own slave address followed by the data direction bit which must be “0” (W) for the I<sup>2</sup>C block to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from STAT. This status code is used to vector to a state service routine. The appropriate action to be taken for each of these status codes is detailed in [Table 141](#). The slave receiver mode may also be entered if arbitration is lost while the I<sup>2</sup>C block is in the master mode (see status 0x68 and 0x78).

If the AA bit is reset during a transfer, the I<sup>2</sup>C block will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, the I<sup>2</sup>C block does not respond to its own slave address or a General Call address. However, the I<sup>2</sup>C-bus is still monitored and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate the I<sup>2</sup>C block from the I<sup>2</sup>C-bus.

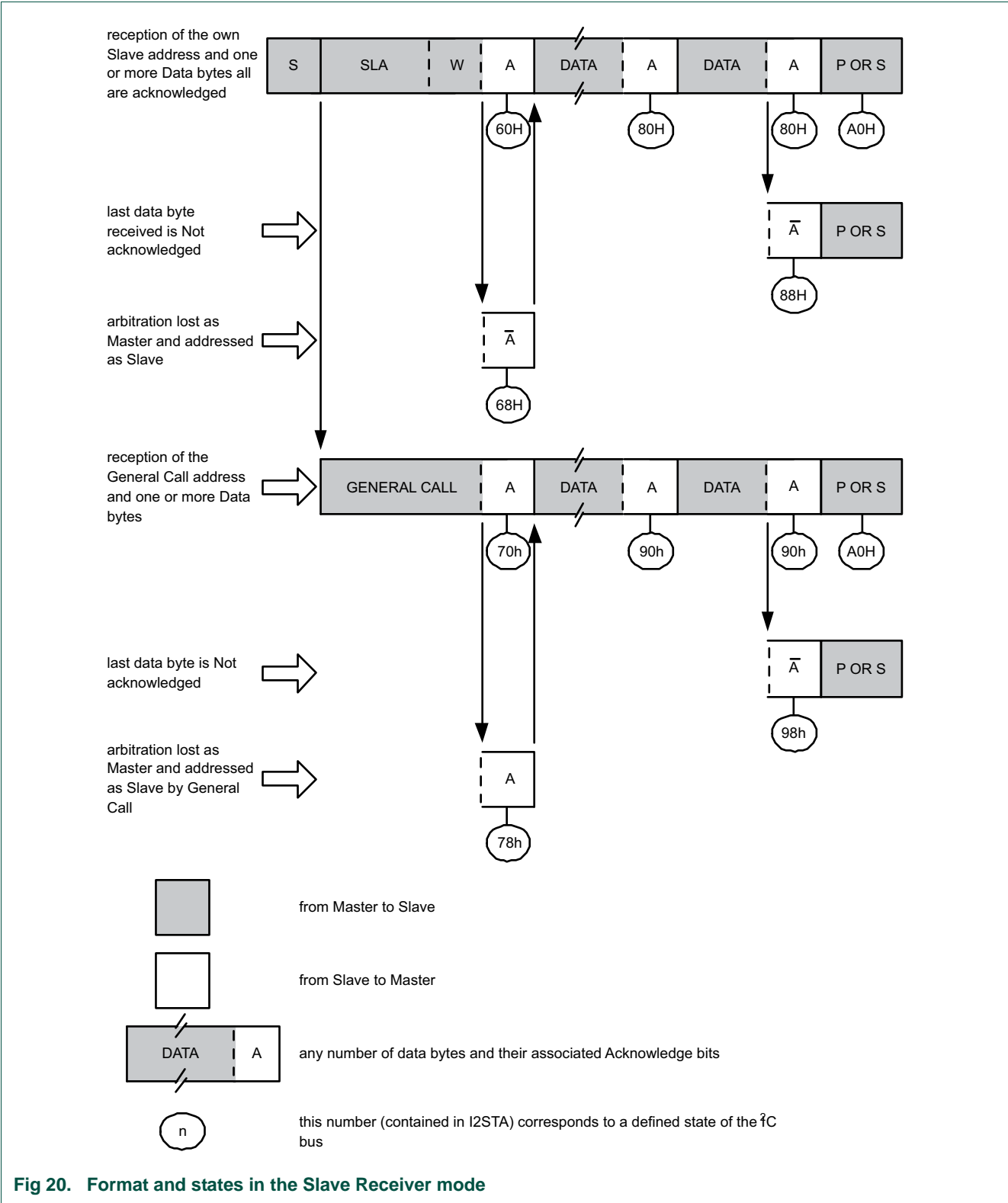


Table 141. Slave Receiver mode

Status Code (STAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x60	Own SLA+W has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master; Own SLA+W has been received, ACK returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (0x00) has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master; General call address has been received, ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address; DATA has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA; DATA byte has been received; NOT ACK has been returned.	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		Read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		Read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with General Call; DATA byte has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.

Table 141. Slave Receiver mode ...continued

Status Code (STAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x98	Previously addressed with General Call; DATA byte has been received; NOT ACK has been returned.	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		Read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		Read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0xA0	A STOP condition or Repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.	No STDAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No STDAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No STDAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No STDAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.



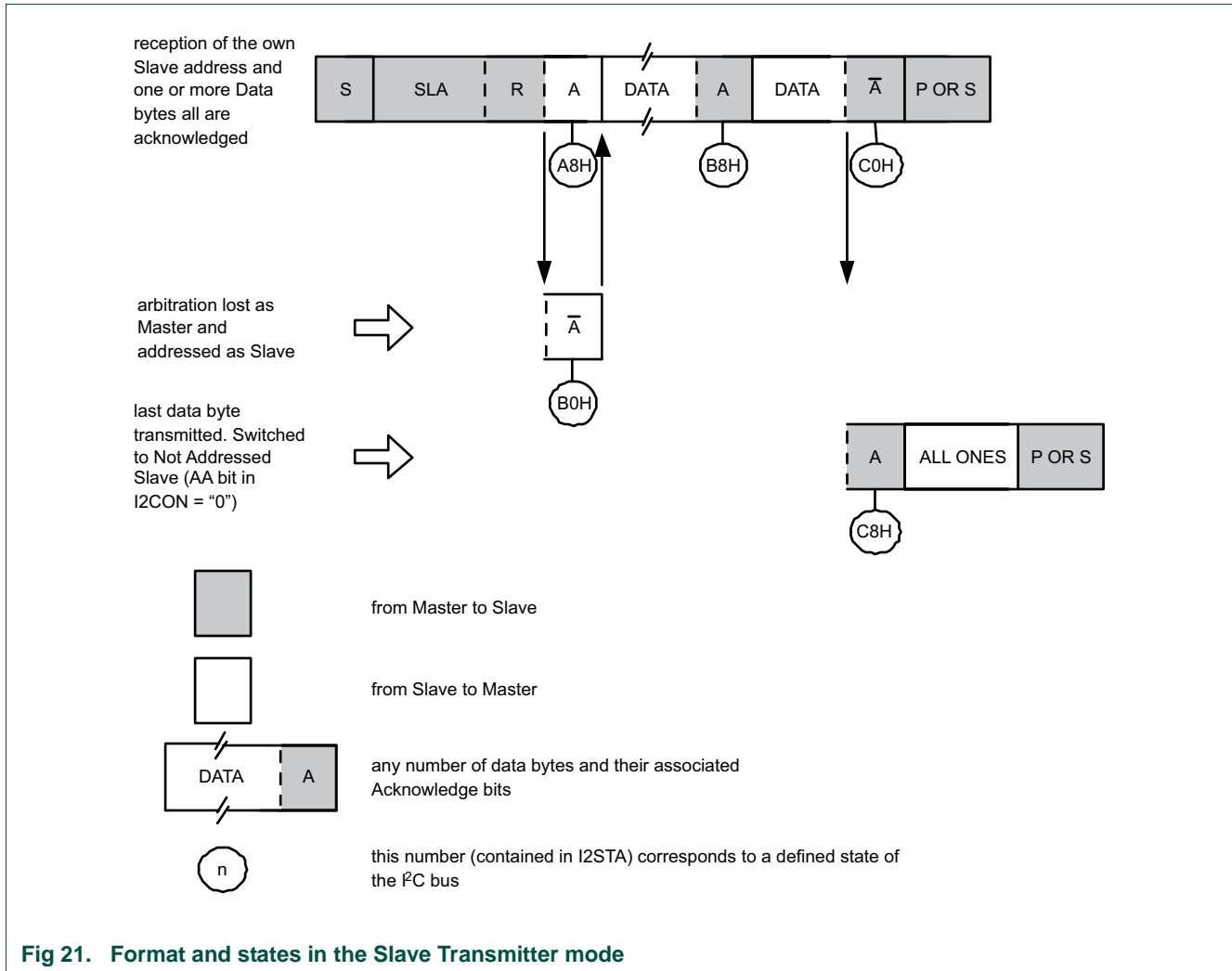
#### 9.6.1.4 Slave Transmitter mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see [Figure 21](#)). Data transfer is initialized as in the slave receiver mode. When ADR and CON have been initialized, the I<sup>2</sup>C block waits until it is addressed by its own slave address followed by the data direction bit which must be “1” (R) for the I<sup>2</sup>C block to operate in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag (SI) is set and a valid status code can be read from STAT. This status code is used to vector to a state service routine, and the appropriate action to be taken for each of these status codes is detailed in [Table 142](#). The slave transmitter mode may also be entered if arbitration is lost while the I<sup>2</sup>C block is in the master mode (see state 0xB0).

If the AA bit is reset during a transfer, the I<sup>2</sup>C block will transmit the last byte of the transfer and enter state 0xC0 or 0xC8. The I<sup>2</sup>C block is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all 1s as serial data. While AA is reset, the I<sup>2</sup>C block does not respond to its own slave address or a General Call address. However, the I<sup>2</sup>C-bus is still monitored, and address recognition may be resumed at any time by setting AA. This means that the AA bit may be used to temporarily isolate the I<sup>2</sup>C block from the I<sup>2</sup>C-bus.

Table 142. Slave Transmitter mode

Status Code (STAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0xA8	Own SLA+R has been received; ACK has been returned.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
0xB0	Arbitration lost in SLA+R/W as master; Own SLA+R has been received, ACK has been returned.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received.
0xB8	Data byte in DAT has been transmitted; ACK has been received.	Load data byte or	X	0	0	0	Last data byte will be transmitted and ACK bit will be received.
		Load data byte	X	0	0	1	Data byte will be transmitted; ACK bit will be received.
0xC0	Data byte in DAT has been transmitted; NOT ACK has been received.	No DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No DAT action	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0xC8	Last data byte in DAT has been transmitted (AA = 0); ACK has been received.	No DAT action or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		No DAT action or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		No DAT action or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		No DAT action	1	0	0	01	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR.0 = logic 1. A START condition will be transmitted when the bus becomes free.



### 9.6.1.5 Miscellaneous states

There are two STAT codes that do not correspond to a defined I<sup>2</sup>C hardware state (see [Table 143](#)). These are discussed below.

#### 9.6.1.5.1 STAT = 0xF8

This status code indicates that no relevant information is available because the serial interrupt flag, SI, is not yet set. This occurs between other states and when the I<sup>2</sup>C block is not involved in a serial transfer.

#### 9.6.1.5.2 STAT = 0x00

This status code indicates that a bus error has occurred during an I<sup>2</sup>C serial transfer. A bus error is caused when a START or STOP condition occurs at an illegal position in the format frame. Examples of such illegal positions are during the serial transfer of an address byte, a data byte, or an acknowledge bit. A bus error may also be caused when external interference disturbs the internal I<sup>2</sup>C block signals. When a bus error occurs, SI is set. To recover from a bus error, the STO flag must be set and SI must be cleared. This

causes the I<sup>2</sup>C block to enter the “not addressed” slave mode (a defined state) and to clear the STO flag (no other bits in CON are affected). The SDA and SCL lines are released (a STOP condition is not transmitted).

**Table 143. Miscellaneous States**

Status Code (STAT)	Status of the I <sup>2</sup> C-bus and hardware	Application software response					Next action taken by I <sup>2</sup> C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0xF8	No relevant state information available; SI = 0.	No DAT action	No CON action				Wait or proceed current transfer.
0x00	Bus error during MST or selected slave modes, due to an illegal START or STOP condition. State 0x00 can also occur when interference causes the I <sup>2</sup> C block to enter an undefined state.	No DAT action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and the I <sup>2</sup> C block is switched to the not addressed SLV mode. STO is reset.

#### 9.6.1.6 Some special cases

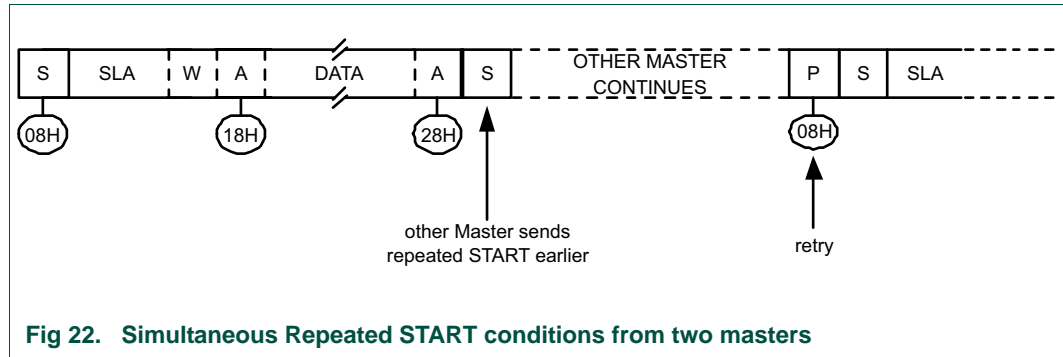
The I<sup>2</sup>C hardware has facilities to handle the following special cases that may occur during a serial transfer:

- Simultaneous Repeated START conditions from two masters.
- Data transfer after loss of arbitration.
- Forced access to the I<sup>2</sup>C-bus.
- I<sup>2</sup>C-bus obstructed by a LOW level on SCL or SDA.
- Bus error.

##### 9.6.1.6.1 Simultaneous Repeated START conditions from two masters

A Repeated START condition may be generated in the master transmitter or master receiver modes. A special case occurs if another master simultaneously generates a Repeated START condition (see [Figure 22](#)). Until this occurs, arbitration is not lost by either master since they were both transmitting the same data.

If the I<sup>2</sup>C hardware detects a Repeated START condition on the I<sup>2</sup>C-bus before generating a Repeated START condition itself, it will release the bus, and no interrupt request is generated. If another master frees the bus by generating a STOP condition, the I<sup>2</sup>C block will transmit a normal START condition (state 0x08), and a retry of the total serial data transfer can commence.



#### 9.6.1.6.2 Data transfer after loss of arbitration

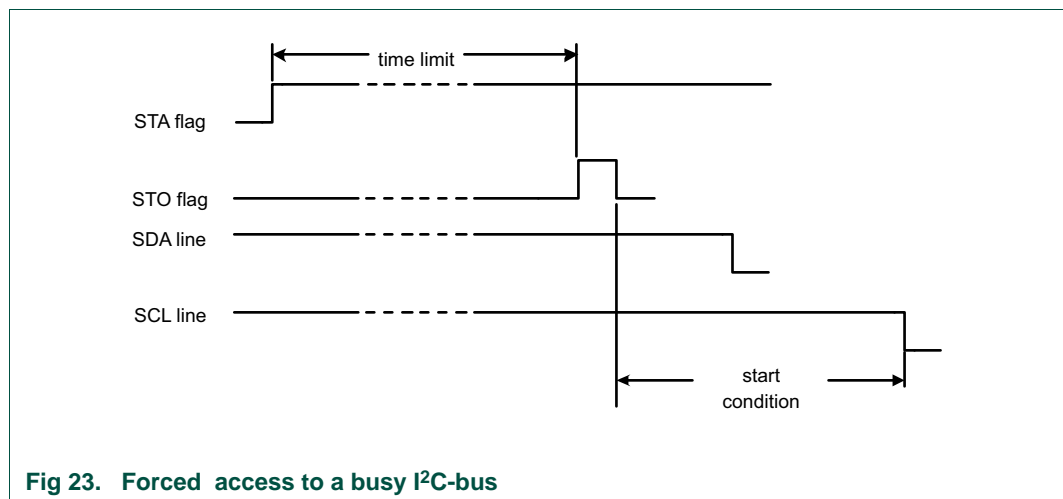
Arbitration may be lost in the master transmitter and master receiver modes (see [Figure 10](#)). Loss of arbitration is indicated by the following states in STAT; 0x38, 0x68, 0x78, and 0xB0 (see [Figure 18](#) and [Figure 19](#)).

If the STA flag in CON is set by the routines which service these states, then, if the bus is free again, a START condition (state 0x08) is transmitted without intervention by the CPU, and a retry of the total serial transfer can commence.

#### 9.6.1.6.3 Forced access to the I<sup>2</sup>C-bus

In some applications, it may be possible for an uncontrolled source to cause a bus hang-up. In such situations, the problem may be caused by interference, temporary interruption of the bus or a temporary short-circuit between SDA and SCL.

If an uncontrolled source generates a superfluous START or masks a STOP condition, then the I<sup>2</sup>C-bus stays busy indefinitely. If the STA flag is set and bus access is not obtained within a reasonable amount of time, then a forced access to the I<sup>2</sup>C-bus is possible. This is achieved by setting the STO flag while the STA flag is still set. No STOP condition is transmitted. The I<sup>2</sup>C hardware behaves as if a STOP condition was received and is able to transmit a START condition. The STO flag is cleared by hardware (see [Figure 23](#)).

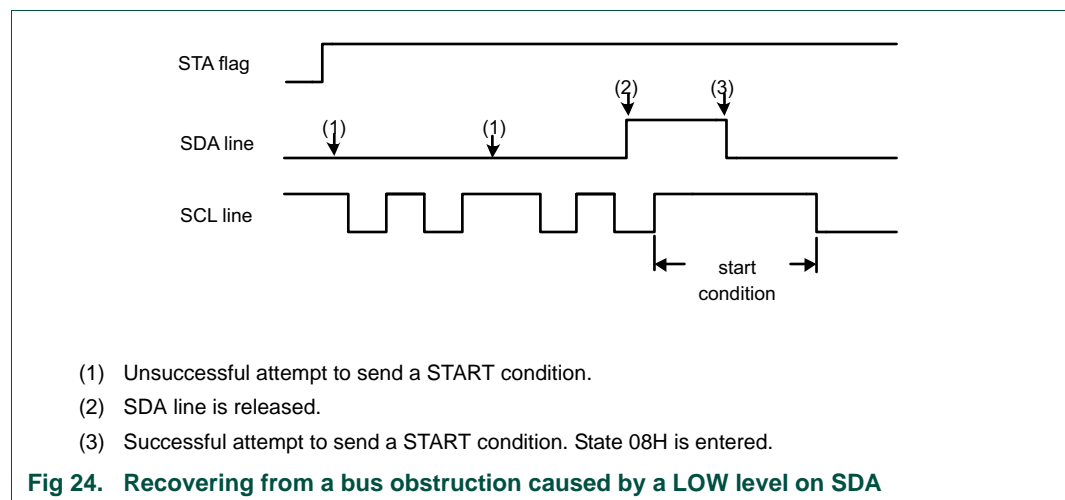




#### 9.6.1.6.4 I<sup>2</sup>C-bus obstructed by a LOW level on SCL or SDA

An I<sup>2</sup>C-bus hang-up can occur if either the SDA or SCL line is held LOW by any device on the bus. If the SCL line is obstructed (pulled LOW) by a device on the bus, no further serial transfer is possible, and the problem must be resolved by the device that is pulling the SCL bus line LOW.

Typically, the SDA line may be obstructed by another device on the bus that has become out of synchronization with the current bus master by either missing a clock, or by sensing a noise pulse as a clock. In this case, the problem can be solved by transmitting additional clock pulses on the SCL line (see [Figure 24](#)). The I<sup>2</sup>C interface does not include a dedicated time-out timer to detect an obstructed bus, but this can be implemented using another timer in the system. When detected, software can force clocks (up to 9 may be required) on SCL until SDA is released by the offending device. At that point, the slave may still be out of synchronization, so a START should be generated to insure that all I<sup>2</sup>C peripherals are synchronized.



#### 9.6.1.6.5 Bus error

A bus error occurs when a START or STOP condition is detected at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data bit, or an acknowledge bit.

The I<sup>2</sup>C hardware only reacts to a bus error when it is involved in a serial transfer either as a master or an addressed slave. When a bus error is detected, the I<sup>2</sup>C block immediately switches to the not addressed slave mode, releases the SDA and SCL lines, sets the interrupt flag, and loads the status register with 0x00. This status code may be used to vector to a state service routine which either attempts the aborted serial transfer again or simply recovers from the error condition as shown in [Table 143](#).

### 9.6.1.7 I<sup>2</sup>C state service routines

This section provides examples of operations that must be performed by various I<sup>2</sup>C state service routines. This includes:

- Initialization of the I<sup>2</sup>C block after a Reset.
- I<sup>2</sup>C Interrupt Service.
- The 26 state service routines providing support for all four I<sup>2</sup>C operating modes.

### 9.6.1.8 Initialization

In the initialization example, the I<sup>2</sup>C block is enabled for both master and slave modes. For each mode, a buffer is used for transmission and reception. The initialization routine performs the following functions:

- ADR is loaded with the part's own slave address and the General Call bit (GC).
- The I<sup>2</sup>C interrupt enable and interrupt priority bits are set.
- The slave mode is enabled by simultaneously setting the I2EN and AA bits in CON and the serial clock frequency (for master modes) is defined by loading the SCLH and SCLL registers. The master routines must be started in the main program.

The I<sup>2</sup>C hardware now begins checking the I<sup>2</sup>C-bus for its own slave address and General Call. If the General Call or the own slave address is detected, an interrupt is requested and STAT is loaded with the appropriate state information.

### 9.6.1.9 I<sup>2</sup>C interrupt service

When the I<sup>2</sup>C interrupt is entered, STAT contains a status code which identifies one of the 26 state services to be executed.

### 9.6.1.10 The state service routines

Each state routine is part of the I<sup>2</sup>C interrupt routine and handles one of the 26 states.

### 9.6.1.11 Adapting state services to an application

The state service examples show the typical actions that must be performed in response to the 26 I<sup>2</sup>C state codes. If one or more of the four I<sup>2</sup>C operating modes are not used, the associated state services can be omitted, as long as care is taken that those states can never occur.

In an application, it may be desirable to implement some kind of time-out during I<sup>2</sup>C operations, in order to trap an inoperative bus or a lost service routine.

## 9.6.2 Software example

### 9.6.2.1 Initialization routine

Example to initialize I<sup>2</sup>C Interface as a Slave and/or Master.

1. Load ADR with own Slave Address, enable General Call recognition if needed.
2. Enable I<sup>2</sup>C interrupt.
3. Write 0x44 to CONSET to set the I2EN and AA bits, enabling Slave functions. For Master only functions, write 0x40 to CONSET.

### 9.6.2.2 Start Master Transmit function

Begin a Master Transmit operation by setting up the buffer, pointer, and data count, then initiating a START.

1. Initialize Master data counter.
2. Set up the Slave Address to which data will be transmitted, and add the Write bit.

3. Write 0x20 to CONSET to set the STA bit.
4. Set up data to be transmitted in Master Transmit buffer.
5. Initialize the Master data counter to match the length of the message being sent.
6. Exit.

### 9.6.2.3 Start Master Receive function

Begin a Master Receive operation by setting up the buffer, pointer, and data count, then initiating a START.

1. Initialize Master data counter.
2. Set up the Slave Address to which data will be transmitted, and add the Read bit.
3. Write 0x20 to CONSET to set the STA bit.
4. Set up the Master Receive buffer.
5. Initialize the Master data counter to match the length of the message to be received.
6. Exit.

### 9.6.2.4 I<sup>2</sup>C interrupt routine

Determine the I<sup>2</sup>C state and which state routine will be used to handle it.

1. Read the I<sup>2</sup>C status from STA.
2. Use the status value to branch to one of 26 possible state routines.

### 9.6.2.5 Non mode specific states

#### 9.6.2.5.1 State: 0x00

Bus Error. Enter not addressed Slave mode and release bus.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

#### 9.6.2.5.2 Master States

State 08 and State 10 are for both Master Transmit and Master Receive modes. The R/W bit decides whether the next state is within Master Transmit mode or Master Receive mode.

#### 9.6.2.5.3 State: 0x08

A START condition has been transmitted. The Slave Address + R/W bit will be transmitted, an ACK bit will be received.

1. Write Slave Address with R/W bit to DAT.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Master Transmit mode data buffer.
5. Set up Master Receive mode data buffer.
6. Initialize Master data counter.

7. Exit.

#### 9.6.2.5.4 State: 0x10

A Repeated START condition has been transmitted. The Slave Address + R/W bit will be transmitted, an ACK bit will be received.

1. Write Slave Address with R/W bit to DAT.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Master Transmit mode data buffer.
5. Set up Master Receive mode data buffer.
6. Initialize Master data counter.
7. Exit.

#### 9.6.2.6 Master Transmitter states

##### 9.6.2.6.1 State: 0x18

Previous state was State 8 or State 10, Slave Address + Write has been transmitted, ACK has been received. The first data byte will be transmitted, an ACK bit will be received.

1. Load DAT with first data byte from Master Transmit buffer.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Increment Master Transmit buffer pointer.
5. Exit.

##### 9.6.2.6.2 State: 0x20

Slave Address + Write has been transmitted, NOT ACK has been received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

##### 9.6.2.6.3 State: 0x28

Data has been transmitted, ACK has been received. If the transmitted data was the last data byte then transmit a STOP condition, otherwise transmit the next data byte.

1. Decrement the Master data counter, skip to step 5 if not the last data byte.
2. Write 0x14 to CONSET to set the STO and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Exit.
5. Load DAT with next data byte from Master Transmit buffer.
6. Write 0x04 to CONSET to set the AA bit.
7. Write 0x08 to CONCLR to clear the SI flag.
8. Increment Master Transmit buffer pointer.

9. Exit.

#### 9.6.2.6.4 State: 0x30

Data has been transmitted, NOT ACK received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

#### 9.6.2.6.5 State: 0x38

Arbitration has been lost during Slave Address + Write or data. The bus has been released and not addressed Slave mode is entered. A new START condition will be transmitted when the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

### 9.6.2.7 Master Receive states

#### 9.6.2.7.1 State: 0x40

Previous state was State 08 or State 10. Slave Address + Read has been transmitted, ACK has been received. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

#### 9.6.2.7.2 State: 0x48

Slave Address + Read has been transmitted, NOT ACK has been received. A STOP condition will be transmitted.

1. Write 0x14 to CONSET to set the STO and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

#### 9.6.2.7.3 State: 0x50

Data has been received, ACK has been returned. Data will be read from DAT. Additional data will be received. If this is the last data byte then NOT ACK will be returned, otherwise ACK will be returned.

1. Read data byte from DAT into Master Receive buffer.
2. Decrement the Master data counter, skip to step 5 if not the last data byte.
3. Write 0x0C to CONCLR to clear the SI flag and the AA bit.
4. Exit.
5. Write 0x04 to CONSET to set the AA bit.
6. Write 0x08 to CONCLR to clear the SI flag.
7. Increment Master Receive buffer pointer.

8. Exit.

#### 9.6.2.7.4 State: 0x58

Data has been received, NOT ACK has been returned. Data will be read from DAT. A STOP condition will be transmitted.

1. Read data byte from DAT into Master Receive buffer.
2. Write 0x14 to CONSET to set the STO and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Exit.

### 9.6.2.8 Slave Receiver states

#### 9.6.2.8.1 State: 0x60

Own Slave Address + Write has been received, ACK has been returned. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit.

#### 9.6.2.8.2 State: 0x68

Arbitration has been lost in Slave Address and R/W bit as bus Master. Own Slave Address + Write has been received, ACK has been returned. Data will be received and ACK will be returned. STA is set to restart Master mode after the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit.

#### 9.6.2.8.3 State: 0x70

General call has been received, ACK has been returned. Data will be received and ACK returned.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit.

**9.6.2.8.4 State: 0x78**

Arbitration has been lost in Slave Address + R/W bit as bus Master. General call has been received and ACK has been returned. Data will be received and ACK returned. STA is set to restart Master mode after the bus is free again.

1. Write 0x24 to CONSET to set the STA and AA bits.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Set up Slave Receive mode data buffer.
4. Initialize Slave data counter.
5. Exit.

**9.6.2.8.5 State: 0x80**

Previously addressed with own Slave Address. Data has been received and ACK has been returned. Additional data will be read.

1. Read data byte from DAT into the Slave Receive buffer.
2. Decrement the Slave data counter, skip to step 5 if not the last data byte.
3. Write 0x0C to CONCLR to clear the SI flag and the AA bit.
4. Exit.
5. Write 0x04 to CONSET to set the AA bit.
6. Write 0x08 to CONCLR to clear the SI flag.
7. Increment Slave Receive buffer pointer.
8. Exit.

**9.6.2.8.6 State: 0x88**

Previously addressed with own Slave Address. Data has been received and NOT ACK has been returned. Received data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

**9.6.2.8.7 State: 0x90**

Previously addressed with General Call. Data has been received, ACK has been returned. Received data will be saved. Only the first data byte will be received with ACK. Additional data will be received with NOT ACK.

1. Read data byte from DAT into the Slave Receive buffer.
2. Write 0x0C to CONCLR to clear the SI flag and the AA bit.
3. Exit.

**9.6.2.8.8 State: 0x98**

Previously addressed with General Call. Data has been received, NOT ACK has been returned. Received data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.

2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

#### 9.6.2.8.9 State: 0xA0

A STOP condition or Repeated START has been received, while still addressed as a Slave. Data will not be saved. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

### 9.6.2.9 Slave Transmitter states

#### 9.6.2.9.1 State: 0xA8

Own Slave Address + Read has been received, ACK has been returned. Data will be transmitted, ACK bit will be received.

1. Load DAT from Slave Transmit buffer with first data byte.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Slave Transmit mode data buffer.
5. Increment Slave Transmit buffer pointer.
6. Exit.

#### 9.6.2.9.2 State: 0xB0

Arbitration lost in Slave Address and R/W bit as bus Master. Own Slave Address + Read has been received, ACK has been returned. Data will be transmitted, ACK bit will be received. STA is set to restart Master mode after the bus is free again.

1. Load DAT from Slave Transmit buffer with first data byte.
2. Write 0x24 to CONSET to set the STA and AA bits.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Set up Slave Transmit mode data buffer.
5. Increment Slave Transmit buffer pointer.
6. Exit.

#### 9.6.2.9.3 State: 0xB8

Data has been transmitted, ACK has been received. Data will be transmitted, ACK bit will be received.

1. Load DAT from Slave Transmit buffer with data byte.
2. Write 0x04 to CONSET to set the AA bit.
3. Write 0x08 to CONCLR to clear the SI flag.
4. Increment Slave Transmit buffer pointer.
5. Exit.



**9.6.2.9.4 State: 0xC0**

Data has been transmitted, NOT ACK has been received. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

**9.6.2.9.5 State: 0xC8**

The last data byte has been transmitted, ACK has been received. Not addressed Slave mode is entered.

1. Write 0x04 to CONSET to set the AA bit.
2. Write 0x08 to CONCLR to clear the SI flag.
3. Exit.

### 10.1 How to read this chapter

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Modem control and RTS/CTS functions are only pinned out for UART0.

### 10.2 Features

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- 16-byte receive and transmit FIFOs.
- Register locations conform to '550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes.
- Built-in baud rate generator.
- Software or hardware flow control.
- RS-485/EIA-485 9-bit mode support with output enable.
- RTS/CTS flow control and other modem control signals.
- Modem control.

### 10.3 Basic configuration

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The UART is configured using the following registers:

- In the SYSAHBCLKCTRL register, set bit 12, 19, and 20 ([Table 19](#)) to enable the clock to the register interfaces.
- The UART peripheral clock PCLK is derived from the main clock divided by the UART peripheral clock divider ([Table 21](#)).
- Baud rate: In register LCR ([Table 154](#)), set bit DLAB =1. This enables access to registers DLL ([Table 148](#)) and DLM ([Table 149](#)) for setting the baud rate. Also, if needed, set the fractional baud rate in the fractional divider register ([Table 160](#)).
- UART FIFO: Use bit FIFO enable (bit 0) in register FCR ([Table 153](#)) to enable the FIFOs.
- Pins: Select UART pins and pin modes through the relevant IOCON registers ([Section 6.4](#)).
- Interrupts: To enable UART interrupts set bit DLAB =0 in register LCR ([Table 154](#)). This enables access to IER ([Table 150](#)). Interrupts are enabled in the NVIC using the appropriate Interrupt Set Enable register.

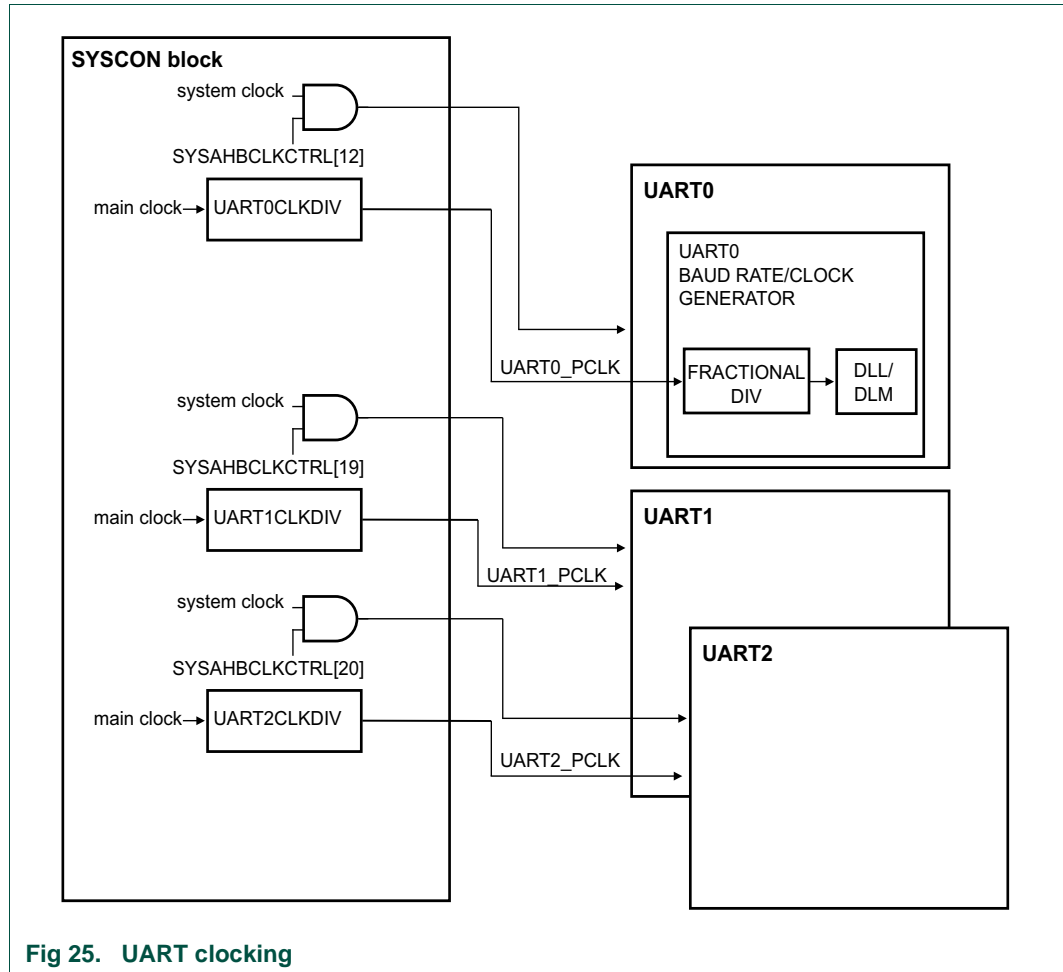


Fig 25. UART clocking

## 10.4 General description

The architecture of the UART is shown below in the block diagram.

The APB interface provides a communications link between the CPU or host and the UART.

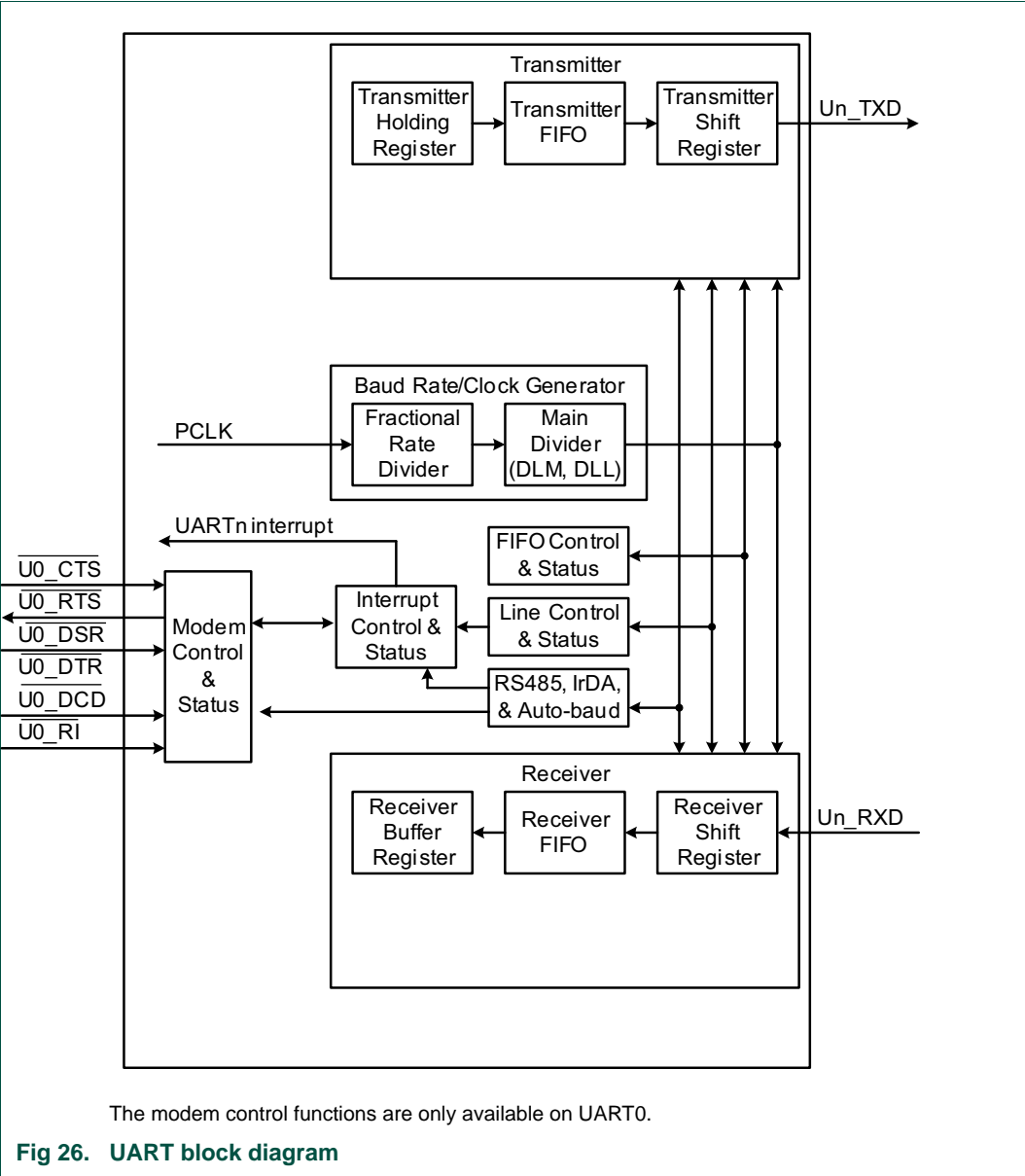
The UART receiver block, RX, monitors the serial input line, RXDn, for valid input. The UART RX Shift Register (RSR) accepts valid characters via RXDn. After a valid character is assembled in RSR, it is passed to the UART RX Buffer Register FIFO to await access by the CPU or host via the generic host interface.

The UART transmitter block, TX, accepts data written by the CPU or host and buffers the data in the UART TX Holding Register FIFO (THR). The UART TX Shift Register (TSR) reads the data stored in THR and assembles the data to transmit via the serial output pin, TXDn.

The UART Baud Rate Generator block, BRG, generates the timing enables used by the UART TX block. The BRG clock input source is the APB clock (PCLK). The main clock is divided down per the divisor specified in the DLL and DLM registers. This divided down clock is the 16x oversample clock.

The interrupt interface contains registers IER and IIR. The interrupt interface receives several one clock wide enables from the TX and RX blocks.

Status information from the TX and RX is stored in the LSR. Control information for the TX and RX is stored in LCR.



10.5 Pin description

Table 144. UART pin description

Pin	Type	Description
U0_RXD	Input	Serial Input. Serial receive data.
U0_TXD	Output	Serial Output. Serial transmit data.
U0_RTS	Output	Request To Send. RS-485 direction control pin.

Table 144. UART pin description

Pin	Type	Description
U0_CTS	Input	Clear To Send.
U0_DTR	Output	Data Terminal Ready.
U0_DSR	Input	Data Set Ready.
U0_DCD	Input	Data Carrier Detect.
U0_RI	Input	Ring Indicator.
U1_RXD	Input	Serial Input. Serial receive data.
U1_TXD	Output	Serial Output. Serial transmit data.
U2_RXD	Input	Serial Input. Serial receive data.
U2_TXD	Output	Serial Output. Serial transmit data.

## 10.6 Register description

The UARTs contain registers organized as shown in [Table 145](#). The Divisor Latch Access Bit (DLAB) is contained in the LCR register bit 7 and enables access to the Divisor Latches.

Offsets/addresses not shown in [Table 145](#) are reserved.

Table 145. Register overview: UART (base address: 0x4000 8000 (UART0), 0x4002 0000 (UART1), 0x4002 4000 (UART2))

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>	Reference
RBR	RO	0x000	Receiver Buffer Register. Contains the next received character to be read. (DLAB=0)	NA	<a href="#">Table 146</a>
THR	WO	0x000	Transmit Holding Register. The next character to be transmitted is written here. (DLAB=0)	NA	<a href="#">Table 147</a>
DLL	R/W	0x000	Divisor Latch LSB. Least significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider. (DLAB=1)	0x01	<a href="#">Table 148</a>
DLM	R/W	0x004	Divisor Latch MSB. Most significant byte of the baud rate divisor value. The full divisor is used to generate a baud rate from the fractional rate divider. (DLAB=1)	0	<a href="#">Table 149</a>
IER	R/W	0x004	Interrupt Enable Register. Contains individual interrupt enable bits for the 7 potential UART interrupts. (DLAB=0)	0	<a href="#">Table 150</a>
IIR	RO	0x008	Interrupt ID Register. Identifies which interrupt(s) are pending.	0x01	<a href="#">Table 151</a>
FCR	WO	0x008	FIFO Control Register. Controls UART FIFO usage and modes.	0	<a href="#">Table 152</a>
LCR	R/W	0x00C	Line Control Register. Contains controls for frame formatting and break generation.	0	<a href="#">Table 154</a>
MCR	R/W	0x010	Modem Control Register.	0	<a href="#">Table 155</a>
LSR	RO	0x014	Line Status Register. Contains flags for transmit and receive status, including line errors.	0x60	<a href="#">Table 156</a>
MSR	RO	0x018	Modem Status Register.	0	<a href="#">Table 157</a>

**Table 145. Register overview: UART (base address: 0x4000 8000 (UART0), 0x4002 0000 (UART1), 0x4002 4000 (UART2))**

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>	Reference
SCR	R/W	0x01C	Scratch Pad Register. Eight-bit temporary storage for software.	0	<a href="#">Table 158</a>
ACR	R/W	0x020	Auto-baud Control Register. Contains controls for the auto-baud feature.	0	<a href="#">Table 159</a>
-	-	0x024	-	0	-
FDR	R/W	0x028	Fractional Divider Register. Generates a clock input for the baud rate divider.	0x10	<a href="#">Table 160</a>
-	-	0x02C	-	-	-
TER	R/W	0x030	Transmit Enable Register. Turns off UART transmitter for use with software flow control.	0x80	<a href="#">Table 161</a>
-	-	0x040	-	-	-
-	-	0x048	-	-	-
RS485CTRL	R/W	0x04C	RS-485/EIA-485 Control. Contains controls to configure various aspects of RS-485/EIA-485 modes.	0	<a href="#">Table 162</a>
RS485ADRMATCH	R/W	0x050	RS-485/EIA-485 address match. Contains the address match value for RS-485/EIA-485 mode.	0	<a href="#">Table 163</a>
RS485DLY	R/W	0x054	RS-485/EIA-485 direction control delay.	0	<a href="#">Table 164</a>

[1] Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

### 10.6.1 UART Receiver Buffer Register (when DLAB = 0, Read Only)

The RBR is the top byte of the UART RX FIFO. The top byte of the RX FIFO contains the oldest character received and can be read via the bus interface. The LSB (bit 0) contains the first-received data bit. If the character received is less than 8 bits, the unused MSBs are padded with zeros.

The Divisor Latch Access Bit (DLAB) in the LCR must be zero in order to access the RBR. The RBR is always Read Only.

Since PE, FE and BI bits (see [Table 156](#)) correspond to the byte on the top of the RBR FIFO (i.e. the one that will be read in the next read from the RBR), the right approach for fetching the valid pair of received byte and its status bits is first to read the content of the LSR register, and then to read a byte from the RBR.

**Table 146. UART Receiver Buffer Register when DLAB = 0, Read Only (RBR, address 0x4000 8000 (UART0), 0x4002 0000 (UART1), 0x4002 4000 (UART2)) bit description**

Bit	Symbol	Description	Reset Value
7:0	RBR	The UART Receiver Buffer Register contains the oldest received byte in the UART RX FIFO.	undefined
31:8	-	Reserved	-

### 10.6.2 UART Transmitter Holding Register (when DLAB = 0, Write Only)

The THR is the top byte of the UART TX FIFO. The top byte is the newest character in the TX FIFO and can be written via the bus interface. The LSB represents the first bit to transmit.

The Divisor Latch Access Bit (DLAB) in the LCR must be zero in order to access the THR. The THR is always Write Only.

**Table 147. UART Transmitter Holding Register when DLAB = 0, Write Only (THR, address 0x4000 8000 (UART0), 0x4002 0000 (UART1), 0x4002 4000 (UART2)) bit description**

Bit	Symbol	Description	Reset Value
7:0	THR	Writing to the UART Transmit Holding Register causes the data to be stored in the UART transmit FIFO. The byte will be sent when it is the oldest byte in the FIFO and the transmitter is available.	NA
31:8	-	Reserved	-

### 10.6.3 UART Divisor Latch LSB and MSB Registers (when DLAB = 1)

The UART Divisor Latch is part of the UART Baud Rate Generator and holds the value used (optionally with the Fractional Divider) to divide the UART\_PCLK clock in order to produce the baud rate clock, which must be the multiple of the desired baud rate that is specified by the Oversampling Register (typically 16X). The DLL and DLM registers together form a 16-bit divisor. DLL contains the lower 8 bits of the divisor and DLM contains the higher 8 bits. A zero value is treated like 0x0001. The Divisor Latch Access Bit (DLAB) in the LCR must be one in order to access the UART Divisor Latches. Details on how to select the right value for DLL and DLM can be found in [Section 10.6.13](#).

**Table 148. UART Divisor Latch LSB Register when DLAB = 1 (DLL, address 0x4000 8000 (UART0), 0x4002 0000 (UART1), 0x4002 4000 (UART2)) bit description**

Bit	Symbol	Description	Reset value
7:0	DLLSB	The UART Divisor Latch LSB Register, along with the DLM register, determines the baud rate of the UART.	0x01
31:8	-	Reserved	-

**Table 149. UART Divisor Latch MSB Register when DLAB = 1 (DLM, address 0x4000 8004 (UART0), 0x4002 0004 (UART1), 0x4002 4004 (UART2)) bit description**

Bit	Symbol	Description	Reset value
7:0	DLMSB	The UART Divisor Latch MSB Register, along with the DLL register, determines the baud rate of the UART.	0x00
31:8	-	Reserved	-

#### 10.6.4 UART Interrupt Enable Register (when DLAB = 0)

The IER is used to enable the various UART interrupt sources.

**Table 150. UART Interrupt Enable Register when DLAB = 0 (IER, address 0x4000 8004 (UART0), 0x4002 0004 (UART1), 0x4002 4004 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	RBRINTEN		RBR Interrupt Enable. Enables the Receive Data Available interrupt. It also controls the Character Receive Time-out interrupt.	0
		0	Disable. Disable the RDA interrupt.	
		1	Enable. Enable the RDA interrupt.	
1	THREINTEN		THRE Interrupt Enable. Enables the THRE interrupt. The status of this interrupt can be read from LSR[5].	0
		0	Disable. Disable the THRE interrupt.	
		1	Enable. Enable the THRE interrupt.	
2	RLSINTEN		Enables the Receive Line Status interrupt. The status of this interrupt can be read from LSR[4:1].	-
		0	Disable. Disable the RLS interrupt.	
		1	Enable. Enable the RLS interrupt.	
3	MSINTEN		Enables the Modem Status interrupt. The components of this interrupt can be read from the MSR.	
		0	Disable. Disable the MS interrupt.	
		1	Enable. Enable the MS interrupt.	
7:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	ABEOINTEN		Enables the end of auto-baud interrupt.	0
		0	Disable. Disable end of auto-baud Interrupt.	
		1	Enable. Enable end of auto-baud Interrupt.	



**Table 150. UART Interrupt Enable Register when DLAB = 0 (IER, address 0x4000 8004 (UART0), 0x4002 0004 (UART1), 0x4002 4004 (UART2)) bit description ...continued**

Bit	Symbol	Value	Description	Reset value
9	ABTOINTEN		Enables the auto-baud time-out interrupt.	0
		0	Disable. Disable auto-baud time-out Interrupt.	
		1	Enable. Enable auto-baud time-out Interrupt.	
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 10.6.5 UART Interrupt Identification Register (Read Only)

IIR provides a status code that denotes the priority and source of a pending interrupt. The interrupts are frozen during a IIR access. If an interrupt occurs during a IIR access, the interrupt is recorded for the next IIR access.

**Table 151. UART Interrupt Identification Register Read only (IIR, address 0x4000 8008 (UART0), 0x4002 0008 (UART1), 0x4002 4008 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	INTSTATUS		Interrupt status. Note that IIR[0] is active low. The pending interrupt can be determined by evaluating IIR[3:1].	1
		0	Interrupt pending. At least one interrupt is pending.	
		1	Not pending. No interrupt is pending.	
3:1	INTID		Interrupt identification. IER[3:1] identifies an interrupt corresponding to the UART Rx FIFO. All other values of IER[3:1] not listed below are reserved.	0
		0x3	RLS. 1 - Receive Line Status .	
		0x2	RDA. 2a - Receive Data Available.	
		0x6	CTI. 2b - Character Time-out Indicator.	
		0x1	THRE. 3 - THRE Interrupt.	
		0x0	Modem status. 4 - Modem status	
5:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	FIFOEN		These bits are equivalent to FCR[0].	0
8	ABEOINT		End of auto-baud interrupt. True if auto-baud has finished successfully and interrupt is enabled.	0
9	ABTOINT		Auto-baud time-out interrupt. True if auto-baud has timed out and interrupt is enabled.	0
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Bits IIR[9:8] are set by the auto-baud function and signal a time-out or end of auto-baud condition. The auto-baud interrupt conditions are cleared by setting the corresponding Clear bits in the Auto-baud Control Register.

If the IntStatus bit is one and no interrupt is pending and the IntId bits will be zero. If the IntStatus is 0, a non auto-baud interrupt is pending in which case the IntId bits identify the type of interrupt and handling as described in [Table 152](#). Given the status of IIR[3:0], an

interrupt handler routine can determine the cause of the interrupt and how to clear the active interrupt. The IIR must be read in order to clear the interrupt prior to exiting the Interrupt Service Routine.

The UART RLS interrupt (IIR[3:1] = 011) is the highest priority interrupt and is set whenever any one of four error conditions occur on the UART RX input: overrun error (OE), parity error (PE), framing error (FE) and break interrupt (BI). The UART Rx error condition that set the interrupt can be observed via LSR[4:1]. The interrupt is cleared upon a LSR read.

The UART RDA interrupt (IIR[3:1] = 010) shares the second level priority with the CTI interrupt (IIR[3:1] = 110). The RDA is activated when the UART Rx FIFO reaches the trigger level defined in FCR7:6 and is reset when the UART Rx FIFO depth falls below the trigger level. When the RDA interrupt goes active, the CPU can read a block of data defined by the trigger level.

The CTI interrupt (IIR[3:1] = 110) is a second level interrupt and is set when the UART Rx FIFO contains at least one character and no UART Rx FIFO activity has occurred in 3.5 to 4.5 character times. Any UART Rx FIFO activity (read or write of UART RSR) will clear the interrupt. This interrupt is intended to flush the UART RBR after a message has been received that is not a multiple of the trigger level size. For example, if a 105 character message was to be sent and the trigger level was 10 characters, the CPU would receive 10 RDA interrupts resulting in the transfer of 100 characters and 1 to 5 CTI interrupts (depending on the service routine) resulting in the transfer of the remaining 5 characters.

**Table 152. UART Interrupt Handling**

IIR[3:0] value <sup>[1]</sup>	Priority	Interrupt type	Interrupt source	Interrupt reset
0001	-	None	None	-
0110	Highest	RX Line Status / Error	OE <sup>[2]</sup> or PE <sup>[2]</sup> or FE <sup>[2]</sup> or BI <sup>[2]</sup>	LSR Read <sup>[2]</sup>
0100	Second	RX Data Available	Rx data available or trigger level reached in FIFO (FCR0=1)	RBR Read <sup>[3]</sup> or UART FIFO drops below trigger level
1100	Second	Character Time-out indication	Minimum of one character in the RX FIFO and no character input or removed during a time period depending on how many characters are in FIFO and what the trigger level is set at (3.5 to 4.5 character times).  The exact time will be: [(word length) × 7 - 2] × 8 + [(trigger level - number of characters) × 8 + 1] RCLKs	RBR Read <sup>[3]</sup>
0010	Third	THRE	THRE <sup>[2]</sup>	IIR Read <sup>[4]</sup> (if source of interrupt) or THR write
0000	Fourth	Modem Status	CTS, DSR, RI, or DCD.	MSR Read

[1] Values "0000", "0011", "0101", "0111", "1000", "1001", "1010", "1011", "1101", "1110", "1111" are reserved.

- [2] For details see [Section 10.6.9 “UART Line Status Register \(Read-Only\)”](#)
- [3] For details see [Section 10.6.1 “UART Receiver Buffer Register \(when DLAB = 0, Read Only\)”](#)
- [4] For details see [Section 10.6.5 “UART Interrupt Identification Register \(Read Only\)”](#) and [Section 10.6.2 “UART Transmitter Holding Register \(when DLAB = 0, Write Only\)”](#)

The UART THRE interrupt (IIR[3:1] = 001) is a third level interrupt and is activated when the UART THR FIFO is empty provided certain initialization conditions have been met. These initialization conditions are intended to give the UART THR FIFO a chance to fill up with data to eliminate many THRE interrupts from occurring at system start-up. The initialization conditions implement a one character delay minus the stop bit whenever THRE = 1 and there have not been at least two characters in the THR at one time since the last THRE = 1 event. This delay is provided to give the CPU time to write data to THR without a THRE interrupt to decode and service. A THRE interrupt is set immediately if the UART THR FIFO has held two or more characters at one time and currently, the THR is empty. The THRE interrupt is reset when a THR write occurs or a read of the IIR occurs and the THRE is the highest interrupt (IIR[3:1] = 001).

The modem status interrupt (IIR3:1 = 000) is the lowest priority UART interrupt and is activated whenever there is a state change on the CTS, DCD, or DSR or a trailing edge on the RI pin. The source of the modem interrupt can be read in MSR3:0. Reading the MSR clears the modem interrupt.

## 10.6.6 UART FIFO Control Register (Write Only)

The FCR controls the operation of the UART RX and TX FIFOs.

**Table 153. UART FIFO Control Register Write only (FCR, address 0x4000 8008 (UART0), 0x4002 0008 (UART1), 0x4002 4008 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	FIFOEN		FIFO enable	0
		0	Disabled. UART FIFOs are disabled. Must not be used in the application.	
		1	Enabled. Active high enable for both UART Rx and TX FIFOs and FCR[7:1] access. This bit must be set for proper UART operation. Any transition on this bit will automatically clear the UART FIFOs.	
1	RXFIFORES		RX FIFO Reset	0
		0	No effect. No impact on either of UART FIFOs.	
		1	Clear. Writing a logic 1 to FCR[1] will clear all bytes in UART Rx FIFO, reset the pointer logic. This bit is self-clearing.	
2	TXFIFORES		TX FIFO Reset	0
		0	No effect. No impact on either of UART FIFOs.	
		1	Clear. Writing a logic 1 to FCR[2] will clear all bytes in UART TX FIFO, reset the pointer logic. This bit is self-clearing.	
5:3	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

**Table 153. UART FIFO Control Register Write only (FCR, address 0x4000 8008 (UART0), 0x4002 0008 (UART1), 0x4002 4008 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
7:6	RXTL		RX Trigger Level. These two bits determine how many UART FIFO characters must be received by the FIFO before an interrupt is activated.	0
		0x0	Trigger level 0. (1 character or 0x01).	
		0x1	Trigger level 1. (4 characters or 0x04).	
		0x2	Trigger level 2. (8 characters or 0x08).	
		0x3	Trigger level 3. (14 characters or 0x0E).	
31:8	-	-	Reserved	-

### 10.6.7 UART Line Control Register

The LCR determines the format of the data character that is to be transmitted or received.

**Table 154. UART Line Control Register (LCR, address 0x4000 800C (UART0), 0x4002 000C (UART1), 0x4002 400C (UART2)) bit description**

Bit	Symbol	Value	Description	Reset Value
1:0	WLS		Word Length Select	0
		0x0	5 bit. 5-bit character length.	
		0x1	6 bit. 6-bit character length.	
		0x2	7 bit. 7-bit character length.	
		0x3	8 bit. 8-bit character length.	
2	SBS		Stop Bit Select	0
		0	1 stop bit.	
		1	2 stop bits. (1.5 if LCR[1:0]=00).	
3	PE		Parity Enable	0
		0	Disable. Disable parity generation and checking.	
		1	Enable. Enable parity generation and checking.	
5:4	PS		Parity Select	0
		0x0	Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.	
		0x1	Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.	
		0x2	Forced 1 stick parity.	
		0x3	Forced 0 stick parity.	
6	BC		Break Control	0
		0	Disable. Disable break transmission.	
		1	Enable. Enable break transmission. Output pin UART TXD is forced to logic 0 when LCR[6] is active high.	
7	DLAB		Divisor Latch Access Bit	0
		0	Disable. Disable access to Divisor Latches.	
		1	Enable. Enable access to Divisor Latches.	
31:8	-	-	Reserved	-

### 10.6.8 UART Modem Control Register

The MCR enables the modem loopback mode and controls the modem output signals.

**Table 155. UART Modem Control Register (MCR, address 0x4000 8010 (UART0), 0x4002 0010 (UART1), 0x4002 4010 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	DTRCTRL		Source for modem output pin $\overline{\text{DTR}}$ . This bit reads as 0 when modem loopback mode is active.	0
1	RTSCTRL		Source for modem output pin $\overline{\text{RTS}}$ . This bit reads as 0 when modem loopback mode is active.	0
3:2	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
4	LMS		Loopback Mode Select. The modem loopback mode provides a mechanism to perform diagnostic loopback testing. Serial data from the transmitter is connected internally to serial input of the receiver. Input pin, RXD, has no effect on loopback and output pin, TXD is held in marking state. The DSR, CTS, DCD, and RI pins are ignored. Externally, DTR and RTS are set inactive. Internally, the upper four bits of the MSR are driven by the lower four bits of the MCR. This permits modem status interrupts to be generated in loopback mode by writing the lower four bits of MCR.	0
		0	Disable. Disable modem loopback mode.	
		1	Enable. Enable modem loopback mode.	
5	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
6	RTSEN		RTS enable	0
		0	Disable. Disable auto-rts flow control.	
		1	Enable. Enable auto-rts flow control.	
7	CTSEN		CTS enable	0
		0	Disable. Disable auto-cts flow control.	
		1	Enable. Enable auto-cts flow control.	
31:8	-	-	Reserved	-

### 10.6.9 UART Line Status Register (Read-Only)

The LSR is a read-only register that provides status information on the UART TX and RX blocks.

**Table 156. UART Line Status Register Read only (LSR, address 0x4000 8014 (UART0), 0x4002 0014 (UART1), 0x4002 4014 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset Value
0	RDR		Receiver Data Ready: LSR[0] is set when the RBR holds an unread character and is cleared when the UART RBR FIFO is empty.	0
		0	Empty. RBR is empty.	
		1	Filled. RBR contains valid data.	

**Table 156. UART Line Status Register Read only (LSR, address 0x4000 8014 (UART0), 0x4002 0014 (UART1), 0x4002 4014 (UART2)) bit description ...continued**

Bit	Symbol	Value	Description	Reset Value
1	OE		Overrun Error. The overrun error condition is set as soon as it occurs. A LSR read clears LSR[1]. LSR[1] is set when UART RSR has a new character assembled and the UART RBR FIFO is full. In this case, the UART RBR FIFO will not be overwritten and the character in the UART RSR will be lost.	0
		0	Inactive. Overrun error status is inactive.	
		1	Active. Overrun error status is active.	
2	PE		Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. A LSR read clears LSR[2]. Time of parity error detection is dependent on FCR[0]. <b>Note:</b> A parity error is associated with the character at the top of the UART RBR FIFO.	0
		0	Inactive. Parity error status is inactive.	
		1	Active. Parity error status is active.	
3	FE		Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. A LSR read clears LSR[3]. The time of the framing error detection is dependent on FCR0. Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. <b>Note:</b> A framing error is associated with the character at the top of the UART RBR FIFO.	0
		0	Inactive. Framing error status is inactive.	
		1	Active. Framing error status is active.	
4	BI		Break Interrupt. When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A LSR read clears this status bit. The time of break detection is dependent on FCR[0]. <b>Note:</b> The break interrupt is associated with the character at the top of the UART RBR FIFO.	0
		0	Inactive. Break interrupt status is inactive.	
		1	Active. Break interrupt status is active.	
5	THRE		Transmitter Holding Register Empty. THRE is set immediately upon detection of an empty UART THR and is cleared on a THR write.	1
		0	Data. THR contains valid data.	
		1	Empty. THR is empty.	
6	TEMT		Transmitter Empty. TEMT is set when both THR and TSR are empty; TEMT is cleared when either the TSR or the THR contain valid data.	1
		0	Data. THR and/or the TSR contains valid data.	
		1	Empty. THR and the TSR are empty.	

**Table 156. UART Line Status Register Read only (LSR, address 0x4000 8014 (UART0), 0x4002 0014 (UART1), 0x4002 4014 (UART2)) bit description ...continued**

Bit	Symbol	Value	Description	Reset Value
7	RXFE		Error in RX FIFO. LSR[7] is set when a character with a RX error such as framing error, parity error or break interrupt, is loaded into the RBR. This bit is cleared when the LSR register is read and there are no subsequent errors in the UART FIFO.	0
		0	Empty. RBR contains no UART RX errors or FCR[0]=0.	
		1	Error. UART RBR contains at least one UART RX error.	
31:8	-	-	Reserved	-

### 10.6.10 UART Modem Status Register

The MSR is a read-only register that provides status information on UART input signals. Bit 0 is cleared when (after) this register is read.

**Table 157. UART Modem Status Register (MSR, address 0x4000 8018 (UART0), 0x4002 0018 (UART1), 0x4002 4018 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	DCTS		Delta CTS. Set upon state change of input CTS. Cleared on an MSR read.	0
		0	No change. No change detected on modem input, CTS.	
		1	Changed. State change detected on modem input, CTS.	
1	DDSR		Delta DSR. Set upon state change of input DSR. Cleared on an MSR read.	0
		0	No change. No change detected on modem input, DSR.	
		1	Changed. State change detected on modem input, DSR.	
2	TERI		Trailing Edge RI. Set upon low to high transition of input RI. Cleared on an MSR read.	0
		0	No change. No change detected on modem input, RI.	
		1	Transition. Low-to-high transition detected on RI.	
3	DDCD		Delta DCD. Set upon state change of input DCD. Cleared on an MSR read.	0
		0	No change. No change detected on modem input, DCD.	
		1	Changed. State change detected on modem input, DCD.	
4	CTS	-	Clear To Send State. Complement of input signal CTS. This bit is connected to MCR[1] in modem loopback mode.	0
5	DSR	-	Data Set Ready State. Complement of input signal DSR. This bit is connected to MCR[0] in modem loopback mode.	0
6	RI	-	Ring Indicator State. Complement of input RI. This bit is connected to MCR[2] in modem loopback mode.	0
7	DCD	-	Data Carrier Detect State. Complement of input DCD. This bit is connected to MCR[3] in modem loopback mode.	0
31:8	-	-	Reserved, the value read from a reserved bit is not defined.	NA

### 10.6.11 UART Scratch Pad Register

The SCR has no effect on the UART operation. This register can be written and/or read at user's discretion. There is no provision in the interrupt interface that would indicate to the host that a read or write of the SCR has occurred.

**Table 158. UART Scratch Pad Register (SCR, address 0x4000 801C (UART0), 0x4002 001C (UART1), 0x4002 401C (UART2)) bit description**

Bit	Symbol	Description	Reset Value
7:0	PAD	A readable, writable byte.	0x00
31:8	-	Reserved	-

### 10.6.12 UART Auto-baud Control Register

The UART Auto-baud Control Register (ACR) controls the process of measuring the incoming clock/data rate for baud rate generation, and can be read and written at the user's discretion.

**Table 159. Auto-baud Control Register (ACR, address 0x4000 8020 (UART0), 0x4002 0020 (UART1), 0x4002 4020 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	START		This bit is automatically cleared after auto-baud completion.	0
		0	Stop. Auto-baud stop (auto-baud is not running).	
		1	Start. Auto-baud start (auto-baud is running). Auto-baud run bit. This bit is automatically cleared after auto-baud completion.	
1	MODE		Auto-baud mode select bit.	0
		0	Mode 0.	
		1	Mode 1.	
2	AUTORESTART		Start mode	0
		0	No restart.	
		1	Time-out restart. Restart in case of time-out (counter restarts at next UART Rx falling edge)	
7:3	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0
8	ABEOINTCLR		End of auto-baud interrupt clear bit (write only accessible).	0
		0	No effect. Writing a 0 has no impact.	
		1	Clear. Writing a 1 will clear the corresponding interrupt in the IIR.	



**Table 159. Auto-baud Control Register (ACR, address 0x4000 8020 (UART0), 0x4002 0020 (UART1), 0x4002 4020 (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
9	ABTOINTCLR		Auto-baud time-out interrupt clear bit (write only accessible).	0
		0	No effect. Writing a 0 has no impact.	
		1	Clear. Writing a 1 will clear the corresponding interrupt in the IIR.	
31:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

### 10.6.13 UART Fractional Divider Register

The UART Fractional Divider Register (FDR) controls the clock pre-scaler for the baud rate generation and can be read and written at the user's discretion. This pre-scaler takes the APB clock and generates an output clock according to the specified fractional requirements.

**Important:** If the fractional divider is active ( $DIVADDVAL > 0$ ) and  $DLM = 0$ , the value of the DLL register must be 3 or greater.

**Table 160. UART Fractional Divider Register (FDR, address 0x4000 8028 (UART0), 0x4002 0028 (UART1), 0x4002 4028 (UART2)) bit description**

Bit	Function	Description	Reset value
3:0	DIVADDVAL	Baud rate generation pre-scaler divisor value. If this field is 0, fractional baud rate generator will not impact the UART baud rate.	0
7:4	MULVAL	Baud rate pre-scaler multiplier value. This field must be greater or equal 1 for UART to operate properly, regardless of whether the fractional baud rate generator is used or not.	1
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0

This register controls the clock pre-scaler for the baud rate generation. The reset value of the register keeps the fractional capabilities of UART disabled making sure that UART is fully software and hardware compatible with UARTs not equipped with this feature.

The UART baud rate can be calculated as:

$$UART_{baudrate} = \frac{PCLK}{16 \times (256 \times DLM + DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)} \quad (3)$$

Where  $UART\_PCLK$  is the peripheral clock,  $DLM$  and  $DLL$  are the standard UART baud rate divider registers, and  $DIVADDVAL$  and  $MULVAL$  are UART fractional baud rate generator specific parameters.

The value of  $MULVAL$  and  $DIVADDVAL$  should comply to the following conditions:

1.  $1 \leq \text{MULVAL} \leq 15$
2.  $0 \leq \text{DIVADDVAL} \leq 14$
3.  $\text{DIVADDVAL} < \text{MULVAL}$

The value of the FDR should not be modified while transmitting/receiving data or data may be lost or corrupted.

If the FDR register value does not comply to these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

#### 10.6.14 UART Transmit Enable Register

In addition to being equipped with full hardware flow control (auto-cts and auto-rts mechanisms described above), TER enables implementation of software flow control. When TxEn = 1, the UART transmitter will keep sending data as long as they are available. As soon as TxEn becomes 0, UART transmission will stop.

Although [Table 161](#) describes how to use TxEn bit in order to achieve hardware flow control, it is strongly suggested to let the UART hardware implemented auto flow control features take care of this and limit the scope of TxEn to software flow control.

[Table 161](#) describes how to use TXEn bit in order to achieve software flow control.

**Table 161. UART Transmit Enable Register (TER, address 0x4000 8030 (UART0), 0x4002 0030 (UART1), 0x4002 4030 (UART2)) bit description**

Bit	Symbol	Description	Reset Value
6:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7	TXEN	When this bit is 1, as it is after a Reset, data written to the THR is output on the TXD pin as soon as any preceding data has been sent. If this bit cleared to 0 while a character is being sent, the transmission of that character is completed, but no further characters are sent until this bit is set again. In other words, a 0 in this bit blocks the transfer of characters from the THR or TX FIFO into the transmit shift register. Software can clear this bit when it detects that the a hardware-handshaking TX-permit signal (CTS) has gone false, or with software handshaking, when it receives an XOFF character (DC3). Software can set this bit again when it detects that the TX-permit signal has gone true, or when it receives an XON (DC1) character.	1
31:8	-	Reserved	-

#### 10.6.15 UART RS485 Control register

The RS485CTRL register controls the configuration of the UART in RS-485/EIA-485 mode.

**Table 162. UART RS485 Control register (RS485CTRL, address 0x4000 804C (UART0), 0x4002 004C (UART1), 0x4002 404C (UART2)) bit description**

Bit	Symbol	Value	Description	Reset value
0	NMMEN		NMM enable.	0
		0	Disabled. RS-485/EIA-485 Normal Multidrop Mode (NMM) is disabled.	
		1	Enabled. RS-485/EIA-485 Normal Multidrop Mode (NMM) is enabled. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.	
1	RXDIS		Receiver enable.	0
		0	Enabled. The receiver is enabled.	
		1	Disabled. The receiver is disabled.	
2	AADEN		AAD enable.	0
		0	Disabled. Auto Address Detect (AAD) is disabled.	
		1	Enabled. Auto Address Detect (AAD) is enabled.	
3	SEL		Select direction control pin	0
		0	Enabled. If direction control is enabled (bit DCTRL = 1), pin $\overline{\text{RTS}}$ is used for direction control.	
		1	Disabled. If direction control is enabled (bit DCTRL = 1), pin $\overline{\text{DTR}}$ is used for direction control.	
4	DCTRL		Auto direction control enable.	0
		0	Disabled. Disable Auto Direction Control.	
		1	Enabled. Enable Auto Direction Control.	
5	OINV		Polarity control. This bit reverses the polarity of the direction control signal on the $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$ ) pin.	0
		0	Low. The direction control pin will be driven to logic 0 when the transmitter has data to be sent. It will be driven to logic 1 after the last bit of data has been transmitted.	
		1	High. The direction control pin will be driven to logic 1 when the transmitter has data to be sent. It will be driven to logic 0 after the last bit of data has been transmitted.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 10.6.16 UART RS-485 Address Match register

The RS485ADRMATCH register contains the address match value for RS-485/EIA-485 mode.

**Table 163. UART RS-485 Address Match register (RS485ADRMATCH, address 0x4000 8050 (UART0), 0x4002 0050 (UART1), 0x4002 4050 (UART2)) bit description**

Bit	Symbol	Description	Reset value
7:0	ADRMATCH	Contains the address match value.	0x00
31:8	-	Reserved	-

### 10.6.17 UART RS-485 Delay value register

The user may program the 8-bit RS485DLY register with a delay between the last stop bit leaving the TXFIFO and the de-assertion of RTS (or DTR). This delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

**Table 164. UART RS-485 Delay value register (RS485DLY, address 0x4000 8054 (UART0), 0x4002 0054 (UART1), 0x4002 4054 (UART2)) bit description**

Bit	Symbol	Description	Reset value
7:0	DLY	Contains the direction control (RTS or DTR) delay value. This register works in conjunction with an 8-bit counter.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 10.7 Functional description

### 10.7.1 Auto-flow control

If auto-RTS mode is enabled, the UART's receiver FIFO hardware controls the  $\overline{\text{RTS}}$  output of the UART. If the auto-CTS mode is enabled, the UART's transmitter will only start sending if the CTS pin is low.

#### 10.7.1.1 Auto-RTS

The auto-RTS function is enabled by setting the RTSen bit. Auto-RTS data flow control originates in the RBR module and is linked to the programmed receiver FIFO trigger level. If auto-RTS is enabled, the data-flow is controlled as follows:

When the receiver FIFO level reaches the programmed trigger level,  $\overline{\text{RTS}}$  is deasserted (to a high value). It is possible that the sending UART sends an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it might not recognize the deassertion of  $\overline{\text{RTS}}$  until after it has begun sending the additional byte.  $\overline{\text{RTS}}$  is automatically reasserted (to a low value) once the receiver FIFO has reached the previous trigger level. The reassertion of  $\overline{\text{RTS}}$  signals the sending UART to continue transmitting data.

If Auto-RTS mode is disabled, the RTSen bit controls the  $\overline{\text{RTS}}$  output of the UART. If Auto-RTS mode is enabled, hardware controls the  $\overline{\text{RTS}}$  output, and the actual value of  $\overline{\text{RTS}}$  will be copied in the RTS Control bit of the UART. As long as Auto-RTS is enabled, the value of the RTS Control bit is read-only for software.

Example: Suppose the UART operating in type '550 mode has the trigger level in FCR set to 0x2, then, if Auto-RTS is enabled, the UART will deassert the  $\overline{\text{RTS}}$  output as soon as the receive FIFO contains 8 bytes ([Table 153 on page 147](#)). The  $\overline{\text{RTS}}$  output will be reasserted as soon as the receive FIFO hits the previous trigger level: 4 bytes.

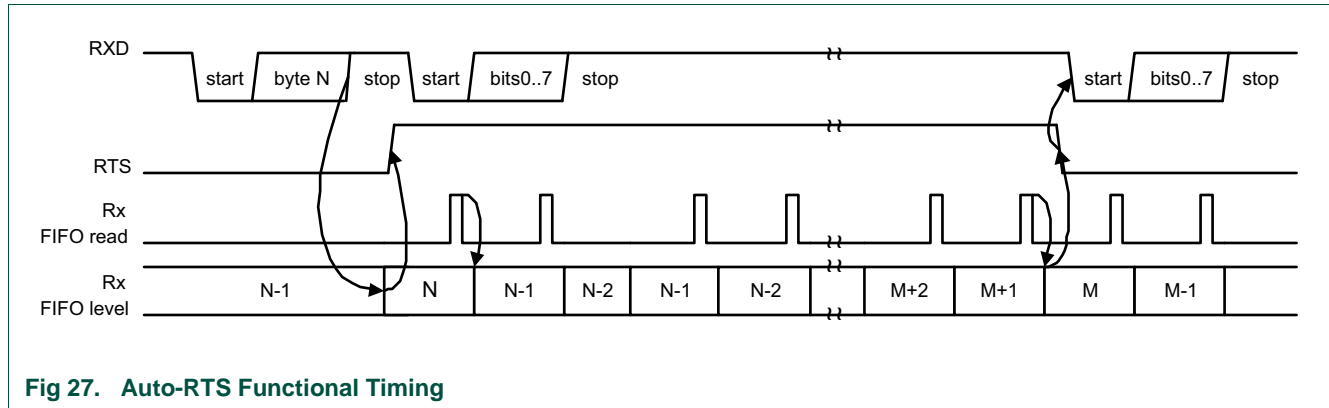


Fig 27. Auto-RTS Functional Timing

### 10.7.1.2 Auto-CTS

The Auto-CTS function is enabled by setting the CTSen bit. If Auto-CTS is enabled, the transmitter circuitry checks the  $\overline{\text{CTS}}$  input before sending the next data byte. When  $\overline{\text{CTS}}$  is active (low), the transmitter sends the next byte. To stop the transmitter from sending the following byte,  $\overline{\text{CTS}}$  must be released before the middle of the last stop bit that is currently being sent. In Auto-CTS mode, a change of the  $\overline{\text{CTS}}$  signal does not trigger a modem status interrupt unless the CTS Interrupt Enable bit is set, but the Delta CTS bit in the MSR will be set. [Table 165](#) lists the conditions for generating a Modem Status interrupt.

Table 165. Modem status interrupt generation

Enable modem status interrupt (IER[3])	CTSen (MCR[7])	CTS interrupt enable (IER[7])	Delta CTS (MSR[0])	Delta DCD or trailing edge RI or Delta DSR (MSR[3:1])	Modem status interrupt
0	x	x	x	x	No
1	0	x	0	0	No
1	0	x	1	x	Yes
1	0	x	x	1	Yes
1	1	0	x	0	No
1	1	0	x	1	Yes
1	1	1	0	0	No
1	1	1	1	x	Yes
1	1	1	x	1	Yes

The auto-CTS function typically eliminates the need for CTS interrupts. When flow control is enabled, a  $\overline{\text{CTS}}$  state change does not trigger host interrupts because the device automatically controls its own transmitter. Without Auto-CTS, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. [Figure 28](#) illustrates the Auto-CTS functional timing.

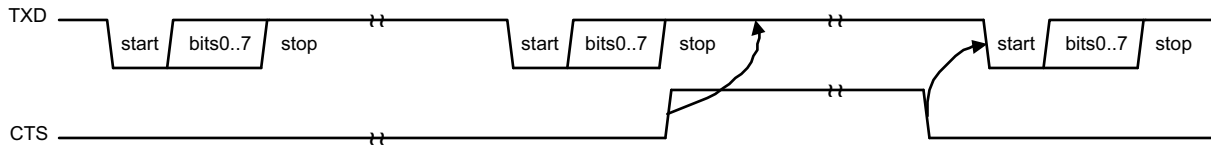


Fig 28. Auto-CTS Functional Timing

During transmission of the second character the  $\overline{\text{CTS}}$  signal is negated. The third character is not sent thereafter. The UART maintains 1 on TXD as long as  $\overline{\text{CTS}}$  is negated (high). As soon as  $\overline{\text{CTS}}$  is asserted, transmission resumes and a start bit is sent followed by the data bits of the next character.

### 10.7.2 Auto-baud

The UART auto-baud function can be used to measure the incoming baud rate based on the “AT” protocol (Hayes command). If enabled the auto-baud feature will measure the bit time of the receive data stream and set the divisor latch registers DLM and DLL accordingly.

Auto-baud is started by setting the ACR Start bit. Auto-baud can be stopped by clearing the ACR Start bit. The Start bit will clear once auto-baud has finished and reading the bit will return the status of auto-baud (pending/finished).

Two auto-baud measuring modes are available which can be selected by the ACR Mode bit. In Mode 0 the baud rate is measured on two subsequent falling edges of the UART Rx pin (the falling edge of the start bit and the falling edge of the least significant bit). In Mode 1 the baud rate is measured between the falling edge and the subsequent rising edge of the UART Rx pin (the length of the start bit).

The ACR AutoRestart bit can be used to automatically restart baud rate measurement if a time-out occurs (the rate measurement counter overflows). If this bit is set, the rate measurement will restart at the next falling edge of the UART Rx pin.

The auto-baud function can generate two interrupts.

- The IIR ABTOInt interrupt will get set if the interrupt is enabled (IER ABTOIntEn is set and the auto-baud rate measurement counter overflows).
- The IIR ABEOInt interrupt will get set if the interrupt is enabled (IER ABEOIntEn is set and the auto-baud has completed successfully).

The auto-baud interrupts have to be cleared by setting the corresponding ACR ABTOINTCLR and ABEOINTEN bits.

The fractional baud rate generator must be disabled ( $\text{DIVADDVAL} = 0$ ) during auto-baud. Also, when auto-baud is used, any write to DLM and DLL registers should be done before ACR register write. The minimum and the maximum baud rates supported by UART are a function of  $\text{UART\_PCLK}$  and the number of data bits, stop bits and parity bits.

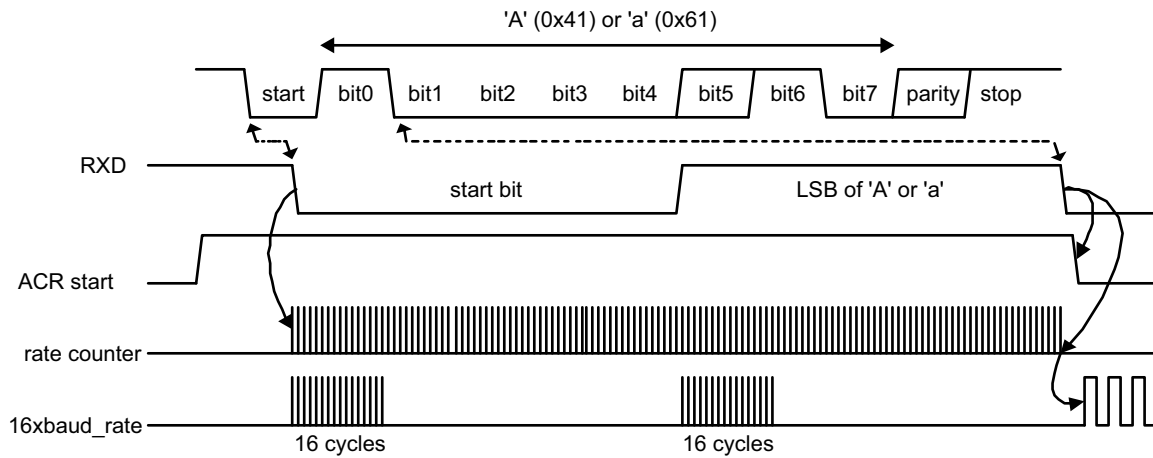
(4)

$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \leq UART_{baudrate} \leq \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax$$

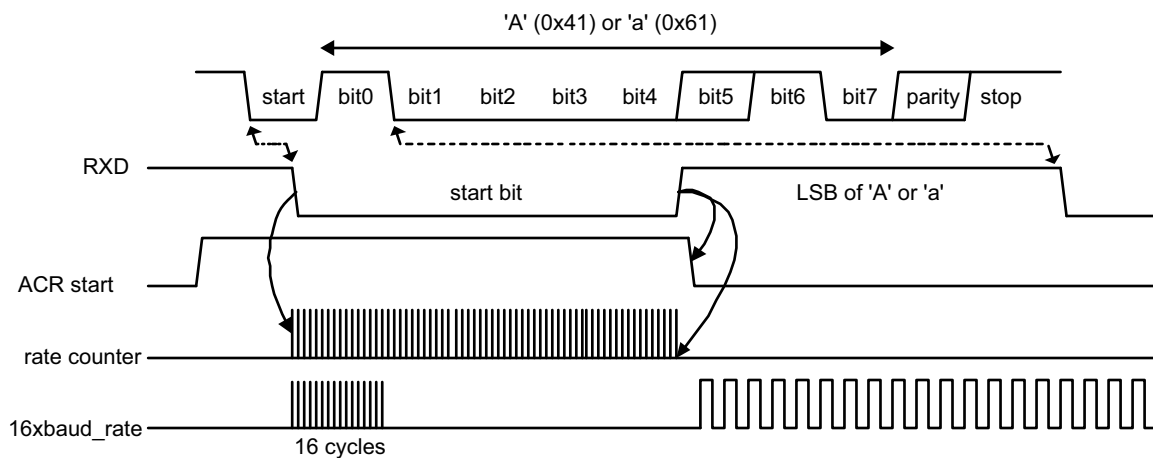
### 10.7.3 Auto-baud modes

When the software is expecting an “AT” command, it configures the UART with the expected character format and sets the ACR Start bit. The initial values in the divisor latches DLM and DLM don’t care. Because of the “A” or “a” ASCII coding (“A” = 0x41, “a” = 0x61), the UART Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On ACR Start bit setting, the baud rate measurement counter is reset and the UART RSR is reset. The RSR baud rate is switched to the highest rate.
2. A falling edge on UART Rx pin triggers the beginning of the start bit. The rate measuring counter will start counting UART\_PCLK cycles.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the UART input clock, guaranteeing the start bit is stored in the RSR.
4. During the receipt of the start bit (and the character LSB for Mode = 0), the rate counter will continue incrementing with the pre-scaled UART input clock (UART\_PCLK).
5. If Mode = 0, the rate counter will stop on next falling edge of the UART Rx pin. If Mode = 1, the rate counter will stop on the next rising edge of the UART Rx pin.
6. The rate counter is loaded into DLM/DLL and the baud rate will be switched to normal operation. After setting the DLM/DLL, the end of auto-baud interrupt IIR ABEOInt will be set, if enabled. The RSR will now continue receiving the remaining bits of the character.



a. Mode 0 (start bit and LSB are used for auto-baud)



b. Mode 1 (only start bit is used for auto-baud)

**Fig 29. Auto-baud a) mode 0 and b) mode 1 waveform**

### 10.7.4 Baud rate calculation

The UART can operate with or without using the Fractional Divider. In real-life applications it is likely that the desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MULVAL, and DIVADDDVAL values. Such a set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.



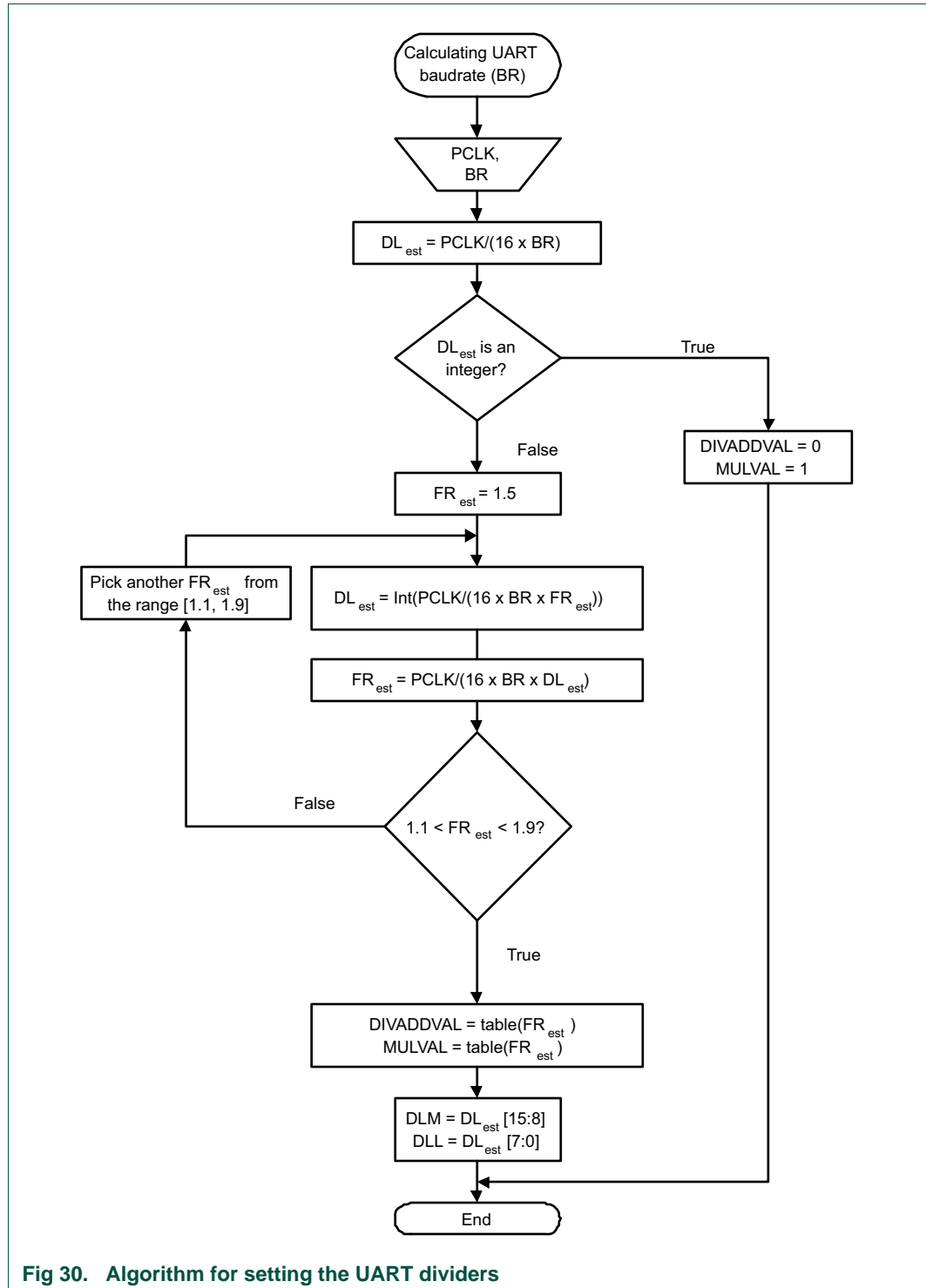


Fig 30. Algorithm for setting the UART dividers

Table 166. Fractional Divider setting look-up table

FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal	FR	DivAddVal/ MulVal
1.000	0/1	1.250	1/4	1.500	1/2	1.750	3/4
1.067	1/15	1.267	4/15	1.533	8/15	1.769	10/13
1.071	1/14	1.273	3/11	1.538	7/13	1.778	7/9
1.077	1/13	1.286	2/7	1.545	6/11	1.786	11/14
1.083	1/12	1.300	3/10	1.556	5/9	1.800	4/5
1.091	1/11	1.308	4/13	1.571	4/7	1.818	9/11
1.100	1/10	1.333	1/3	1.583	7/12	1.833	5/6
1.111	1/9	1.357	5/14	1.600	3/5	1.846	11/13
1.125	1/8	1.364	4/11	1.615	8/13	1.857	6/7
1.133	2/15	1.375	3/8	1.625	5/8	1.867	13/15
1.143	1/7	1.385	5/13	1.636	7/11	1.875	7/8
1.154	2/13	1.400	2/5	1.643	9/14	1.889	8/9
1.167	1/6	1.417	5/12	1.667	2/3	1.900	9/10
1.182	2/11	1.429	3/7	1.692	9/13	1.909	10/11
1.200	1/5	1.444	4/9	1.700	7/10	1.917	11/12
1.214	3/14	1.455	5/11	1.714	5/7	1.923	12/13
1.222	2/9	1.462	6/13	1.727	8/11	1.929	13/14
1.231	3/13	1.467	7/15	1.733	11/15	1.933	14/15

#### 10.7.4.1 Example 1: UART\_PCLK = 14.7456 MHz, BR = 9600

According to the provided algorithm  $DL_{est} = PCLK / (16 \times BR) = 14.7456 \text{ MHz} / (16 \times 9600) = 96$ . Since this  $DL_{est}$  is an integer number,  $DIVADDVAL = 0$ ,  $MULVAL = 1$ ,  $DLM = 0$ , and  $DLL = 96$ .

#### 10.7.4.2 Example 2: UART\_PCLK = 12.0 MHz, BR = 115200

According to the provided algorithm  $DL_{est} = PCLK / (16 \times BR) = 12 \text{ MHz} / (16 \times 115200) = 6.51$ . This  $DL_{est}$  is not an integer number and the next step is to estimate the FR parameter. Using an initial estimate of  $FR_{est} = 1.5$  a new  $DL_{est} = 4$  is calculated and  $FR_{est}$  is recalculated as  $FR_{est} = 1.628$ . Since  $FR_{est} = 1.628$  is within the specified range of 1.1 and 1.9,  $DIVADDVAL$  and  $MULVAL$  values can be obtained from the attached look-up table.

The closest value for  $FR_{est} = 1.628$  in the look-up [Table 166](#) is  $FR = 1.625$ . It is equivalent to  $DIVADDVAL = 5$  and  $MULVAL = 8$ .

Based on these findings, the suggested UART setup would be:  $DLM = 0$ ,  $DLL = 4$ ,  $DIVADDVAL = 5$ , and  $MULVAL = 8$ . According to [Equation 3](#), the UART's baud rate is 115384. This rate has a relative error of 0.16% from the originally specified 115200.

### 10.7.5 RS-485/EIA-485 modes of operation

The RS-485/EIA-485 feature allows the UART to be configured as an addressable slave. The addressable slave is one of multiple slaves controlled by a single master.

The UART master transmitter will identify an address character by setting the parity (9th) bit to '1'. For data characters, the parity bit is set to '0'.

Each UART slave receiver can be assigned a unique address. The slave can be programmed to either manually or automatically reject data following an address which is not theirs.

### RS-485/EIA-485 Normal Multidrop Mode

Setting the RS485CTRL bit 0 enables this mode. In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.

If the receiver is disabled (RS485CTRL bit 1 = '1'), any received data bytes will be ignored and will not be stored in the RXFIFO. When an address byte is detected (parity bit = '1') it will be placed into the RXFIFO and an Rx Data Ready Interrupt will be generated. The processor can then read the address byte and decide whether or not to enable the receiver to accept the following data.

While the receiver is enabled (RS485CTRL bit 1 = '0'), all received bytes will be accepted and stored in the RXFIFO regardless of whether they are data or address. When an address character is received a parity error interrupt will be generated and the processor can decide whether or not to disable the receiver.

### RS-485/EIA-485 Auto Address Detection (AAD) mode

When both RS485CTRL register bits 0 (9-bit mode enable) and 2 (AAD mode enable) are set, the UART is in auto address detect mode.

In this mode, the receiver will compare any address byte received (parity = '1') to the 8-bit value programmed into the RS485ADRMATCH register.

If the receiver is disabled (RS485CTRL bit 1 = '1'), any received byte will be discarded if it is either a data byte OR an address byte which fails to match the RS485ADRMATCH value.

When a matching address character is detected it will be pushed onto the RXFIFO along with the parity bit, and the receiver will be automatically enabled (RS485CTRL bit 1 will be cleared by hardware). The receiver will also generate an Rx Data Ready Interrupt.

While the receiver is enabled (RS485CTRL bit 1 = '0'), all bytes received will be accepted and stored in the RXFIFO until an address byte which does not match the RS485ADRMATCH value is received. When this occurs, the receiver will be automatically disabled in hardware (RS485CTRL bit 1 will be set). The received non-matching address character will not be stored in the RXFIFO.

### RS-485/EIA-485 Auto Direction Control

RS485/EIA-485 mode includes the option of allowing the transmitter to automatically control the state of the DIR pin as a direction control output signal.

Setting RS485CTRL bit 4 = '1' enables this feature.

Keep RS485CTRL bit 3 zero so that direction control, if enabled, will use the  $\overline{\text{RTS}}$  pin.

When Auto Direction Control is enabled, the selected pin will be asserted (driven LOW) when the CPU writes data into the TXFIFO. The pin will be de-asserted (driven HIGH) once the last bit of data has been transmitted. See bits 4 and 5 in the RS485CTRL register.

The RS485CTRL bit 4 takes precedence over all other mechanisms controlling the direction control pin with the exception of loopback mode.

#### RS485/EIA-485 driver delay time

The driver delay time is the delay between the last stop bit leaving the TXFIFO and the de-assertion of  $\overline{\text{RTS}}$ . This delay time can be programmed in the 8-bit RS485DLY register. The delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be used.

#### RS485/EIA-485 output inversion

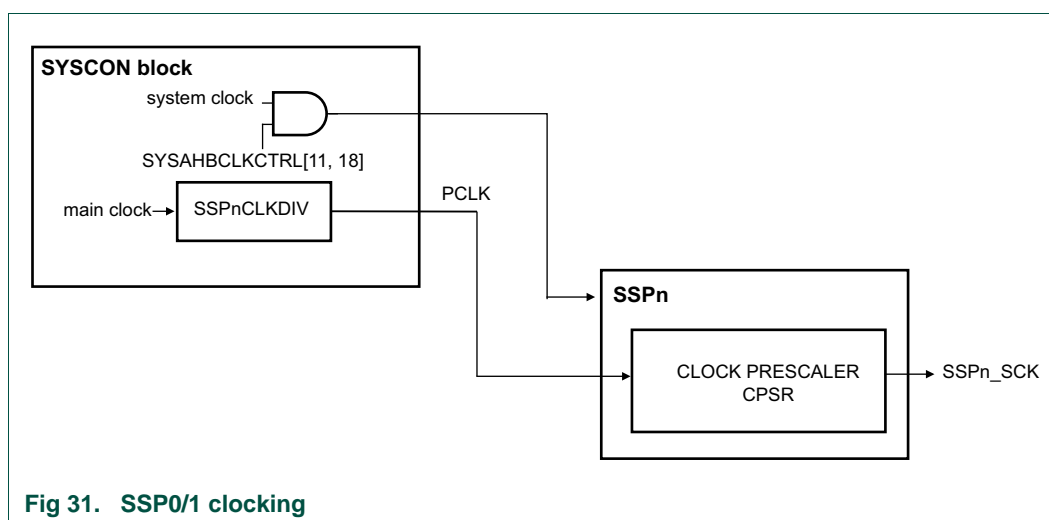
The polarity of the direction control signal on the  $\overline{\text{RTS}}$  (or  $\overline{\text{DTR}}$ ) pins can be reversed by programming bit 5 in the RS485CTRL register. When this bit is set, the direction control pin will be driven to logic 1 when the transmitter has data waiting to be sent. The direction control pin will be driven to logic 0 after the last bit of data has been transmitted.

## 11.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Supports master or slave operation.
- Eight-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

## 11.2 Basic configuration

1. Pins: The SSP pins must be configured in the IOCON register block.
2. Power: In the SYSAHBCLKCTRL register, set bit 11 for SSP0 and bit 18 for SSP1 ([Table 19](#)).
3. Peripheral clock: Enable the SSP0/SSP1 peripheral clocks by writing to the SSP0/1CLKDIV registers ([Table 20/](#)[Table 22](#)).
4. Reset: Before accessing the SSP block, ensure that the SSP0/1\_RST\_N bits (bit 0 and bit 2) in the PRESETCTRL register ([Table 7](#)) are set to 1. This de-asserts the reset signal to the SSP block.



## 11.3 General description

The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

## 11.4 Pin description

Table 167. SSP pin descriptions

Pin name	Type	Interface pin name/function			Pin description
		SPI	SSI	Microwire	
SSP0_SCK, SSP1_SCK	I/O	SCK	CLK	SK	<b>Serial Clock.</b> SCK/CLK/SK is a clock signal used to synchronize the transfer of data. It is driven by the master and received by the slave. When SSP interface is used, the clock is programmable to be active-high or active-low, otherwise it is always active-high. SCK only switches during a data transfer. Any other time, the SSP interface either holds it in its inactive state or does not drive it (leaves it in high-impedance state).
SSP0_SSEL, SSP1_SSEL	I/O	SSEL	FS	CS	<b>Frame Sync/Slave Select.</b> When the SSP interface is a bus master, it drives this signal to an active state before the start of serial data and then releases it to an inactive state after the data has been sent. The active state of this signal can be high or low depending upon the selected bus and mode. When the SSP interface is a bus slave, this signal qualifies the presence of data from the Master according to the protocol in use.  When there is just one bus master and one bus slave, the Frame Sync or Slave Select signal from the Master can be connected directly to the slave's corresponding input. When there is more than one slave on the bus, further qualification of their Frame Select/Slave Select inputs will typically be necessary to prevent more than one slave from responding to a transfer.
SSP0_MISO, SSP1_MISO	I/O	MISO	DR(M) DX(S)	SI(M) SO(S)	<b>Master In Slave Out.</b> The MISO signal transfers serial data from the slave to the master. When the SSP is a slave, serial data is output on this signal. When the SSP is a master, it clocks in serial data from this signal. When the SSP is a slave and is not selected by FS/SSEL, it does not drive this signal (leaves it in high-impedance state).
SSP0_MOSI, SSP1_MOSI	I/O	MOSI	DX(M) DR(S)	SO(M) SI(S)	<b>Master Out Slave In.</b> The MOSI signal transfers serial data from the master to the slave. When the SSP is a master, it outputs serial data on this signal. When the SSP is a slave, it clocks in serial data from this signal.

## 11.5 Register description

The register addresses of the SSP controllers are shown in [Table 168](#).

The reset value reflects the data stored in used bits only. It does not include the content of reserved bits.

Table 168. Register overview: SSP0 (base address 0x4004 0000)

Name	Access	Address offset	Description	Reset value	Reference
CR0	R/W	0x000	Control register 0. Selects the serial clock rate, bus type, and data size.	0	<a href="#">Table 170</a>
CR1	R/W	0x004	Control register 1. Selects master/slave and other modes.	0	<a href="#">Table 171</a>
DR	R/W	0x008	Data register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	0	<a href="#">Table 172</a>

Table 168. Register overview: SSP0 (base address 0x4004 0000)

Name	Access	Address offset	Description	Reset value	Reference
SR	RO	0x00C	Status register	0x0000 0003	<a href="#">Table 173</a>
CPSR	R/W	0x010	Clock Prescale register	0	<a href="#">Table 174</a>
IMSC	R/W	0x014	Interrupt Mask Set and Clear register	0	<a href="#">Table 175</a>
RIS	RO	0x018	Raw Interrupt Status register	0x0000 0008	<a href="#">Table 176</a>
MIS	RO	0x01C	Masked Interrupt Status register	0	<a href="#">Table 177</a>
ICR	WO	0x020	SSPICR Interrupt Clear register	NA	<a href="#">Table 178</a>

Table 169. Register overview: SSP1 (base address 0x4005 8000)

Name	Access	Address offset	Description	Reset value	Reference
CR0	R/W	0x000	Control register 0. Selects the serial clock rate, bus type, and data size.	0	<a href="#">Table 170</a>
CR1	R/W	0x004	Control register 1. Selects master/slave and other modes.	0	<a href="#">Table 171</a>
DR	R/W	0x008	Data register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	0	<a href="#">Table 172</a>
SR	RO	0x00C	Status register	0x0000 0003	<a href="#">Table 173</a>
CPSR	R/W	0x010	Clock Prescale register	0	<a href="#">Table 174</a>
IMSC	R/W	0x014	Interrupt Mask Set and Clear register	0	<a href="#">Table 175</a>
RIS	RO	0x018	Raw Interrupt Status register	0x0000 0008	<a href="#">Table 176</a>
MIS	RO	0x01C	Masked Interrupt Status register	0	<a href="#">Table 177</a>
ICR	WO	0x020	SSPICR Interrupt Clear register	NA	<a href="#">Table 178</a>

### 11.5.1 SSP Control register 0

This register controls the basic operation of the SSP controller.

**Table 170. SSP Control register 0 (CR0, address 0x4004 0000 (SSP0) and 0x4005 8000 (SSP1)) bit description**

Bit	Symbol	Value	Description	Reset Value
3:0	DSS		Data Size Select. This field controls the number of bits transferred in each frame. Values 0000-0010 are not supported and should not be used.	0000
		0x3	4-bit transfer	
		0x4	5-bit transfer	
		0x5	6-bit transfer	
		0x6	7-bit transfer	
		0x7	8-bit transfer	
		0x8	9-bit transfer	
		0x9	10-bit transfer	
		0xA	11-bit transfer	
		0xB	12-bit transfer	
		0xC	13-bit transfer	
		0xD	14-bit transfer	
		0xE	15-bit transfer	
		0xF	16-bit transfer	
5:4	FRF		Frame Format.	00
		0x0	SPI	
		0x1	TI	
		0x2	Microwire	
		0x3	This combination is not supported and should not be used.	
6	CPOL		Clock Out Polarity. This bit is only used in SPI mode.	0
		0	Low. SSP controller maintains the bus clock low between frames.	
		1	High. SSP controller maintains the bus clock high between frames.	
7	CPHA		Clock Out Phase. This bit is only used in SPI mode.	0
		0	Away. SSP controller captures serial data on the first clock transition of the frame, that is, the transition <b>away from</b> the inter-frame state of the clock line.	
		1	Back. SSP controller captures serial data on the second clock transition of the frame, that is, the transition <b>back to</b> the inter-frame state of the clock line.	
15:8	SCR		Serial Clock Rate. The number of prescaler output clocks per bit on the bus, minus one. Given that CPSDVSR is the prescale divider, and the APB clock PCLK clocks the prescaler, the bit frequency is $PCLK / (CPSDVSR \times [SCR+1])$ .	0x00
31:16	-	-	Reserved	-

### 11.5.2 SSP Control register 1

This register controls certain aspects of the operation of the SSP controller.



**Table 171. SSP Control register 1 (CR1, address 0x4004 0004 (SSP0) and 0x4005 8004 (SSP1)) bit description**

Bit	Symbol	Value	Description	Reset Value
0	LBM		Loop Back Mode.	0
		0	Normal. During normal operation.	
		1	Loop back. Serial input is taken from the serial output (MOSI or MISO) rather than the serial input pin (MISO or MOSI respectively).	
1	SSE		SPI Enable.	0
		0	Disabled. The SSP controller is disabled.	
		1	Enabled. The SSP controller will interact with other devices on the serial bus. Software should write the appropriate control information to the other SSP registers and interrupt controller registers, before setting this bit.	
2	MS		Master/Slave Mode. This bit can only be written when the SSE bit is 0.	0
		0	Master. The SSP controller acts as a master on the bus, driving the SCLK, MOSI, and SSEL lines and receiving the MISO line.	
		1	Slave. The SSP controller acts as a slave on the bus, driving MISO line and receiving SCLK, MOSI, and SSEL lines.	
3	SOD		Slave Output Disable. This bit is relevant only in slave mode (MS = 1). If it is 1, this blocks this SSP controller from driving the transmit data line (MISO).	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 11.5.3 SSP Data register

Software can write data to be transmitted to this register and read data that has been received.

**Table 172. SSP Data register (DR, address 0x4004 0008 (SSP0) and 0x4005 8008 (SSP1)) bit description**

Bit	Symbol	Description	Reset Value
15:0	DATA	<p><b>Write:</b> software can write data to be sent in a future frame to this register whenever the TNF bit in the Status register is 1, indicating that the Tx FIFO is not full. If the Tx FIFO was previously empty and the SSP controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received). If the data length is less than 16 bit, software must right-justify the data written to this register.</p> <p><b>Read:</b> software can read data from this register whenever the RNE bit in the Status register is 1, indicating that the Rx FIFO is not empty. When software reads this register, the SSP controller returns data from the least recent frame in the Rx FIFO. If the data length is less than 16 bit, the data is right-justified in this field with higher order bits filled with 0s.</p>	0x0000
31:16	-	Reserved.	-

### 11.5.4 SSP Status register

This read-only register reflects the current status of the SSP controller.

**Table 173. SSP Status register (SR, address 0x4004 000C (SSP0) and 0x4005 800C (SSP1)) bit description**

Bit	Symbol	Description	Reset Value
0	TFE	Transmit FIFO Empty. This bit is 1 if the Transmit FIFO is empty, 0 if not.	1
1	TNF	Transmit FIFO Not Full. This bit is 0 if the Tx FIFO is full, 1 if not.	1
2	RNE	Receive FIFO Not Empty. This bit is 0 if the Receive FIFO is empty, 1 if not.	0
3	RFF	Receive FIFO Full. This bit is 1 if the Receive FIFO is full, 0 if not.	0
4	BSY	Busy. This bit is 0 if the SSP controller is idle, 1 if it is currently sending/receiving a frame and/or the Tx FIFO is not empty.	0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 11.5.5 SSP Clock Prescale register

This register controls the factor by which the Prescaler divides the SPI peripheral clock SPI\_PCLK to yield the prescaler clock that is, in turn, divided by the SCR factor in the SSPCR0 registers, to determine the bit clock.

**Table 174. SSP Clock Prescale register (CPSR, address 0x4004 0010 (SSP0) and 0x4005 8010 (SSP1)) bit description**

Bit	Symbol	Description	Reset Value
7:0	CPSDVSR	This even value between 2 and 254, by which SPI_PCLK is divided to yield the prescaler output clock. Bit 0 always reads as 0.	0
31:8	-	Reserved.	-

**Important:** the CPSR value must be properly initialized, or the SSP controller will not be able to transmit data correctly.

In Slave mode, the SPI clock rate provided by the master must not exceed 1/12 of the SPI peripheral clock selected. The content of the SSPnCPSR register is not relevant.

In master mode,  $CPSDVSR_{min} = 2$  or larger (even numbers only).

### 11.5.6 SSP Interrupt Mask Set/Clear register

This register controls whether each of the four possible interrupt conditions in the SSP controller are enabled.

**Table 175. SSP Interrupt Mask Set/Clear register (IMSC, address 0x4004 0014 (SSP0) and 0x4005 8014 (SSP1)) bit description**

Bit	Symbol	Description	Reset Value
0	RORIM	Software should set this bit to enable interrupt when a Receive Overrun occurs, that is, when the Rx FIFO is full and another frame is completely received. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTIM	Software should set this bit to enable interrupt when a Receive Time-out condition occurs. A Receive Time-out occurs when the Rx FIFO is not empty, and no has not been read for a time-out period. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPDVSr × [SCR+1]).	0
2	RXIM	Software should set this bit to enable interrupt when the Rx FIFO is at least half full.	0
3	TXIM	Software should set this bit to enable interrupt when the Tx FIFO is at least half empty.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 11.5.7 SSP Raw Interrupt Status register

This read-only register contains a 1 for each interrupt condition that is asserted, regardless of whether or not the interrupt is enabled in the IMSC registers.

**Table 176. SSP Raw Interrupt Status register (RIS, address 0x4004 0018 (SSP0) and 0x4005 8018 (SSP1)) bit description**

	Symbol	Description	Reset value
0	RORRIS	This bit is 1 if another frame was completely received while the Rx FIFO was full. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTRIS	This bit is 1 if the Rx FIFO is not empty, and has not been read for a time-out period. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPDVSr × [SCR+1]).	0
2	RXRIS	This bit is 1 if the Rx FIFO is at least half full.	0
3	TXRIS	This bit is 1 if the Tx FIFO is at least half empty.	1
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 11.5.8 SSP Masked Interrupt Status register

This read-only register contains a 1 for each interrupt condition that is asserted and enabled in the IMSC registers. When an SSP interrupt occurs, the interrupt service routine should read this register to determine the causes of the interrupt.

**Table 177. SSP Masked Interrupt Status register (MIS, address 0x4004 001C (SSP0) and 0x4005 801C (SSP1)) bit description**

Bit	Symbol	Description	Reset value
0	RORMIS	This bit is 1 if another frame was completely received while the Rx FIFO was full, and this interrupt is enabled.	0
1	RTMIS	This bit is 1 if the Rx FIFO is not empty, has not been read for a time-out period, and this interrupt is enabled. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at $PCLK / (CPSDVSR \times [SCR+1])$ .	0
2	RXMIS	This bit is 1 if the Rx FIFO is at least half full, and this interrupt is enabled.	0
3	TXMIS	This bit is 1 if the Tx FIFO is at least half empty, and this interrupt is enabled.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 11.5.9 SSP Interrupt Clear register

Software can write one or more ones to this write-only register, to clear the corresponding interrupt conditions in the SSP controller. Note that the other two interrupt conditions can be cleared by writing or reading the appropriate FIFO or disabled by clearing the corresponding bit in SSP IMSC registers.

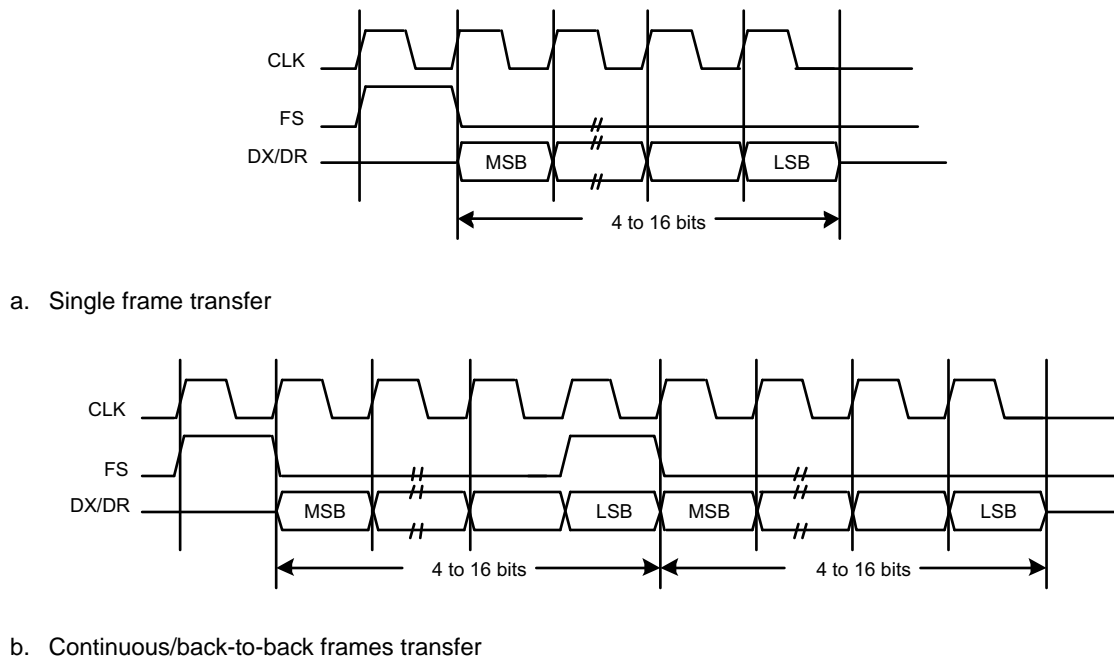
**Table 178. SSP interrupt Clear register (ICR, address 0x4004 0020 (SSP0) and 0x4005 8020 (SSP1)) bit description**

Bit	Symbol	Description	Reset Value
0	RORIC	Writing a 1 to this bit clears the “frame was received when Rx FIFO was full” interrupt.	NA
1	RTIC	Writing a 1 to this bit clears the Rx FIFO was not empty and has not been read for a timeout period interrupt. The timeout period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at $PCLK / (CPSDVSR \times [SCR+1])$ .	NA
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 11.6 Functional description

### 11.6.1 Texas Instruments serial frame format

[Figure 32](#) shows the 4-wire Texas Instruments synchronous serial frame format supported by the SPI module.



**Fig 32. Texas Instruments Synchronous Serial Frame Format: a) Single and b) Continuous/back-to-back two frames transfer**

For device configured as a master in this mode, CLK and FS are forced LOW, and the transmit data line DX is in 3-state mode whenever the SSP is idle. Once the bottom entry of the transmit FIFO contains data, FS is pulsed HIGH for one CLK period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of CLK, the MSB of the 4-bit to 16-bit data frame is shifted out on the DX pin. Likewise, the MSB of the received data is shifted onto the DR pin by the off-chip serial slave device.

Both the SSP and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each CLK. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of CLK after the LSB has been latched.

## 11.6.2 SPI frame format

The SPI interface is a four-wire interface where the SSEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits within the SSPCR0 control register.

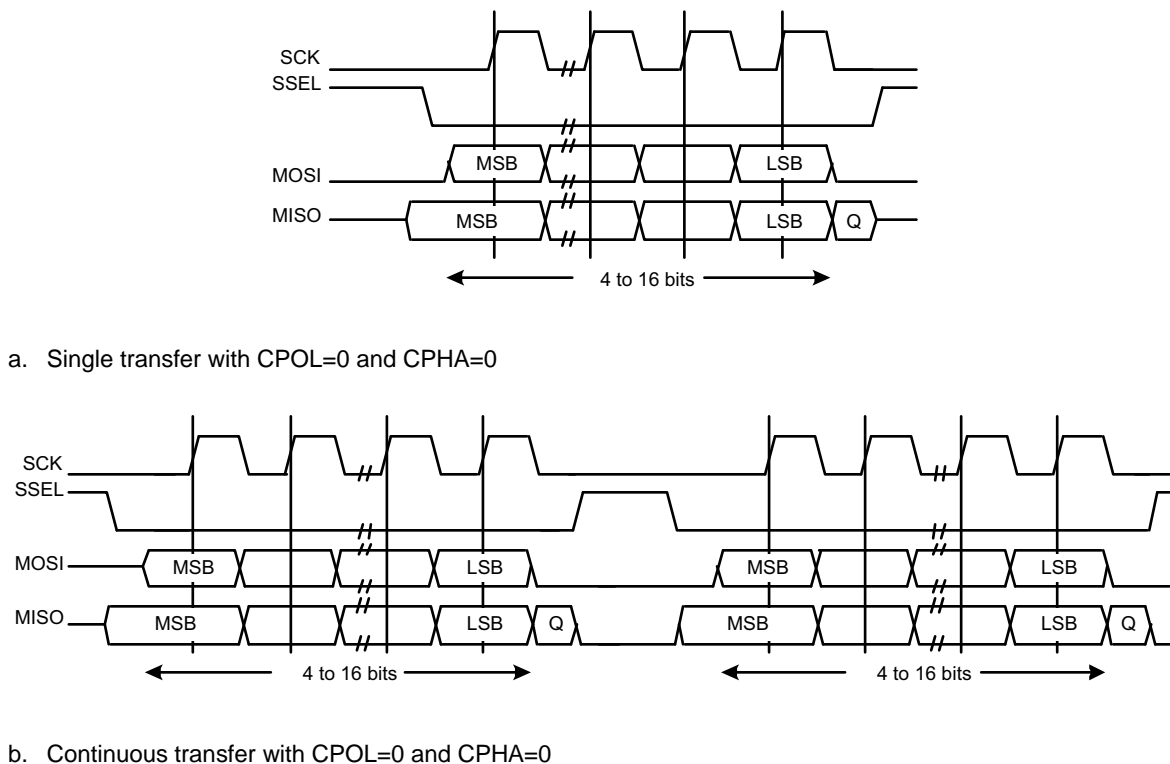
### 11.6.2.1 Clock Polarity (CPOL) and Phase (CPHA) control

When the CPOL clock polarity control bit is LOW, it produces a steady state low value on the SCK pin. If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred.

The CPHA control bit selects the clock edge that captures data and allows it to change state. It has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge. When the CPHA phase control bit is LOW, data is captured on the first clock edge transition. If the CPHA clock phase control bit is HIGH, data is captured on the second clock edge transition.

### 11.6.2.2 SPI format with CPOL=0,CPHA=0

Single and continuous transmission signal sequences for SPI format with CPOL = 0, CPHA = 0 are shown in [Figure 33](#).



**Fig 33. SPI frame format with CPOL=0 and CPHA=0 (a) single and b) continuous transfer**

In this configuration, during idle periods:

- The CLK signal is forced LOW.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. This causes slave data to be enabled onto the MISO input line of the master. Master's MOSI is enabled.

One half SCK period later, valid master data is transferred to the MOSI pin. Now that both the master and slave data have been set, the SCK master clock pin goes HIGH after one further half SCK period.

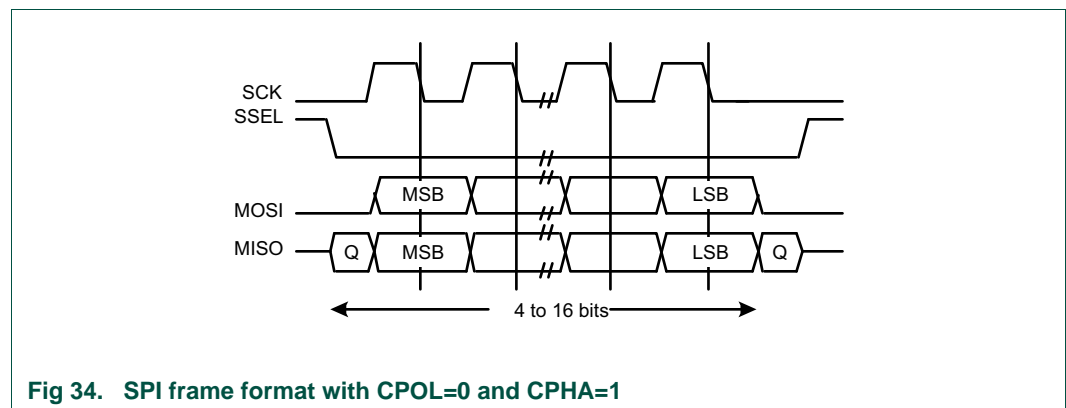
The data is captured on the rising and propagated on the falling edges of the SCK signal.

In the case of a single word transmission, after all bits of the data word have been transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSEL signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the CPHA bit is logic zero. Therefore the master device must raise the SSEL pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSEL pin is returned to its idle state one SCK period after the last bit has been captured.

### 11.6.2.3 SPI format with CPOL=0,CPHA=1

The transfer signal sequence for SPI format with CPOL = 0, CPHA = 1 is shown in [Figure 34](#), which covers both single and continuous transfers.



In this configuration, during idle periods:

- The CLK signal is forced LOW.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. Master's MOSI pin is enabled. After a further one half SCK period, both master and slave valid data is enabled onto their respective transmission lines. At the same time, the SCK is enabled with a rising edge transition.

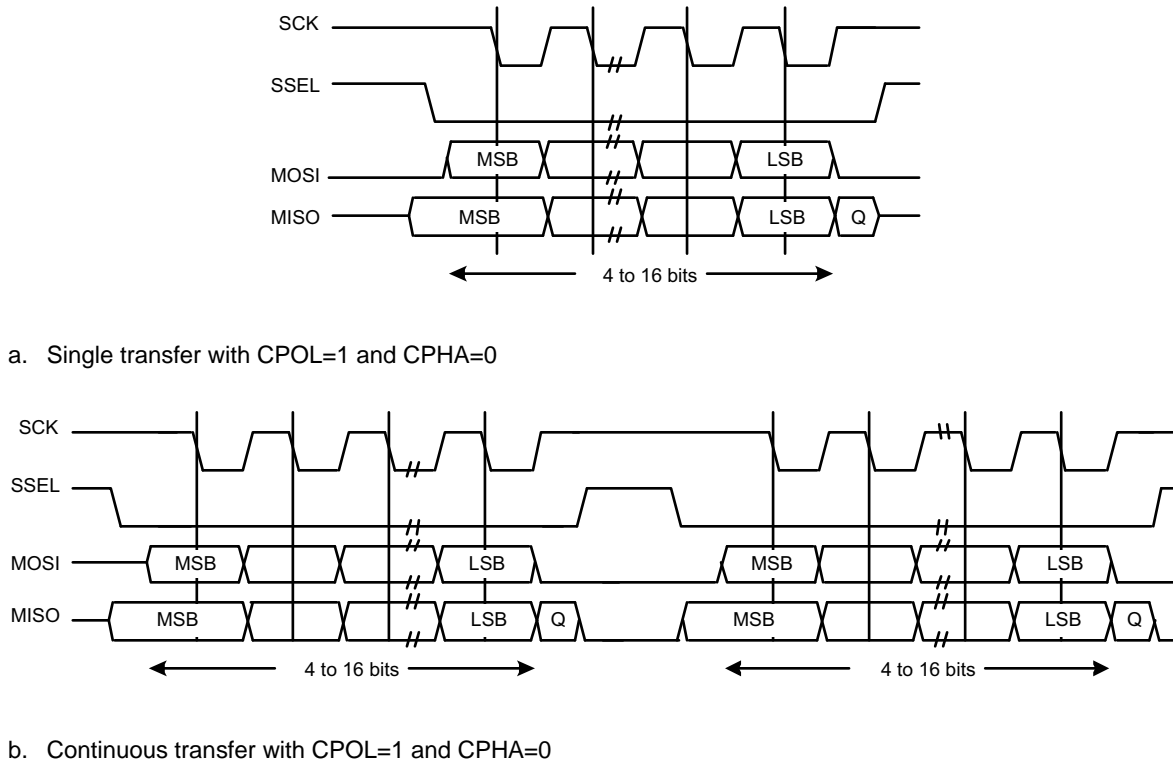
Data is then captured on the falling edges and propagated on the rising edges of the SCK signal.

In the case of a single word transfer, after all bits have been transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.

For continuous back-to-back transfers, the SSEL pin is held LOW between successive data words and termination is the same as that of the single word transfer.

#### 11.6.2.4 SPI format with CPOL = 1, CPHA = 0

Single and continuous transmission signal sequences for SPI format with CPOL=1, CPHA=0 are shown in [Figure 35](#).



**Fig 35. SPI frame format with CPOL = 1 and CPHA = 0 (a) Single and b) Continuous Transfer)**

In this configuration, during idle periods:

- The CLK signal is forced HIGH.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW, which causes slave data to be immediately transferred onto the MISO line of the master. Master's MOSI pin is enabled.

One half period later, valid master data is transferred to the MOSI line. Now that both the master and slave data have been set, the SCK master clock pin becomes LOW after one further half SCK period. This means that data is captured on the falling edges and be propagated on the rising edges of the SCK signal.

In the case of a single word transmission, after all bits of the data word are transferred, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured.



However, in the case of continuous back-to-back transmissions, the SSEL signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the CPHA bit is logic zero. Therefore the master device must raise the SSEL pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSEL pin is returned to its idle state one SCK period after the last bit has been captured.

#### 11.6.2.5 SPI format with CPOL = 1, CPHA = 1

The transfer signal sequence for SPI format with CPOL = 1, CPHA = 1 is shown in [Figure 36](#), which covers both single and continuous transfers.

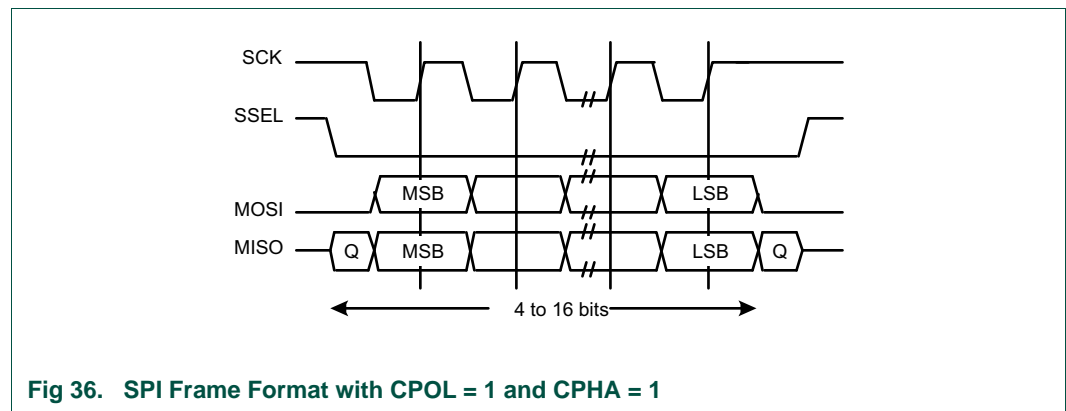


Fig 36. SPI Frame Format with CPOL = 1 and CPHA = 1

In this configuration, during idle periods:

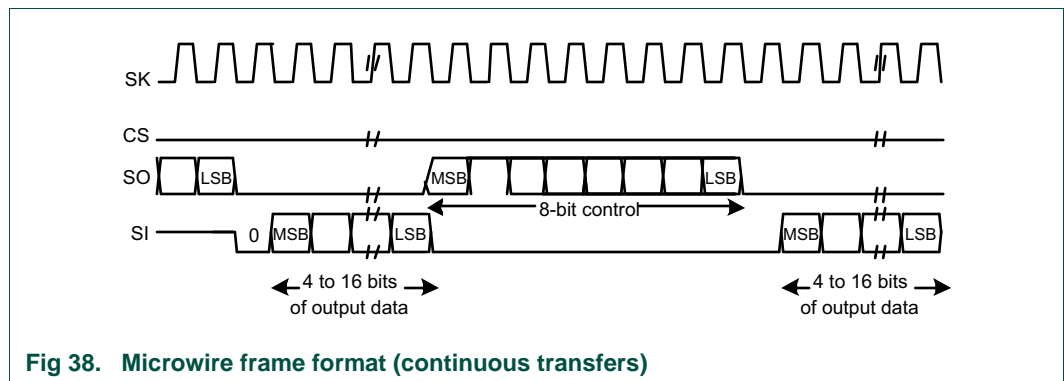
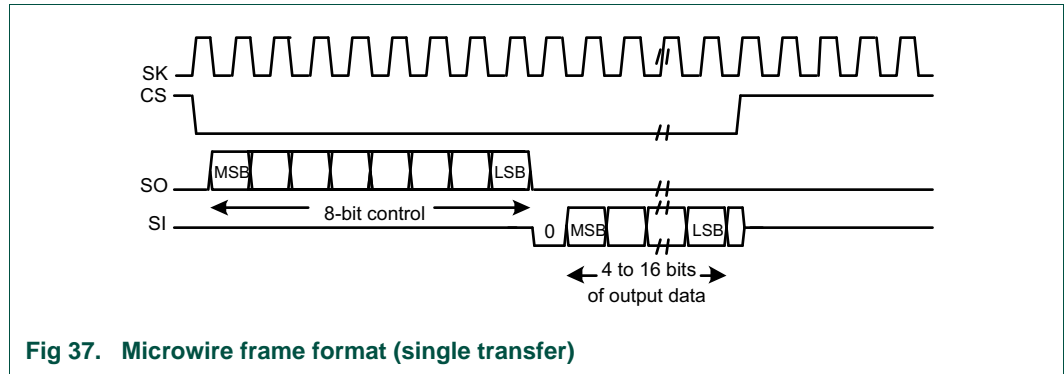
- The CLK signal is forced HIGH.
- SSEL is forced HIGH.
- The transmit MOSI/MISO pad is in high impedance.

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSEL master signal being driven LOW. Master's MOSI is enabled. After a further one half SCK period, both master and slave data are enabled onto their respective transmission lines. At the same time, the SCK is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SCK signal.

After all bits have been transferred, in the case of a single word transmission, the SSEL line is returned to its idle HIGH state one SCK period after the last bit has been captured. For continuous back-to-back transmissions, the SSEL pins remains in its active LOW state, until the final bit of the last word has been captured, and then returns to its idle state as described above. In general, for continuous back-to-back transfers the SSEL pin is held LOW between successive data words and termination is the same as that of the single word transfer.

#### 11.6.3 Semiconductor Microwire frame format

[Figure 37](#) shows the Microwire frame format for a single frame. [Figure 38](#) shows the same format when back-to-back frames are transmitted.



Microwire format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex, using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SSP to the off-chip slave device. During this transmission, no incoming data is received by the SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bit in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

- The SK signal is forced LOW.
- CS is forced HIGH.
- The transmit data line SO is arbitrarily forced LOW.

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of CS causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic, and the MSB of the 8-bit control frame to be shifted out onto the SO pin. CS remains LOW for the duration of the frame transmission. The SI pin remains tri-stated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on the rising edge of each SK. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SSP. Each bit is driven onto SI line on the falling edge of SK. The SSP in turn

latches each bit on the rising edge of SK. At the end of the frame, for single transfers, the CS signal is pulled HIGH one clock period after the last bit has been latched in the receive serial shifter, that causes the data to be transferred to the receive FIFO.

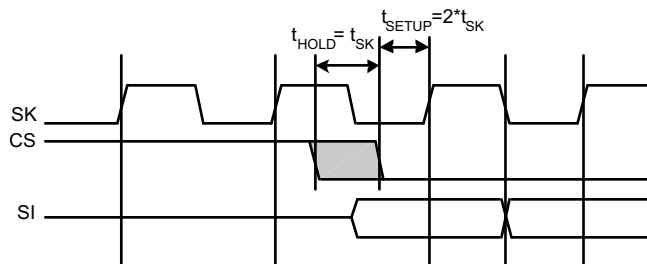
**Note:** The off-chip slave device can tri-state the receive line either on the falling edge of SK after the LSB has been latched by the receive shifter, or when the CS pin goes HIGH.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the CS line is continuously asserted (held LOW) and transmission of data occurs back to back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge SK, after the LSB of the frame has been latched into the SSP.

### 11.6.3.1 Setup and hold time requirements on CS with respect to SK in Microwire mode

In the Microwire mode, the SSP slave samples the first bit of receive data on the rising edge of SK after CS has gone LOW. Masters that drive a free-running SK must ensure that the CS signal has sufficient setup and hold margins with respect to the rising edge of SK.

[Figure 39](#) illustrates these setup and hold time requirements. With respect to the SK rising edge on which the first bit of receive data is to be sampled by the SSP slave, CS must have a setup of at least two times the period of SK on which the SSP operates. With respect to the SK rising edge previous to this edge, CS must have a hold of at least one SK period.



**Fig 39. Microwire frame format setup and hold details**

### 12.1 Features

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- Two 16-bit counter/timers with a programmable 16-bit prescaler.
- Counter or timer operation.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Two 16-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to three (CT16B0) or two (CT16B1) external outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- For each timer, up to four match registers can be configured as PWM allowing to use up to three match outputs as single edge controlled PWM outputs.

### 12.2 Basic configuration

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The CT16B0/1 are configured as follows:

- Pins: The CT16B0/1 pins must be configured in the IOCON register block.
- Power and peripheral clock: In the SYSAHBCLKCTRL register, set bit 7 and bit 8 ([Table 19](#)). The peripheral clock is provided by the system clock (see [Figure 3](#)).

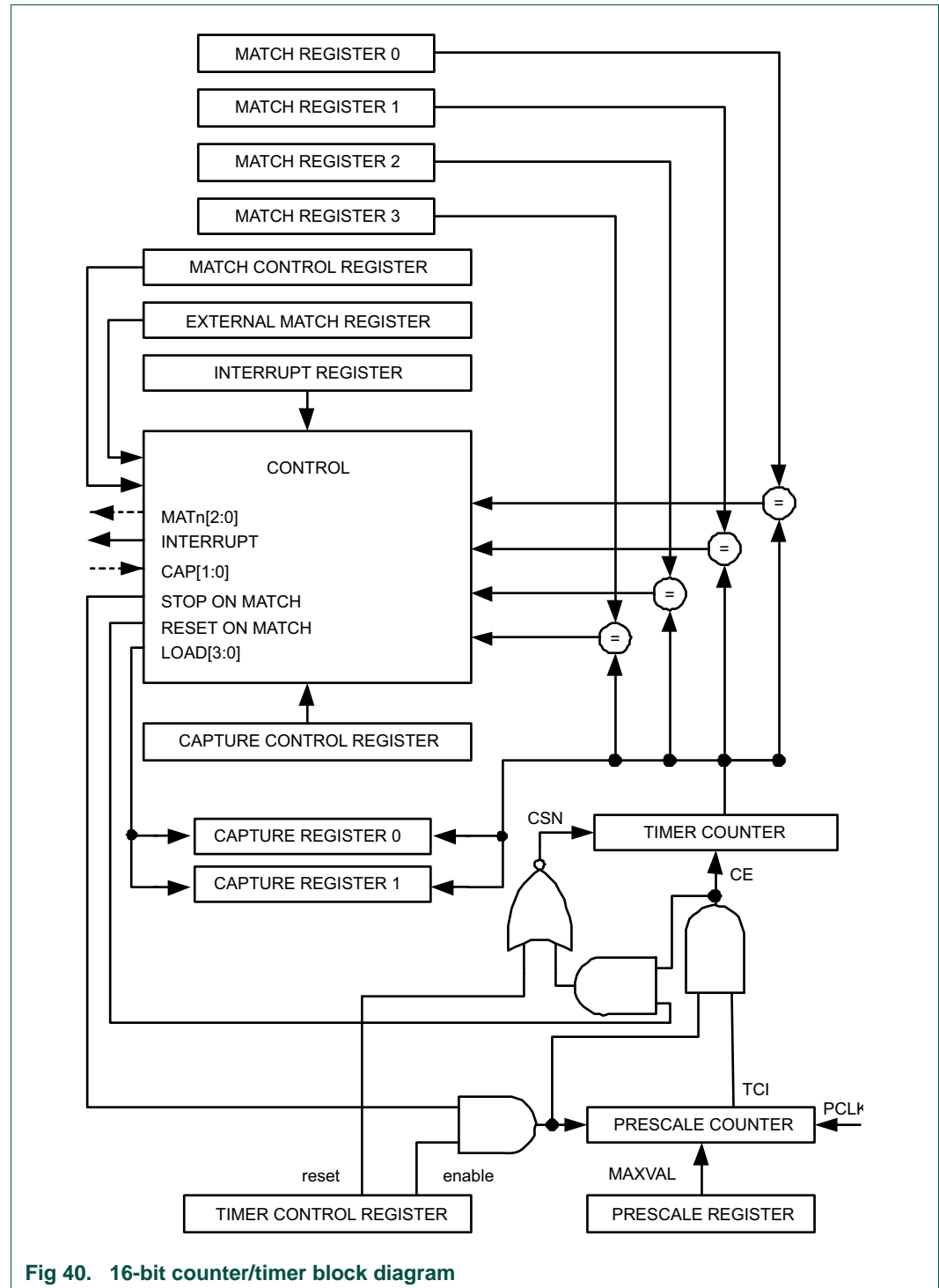
### 12.3 General description

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Each Counter/timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock (see [Figure 3](#)). Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, three match registers on CT16B0 and two match registers on CT16B1 can be used to provide a single-edge controlled PWM output on the match output pins. It is recommended to use the match registers that are not pinned out to control the PWM cycle length.

**Remark:** The 16-bit counter/timer0 (CT16B0) and the 16-bit counter/timer1 (CT16B1) are functionally identical except for the peripheral base address.



### 12.3.1 Applications

- Interval timer for counting internal events

- Pulse Width Demodulator via capture input
- Free-running timer
- Pulse Width Modulator via match outputs

## 12.4 Pin description

[Table 179](#) gives a brief summary of each of the counter/timer related pins.

**Table 179. Counter/timer pin description**

Pin	Type	Description
CT16B0_CAP[1:0] CT16B1_CAP0[1:0]	Input	Capture Signal: A transition on a capture pin can be configured to load the Capture register with the value in the counter/timer and optionally generate an interrupt.  Counter/Timer block can select a capture signal as a clock source instead of the PCLK derived clock. For more details see <a href="#">Section 12.5.11</a> .
CT16B0_MAT[2:0] CT16B1_MAT[1:0]	Output	External Match Outputs of CT16B0/1: When a match register of CT16B0/1 (MR3:0) equals the timer counter (TC), this output can either toggle, go LOW, go HIGH, or do nothing. The External Match register (EMR) and the PWM Control register (PWMC) control the functionality of this output.

## 12.5 Register description

The 16-bit counter/timer0 contains the registers shown in [Table 180](#) and the 16-bit counter/timer1 contains the registers shown in [Table 181](#). More detailed descriptions follow.

Reset value reflects the data stored in used bits only. It does not include reserved bits content.

**Table 180. Register overview: 16-bit counter/timer 0 CT16B0 (base address 0x4000 C000)**

Name	Access	Address offset	Description	Reset value	Reference
IR	R/W	0x000	Interrupt register (IR). The IR can be written to clear interrupts. The IR can be read to identify which of five possible interrupt sources are pending.	0	<a href="#">Table 182</a>
TCR	R/W	0x004	Timer Control register (TCR). The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	0	<a href="#">Table 183</a>
TC	R/W	0x008	Timer Counter (TC). The 16-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	0	<a href="#">Table 184</a>
PR	R/W	0x00C	Prescale register (PR). When the Prescale Counter (below) is equal to this value, the next clock increments the TC and clears the PC.	0	<a href="#">Table 185</a>
PC	R/W	0x010	Prescale Counter (PC). The 16-bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.	0	<a href="#">Table 186</a>
MCR	R/W	0x014	Match Control register (MCR). The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	0	<a href="#">Table 187</a>

**Table 180. Register overview: 16-bit counter/timer 0 CT16B0 (base address 0x4000 C000) ...continued**

Name	Access	Address offset	Description	Reset value	Reference
MR0	R/W	0x018	Match register 0 (MR0). MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	0	<a href="#">Table 188</a>
MR1	R/W	0x01C	Match register 1 (MR1).	0	<a href="#">Table 188</a>
MR2	R/W	0x020	Match register 2 (MR2).	0	<a href="#">Table 188</a>
MR3	R/W	0x024	Match register 3 (MR3).	0	<a href="#">Table 188</a>
CCR	R/W	0x028	Capture Control register (CCR). The CCR controls which edges of the capture inputs are used to load the Capture registers and whether or not an interrupt is generated when a capture takes place.	0	<a href="#">Table 189</a>
CR0	RO	0x02C	Capture register 0 (CR0). CR0 is loaded with the value of TC when there is an event on the CT16B0_CAP0 input.	0	<a href="#">Table 190</a>
CR1	RO	0x030	Capture register 1 (CR1). CR1 is loaded with the value of TC when there is an event on the CT16B0_CAP1 input.	0	<a href="#">Table 190</a>
-	-	0x034 - 0x038	Reserved	-	-
EMR	R/W	0x03C	External Match register (EMR). The EMR controls the match function and the external match pins CT16B0_MAT[2:0].	0	<a href="#">Table 191</a>
-	-	0x040 - 0x06C	Reserved	-	-
CTCR	R/W	0x070	Count Control register (CTCR). The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	0	<a href="#">Table 193</a>
PWMC	R/W	0x074	PWM Control register (PWMCON). The PWMCON enables PWM mode for the external match pins CT16B0_MAT[2:0].	0	<a href="#">Table 194</a>

**Table 181. Register overview: 16-bit counter/timer 1 CT16B1 (base address 0x4001 0000)**

Name	Access	Address offset	Description	Reset value	Reference
IR	R/W	0x000	Interrupt register (IR). The IR can be written to clear interrupts. The IR can be read to identify which of five possible interrupt sources are pending.	0	<a href="#">Table 182</a>
TCR	R/W	0x004	Timer Control register (TCR). The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	0	<a href="#">Table 183</a>
TC	R/W	0x008	Timer Counter (TC). The 16-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	0	<a href="#">Table 184</a>
PR	R/W	0x00C	Prescale register (PR). When the Prescale Counter (below) is equal to this value, the next clock increments the TC and clears the PC.	0	<a href="#">Table 185</a>
PC	R/W	0x010	Prescale Counter (PC). The 16-bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.	0	<a href="#">Table 186</a>

Table 181. Register overview: 16-bit counter/timer 1 CT16B1 (base address 0x4001 0000) ...continued

Name	Access	Address offset	Description	Reset value	Reference
MCR	R/W	0x014	Match Control register (MCR). The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	0	<a href="#">Table 187</a>
MR0	R/W	0x018	Match register 0 (MR0). MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	0	<a href="#">Table 188</a>
MR1	R/W	0x01C	Match register 1 (MR1). See MR0 description.	0	<a href="#">Table 188</a>
MR2	R/W	0x020	Match register 2 (MR2). See MR0 description.	0	<a href="#">Table 188</a>
MR3	R/W	0x024	Match register 3 (MR3). See MR0 description.	0	<a href="#">Table 188</a>
CCR	R/W	0x028	Capture Control register (CCR). The CCR controls which edges of the capture inputs are used to load the Capture registers and whether or not an interrupt is generated when a capture takes place.	0	<a href="#">Table 189</a>
CR0	RO	0x02C	Capture register 0 (CR0). CR0 is loaded with the value of TC when there is an event on the CT16B1_CAP0 input.	0	<a href="#">Table 190</a>
CR1	RO	0x030	Capture register 1 (CR1). CR1 is loaded with the value of TC when there is an event on the CT16B1_CAP1 input.	0	<a href="#">Table 190</a>
-	-	0x034 - 0x038	Reserved	-	-
EMR	R/W	0x03C	External Match register (EMR). The EMR controls the match function and the external match pins CT16B1_MAT[1:0].	0	<a href="#">Table 191</a>
-	-	0x040 - 0x06C	Reserved	-	-
CTCR	R/W	0x070	Count Control register (CTCR). The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	0	<a href="#">Table 193</a>
PWMC	R/W	0x074	PWM Control register (PWMCON). The PWMCON enables PWM mode for the external match pins CT16B1_MAT[1:0].	0	<a href="#">Table 194</a>

### 12.5.1 Interrupt register

The Interrupt register (IR) consists of four bits for the match interrupts and one bit for the capture interrupt. If an interrupt is generated then the corresponding bit in the IR will be HIGH. Otherwise, the bit will be LOW. Writing a logic one to the corresponding IR bit will reset the interrupt. Writing a zero has no effect.

Table 182. Interrupt register (IR, 0x4000 C000 (CT16B0) and 0x4001 0000 (CT16B1)) bit description

Bit	Symbol	Description	Reset value
0	MR0INT	Interrupt flag for match channel 0.	0
1	MR1INT	Interrupt flag for match channel 1.	0
2	MR2INT	Interrupt flag for match channel 2.	0
3	MR3INT	Interrupt flag for match channel 3.	0



Table 182. Interrupt register (IR, 0x4000 C000 (CT16B0) and 0x4001 0000 (CT16B1)) bit description

Bit	Symbol	Description	Reset value
4	CR0INT	Interrupt flag for capture channel 0 event.	0
5	CR1INT	Interrupt flag for capture channel 1 event.	0
31:6	-	Reserved	-

## 12.5.2 Timer Control register

The Timer Control register (TCR) is used to control the operation of the counter/timer.

Table 183. Timer Control register (TCR, address 0x4000 C004 (CT16B0) and 0x4001 0004 (CT16B1)) bit description

Bit	Symbol	Description	Reset value
0	CEN	Counter Enable. When one, the Timer Counter and Prescale Counter are enabled for counting. When zero, the counters are disabled.	0
1	CRST	Counter Reset. When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 12.5.3 Timer Counter

The 16-bit Timer Counter is incremented when the Prescale Counter reaches its terminal count. Unless it is reset before reaching its upper limit, the TC will count up through the value 0x0000 FFFF and then wrap back to the value 0x0000 0000. This event does not cause an interrupt, but a Match register can be used to detect an overflow if needed.

Table 184. Timer counter registers (TC, address 0x4000 C008 (CT16B0) and 0x4001 0008 (CT16B1)) bit description

Bit	Symbol	Description	Reset value
15:0	TCVAL	Timer counter value.	0
31:16	-	Reserved.	-

## 12.5.4 Prescale register

The 16-bit Prescale register specifies the maximum value for the Prescale Counter.

Table 185. Prescale registers (PR, address 0x4000 C00C (CT16B0) and 0x4001 000C (CT16B1)) bit description

Bit	Symbol	Description	Reset value
15:0	PRVAL	Prescale max value.	0
31:16	-	Reserved.	-

### 12.5.5 Prescale Counter register

The 16-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship between the resolution of the timer and the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale register, the Timer Counter is incremented, and the Prescale Counter is reset on the next PCLK. This causes the TC to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

**Table 186. Prescale counter registers (PC, address 0x4001 C010 (CT16B0) and 0x4000 0010 (CT16B1)) bit description**

Bit	Symbol	Description	Reset value
15:0	PCVAL	Prescale counter value.	0
31:16	-	Reserved.	-

### 12.5.6 Match Control register

The Match Control register is used to control what operations are performed when one of the Match registers matches the Timer Counter. The function of each of the bits is shown in [Table 187](#).

**Table 187. Match Control register (MCR, address 0x4000 C014 (CT16B0) and 0x4001 0014 (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	MR0I		Interrupt on MR0: an interrupt is generated when MR0 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
1	MR0R		Reset on MR0: the TC will be reset if MR0 matches it.	0
		1	Enabled	
		0	Disabled	
2	MR0S		Stop on MR0: the TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC.	0
		1	Enabled	
		0	Disabled	
3	MR1I		Interrupt on MR1: an interrupt is generated when MR1 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
4	MR1R		Reset on MR1: the TC will be reset if MR1 matches it.	0
		1	Enabled	
		0	Disabled	
5	MR1S		Stop on MR1: the TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC.	0
		1	Enabled	
		0	Disabled	

**Table 187. Match Control register (MCR, address 0x4000 C014 (CT16B0) and 0x4001 0014 (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
6	MR2I		Interrupt on MR2: an interrupt is generated when MR2 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
7	MR2R		Reset on MR2: the TC will be reset if MR2 matches it.	0
		1	Enabled	
		0	Disabled	
8	MR2S		Stop on MR2: the TC and PC will be stopped and TCR[0] will be set to 0 if MR2 matches the TC.	0
		1	Enabled	
		0	Disabled	
9	MR3I		Interrupt on MR3: an interrupt is generated when MR3 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
10	MR3R		Reset on MR3: the TC will be reset if MR3 matches it.	0
		1	Enabled	
		0	Disabled	
11	MR3S		Stop on MR3: the TC and PC will be stopped and TCR[0] will be set to 0 if MR3 matches the TC.	0
		1	Enabled	
		0	Disabled	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 12.5.7 Match registers

The Match register values are continuously compared to the Timer Counter value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the MCR register.

**Table 188. Match registers (MR[0:3], addresses 0x4000 C018 (MR0) to 0x4000 C024 (MR3) (CT16B0) and 0x4001 0018 (MR0) to 0x4001 0024 (MR3) (CT16B1)) bit description**

Bit	Symbol	Description	Reset value
15:0	MATCH	Timer counter match value.	0
31:16	-	Reserved.	-

### 12.5.8 Capture Control register

The Capture Control register is used to control whether the Capture register is loaded with the value in the Counter/timer when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges. In the description below, n represents the Timer number, 0 or 1.

**Table 189. Capture Control register (CCR, address 0x4000 C028 (CT16B0) and 0x4001 0028 (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	CAP0RE		Capture on CT16Bn_CAP0 rising edge: a sequence of 0 then 1 on CT16Bn_CAP0 will cause CR0 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
1	CAP0FE		Capture on CT16Bn_CAP0 falling edge: a sequence of 1 then 0 on CT16Bn_CAP0 will cause CR0 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
2	CAP0I		Interrupt on CT16Bn_CAP0 event: a CR0 load due to a CT16Bn_CAP0 event will generate an interrupt.	0
		1	Enabled	
		0	Disabled	
3	CAP1RE		Capture on CT16Bn_CAP1 rising edge: a sequence of 0 then 1 on CT16Bn_CAP1 will cause CR1 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
4	CAP1FE		Capture on CT16Bn_CAP1 falling edge: a sequence of 1 then 0 on CT16Bn_CAP1 will cause CR1 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
5	CAP1I		Interrupt on CT16Bn_CAP1 event: a CR1 load due to a CT16Bn_CAP1 event will generate an interrupt.	0
		1	Enabled	
		0	Disabled	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 12.5.9 Capture register

Each Capture register is associated with a device pin and may be loaded with the counter/timer value when a specified event occurs on that pin. The settings in the Capture Control register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

**Table 190. Capture registers (CR[0:1], address 0x4000 C02C (CR0) to 0x4000 C030 (CR1) (CT16B0) and 0x4001 002C (CR0) to 0x4001 0030 (CR1) (CT16B1)) bit description**

Bit	Symbol	Description	Reset value
15:0	CAP	Timer counter capture value.	0
31:16	-	Reserved.	-

### 12.5.10 External Match register

The External Match register provides both control and status of the external match channels and external match pins CT16B0\_MAT[2:0] and CT16B1\_MAT[1:0].

If the match outputs are configured as PWM output in the PWMCON registers ([Section 12.5.12](#)), the function of the external match registers is determined by the PWM rules ([Section 12.6.1 “Rules for single edge controlled PWM outputs”](#)).

**Table 191. External Match register (EMR, 0x4000 C03C (CT16B0) and 0x4001 003C (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	EM0		External Match 0. This bit reflects the state of output CT16B0_MAT0/CT16B1_MAT0, whether or not this output is connected to its pin. When a match occurs between the TC and MR0, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[5:4] control the functionality of this output. This bit is driven to the CT16B0_MAT0/CT16B1_MAT0 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
1	EM1		External Match 1. This bit reflects the state of output CT16B0_MAT1/CT16B1_MAT1, whether or not this output is connected to its pin. When a match occurs between the TC and MR1, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[7:6] control the functionality of this output. This bit is driven to the CT16B0_MAT1/CT16B1_MAT1 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
2	EM2		External Match 2. This bit reflects the state of output match channel 2, whether or not this output is connected to its pin. When a match occurs between the TC and MR2, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[9:8] control the functionality of this output. Note that on counter/timer 0 this match channel is not pinned out. This bit is driven to the CT16B1_MAT2 pin if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
3	EM3		External Match 3. This bit reflects the state of output of match channel 3. When a match occurs between the TC and MR3, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[11:10] control the functionality of this output. There is no output pin available for this channel on either of the 16-bit timers.	0
5:4	EMC0		External Match Control 0. Determines the functionality of External Match 0.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (CT16Bn_MATm pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (CT16Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
7:6	EMC1		External Match Control 1. Determines the functionality of External Match 1.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (CT16Bn_MATm pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (CT16Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
9:8	EMC2		External Match Control 2. Determines the functionality of External Match 2.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (CT16Bn_MATm pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (CT16Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	

Table 191. External Match register (EMR, 0x4000 C03C ((CT16B0) and 0x4001 003C (CT16B1)) bit description

Bit	Symbol	Value	Description	Reset value
11:10	EMC3		External Match Control 3. Determines the functionality of External Match 3.	00
		0x0	Do Nothing.	
		0x1	Clear the corresponding External Match bit/output to 0 (CT16Bn_MATm pin is LOW if pinned out).	
		0x2	Set the corresponding External Match bit/output to 1 (CT16Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle the corresponding External Match bit/output.	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 192. External match control

EMR[11:10], EMR[9:8], EMR[7:6], or EMR[5:4]	Function
00	Do Nothing.
01	Clear the corresponding External Match bit/output to 0 (CT16Bn_MATm pin is LOW if pinned out).
10	Set the corresponding External Match bit/output to 1 (CT16Bn_MATm pin is HIGH if pinned out).
11	Toggle the corresponding External Match bit/output.

### 12.5.11 Count Control register

The Count Control register (CTCR) is used to select between Timer and Counter mode, and in Counter mode to select the pin and edge(s) for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by the CTCR bits 3:2) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event occurs, and the event corresponds to the one selected by bits 1:0 in the CTCR register, will the Timer Counter register be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input can not exceed one half of the PCLK clock. Consequently, duration of the HIGH/LOW levels on the same CAP input in this case can not be shorter than  $1/(2 \times \text{PCLK})$ .

Bits 7:4 of this register are used to enable and configure the capture-clears-timer feature. This feature allows for a designated edge on a particular CAP input to reset the timer to all zeros. Using this mechanism to clear the timer on the leading edge of an input pulse and performing a capture on the trailing edge permits direct pulse-width measurement using a single capture input without the need to perform a subtraction operation in software.

**Table 193. Count Control register (CTCR, 0x4000 C070 (CT16B0) and 0x4001 0070 (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	CTM		Counter/Timer Mode. This field selects which rising PCLK edges can increment Timer's Prescale Counter (PC), or clear PC and increment Timer Counter (TC).	00
		0x0	Timer Mode: every rising PCLK edge	
		0x1	Counter Mode: TC is incremented on rising edges on the CAP input selected by bits 3:2.	
		0x2	Counter Mode: TC is incremented on falling edges on the CAP input selected by bits 3:2.	
		0x3	Counter Mode: TC is incremented on both edges on the CAP input selected by bits 3:2.	
3:2	CIS		Count Input Select. In counter mode (when bits 1:0 in this register are not 00), these bits select which CAP pin is sampled for clocking. <b>Note:</b> If Counter mode is selected in the CTCR register, bits 2:0 in the Capture Control register (CCR) must be programmed as 000.	00
		0x0	CT16Bn_CAP0	
		0x1	CT16Bn_CAP1	
		0x2	Reserved.	
		0x3	Reserved.	
4	ENCC		Setting this bit to one enables clearing of the timer and the prescaler when the capture-edge event specified in bits 7:5 occurs.	0
7:5	SELCC		When bit 4 is one, these bits select which capture input edge will cause the timer and prescaler to be cleared. These bits have no effect when bit 4 is zero.	0
		0x0	Rising Edge of CAP0 clears the timer (if bit 4 is set).	
		0x1	Falling Edge of CAP0 clears the timer (if bit 4 is set).	
		0x2	Rising Edge of CAP1 clears the timer (if bit 4 is set).	
		0x3	Falling Edge of CAP1 clears the timer (if bit 4 is set).	
		0x4	Reserved.	
		0x5	Reserved.	
		0x6	Reserved.	
		0x7	Reserved.	
31:8	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

### 12.5.12 PWM Control register

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by the External Match register (EMR).

For timer 0, three single-edge controlled PWM outputs can be selected on the CT16B0\_MAT[2:0] outputs. For timer 1, two single-edged PWM outputs can be selected on the CT16B1\_Mat[1:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

**Table 194. PWM Control register (PWMC, 0x4000 C074 (CT16B0) and 0x4001 0074 (CT16B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	PWMEN0		PWM channel0 enable	0
		0	CT16Bn_MAT0 is controlled by EM0.	
		1	PWM mode is enabled for CT16Bn_MAT0.	
1	PWMEN1		PWM channel1 enable	0
		0	CT16Bn_MAT1 is controlled by EM1.	
		1	PWM mode is enabled for CT16Bn_MAT1.	
2	PWMEN2		PWM channel2 enable	0
		0	Match channel 2 or pin CT16B0_MAT2 is controlled by EM2. Match channel 2 is not pinned out on timer 1.	
		1	PWM mode is enabled for match channel 2 or pin CT16B0_MAT2.	
3	PWMEN3		PWM channel3 enable <b>Note:</b> It is recommended to use match channel 3 to set the PWM cycle because it is not pinned out.	0
		0	Match channel 3 match channel 3 is controlled by EM3.	
		1	PWM mode is enabled for match channel 3match channel 3.	
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 12.6 Functional description

[Figure 41](#) shows a timer configured to reset the count and generate an interrupt on match. The prescaler is set to 2 and the match register set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.

[Figure 42](#) shows a timer configured to stop and generate an interrupt on match. The prescaler is again set to 2 and the match register set to 6. In the next clock after the timer reaches the match value, the timer enable bit in TCR is cleared, and the interrupt indicating that a match occurred is generated.



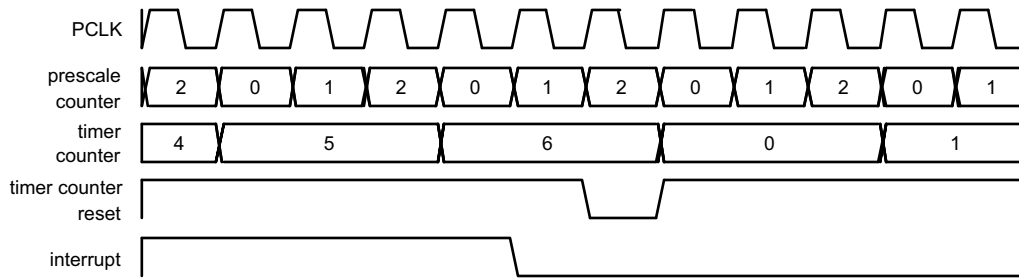


Fig 41. A timer cycle in which PR=2, MRx=6, and both interrupt and reset on match are enabled

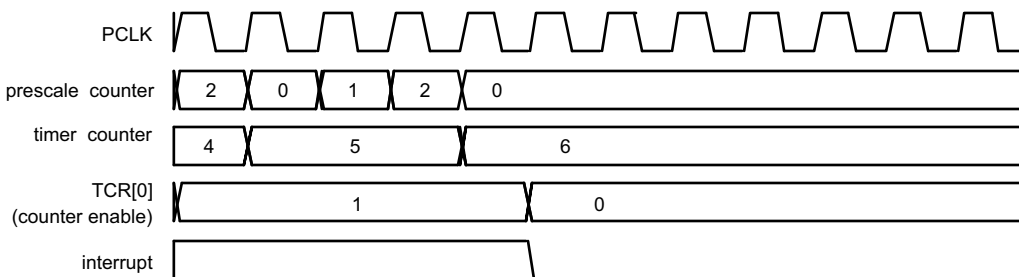
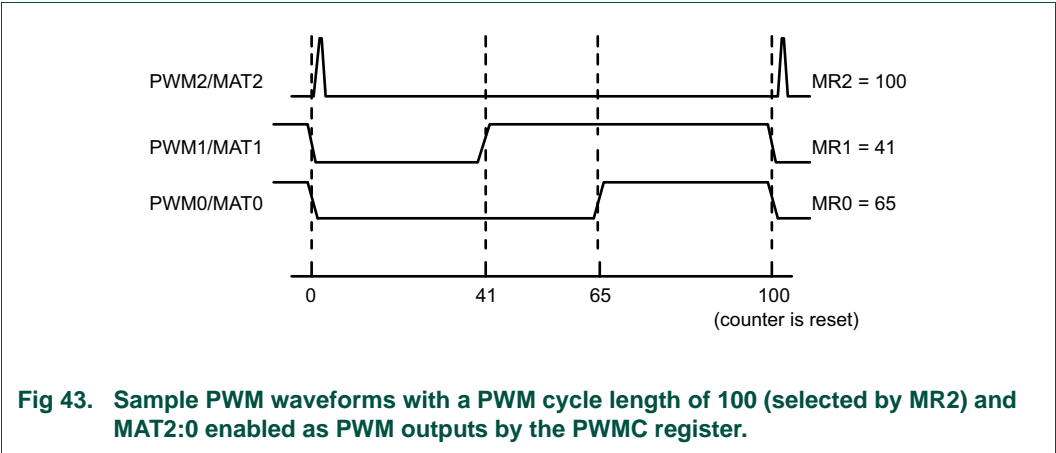


Fig 42. A timer cycle in which PR=2, MRx=6, and both interrupt and stop on match are enabled

### 12.6.1 Rules for single edge controlled PWM outputs

1. All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle (timer is set to zero) unless their match value is equal to zero.
2. Each PWM output will go HIGH when its match value is reached. If no match occurs (i.e. the match value is greater than the PWM cycle length), the PWM output remains continuously LOW.
3. If a match value larger than the PWM cycle length is written to the match register, and the PWM signal is HIGH already, then the PWM signal will be cleared on the next start of the next PWM cycle.
4. If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to LOW on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide positive pulse with a period determined by the PWM cycle length (i.e. the timer reload value).
5. If a match register is set to zero, then the PWM output will go to HIGH the first time the timer goes back to zero and will stay HIGH continuously.

**Note:** When the match outputs are selected to perform as PWM outputs, the timer reset (MRnR) and timer stop (MRnS) bits in the Match Control register MCR must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.



### 13.1 Features

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- Two 32-bit counter/timers with a programmable 32-bit prescaler.
- Counter or Timer operation.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Two 32-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- For each timer, up to four match registers can be configured as PWM allowing to use up to three match outputs as single edge controlled PWM outputs.

### 13.2 Basic configuration

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The CT32B0/1 are configured as follows:

- Pins: The CT32B0/1 pins must be configured in the IOCON register block.
- Power and peripheral clock: In the SYSAHBCLKCTRL register, set bit 9 and bit 10 ([Table 19](#)). The peripheral clock (PCLK) is provided by the system clock (see [Figure 3](#)).

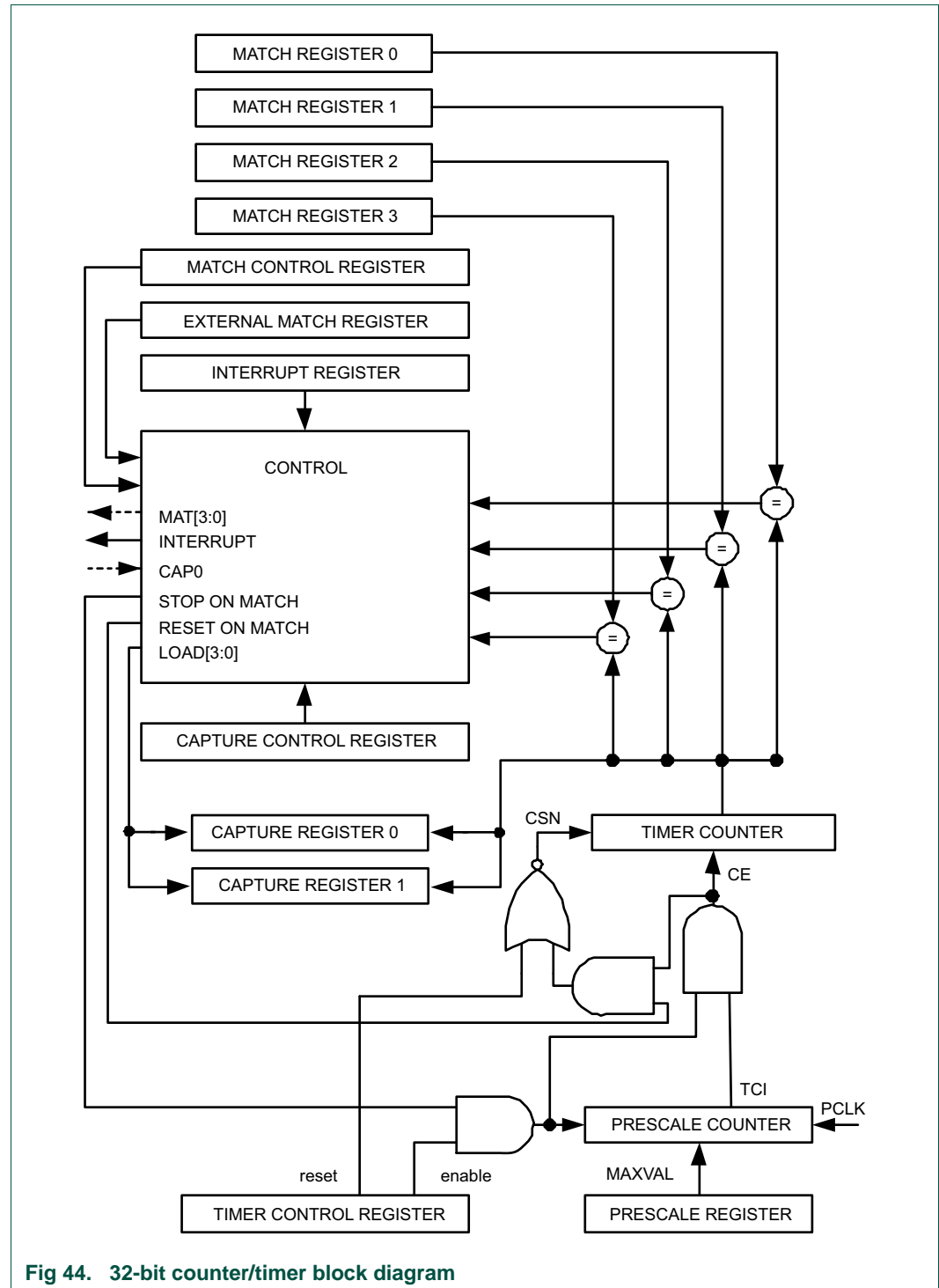
### 13.3 General description

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Each Counter/timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock (see [Figure 3](#)). Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, three match registers can be used to provide a single-edge controlled PWM output on the match output pins. One match register is used to control the PWM cycle length.

**Remark:** 32-bit counter/timer0 (CT32B0) and 32-bit counter/timer1 (CT32B1) are functionally identical except for the peripheral base address.



### 13.3.1 Applications

- Interval timer for counting internal events

- Pulse Width Demodulator via capture input
- Free running timer
- Pulse Width Modulator via match outputs

## 13.4 Pin description

[Table 195](#) gives a brief summary of each of the counter/timer related pins.

**Table 195. Counter/timer pin description**

Pin	Type	Description
CT32B0_CAP[1:0] CT32B1_CAP[1:0]	Input	Capture Signals: A transition on a capture pin can be configured to load one of the Capture registers with the value in the Timer Counter and optionally generate an interrupt.  The counter/timer block can select a capture signal as a clock source instead of the PCLK derived clock. For more details see <a href="#">Section 13.5.11 "Count Control register" on page 205</a> .
CT32B0_MAT[3:0] CT32B1_MAT[3:0]	Output	External Match Output of CT32B0/1: When a match register TMR32B0/1MR3:0 equals the timer counter (TC), this output can either toggle, go LOW, go HIGH, or do nothing. The External Match register (EMR) and the PWM Control register (PWMC) control the functionality of this output.

## 13.5 Register description

32-bit counter/timer0 contains the registers shown in [Table 196](#) and 32-bit counter/timer1 contains the registers shown in [Table 197](#). More detailed descriptions follow.

**Table 196. Register overview: 32-bit counter/timer 0 CT32B0 (base address 0x4001 4000)**

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>
IR	R/W	0x000	Interrupt register (IR). The IR can be written to clear interrupts. The IR can be read to identify which of five possible interrupt sources are pending.	0
TCR	R/W	0x004	Timer Control register (TCR). The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	0
TC	R/W	0x008	Timer Counter (TC). The 32-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	0
PR	R/W	0x00C	Prescale register (PR). When the Prescale Counter (below) is equal to this value, the next clock increments the TC and clears the PC.	0
PC	R/W	0x010	Prescale Counter (PC). The 32-bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.	0
MCR	R/W	0x014	Match Control register (MCR). The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	0
MR0	R/W	0x018	Match register 0 (MR0). MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	0
MR1	R/W	0x01C	Match register 1 (MR1). See MR0 description.	0
MR2	R/W	0x020	Match register 2 (MR2). See MR0 description.	0

Table 196. Register overview: 32-bit counter/timer 0 CT32B0 (base address 0x4001 4000) ...continued

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>
MR3	R/W	0x024	Match register 3 (MR3). See MR0 description.	0
CCR	R/W	0x028	Capture Control register (CCR). The CCR controls which edges of the capture inputs are used to load the Capture registers and whether or not an interrupt is generated when a capture takes place.	0
CR0	RO	0x02C	Capture register 0 (CR0). CR0 is loaded with the value of TC when there is an event on the CT32B0_CAP0 input.	0
CR1	RO	0x030	Capture register 1 (CR1). CR1 is loaded with the value of TC when there is an event on the CT32B0_CAP1 input.	0
-	-	0x034 - 0x038	Reserved	-
EMR	R/W	0x03C	External Match register (EMR). The EMR controls the match function and the external match pins CT32B0_MAT[3:0].	0
-	-	0x040 - 0x06C	Reserved	-
CTCR	R/W	0x070	Count Control register (CTCR). The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	0
PWMC	R/W	0x074	PWM Control register (PWMCON). The PWMCON enables PWM mode for the external match pins CT32B0_MAT[3:0].	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 197. Register overview: 32-bit counter/timer 1 CT32B1 (base address 0x4001 8000)

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>
IR	R/W	0x000	Interrupt register (IR). The IR can be written to clear interrupts. The IR can be read to identify which of five possible interrupt sources are pending.	0
TCR	R/W	0x004	Timer Control register (TCR). The TCR is used to control the Timer Counter functions. The Timer Counter can be disabled or reset through the TCR.	0
TC	R/W	0x008	Timer Counter (TC). The 32-bit TC is incremented every PR+1 cycles of PCLK. The TC is controlled through the TCR.	0
PR	R/W	0x00C	Prescale register (PR). When the Prescale Counter (below) is equal to this value, the next clock increments the TC and clears the PC.	0
PC	R/W	0x010	Prescale Counter (PC). The 32-bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared. The PC is observable and controllable through the bus interface.	0
MCR	R/W	0x014	Match Control register (MCR). The MCR is used to control if an interrupt is generated and if the TC is reset when a Match occurs.	0
MR0	R/W	0x018	Match register 0 (MR0). MR0 can be enabled through the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt every time MR0 matches the TC.	0
MR1	R/W	0x01C	Match register 1 (MR1). See MR0 description.	0
MR2	R/W	0x020	Match register 2 (MR2). See MR0 description.	0
MR3	R/W	0x024	Match register 3 (MR3). See MR0 description.	0

Table 197. Register overview: 32-bit counter/timer 1 CT32B1 (base address 0x4001 8000) ...continued

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>
CCR	R/W	0x028	Capture Control register (CCR). The CCR controls which edges of the capture inputs are used to load the Capture registers and whether or not an interrupt is generated when a capture takes place.	0
CR0	RO	0x02C	Capture register 0 (CR0). CR0 is loaded with the value of TC when there is an event on the CT32B1_CAP0 input.	0
CR1	RO	0x030	Capture register 1 (CR1). CR1 is loaded with the value of TC when there is an event on the CT32B1_CAP1 input.	0
-	-	0x034 - 0x038	Reserved	-
EMR	R/W	0x03C	External Match register (EMR). The EMR controls the match function and the external match pins CT32B1_MAT[3:0].	0
-	-	0x040 - 0x06C	Reserved	-
CTCR	R/W	0x070	Count Control register (CTCR). The CTCR selects between Timer and Counter mode, and in Counter mode selects the signal and edge(s) for counting.	0
PWMC	R/W	0x074	PWM Control register (PWMCON). The PWMCON enables PWM mode for the external match pins CT32B1_MAT[3:0].	0

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

### 13.5.1 Interrupt register

The Interrupt register consists of four bits for the match interrupts and one bit for the capture interrupts. If an interrupt is generated then the corresponding bit in the IR will be HIGH. Otherwise, the bit will be LOW. Writing a logic one to the corresponding IR bit will reset the interrupt. Writing a zero has no effect.

Table 198. Interrupt register (IR, address 0x4001 4000 (CT32B0) and 0x4001 8000 (CT32B1)) bit description

Bit	Symbol	Description	Reset value
0	MR0INT	Interrupt flag for match channel 0.	0
1	MR1INT	Interrupt flag for match channel 1.	0
2	MR2INT	Interrupt flag for match channel 2.	0
3	MR3INT	Interrupt flag for match channel 3.	0
4	CR0INT	Interrupt flag for capture channel 0 event.	0
5	CR1INT	Interrupt flag for capture channel 1 event.	0
31:6	-	Reserved	-

### 13.5.2 Timer Control register

The Timer Control register (TCR) is used to control the operation of the counter/timer.

**Table 199. Timer Control register (TCR, address 0x4001 4004 (CT32B0) and 0x4001 8004 (CT32B1)) bit description**

Bit	Symbol	Description	Reset value
0	CEN	When one, the Timer Counter and Prescale Counter are enabled for counting. When zero, the counters are disabled.	0
1	CRST	When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 13.5.3 Timer Counter register

The 32-bit Timer Counter is incremented when the Prescale Counter reaches its terminal count. Unless it is reset before reaching its upper limit, the TC will count up through the value 0xFFFF FFFF and then wrap back to the value 0x0000 0000. This event does not cause an interrupt, but a Match register can be used to detect an overflow if needed.

**Table 200. Timer counter registers (TC, address 0x4001 4008 and TMR32B1TC 0x4001 8008) bit description**

Bit	Symbol	Description	Reset value
31:0	TCVAL	Timer counter value.	0

### 13.5.4 Prescale register

The 32-bit Prescale register specifies the maximum value for the Prescale Counter.

**Table 201. Prescale registers (PR, address 0x4001 400C (CT32B0) and 0x4001 800C (CT32B1)) bit description**

Bit	Symbol	Description	Reset value
31:0	PRVAL	Prescale value.	0

### 13.5.5 Prescale Counter register

The 32-bit Prescale Counter controls division of PCLK by some constant value before it is applied to the Timer Counter. This allows control of the relationship between the resolution of the timer and the maximum time before the timer overflows. The Prescale Counter is incremented on every PCLK. When it reaches the value stored in the Prescale register, the Timer Counter is incremented, and the Prescale Counter is reset on the next PCLK. This causes the TC to increment on every PCLK when PR = 0, every 2 PCLKs when PR = 1, etc.

**Table 202. Prescale counter registers (PC, address 0x4001 4010 (CT32B0) and 0x4001 8010 (CT32B1)) bit description**

Bit	Symbol	Description	Reset value
31:0	PCVAL	Prescale counter value.	0



### 13.5.6 Match Control register

The Match Control register is used to control what operations are performed when one of the Match registers matches the Timer Counter. The function of each of the bits is shown in [Table 203](#).

**Table 203. Match Control register (MCR, address 0x4001 4014 (CT32B0) and 0x4001 8014 (CT32B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	MR0I		Interrupt on MR0: an interrupt is generated when MR0 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
1	MR0R		Reset on MR0: the TC will be reset if MR0 matches it.	0
		1	Enabled	
		0	Disabled	
2	MR0S		Stop on MR0: the TC and PC will be stopped and TCR[0] will be set to 0 if MR0 matches the TC.	0
		1	Enabled	
		0	Disabled	
3	MR1I		Interrupt on MR1: an interrupt is generated when MR1 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
4	MR1R		Reset on MR1: the TC will be reset if MR1 matches it.	0
		1	Enabled	
		0	Disabled	
5	MR1S		Stop on MR1: the TC and PC will be stopped and TCR[0] will be set to 0 if MR1 matches the TC.	0
		1	Enabled	
		0	Disabled	
6	MR2I		Interrupt on MR2: an interrupt is generated when MR2 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
7	MR2R		Reset on MR2: the TC will be reset if MR2 matches it.	0
		1	Enabled	
		0	Disabled	
8	MR2S		Stop on MR2: the TC and PC will be stopped and TCR[0] will be set to 0 if MR2 matches the TC.	0
		1	Enabled	
		0	Disabled	
9	MR3I		Interrupt on MR3: an interrupt is generated when MR3 matches the value in the TC.	0
		1	Enabled	
		0	Disabled	
10	MR3R		Reset on MR3: the TC will be reset if MR3 matches it.	0
		1	Enabled	
		0	Disabled	

Table 203. Match Control register (MCR, address 0x4001 4014 (CT32B0) and 0x4001 8014 (CT32B1)) bit description

Bit	Symbol	Value	Description	Reset value
11	MR3S		Stop on MR3: the TC and PC will be stopped and TCR[0] will be set to 0 if MR3 matches the TC.	0
		1	Enabled	
		0	Disabled	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 13.5.7 Match registers

The Match register values are continuously compared to the Timer Counter value. When the two values are equal, actions can be triggered automatically. The action possibilities are to generate an interrupt, reset the Timer Counter, or stop the timer. Actions are controlled by the settings in the MCR register.

Table 204. Match registers (MR[0:3], addresses 0x4001 4018 (MR0) to 0x4001 4024 (MR3) (CT32B0) and 0x4001 8018 (MR0) to 0x4001 8024 (MR3) (CT32B1)) bit description

Bit	Symbol	Description	Reset value
31:0	MATCH	Timer counter match value.	0

### 13.5.8 Capture Control register

The Capture Control register is used to control whether the Capture register is loaded with the value in the Timer Counter when the capture event occurs, and whether an interrupt is generated by the capture event. Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges. In the description below, “n” represents the Timer number, 0 or 1.

Table 205. Capture Control register (CCR, address 0x4001 4028 (CT32B0) and 0x4001 8028 (CT32B1)) bit description

Bit	Symbol	Value	Description	Reset value
0	CAP0RE		Capture on CT32Bn_CAP0 rising edge: a sequence of 0 then 1 on CT32Bn_CAP0 will cause CR0 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
1	CAP0FE		Capture on CT32Bn_CAP0 falling edge: a sequence of 1 then 0 on CT32Bn_CAP0 will cause CR0 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
2	CAP0I		Interrupt on CT32Bn_CAP0 event: a CR0 load due to a CT32Bn_CAP0 event will generate an interrupt.	0
		1	Enabled	
		0	Disabled	
3	CAP1RE		Capture on CT32Bn_CAP1 rising edge: a sequence of 0 then 1 on CT32Bn_CAP1 will cause CR1 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	

Table 205. Capture Control register (CCR, address 0x4001 4028 (CT32B0) and 0x4001 8028 (CT32B1)) bit description

Bit	Symbol	Value	Description	Reset value
4	CAP1FE		Capture on CT32Bn_CAP1 falling edge: a sequence of 1 then 0 on CT32Bn_CAP1 will cause CR1 to be loaded with the contents of TC.	0
		1	Enabled	
		0	Disabled	
5	CAP1I		Interrupt on CT32Bn_CAP1 event: a CR1 load due to a CT32Bn_CAP1 event will generate an interrupt.	0
		1	Enabled	
		0	Disabled	
31:6	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 13.5.9 Capture register

Each Capture register is associated with a device pin and may be loaded with the Timer Counter value when a specified event occurs on that pin. The settings in the Capture Control register determine whether the capture function is enabled and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

Table 206. Capture registers (CR[0:1], addresses 0x4001 402C (CR0) to 0x4001 4030 (CR1) (CT32B0) and 0x4001 802C (CR0) to 0x4001 8030 (CR1) (CT32B1)) bit description

Bit	Symbol	Description	Reset value
31:0	CAP	Timer counter capture value.	0

### 13.5.10 External Match register

The External Match register provides both control and status of the external match pins CAP32Bn\_MAT[3:0].

If the match outputs are configured as PWM output, the function of the external match registers is determined by the PWM rules ([Section 12.6.1 “Rules for single edge controlled PWM outputs”](#)).

Table 207. External Match register (EMR, address 0x4001 403C (CT32B0) and 0x4001 803C (CT32B1)) bit description

Bit	Symbol	Value	Description	Reset value
0	EM0		External Match 0. This bit reflects the state of output CT32Bn_MAT0, whether or not this output is connected to its pin. When a match occurs between the TC and MR0, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[5:4] control the functionality of this output. This bit is driven to the CT32B0_MAT0/CT16B1_MAT0 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
1	EM1		External Match 1. This bit reflects the state of output CT32Bn_MAT1, whether or not this output is connected to its pin. When a match occurs between the TC and MR1, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[7:6] control the functionality of this output. This bit is driven to the CT32B0_MAT1/CT16B1_MAT1 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
2	EM2		External Match 2. This bit reflects the state of output CT32Bn_MAT2, whether or not this output is connected to its pin. When a match occurs between the TC and MR2, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[9:8] control the functionality of this output. This bit is driven to the CT32B0_MAT2/CT16B1_MAT2 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
3	EM3		External Match 3. This bit reflects the state of output CT32Bn_MAT3, whether or not this output is connected to its pin. When a match occurs between the TC and MR3, this bit can either toggle, go LOW, go HIGH, or do nothing. Bits EMR[11:10] control the functionality of this output. This bit is driven to the CT32B0_MAT3/CT16B1_MAT3 pins if the match function is selected in the IOCON registers (0 = LOW, 1 = HIGH).	0
5:4	EMC0		External Match Control 0. Determines the functionality of External Match 0.	00
		0x0	Do Nothing.	
		0x1	Clear. Clear the corresponding External Match bit/output to 0 (CT32Bn_MATm pin is LOW if pinned out).	
		0x2	Set. Set the corresponding External Match bit/output to 1 (CT32Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle. Toggle the corresponding External Match bit/output.	
7:6	EMC1		External Match Control 1. Determines the functionality of External Match 1.	00
		0x0	Do Nothing.	
		0x1	Clear. Clear the corresponding External Match bit/output to 0 (CT32Bn_MATm pin is LOW if pinned out).	
		0x2	Set. Set the corresponding External Match bit/output to 1 (CT32Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle. Toggle the corresponding External Match bit/output.	
9:8	EMC2		External Match Control 2. Determines the functionality of External Match 2.	00
		0x0	Do Nothing.	
		0x1	Clear. Clear the corresponding External Match bit/output to 0 (CT32Bn_MATm pin is LOW if pinned out).	
		0x2	Set. Set the corresponding External Match bit/output to 1 (CT32Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle. Toggle the corresponding External Match bit/output.	

Table 207. External Match register (EMR, address 0x4001 403C (CT32B0) and 0x4001 803C (CT32B1)) bit description

Bit	Symbol	Value	Description	Reset value
11:10	EMC3		External Match Control 3. Determines the functionality of External Match 3.	00
		0x0	Do Nothing.	
		0x1	Clear. Clear the corresponding External Match bit/output to 0 (CT32Bn_MATm pin is LOW if pinned out).	
		0x2	Set. Set the corresponding External Match bit/output to 1 (CT32Bn_MATm pin is HIGH if pinned out).	
		0x3	Toggle. Toggle the corresponding External Match bit/output.	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 208. External match control

EMR[11:10], EMR[9:8], EMR[7:6], or EMR[5:4]	Function
00	Do Nothing.
01	Clear the corresponding External Match bit/output to 0 (CT32Bn_MATm pin is LOW if pinned out).
10	Set the corresponding External Match bit/output to 1 (CT32Bn_MATm pin is HIGH if pinned out).
11	Toggle the corresponding External Match bit/output.

### 13.5.11 Count Control register

The Count Control register (CTCR) is used to select between Timer and Counter mode, and in Counter mode to select the pin and edge(s) for counting.

When Counter Mode is chosen as a mode of operation, the CAP input (selected by the CTCR bits 3:2) is sampled on every rising edge of the PCLK clock. After comparing two consecutive samples of this CAP input, one of the following four events is recognized: rising edge, falling edge, either of edges or no changes in the level of the selected CAP input. Only if the identified event occurs, and the event corresponds to the one selected by bits 1:0 in the CTCR register, will the Timer Counter register be incremented.

Effective processing of the externally supplied clock to the counter has some limitations. Since two successive rising edges of the PCLK clock are used to identify only one edge on the CAP selected input, the frequency of the CAP input can not exceed one half of the PCLK clock. Consequently, duration of the HIGH/LOW levels on the same CAP input in this case can not be shorter than  $1/(2 \times \text{PCLK})$ .

Bits 7:4 of this register are used to enable and configure the capture-clears-timer feature. This feature allows for a designated edge on a particular CAP input to reset the timer to all zeros. Using this mechanism to clear the timer on the leading edge of an input pulse and performing a capture on the trailing edge permits direct pulse-width measurement using a single capture input without the need to perform a subtraction operation in software.

**Table 209. Count Control register (CTCR, address 0x4001 4070 (CT32B0) and 0x4001 8070 (CT32B1)) bit description**

Bit	Symbol	Value	Description	Reset value
1:0	CTM		Counter/Timer Mode. This field selects which rising PCLK edges can increment Timer's Prescale Counter (PC), or clear PC and increment Timer Counter (TC). Timer Mode: every rising PCLK edge	00
		0x0	Timer mode. Timer Mode: every rising PCLK edge	
		0x1	Counter mode rising edge. Counter Mode: TC is incremented on rising edges on the CAP input selected by bits 3:2.	
		0x2	Counter mode falling edge. Counter Mode: TC is incremented on falling edges on the CAP input selected by bits 3:2.	
		0x3	Counter mode edges. Counter Mode: TC is incremented on both edges on the CAP input selected by bits 3:2.	
3:2	CIS		Count Input Select. When bits 1:0 in this register are not 00, these bits select which CAP pin is sampled for clocking. <b>Note:</b> If Counter mode is selected in the CTCR, the 3 bits for that input in the Capture Control register (CCR) must be programmed as 000.	00
		0x0	CT32Bn_CAP0	
		0x1	CT32Bn_CAP1	
		0x2	Reserved	
		0x3	Reserved	
4	ENCC		Setting this bit to one enables clearing of the timer and the prescaler when the capture-edge event specified in bits 7:5 occurs.	0
7:5	SELCC		When bit 4 is one, these bits select which capture input edge will cause the timer and prescaler to be cleared. These bits have no effect when bit 4 is zero.	0
		0x0	Rising edge CAP0. Rising Edge of CAP0 clears the timer (if bit 4 is set).	
		0x1	Falling edge CAP1. Falling Edge of CAP0 clears the timer (if bit 4 is set).	
		0x2	Rising edge CAP1. Rising Edge of CAP1 clears the timer (if bit 4 is set).	
		0x3	Falling edge CAP1. Falling Edge of CAP1 clears the timer (if bit 4 is set).	
		0x4	Reserved.	
		0x5	Reserved.	
		0x6	Reserved.	
		0x7	Reserved.	
31:8	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

### 13.5.12 PWM Control register

The PWM Control register is used to configure the match outputs as PWM outputs. Each match output can be independently set to perform either as PWM output or as match output whose function is controlled by the External Match register (EMR).

For each timer, a maximum of three-single edge controlled PWM outputs can be selected on the MATn[2:0] outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to HIGH. The timer is reset by the match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

**Table 210. PWM Control register (PWMC, address 0x4001 4074 (CT32B0) and 0x4001 8074 (CT32B1)) bit description**

Bit	Symbol	Value	Description	Reset value
0	PWMEN0		PWM channel 0 enable	0
		0	EM0. CT32Bn_MAT0 is controlled by EM0.	
		1	MAT0. PWM mode is enabled for CT32Bn_MAT0.	
1	PWMEN1		PWM channel 1 enable	0
		0	EM1. CT32Bn_MAT1 is controlled by EM1.	
		1	MAT1. PWM mode is enabled for CT32Bn_MAT1.	
2	PWMEN2		PWM channel 2 enable	0
		0	EM2. CT32Bn_MAT2 is controlled by EM2.	
		1	MAT2. PWM mode is enabled for CT32Bn_MAT2.	
3	PWMEN3		PWM channel 3 enable <b>Note:</b> It is recommended to use match channel 3 to set the PWM cycle.	0
		0	EM3. CT32Bn_MAT3 is controlled by EM3.	
		1	MAT3. PWM mode is enabled for CT32Bn_MAT3.	
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 13.6 Functional description

The counter/timer functions are identical to the counter timer functions of the 16-bit timer. See [Section 12.6](#).

### 14.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time-out period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ( $T_{WDCLK} \times 256 \times 4$ ) to over 67 million watchdog clocks ( $T_{WDCLK} \times 2^{24} \times 4$ ) in increments of 4 watchdog clocks.
- “Safe” watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- A dedicated on-chip watchdog oscillator provides a reliable clock source that cannot be turned off when the Watchdog Timer is running.
- Incorrect feed sequence causes immediate watchdog reset if the watchdog is enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.

### 14.2 Basic configuration

The WDT is configured using the following registers:

1. Pins: The WDT uses no external pins.
2. Power: In the SYSAHBCLKCTRL register, set bit 15 ([Table 19](#)).
3. Peripheral clock: Select the WDT clock source ([Table 25](#)) and enable the WDT peripheral clock by writing to the WDTCLKDIV register ([Table 27](#)).

**Remark:** The frequency of the watchdog oscillator is undefined after reset. The watchdog oscillator frequency must be programmed by writing to the WDTOSCCTRL register (see [Table 11](#)) before using the watchdog oscillator for the WDT.

4. Lock features: Once the watchdog timer is enabled by setting the WDEN bit in the MOD register, the following lock features are in effect:
  - a. The WDEN bit cannot be changed to 0, that is the WDT cannot be disabled.
  - b. The watch dog clock source cannot be changed. If the WDT is needed in Deep-sleep mode, select the watch dog oscillator as the clock source before setting the WDEN bit.



## 14.3 General description

The Watchdog consists of a fixed divide-by-4 pre-scaler and a 24-bit counter which decrements when clocked. The minimum value from which the counter decrements is 0xFF. Setting a value lower than 0xFF causes 0xFF to be loaded in the counter. Hence the minimum Watchdog interval is  $(T_{WDCLK} \times 256 \times 4)$  and the maximum Watchdog interval is  $(T_{WDCLK} \times 2^{24} \times 4)$  in multiples of  $(T_{WDCLK} \times 4)$ . The Watchdog should be used in the following manner:

- Set the Watchdog timer constant reload value in TC register.
- Setup the Watchdog timer operating mode in MOD register.
- Set a value for the watchdog window time in WINDOW register if windowed operation is required.
- Set a value for the watchdog warning interrupt in the WARNINT register if a warning interrupt is required.
- Enable the Watchdog by writing 0xAA followed by 0x55 to the FEED register.
- The Watchdog must be fed again before the Watchdog counter reaches zero in order to prevent a watchdog event. If a window value is programmed, the feed must also occur after the watchdog counter passes that value.

When the Watchdog Timer is configured so that a watchdog event will cause a reset and the counter reaches zero, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. The Watchdog time-out flag (WDTOF) can be examined to determine if the Watchdog has caused the reset condition. The WDTOF flag must be cleared by software.

When the Watchdog Timer is configured to generate a warning interrupt, the interrupt will occur when the counter matches the value defined by the WARNINT register.

The block diagram of the Watchdog is shown below in the [Figure 45](#). The synchronization logic (PCLK - WDCLK) is not shown in the block diagram.

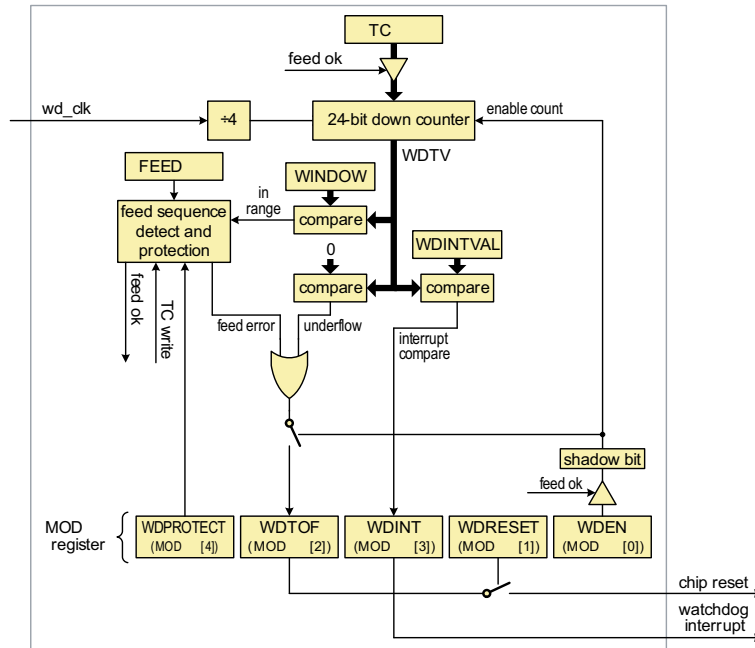


Fig 45. Windowed Watchdog Timer (WWDT) block diagram

### 14.3.1 Clock control

The watchdog timer block uses two clocks: PCLK and WDCLK. PCLK is used for the APB accesses to the watchdog registers and is derived from the system clock (see [Figure 3](#)). The WDCLK is used for the watchdog timer counting and is derived from the WDT clock divider in [Figure 3](#). Several clocks can be used as a clock source for wdt\_clk clock: the IRC, the watchdog oscillator, and the main clock. The clock source is selected in the syscon block (see [Table 25](#)). The WDCLK has its own clock divider ([Table 27](#)) which can also disable this clock.

There is some synchronization logic between these two clock domains. When the MOD and TC registers are updated by APB operations, the new value will take effect in 3 WDCLK cycles on the logic in the WDCLK clock domain. When the watchdog timer is counting on WDCLK, the synchronization logic will first lock the value of the counter on WDCLK and then synchronize it with the PCLK for reading as the TV register by the CPU.

The watchdog oscillator can be powered down in the PDRUNCFG register ([Table 44](#)) if it is not used. The clock to the watchdog register block (PCLK) can be disabled in the SYSAHBCLKCTRL register ([Table 19](#)) for power savings.

**Remark:** The frequency of the watchdog oscillator is undefined after reset. The watchdog oscillator frequency must be programmed by writing to the WDTOSCCTRL register (see [Table 11](#)) before using the watchdog oscillator for the WDT.

### 14.3.2 Applications

The purpose of the Watchdog Timer is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, a watchdog event will be generated if the user program fails to feed (or reload) the Watchdog within a predetermined amount of time. The Watchdog event will cause a chip reset if configured to do so.

When a watchdog window is programmed, an early watchdog feed is also treated as a watchdog event. This allows preventing situations where a system failure may still feed the watchdog. For example, application code could be stuck in an interrupt service that contains a watchdog feed. Setting the window such that this would result in an early feed will generate a watchdog event, allowing for system recovery.

## 14.4 Register description

Reset Value reflects the data stored in used bits only. It does not include reserved bits content.

**Table 211. Register overview: Watchdog timer (base address 0x4000 4000)**

Name	Access	Address offset	Description	Reset value
MOD	R/W	0x000	Watchdog mode register. This register contains the basic mode and status of the Watchdog Timer.	0
TC	R/W	0x004	Watchdog timer constant register. This register determines the time-out value.	0xFF
FEED	WO	0x008	Watchdog feed sequence register. Writing 0xAA followed by 0x55 to this register reloads the Watchdog timer with the value contained in TC.	-
TV	RO	0x00C	Watchdog timer value register. This register reads out the current value of the Watchdog timer.	0xFF
WARNINT	R/W	0x014	Watchdog Warning Interrupt compare value.	0
WINDOW	R/W	0x018	Watchdog Window compare value.	0xFF FFFF

### 14.4.1 Watchdog Mode register

The MOD register controls the operation of the Watchdog as per the combination of WDEN and RESET bits. Note that a watchdog feed must be performed before any changes to the MOD register take effect.

**Table 212. Watchdog Mode register (MOD, address 0x4000 4000) bit description**

Bit	Symbol	Value	Description	Reset value
0	WDEN		Watchdog enable bit. This bit is Set Only.  <b>Remark:</b> Setting this bit to one also locks the watchdog clock source. Once the watchdog timer is enabled, the watchdog timer clock source cannot be changed. If the watchdog timer is needed in Deep-sleep mode, the watchdog clock source must be changed to the watchdog oscillator before setting this bit to one.	0
		0	The watchdog timer is stopped.	
		1	The watchdog timer is running.	
1	WDRESET		Watchdog reset enable bit. This bit is Set Only.	0
		0	A watchdog timeout will not cause a chip reset.	
		1	A watchdog timeout will cause a chip reset.	
2	WDTOF		Watchdog time-out flag. Set when the watchdog timer times out, by a feed error, or by events associated with WDPROTECT, cleared by software. Causes a chip reset if WDRESET = 1.	0 (Only after external reset)
3	WDINT		Watchdog interrupt flag. Set when the timer reaches the value in WARNINT. Cleared by software.	0

Table 212. Watchdog Mode register (MOD, address 0x4000 4000) bit description

Bit	Symbol	Value	Description	Reset value
4	WDPROTECT		Watchdog update mode. This bit is Set Only.	0
		0	The watchdog reload value (TC) can be changed at any time.	
		1	The watchdog reload value (TC) can be changed only after the counter is below the value of WARNINT and WINDOW. <b>Note:</b> this mode is intended for use only when WDRESET = 1.	
31:5	-		Reserved. Read value is undefined, only zero should be written.	-

Once the **WDEN**, **WDPROTECT**, or **WDRESET** bits are set they can not be cleared by software. Both flags are cleared by an external reset or a Watchdog timer reset.

**WDTOF** The Watchdog time-out flag is set when the Watchdog times out, when a feed error occurs, or when **WDPROTECT** = 1 and an attempt is made to write to the TC register. This flag is cleared by software writing a 0 to this bit.

**WDINT** The Watchdog interrupt flag is set when the Watchdog counter reaches the value specified by **WARNINT**. This flag is cleared when any reset occurs, and is cleared by software by writing a 1 to this bit.

Watchdog reset or interrupt will occur any time the watchdog is running. If a watchdog interrupt occurs in Sleep mode, it will wake up the device.

Table 213. Watchdog operating modes selection

WDEN	WDRESET	Mode of Operation
0	X (0 or 1)	Debug/Operate without the Watchdog running.
1	0	Watchdog interrupt mode: the watchdog warning interrupt will be generated but watchdog reset will not. When this mode is selected, the watchdog counter reaching the value specified by <b>WARNINT</b> will set the <b>WDINT</b> flag and the Watchdog interrupt request will be generated.
1	1	Watchdog reset mode: both the watchdog interrupt and watchdog reset are enabled. When this mode is selected, the watchdog counter reaching the value specified by <b>WARNINT</b> will set the <b>WDINT</b> flag and the Watchdog interrupt request will be generated, and the watchdog counter reaching zero will reset the microcontroller. A watchdog feed prior to reaching the value of <b>WINDOW</b> will also cause a watchdog reset.

#### 14.4.2 Watchdog Timer Constant register

The TC register determines the time-out value. Every time a feed sequence occurs the TC content is reloaded in to the Watchdog timer. This is pre-loaded with the value 0x00 00FF upon reset. Writing values below 0xFF will cause 0x00 00FF to be loaded into the TC. Thus the minimum time-out interval is  $T_{WDCLK} \times 256 \times 4$ .

If the **WDPROTECT** bit in **MOD** = 1, an attempt to change the value of TC before the watchdog counter is below the values of **WARNINT** and **WINDOW** will cause a watchdog reset and set the **WDTOF** flag.

**Table 214. Watchdog Timer Constant register (TC, address 0x4000 4004) bit description**

Bit	Symbol	Description	Reset value
23:0	COUNT	Watchdog time-out interval.	0x00 00FF
31:24	-	Reserved. Read value is undefined, only zero should be written.	NA

### 14.4.3 Watchdog Feed register

Writing 0xAA followed by 0x55 to this register will reload the Watchdog timer with the TC value. This operation will also start the Watchdog if it is enabled via the MOD register. Setting the WDEN bit in the MOD register is not sufficient to enable the Watchdog. A valid feed sequence must be completed after setting WDEN before the Watchdog is capable of generating a reset. Until then, the Watchdog will ignore feed errors. After writing 0xAA to FEED, access to any Watchdog register other than writing 0x55 to FEED causes an immediate reset/interrupt when the Watchdog is enabled, and sets the WDTOF flag. The reset will be generated during the second PCLK following an incorrect access to a Watchdog register during a feed sequence.

**Table 215. Watchdog Feed register (FEED, address 0x4000 4008) bit description**

Bit	Symbol	Description	Reset value
7:0	FEEDVAL	Feed value should be 0xAA followed by 0x55.	-
31:8	-	Reserved	-

### 14.4.4 Watchdog Timer Value register

The TV register is used to read the current value of Watchdog timer counter.

When reading the value of the 24-bit counter, the lock and synchronization procedure takes up to 6 WDCLK cycles plus 6 PCLK cycles, so the value of TV is older than the actual value of the timer when it's being read by the CPU.

**Table 216. Watchdog Timer Value register (TV, address 0x4000 400C) bit description**

Bit	Symbol	Description	Reset value
23:0	COUNT	Counter timer value.	0x00 00FF
31:24	-	Reserved. Read value is undefined, only zero should be written.	-

### 14.4.5 Watchdog Timer Warning Interrupt register

The WARNINT register determines the watchdog timer counter value that will generate a watchdog interrupt. When the watchdog timer counter matches the value defined by WARNINT, an interrupt will be generated after the subsequent WDCLK.

A match of the watchdog timer counter to WARNINT occurs when the bottom 10 bits of the counter have the same value as the 10 bits of WARNINT, and the remaining upper bits of the counter are all 0. This gives a maximum time of 1,023 watchdog timer counts (4,096 watchdog clocks) for the interrupt to occur prior to a watchdog event. If WARNINT is set to 0, the interrupt will occur at the same time as the watchdog event.

**Table 217. Watchdog Timer Warning Interrupt register (WARNINT, address 0x4000 4014) bit description**

Bit	Symbol	Description	Reset value
9:0	COMPVAL	Watchdog warning interrupt compare value.	0
31:10	-	Reserved. Read value is undefined, only zero should be written.	-

#### 14.4.6 Watchdog Timer Window register

The WINDOW register determines the highest TV value allowed when a watchdog feed is performed. If a feed valid sequence completes prior to TV reaching the value in WINDOW, a watchdog event will occur.

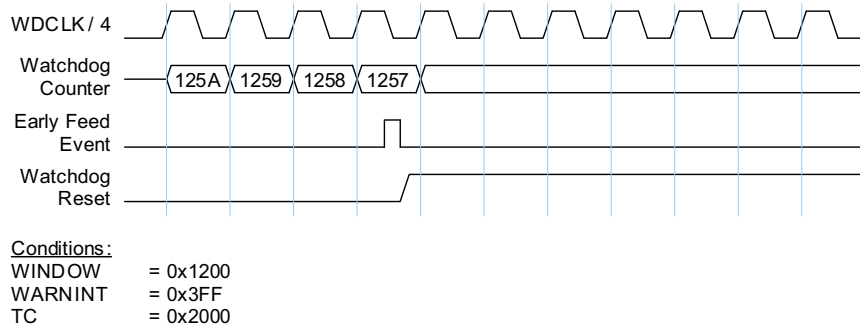
WINDOW resets to the maximum possible TV value, so windowing is not in effect.

**Table 218. Watchdog Timer Window register (WINDOW, address 0x4000 4018) bit description**

Bit	Symbol	Description	Reset value
23:0	WINVAL	Watchdog window value.	0xFF FFFF
31:24	-	Reserved. Read value is undefined, only zero should be written.	-

#### 14.4.7 Watchdog timing examples

The following figures illustrate several aspects of Watchdog Timer operation.

**Fig 46. Early Watchdog Feed with Windowed Mode Enabled**

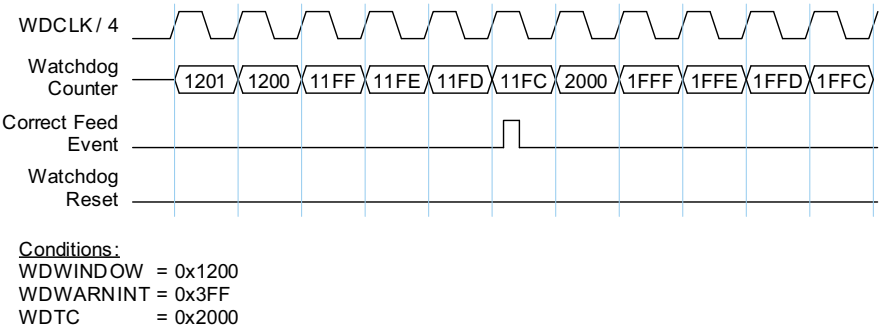


Fig 47. Correct Watchdog Feed with Windowed Mode Enabled

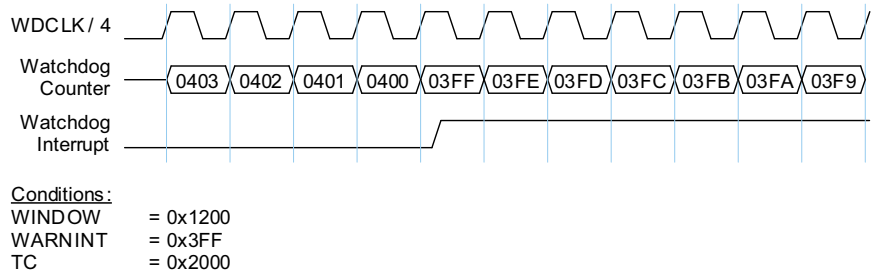


Fig 48. Watchdog Warning Interrupt



### 15.1 How to read this chapter

The system tick timer (SysTick timer) is part of the ARM Cortex-M0 core and is described in the ARM Cortex-M0 technical reference manual.

### 15.2 Features

- Simple 24-bit timer.
- Uses dedicated exception vector.
- Clocked internally by the system clock or the system clock/2.

### 15.3 Basic configuration

The system tick timer is configured using the following registers:

- Pins: The system tick timer uses no external pins.
- Power: The system tick timer is enabled through the SysTick control register ([Section 21.5.4.1](#)). The system tick timer clock is fixed to half the frequency of the system clock.
- Enable the clock source for the SysTick timer in the SYST\_CSR register ([Table 220](#)).

### 15.4 General description

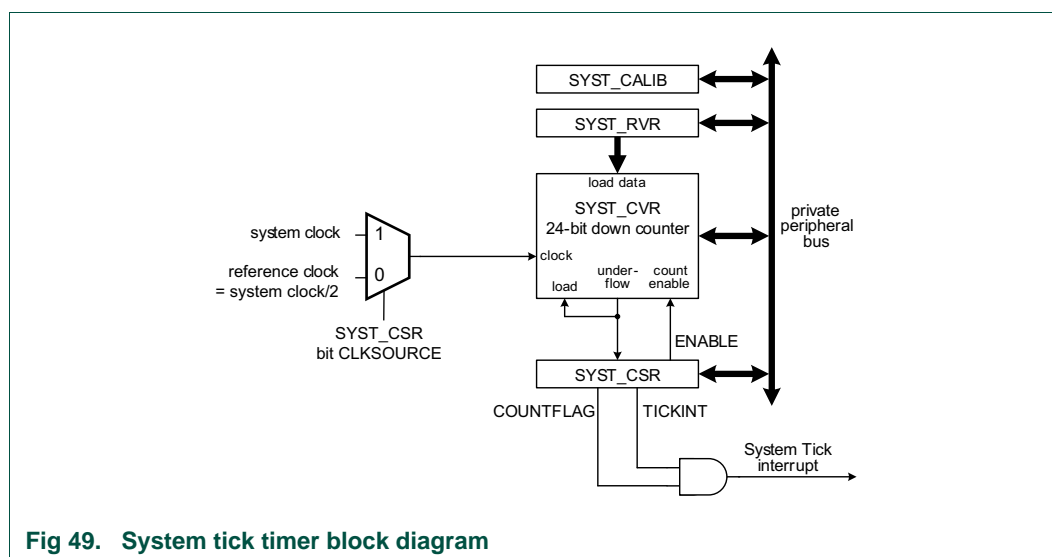


Fig 49. System tick timer block diagram

The SysTick timer is an integral part of the Cortex-M0. The SysTick timer is intended to generate a fixed 10 millisecond interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices. The SysTick timer can be used for:

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the core clock.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

Refer to the *Cortex-M0 User Guide* for details.

## 15.5 Register description

The systick timer registers are located on the ARM Cortex-M0 private peripheral bus (see [Figure 62](#)), and are part of the ARM Cortex-M0 core peripherals. For details, see [Section 21.5.4](#).

**Table 219. Register overview: SysTick timer (base address 0xE000 E000)**

Name	Access	Address offset	Description	Reset value <sup>[1]</sup>
SYST_CSR	R/W	0x010	System Timer Control and status register	0x000 0000
SYST_RVR	R/W	0x014	System Timer Reload value register	0
SYST_CVR	R/W	0x018	System Timer Current value register	0
SYST_CALIB	R/W	0x01C	System Timer Calibration value register	0x4

[1] Reset Value reflects the data stored in used bits only. It does not include content of reserved bits.

### 15.5.1 System Timer Control and status register

The SYST\_CSR register contains control information for the SysTick timer and provides a status flag. This register is part of the ARM Cortex-M0 core system timer register block. For a bit description of this register, see [Section 21.5.4 “System timer, SysTick”](#).

This register determines the clock source for the system tick timer.

**Table 220. SysTick Timer Control and status register (SYST\_CSR - 0xE000 E010) bit description**

Bit	Symbol	Description	Reset value
0	ENABLE	System Tick counter enable. When 1, the counter is enabled. When 0, the counter is disabled.	0
1	TICKINT	System Tick interrupt enable. When 1, the System Tick interrupt is enabled. When 0, the System Tick interrupt is disabled. When enabled, the interrupt is generated when the System Tick counter counts down to 0.	0
2	CLKSOURCE	System Tick clock source selection. When 1, the system clock (CPU) clock is selected. When 0, the system clock/2 is selected as the reference clock.	0
15:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
16	COUNTFLAG	Returns 1 if the SysTick timer counted to 0 since the last read of this register.	0
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 15.5.2 System Timer Reload value register

The SYST\_RVR register is set to the value that will be loaded into the SysTick timer whenever it counts down to zero. This register is loaded by software as part of timer initialization. The SYST\_CALIB register may be read and used as the value for SYST\_RVR register if the CPU is running at the frequency intended for use with the SYST\_CALIB value.

**Table 221. System Timer Reload value register (SYST\_RVR - 0xE000 E014) bit description**

Bit	Symbol	Description	Reset value
23:0	RELOAD	This is the value that is loaded into the System Tick counter when it counts down to 0.	0
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 15.5.3 System Timer Current value register

The SYST\_CVR register returns the current count from the System Tick counter when it is read by software.

**Table 222. System Timer Current value register (SYST\_CVR - 0xE000 E018) bit description**

Bit	Symbol	Description	Reset value
23:0	CURRENT	Reading this register returns the current value of the System Tick counter. Writing any value clears the System Tick counter and the COUNTFLAG bit in STCTRL.	0
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 15.5.4 System Timer Calibration value register (SYST\_CALIB - 0xE000 E01C)

The value of the SYST\_CALIB register is driven by the value of the SYSTCKCAL register in the system configuration block (see [Table 34](#)).

**Table 223. System Timer Calibration value register (SYST\_CALIB - 0xE000 E01C) bit description**

Bit	Symbol	Value	Description	Reset value
23:0	TENMS		See <a href="#">Table 340</a> .	0x4
29:24	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
30	SKEW		See <a href="#">Table 340</a> .	0
31	NOREF		See <a href="#">Table 340</a> .	0

## 15.6 Functional description

The SysTick timer is a 24-bit timer that counts down to zero and generates an interrupt. The intent is to provide a fixed 10 millisecond time interval between interrupts. The SysTick timer is clocked from the CPU clock (the system clock, see [Figure 3](#)) or from the reference clock, which is fixed to half the frequency of the CPU clock. In order to generate recurring interrupts at a specific interval, the SYST\_RVR register must be initialized with the correct value for the desired interval. A default value is provided in the SYST\_CALIB register and may be changed by software. The default value gives a 10 millisecond interrupt rate if the CPU clock is set to 50 MHz.

## 15.7 Example timer calculations

To use the system tick timer, do the following:

1. Program the SYST\_RVR register with the reload value RELOAD to obtain the desired time interval.
2. Clear the SYST\_CVR register by writing to it. This ensures that the timer will count from the SYST\_RVR value rather than an arbitrary value when the timer is enabled.
3. Program the SYST\_SCR register with the value 0x7 which enables the SysTick timer and the SysTick timer interrupt.

The following example illustrates selecting the SysTick timer reload value to obtain a 10 ms time interval with the LPC111x/LPC11Cxx system clock set to 50 MHz.

### Example (system clock = 50 MHz)

The system tick clock = system clock = 50 MHz. Bit CLKSOURCE in the SYST\_CSR register set to 1 (system clock).

$RELOAD = (\text{system tick clock frequency} \times 10 \text{ ms}) - 1 = (50 \text{ MHz} \times 10 \text{ ms}) - 1 = 500000 - 1 = 499999 = 0x0007A11F$ .

### 16.1 Features

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- 12-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 2 MHz.
- Burst conversion mode for single or multiple inputs.

### 16.2 Basic configuration

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Configure the ADC as follows:

- Use the SYSAHBCLKCTRL register ([Table 19](#)) to enable the clock to the ADC register interface and the ADC clock.
- The ADC block creates four interrupts. The ADC threshold crossing and end-of-sequence A interrupts are combined and connected to the ADC\_A\_IRQ (slot #24). The end-of-sequence B and overrun interrupts are combined and connected to the ADC\_B\_IRQ (slot # 13).
- The ADC analog inputs are selected in the IOCON block. See [Table 106](#).
- The power to the ADC block is controlled by the PDRUNCFG register in the SYSCON block. See [Table 44](#).
- Calibration is required after every reset. That is after power-up or wake-up from Deep power-down mode.
- Configure the ADC for the appropriate analog supply voltage using the TRM register ([Table 240](#)).

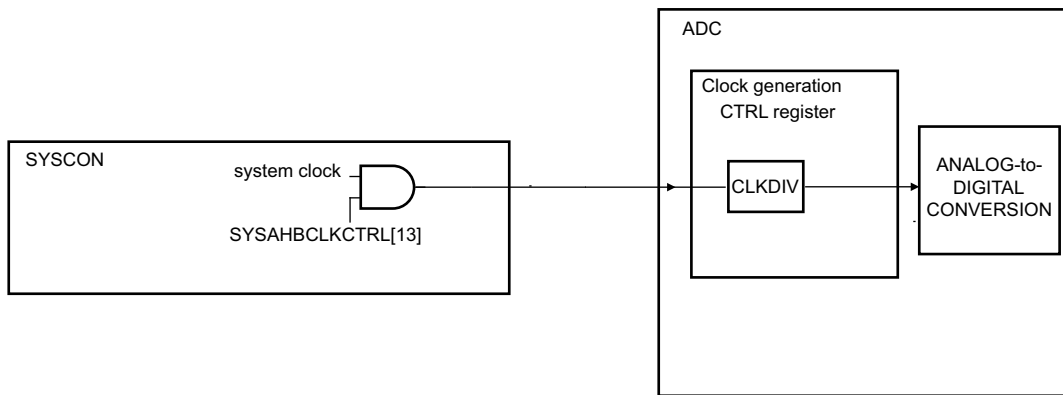


Fig 50. ADC clocking

### 16.2.1 ADC hardware trigger inputs

An analog-to-digital conversion can be initiated by a hardware trigger. You can select the trigger independently for each of the two conversion sequences in the ADC SEQA\_CTRL or SEQB\_CTRL registers by programming the hardware trigger input # into the TRIGGER bits.

To use the pin trigger inputs, select the ADC\_PIN\_TRIG function in the FUNC bits of pins PIO0\_2, PIO0\_7, PIO0\_8, PIO0\_9, and PIO2\_0.

Related registers:

- [Table 228 “A/D Conversion Sequence A Control Register \(SEQA\\_CTRL, address 0x4001 C008\) bit description”](#)
- [Table 229 “A/D Conversion Sequence B Control Register \(SEQB\\_CTRL, address 0x4001 C00C\) bit description”](#)

**Table 224. ADC hardware trigger inputs**

Input #	Source	Description
0	ARM_TXEV	
1	CT16BB1_MAT3	Match output 3 of 16-bit timer CT16B1.
2	CT16BB1_MAT2	Match output 2 of 16-bit timer CT16B1.
3	PIO0_2/SSP0_SSEL/CT16B0_CAP0/ ADC_PIN_TRIG0	Pin trigger input 0. See <a href="#">Table 60</a> .
4	PIO0_7/U0_CTS/ADC_PIN_TRIG1/U1_RXD	Pin trigger input 1. See <a href="#">Table 98</a> .
5	PIO0_8/SSP0_MISO/CT16B0_MAT0/R/ ADC_PIN_TRIG2	Pin trigger input 2. See <a href="#">Table 74</a> .
6	PIO0_9SSP0_MOSI/CT16B0_MAT1/R/ADC_ PIN_TRIG3	Pin trigger input 3. See <a href="#">Table 75</a> .
7	PIO2_0/U0_DTR/SSP1_SSEL/ ADC_PIN_TRIG4	Pin trigger input 4. See <a href="#">Table 56</a> .

### 16.2.2 Perform a single ADC conversion

The ADC converts an analog input signal VIN on the ADC\_[8:1]. The VREFP and VREFN pins provide a positive and negative reference voltage input. The result of the conversion is  $(4095 \times VIN)/(VREFP - VREFN)$ . The result of an input voltage below VREFN is 0, and the result of an input voltage above VREFP is 4095 (0xFFFF).

To perform a single ADC conversion for ADC channel 1 using the analog signal on pin ADC\_1, follow these steps:

1. Enable the analog function on pin ADC\_1.
2. Configure the system clock to be 50 MHz and select a CLKDIV value of 0 for a sampling rate of 50 MHz using the ADC CTRL register.
3. Select the synchronous mode in the CTRL register.
4. Select ADC channel 1 to perform the conversion by setting the CHANNELS bits to 0x2 in the SEQA\_CTL register.
5. Set the START bit to 1 in the SEQA\_CTRL register.
6. Read the RESULT bits in the DAT1 register for the conversion result.

### 16.2.3 Perform a sequence of conversions triggered by an external pin

The ADC can perform conversions on a sequence of selected channels. Each individual conversion of the sequence (single-step) or the entire sequence can be triggered by hardware. Hardware triggers are either a signal from an external pin or an internal signal. See [Section 16.2.1](#).

To perform a single-step conversion on the first four channels of ADC0 triggered by a rising edge on ADC\_PIN\_TRIG0 (pin PIO0\_2), follow these steps:

1. Enable the analog function on pin ADC\_1 to ADC\_4 in the IOCON block.
2. Configure the system clock to be 50 MHz and select a CLKDIV value of 0 for a sampling rate of 50 MHz using the ADC CTRL register.
3. Select the synchronous mode in the CTRL register.
4. Select ADC channels 1 to 4 to perform the conversion by setting the CHANNELS bits to 0xF in the SEQA\_CTL register.
5. Select ADC\_PIN\_TRIG0 by writing 0x3 to the TRIGGER bits in the SEQA\_CTRL register. Also select ADC\_PIN\_TRIG0 in the IOCON PIO0\_2 register ([Table 60](#)).
6. To generate one interrupt at the end of the entire sequence, set the MODE bit to 1 in the SEQA\_CTRL register.
7. Select single-step mode by setting the SINGLESTEP bit in the SEQA\_CTRL register to 1.
8. Enable the Sequence A by setting the SEQA\_ENA bit.

A conversion on ADC0 channel 1 will be triggered whenever the pin PIO0\_2 goes from LOW to HIGH. The conversion on the next channel (channel 2) is triggered on the next rising edge of ADC\_PIN\_TRIG0. The ADC\_A interrupt is generated when the sequence has finished after four rising edges on ADC\_PIN\_TRIG0.

9. Read the RESULT bits in the DAT1 to DAT4 registers for the conversion result.

## 16.3 Pin description

The ADC cell can measure the voltage on any of the input signals on the analog input channel. Digital signals are disconnected from the ADC input pins when the ADC function is selected on that pin in the IOCON register.

**Warning:** If the ADC is used, signal levels on analog input pins must not be above the level of  $V_{DDA}$  at any time. Otherwise, ADC readings will be invalid. If the ADC is not used in an application, then the pins associated with ADC inputs can be used as 5 V tolerant digital I/O pins.

The VREFP and VREFN pins provide a positive and negative reference voltage input. The result of the conversion is  $(4095 \times \text{input voltage } VIN) / (V_{REFP} - V_{REFN})$ . The result of an input voltage below VREFN is 0, and the result of an input voltage above VREFP is 4095 (0xFFF).

When the ADC is not used, tie VDDA and VREFP to VDD and VSSA and VREFN to VSS.

Analog Power and Ground should typically be the same voltages as  $V_{DD}$  and  $V_{SS}$ , but should be isolated to minimize noise and error.

**Table 225. ADC pin description**

Function	Direction	Description
V <sub>REFP</sub>	Ref	Positive voltage reference. VREFP must be >2.4 V. For best performance, select VREFP = V <sub>DDA</sub> and VREFN = V <sub>SSA</sub> . To operate the ADC within specifications at the maximum sampling rate, ensure that VREFP = VDDA.
V <sub>REFN</sub>	Ref	Negative voltage reference
V <sub>DDA</sub>	Supply	ADC power supply
V <sub>SSA</sub>	Supply	ADC ground
ADC_1	AI	Analog input channel 1.
ADC_2	AI	Analog input channel 2.
ADC_3	AI	Analog input channel 3.
ADC_4	AI	Analog input channel 4.
ADC_5	AI	Analog input channel 5.
ADC_6	AI	Analog input channel 6.
ADC_7	AI	Analog input channel 7.
ADC_8	AI	Analog input channel 8.
ADC_PIN_TRIG0	I	Pin trigger input 0.
ADC_PIN_TRIG1	I	Pin trigger input 1.
ADC_PIN_TRIG2	I	Pin trigger input 2.
ADC_PIN_TRIG3	I	Pin trigger input 3.
ADC_PIN_TRIG4	I	Pin trigger input 4.



## 16.4 General description

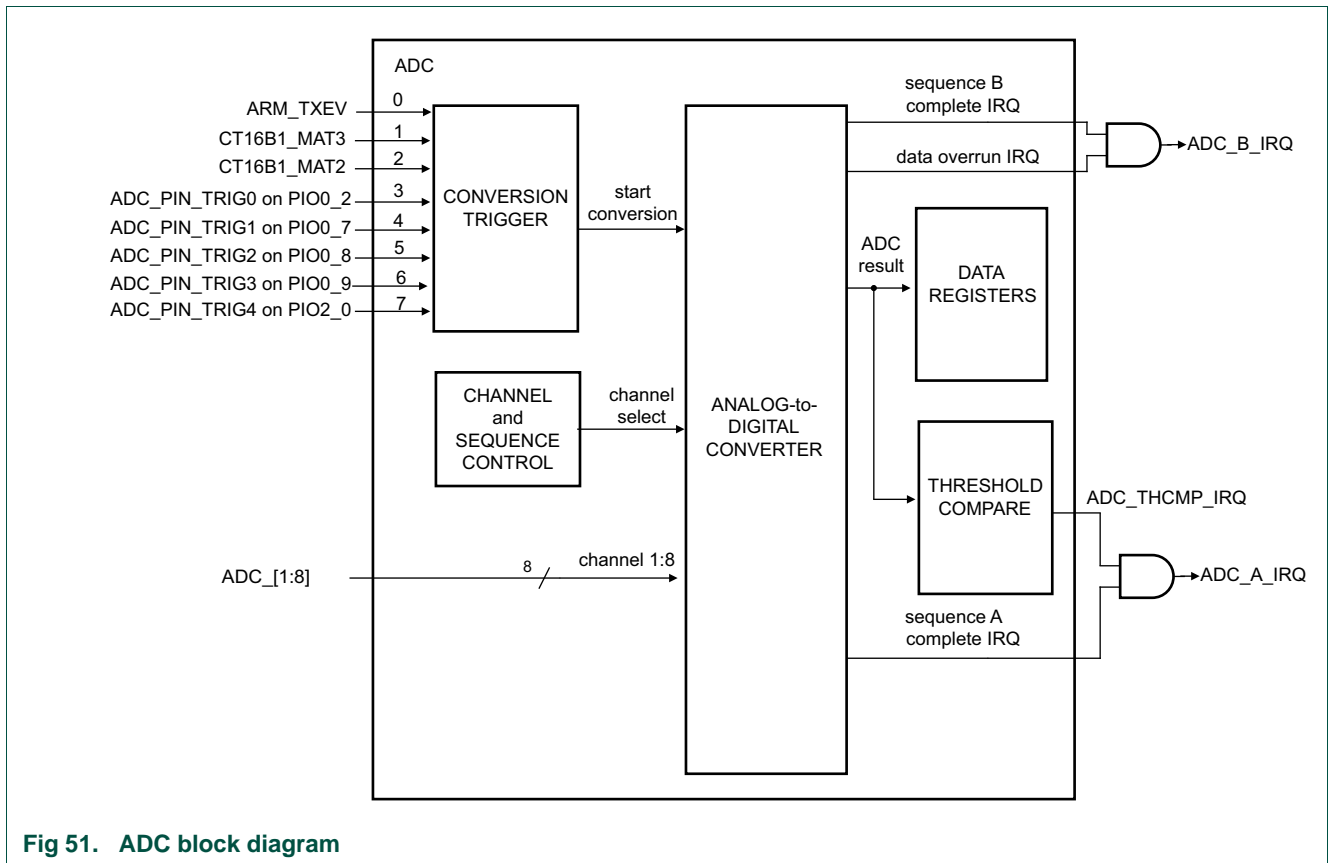


Fig 51. ADC block diagram

The ADC controller provides great flexibility in launching and controlling sequences of A/D conversions using the associated 12-bit, successive approximation A/D converter. A/D conversion sequences can be initiated under software control or in response to a selected hardware trigger. The ADC supports eight hardware triggers.

The ADC controller uses the system clock as a bus clock. The ADC clock is derived from the system clock. A programmable divider is included to scale the system clock to the maximum ADC clock rate of 50 MHz. The ADC clock drives the successive approximation process.

A fully accurate conversion requires 25 of these ADC clocks.

## 16.5 Register description

The reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 226. Register overview: 12-bit ADC (base address 0x4001 C000)

Name	Access	Address offset	Description	Reset value	Reference
CTRL	R/W	0x000	A/D Control Register. Contains the clock divide value, enable bits for each sequence and the A/D power-down bit.	0x0	<a href="#">Table 227</a>
-	-	0x004	Reserved.	-	-
SEQA_CTRL	R/W	0x008	A/D Conversion Sequence-A control Register: Controls triggering and channel selection for conversion sequence-A. Also specifies interrupt mode for sequence-A.	0x0	<a href="#">Table 228</a>
SEQB_CTRL	R/W	0x00C	A/D Conversion Sequence-B Control Register: Controls triggering and channel selection for conversion sequence-B. Also specifies interrupt mode for sequence-B.	0x0	<a href="#">Table 229</a>
SEQA_GDAT	R/W	0x010	A/D Sequence-A Global Data Register. This register contains the result of the most recent A/D conversion performed under sequence-A	NA	<a href="#">Table 230</a>
SEQB_GDAT	R/W	0x014	A/D Sequence-B Global Data Register. This register contains the result of the most recent A/D conversion performed under sequence-B	NA	<a href="#">Table 231</a>
-	-	0x020	Reserved.	-	-
DAT1	RO	0x024	A/D Channel 1 Data Register. This register contains the result of the most recent conversion completed on channel 1.	NA	<a href="#">Table 232</a>
DAT2	RO	0x028	A/D Channel 2 Data Register. This register contains the result of the most recent conversion completed on channel 2.	NA	<a href="#">Table 232</a>
DAT3	RO	0x02C	A/D Channel 3 Data Register. This register contains the result of the most recent conversion completed on channel 3.	NA	<a href="#">Table 232</a>
DAT4	RO	0x030	A/D Channel 4 Data Register. This register contains the result of the most recent conversion completed on channel 4.	NA	<a href="#">Table 232</a>
DAT5	RO	0x034	A/D Channel 5 Data Register. This register contains the result of the most recent conversion completed on channel 5.	NA	<a href="#">Table 232</a>
DAT6	RO	0x038	A/D Channel 6 Data Register. This register contains the result of the most recent conversion completed on channel 6.	NA	<a href="#">Table 232</a>

Table 226. Register overview: 12-bit ADC (base address 0x4001 C000)

Name	Access	Address offset	Description	Reset value	Reference
DAT7	RO	0x03C	A/D Channel 7 Data Register. This register contains the result of the most recent conversion completed on channel 7.	NA	<a href="#">Table 232</a>
DAT8	RO	0x040	A/D Channel 8 Data Register. This register contains the result of the most recent conversion completed on channel 7.	NA	<a href="#">Table 232</a>
-	-	0x044	Reserved.	-	-
-	-	0x048	Reserved.	-	-
-	-	0x04C	Reserved.	-	-
THR0_LOW	R/W	0x050	A/D Low Compare Threshold Register 0 : Contains the lower threshold level for automatic threshold comparison for any channels linked to threshold pair 0.	0x0	<a href="#">Table 233</a>
THR1_LOW	R/W	0x054	A/D Low Compare Threshold Register 1: Contains the lower threshold level for automatic threshold comparison for any channels linked to threshold pair 1.	0x0	<a href="#">Table 234</a>
THR0_HIGH	R/W	0x058	A/D High Compare Threshold Register 0: Contains the upper threshold level for automatic threshold comparison for any channels linked to threshold pair 0.	0x0	<a href="#">Table 235</a>
THR1_HIGH	R/W	0x05C	A/D High Compare Threshold Register 1: Contains the upper threshold level for automatic threshold comparison for any channels linked to threshold pair 1.	0x0	<a href="#">Table 236</a>
CHAN_THRSEL	R/W	0x060	A/D Channel-Threshold Select Register. Specifies which set of threshold compare registers are to be used for each channel	0x0	<a href="#">Table 237</a>
INTEN	R/W	0x064	A/D Interrupt Enable Register. This register contains enable bits that enable the sequence-A, sequence-B, threshold compare and data overrun interrupts to be generated.	0x0	<a href="#">Table 238</a>
FLAGS	R/W	0x068	A/D Flags Register. Contains the four interrupt request flags and the individual component overrun and threshold-compare flags. (The overrun bits replicate information stored in the result registers).	0x0	<a href="#">Table 239</a>
TRM	R/W	0x06C	ADC trim register.	0x000 0 0F00	<a href="#">Table 240</a>

### 16.5.1 ADC Control Register

This register specifies the clock divider value to be used to generate the ADC clock in synchronous mode and general operating mode bits including the power-down bit that allows the A/D to be turned off to save power when not in use.

**Table 227. A/D Control Register (CTRL, addresses 0x4001 C000) bit description**

Bit	Symbol	Value	Description	Reset value
7:0	CLKDIV		The system clock is divided by this value plus one to produce the clock for the A/D converter, which should be less than or equal to 50 MHz (up to 100 MHz in 10-bit mode).  Typically, software should program the smallest value in this field that yields this maximum clock rate or slightly less, but in certain cases (such as a high-impedance analog source) a slower clock may be desirable.	0
9:8	-		Reserved.	-
10	LPWRMODE		Select low-power ADC mode.  The analog circuitry is automatically powered-down when no conversions are taking place. When any (hardware or software) triggering event is detected, the analog circuitry is enabled. After the required start-up time, the requested conversion will be launched. Once the conversion completes, the analog-circuitry will again be powered-down provided no further conversions are pending.  Using this mode can save an appreciable amount of current (approximately 2.5 mA) when conversions are required relatively infrequently.  The penalty for using this mode is an approximately 15 ADC clock delay (30 clocks in 10-bit mode), based on the frequency specified in the CLKDIV field, from the time the trigger event occurs until sampling of the A/D input commences. <b>Remark:</b> This mode will NOT power-up the A/D if the ADC_ENA bit is low.	0
		0	Disabled. The low-power ADC mode is disabled. The analog circuitry remains activated even when no conversions are requested.	
		1	Enabled. The low-power ADC mode is enabled.	
29:11			Reserved, user software should not write ones to reserved bits.	0
30	CAL_MODE		Writing a 1 to this bit initiates a self-calibration cycle. This bit will be automatically cleared by hardware after the calibration cycle is complete. <b>Remark:</b> Other bits of this register may be written to concurrently with setting this bit, however once this bit has been set no further writes to this register are permitted until the full calibration cycle has ended.	0
31	-		Reserved.	0

### 16.5.2 A/D Conversion Sequence A Control Register

There are two, independent conversion sequences that can be configured, each consisting of a set of conversions on one or more channels. This control register specifies the channel selection and trigger conditions for the A sequence and contains bits to allow software to initiate that conversion sequence.

**Remark:** Set the BURST and SEQU\_ENA bits at the same time.

Table 228. A/D Conversion Sequence A Control Register (SEQA\_CTRL, address 0x4001 C008) bit description

Bit	Symbol	Value	Description	Reset value
0	-		Reserved.	-
8:1	CHANNELS		<p>Selects which one or more of the twelve channels will be sampled and converted when this sequence is launched. A 1 in any bit of this field will cause the corresponding channel to be included in the conversion sequence, where bit 0 corresponds to channel 0, bit 1 to channel 1 and so forth.</p> <p>When this conversion sequence is triggered, either by a hardware trigger or via software command, A/D conversions will be performed on each enabled channel, in sequence, beginning with the lowest-ordered channel.</p> <p><b>Remark:</b> This field can ONLY be changed while the SEQA_ENA bit (bit 31) is LOW. It is allowed to change this field and set bit 31 in the same write.</p>	0x00
11:9	-		Reserved.	-
17:12	TRIGGER		<p>Selects which of the available hardware trigger sources will cause this conversion sequence to be initiated. Program the trigger input number in this field.</p> <p><b>Remark:</b> In order to avoid generating a spurious trigger, it is recommended writing to this field only when the SEQA_ENA bit (bit 31) is low. It is safe to change this field and set bit 31 in the same write.</p>	0x0
18	TRIGPOL		Select the polarity of the selected input trigger for this conversion sequence.	0
		0	Negative edge. A negative edge launches the conversion sequence on the selected trigger input.	
		1	Positive edge. A positive edge launches the conversion sequence on the selected trigger input.	
19	SYNCBYPASS		<p>Setting this bit allows the hardware trigger input to bypass synchronization flip-flops stages and therefore shorten the time between the trigger input signal and the start of a conversion. There are slightly different criteria for whether or not this bit can be set depending on the clock operating mode:</p> <p>Synchronous mode: Synchronization may be bypassed (this bit may be set) if the selected trigger source is already synchronous with the main system clock (eg. coming from an on-chip, system-clock-based timer). Whether this bit is set or not, a trigger pulse must be maintained for at least one system clock period.</p> <p>Asynchronous mode: Synchronization may be bypassed (this bit may be set) if it is certain that the duration of a trigger input pulse will be at least one cycle of the ADC clock (regardless of whether the trigger comes from and on-chip or off-chip source). If this bit is NOT set, the trigger pulse must at least be maintained for one system clock period.</p>	0
		0	Enable synchronization. The hardware trigger bypass is not enabled.	
		1	Bypass synchronization. The hardware trigger bypass is enabled.	
25:20	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	N/A

Table 228. A/D Conversion Sequence A Control Register (SEQA\_CTRL, address 0x4001 C008) bit description

Bit	Symbol	Value	Description	Reset value
26	START		Writing a 1 to this field will launch one pass through this conversion sequence. The behavior will be identical to a sequence triggered by a hardware trigger. Do not write 1 to this bit if the BURST bit is set.  <b>Remark:</b> This bit is only set to a 1 momentarily when written-to in order to launch a conversion sequence. It will consequently always read-back as a zero.	0
27	BURST		Writing a 1 to this bit will cause this conversion sequence to be continuously cycled through. Other sequence A triggers will be ignored while this bit is set. Repeated conversions can be halted by clearing this bit. The sequence currently in progress will be completed before conversions are terminated.	0
28	SINGLESTEP		When this bit is set, a hardware trigger or a write to the START bit will launch a single conversion on the next channel in the sequence instead of the default response of launching an entire sequence of conversions. Once all of the channels comprising a sequence have been converted, a subsequent trigger will repeat the sequence beginning with the first enabled channel. Interrupt generation will still occur either after each individual conversion or at the end of the entire sequence, depending on the state of the MODE bit.	0
29	LOWPRIO		Set priority for sequence A.	0
		0	Low priority. Any B trigger which occurs while an A conversion sequence is active will be ignored and lost.	
		1	High priority. Setting this bit to a 1 will permit any enabled B sequence trigger (including a B sequence software start) to immediately interrupt this sequence and launch a B sequence in its place. The conversion currently in progress will be terminated. The A sequence that was interrupted will automatically resume after the B sequence completes. The channel whose conversion was terminated will be re-sampled and the conversion sequence will resume from that point.	
30	MODE		Indicates whether the primary method for retrieving conversion results for this sequence will be accomplished via reading the global data register (SEQA_GDAT) at the end of each conversion, or the individual channel result registers at the end of the entire sequence. Impacts when conversion-complete interrupt for sequence-A will be generated and which overrun conditions contribute to an overrun interrupt as described below:	0
		0	End of conversion. The sequence A interrupt will be set at the end of each individual A/D conversion performed under sequence A. This flag will mirror the DATAVALID bit in the SEQA_GDAT register. The OVERRUN bit in the SEQA_GDAT register will contribute to generation of an overrun interrupt if enabled.	
		1	End of sequence. The sequence A interrupt will be set when the entire set of sequence-A conversions completes. This flag will need to be explicitly cleared by software in this mode. The OVERRUN bit in the SEQA_GDAT register will NOT contribute to generation of an overrun interrupt since it is assumed this register may not be utilized in this mode.	

Table 228. A/D Conversion Sequence A Control Register (SEQA\_CTRL, address 0x4001 C008) bit description

Bit	Symbol	Value	Description	Reset value
31	SEQA_ENA		Sequence Enable. In order to avoid spuriously triggering the sequence, care should be taken to only set the SEQA_ENA bit when the selected trigger input is in its INACTIVE state (as defined by the TRIGPOL bit). If this condition is not met, the sequence will be triggered immediately upon being enabled.	0
		0	Disabled. Sequence A is disabled. Sequence A triggers are ignored. If this bit is cleared while sequence A is in progress, the sequence will be halted at the end of the current conversion. After the sequence is re-enabled, a new trigger will be required to restart the sequence beginning with the next enabled channel.	
		1	Enabled. Sequence A is enabled.	

### 16.5.3 A/D Conversion Sequence B Control Register

There are two, independent conversion sequences that can be configured, each consisting of a set of conversions on one or more channels. This control register specifies the channel selection and trigger conditions for the B sequence, as well as bits to allow software to initiate that conversion sequence.

Table 229. A/D Conversion Sequence B Control Register (SEQB\_CTRL, address 0x4001 C00C) bit description

Bit	Symbol	Value	Description	Reset value
0	-		Reserved.	-
8:1	CHANNELS		<p>Selects which one or more of the twelve channels will be sampled and converted when this sequence is launched. A 1 in any bit of this field will cause the corresponding channel to be included in the conversion sequence, where bit 0 corresponds to channel 0, bit 1 to channel 1 and so forth.</p> <p>When this conversion sequence is triggered, either by a hardware trigger or via software command, A/D conversions will be performed on each enabled channel, in sequence, beginning with the lowest-ordered channel.</p> <p><b>Remark:</b> This field can ONLY be changed while the SEQB_ENA bit (bit 31) is LOW. It is permissible to change this field and set bit 31 in the same write.</p>	0x00
11:9	-		Reserved.	-
17:12	TRIGGER		<p>Selects which of the available hardware trigger sources will cause this conversion sequence to be initiated. Program the trigger input number in this field.</p> <p><b>Remark:</b> In order to avoid generating a spurious trigger, it is recommended writing to this field only when the SEQA_ENA bit (bit 31) is low. It is safe to change this field and set bit 31 in the same write.</p>	0x0

Table 229. A/D Conversion Sequence B Control Register (SEQB\_CTRL, address 0x4001 C00C) bit description

Bit	Symbol	Value	Description	Reset value
18	TRIGPOL		Select the polarity of the selected input trigger for this conversion sequence.  <b>Remark:</b> In order to avoid generating a spurious trigger, it is recommended writing to this field only when the SEQA_ENA bit (bit 31) is low. It is safe to change this field and set bit 31 in the same write.	0
		0	Negative edge. A negative edge launches the conversion sequence on the selected trigger input.	
		1	Positive edge. A positive edge launches the conversion sequence on the selected trigger input.	
19	SYNCBYPASS		Setting this bit allows the hardware trigger input to bypass synchronization flip-flops stages and therefore shorten the time between the trigger input signal and the start of a conversion. There are slightly different criteria for whether or not this bit can be set depending on the clock operating mode:  Synchronous mode: Synchronization may be bypassed (this bit may be set) if the selected trigger source is already synchronous with the main system clock (eg. coming from an on-chip, system-clock-based timer). Whether this bit is set or not, a trigger pulse must be maintained for at least one system clock period.  Asynchronous mode: Synchronization may be bypassed (this bit may be set) if it is certain that the duration of a trigger input pulse will be at least one cycle of the ADC clock (regardless of whether the trigger comes from and on-chip or off-chip source). If this bit is NOT set, the trigger pulse must at least be maintained for one system clock period.	0
		0	Enable synchronization. The hardware trigger bypass is not enabled.	
		1	Bypass synchronization. The hardware trigger bypass is enabled.	
25:20	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	N/A
26	START		Writing a 1 to this field will launch one pass through this conversion sequence. The behavior will be identical to a sequence triggered by a hardware trigger. Do not write a 1 to this bit if the BURST bit is set.  <b>Remark:</b> This bit is only set to a 1 momentarily when written to in order to launch a conversion sequence. It will consequently always read-back as a zero.	0
27	BURST		Writing a 1 to this bit will cause this conversion sequence to be continuously cycled through. Other B triggers will be ignored while this bit is set.  Repeated conversions can be halted by clearing this bit. The sequence currently in progress will be completed before conversions are terminated.	0



Table 229. A/D Conversion Sequence B Control Register (SEQB\_CTRL, address 0x4001 C00C) bit description

Bit	Symbol	Value	Description	Reset value
28	SINGLESTEP		When this bit is set, a hardware trigger or a write to the START bit will launch a single conversion on the next channel in the sequence instead of the default response of launching an entire sequence of conversions. Once all of the channels comprising a sequence have been converted, a subsequent trigger will repeat the sequence beginning with the first enabled channel.  Interrupt generation will still occur either after each individual conversion or at the end of the entire sequence, depending on the state of the MODE bit.	0
29	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	N/A
30	MODE		Indicates whether the primary method for retrieving conversion results for this sequence will be accomplished via reading the global data register (SEQB_GDAT) at the end of each conversion, or the individual channel result registers at the end of the entire sequence.  Impacts when conversion-complete interrupt for sequence-B will be generated and which overrun conditions contribute to an overrun interrupt as described below:	0
		0	End of conversion. The sequence B interrupt will be set at the end of each individual A/D conversion performed under sequence B. This flag will mirror the DATAVALID bit in the SEQB_GDAT register.  The OVERRUN bit in the SEQB_GDAT register will contribute to generation of an overrun interrupt if enabled.	
		1	End of sequence. The sequence B interrupt will be set when the entire set of sequence B conversions completes. This flag will need to be explicitly cleared by software in this mode.  The OVERRUN bit in the SEQB_GDAT register will NOT contribute to generation of an overrun interrupt since it is assumed this register will not be utilized in this mode.	
31	SEQB_ENA		Sequence Enable. In order to avoid spuriously triggering the sequence, care should be taken to only set the SEQB_ENA bit when the selected trigger input is in its INACTIVE state (as defined by the TRIGPOL bit). If this condition is not met, the sequence will be triggered immediately upon being enabled.	0
		0	Disabled. Sequence B is disabled. Sequence B triggers are ignored. If this bit is cleared while sequence B is in progress, the sequence will be halted at the end of the current conversion. After the sequence is re-enabled, a new trigger will be required to restart the sequence beginning with the next enabled channel.	
		1	Enabled. Sequence B is enabled.	

### 16.5.4 A/D Global Data Register A and B

The A/D Global Data Registers contain the result of the most recent A/D conversion completed under each conversion sequence.

Results of A/D conversions can be read in one of two ways. One is to use these A/D Global Data Registers to read data from the ADC at the end of each A/D conversion. Another is to read the individual A/D Channel Data Registers, typically after the entire sequence has completed. It is recommended to use one method consistently for a given conversion sequence.

For interrupt-driven code it will more likely be advantageous to wait for an entire sequence to complete and then retrieve the results from the individual channel registers than reading the global data register.

**Remark:** The method to be employed for each sequence should be reflected in the MODE bit in the corresponding ADSEQn\_CTRL register since this will impact interrupt and overrun flag generation.

**Table 230. A/D Sequence A Global Data Register (SEQA\_GDAT, address 0x4001 C010) bit description**

Bit	Symbol	Description	Reset value
3:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	RESULT	<p>This field contains the 12-bit A/D conversion result from the most recent conversion performed under conversion sequence associated with this register.</p> <p>The result is the a binary fraction representing the voltage on the currently-selected input channel as it falls within the range of <math>V_{REFP}</math> to <math>V_{REFN}</math>. Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on <math>V_{REFN}</math>, while 0xFFF indicates that the voltage on the input was close to, equal to, or greater than that on <math>V_{REFP}</math>.</p> <p>DATAVALID = 1 indicates that this result has not yet been read.</p>	NA
17:16	THCMPRANGE	Indicates whether the result of the last conversion performed was above, below or within the range established by the designated threshold comparison registers (THRn_LOW and THRn_HIGH).	
19:18	THCMPCROSS	Indicates whether the result of the last conversion performed represented a crossing of the threshold level established by the designated LOW threshold comparison register (THRn_LOW) and, if so, in what direction the crossing occurred.	
25:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
29:26	CHN	These bits contain the channel from which the RESULT bits were converted (e.g. 0000 identifies channel 0, 0001 channel 1...).	NA
30	OVERRUN	<p>This bit is set if a new conversion result is loaded into the RESULT field before a previous result has been read - i.e. while the DATAVALID bit is set. This bit is cleared, along with the DATAVALID bit, whenever this register is read.</p> <p>This bit will contribute to an overrun interrupt request if the MODE bit (in SEQA_CTRL) for the corresponding sequence is set to '0' (and if the overrun interrupt is enabled).</p>	0
31	DATAVALID	<p>This bit is set to 1 at the end of each conversion when a new result is loaded into the RESULT field. It is cleared whenever this register is read.</p> <p>This bit will cause a conversion-complete interrupt for the corresponding sequence if the MODE bit (in SEQA_CTRL) for that sequence is set to 0 (and if the interrupt is enabled).</p>	0

Table 231. A/D Sequence B Global Data Register (SEQB\_GDAT, address 0x4001 C014) bit description

Bit	Symbol	Description	Reset value
3:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	RESULT	<p>This field contains the 12-bit A/D conversion result from the most recent conversion performed under conversion sequence associated with this register.</p> <p>This will be a binary fraction representing the voltage on the currently-selected input channel as it falls within the range of <math>V_{REFP}</math> to <math>V_{REFN}</math>. Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on <math>V_{REFN}</math>, while 0xFFF indicates that the voltage on the input was close to, equal to, or greater than that on <math>V_{REFP}</math>.</p> <p>DATAVALID = 1 indicates that this result has not yet been read.</p>	NA
17:16	THCMPRANGE	<p>Indicates whether the result of the last conversion performed was above, below or within the range established by the designated threshold comparison registers (THRn_LOW and THRn_HIGH).</p> <p>Threshold Range Comparison result.</p> <p>0x0 = In Range: The last completed conversion was greater than or equal to the value programmed into the designated LOW threshold register (THRn_LOW) but less than or equal to the value programmed into the designated HIGH threshold register (THRn_HIGH).</p> <p>0x1 = Below Range: The last completed conversion on was less than the value programmed into the designated LOW threshold register (THRn_LOW).</p> <p>0x2 = Above Range: The last completed conversion was greater than the value programmed into the designated HIGH threshold register (THRn_HIGH).</p> <p>0x3 = Reserved.</p>	
19:18	THCMPCROSS	<p>Indicates whether the result of the last conversion performed represented a crossing of the threshold level established by the designated LOW threshold comparison register (THRn_LOW) and, if so, in what direction the crossing occurred.</p> <p>0x0 = No threshold Crossing detected: The most recent completed conversion on this channel had the same relationship (above or below) to the threshold value established by the designated LOW threshold register (THRn_LOW) as did the previous conversion on this channel.</p> <p>0x1 = Reserved.</p> <p>0x2 = Downward Threshold Crossing Detected. Indicates that a threshold crossing in the downward direction has occurred - i.e. the previous sample on this channel was above the threshold value established by the designated LOW threshold register (THRn_LOW) and the current sample is below that threshold.</p> <p>0x3 = Upward Threshold Crossing Detected. Indicates that a threshold crossing in the upward direction has occurred - i.e. the previous sample on this channel was below the threshold value established by the designated LOW threshold register (THRn_LOW) and the current sample is above that threshold.</p>	
25:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 231. A/D Sequence B Global Data Register (SEQB\_GDAT, address 0x4001 C014) bit description

Bit	Symbol	Description	Reset value
29:26	CHN	These bits contain the channel from which the RESULT bits were converted (e.g. 0b0000 identifies channel 0, 0b0001 channel 1...).	NA
30	OVERRUN	<p>This bit is set if a new conversion result is loaded into the RESULT field before a previous result has been read - i.e. while the DATAVALID bit is set. This bit is cleared, along with the DATAVALID bit, whenever this register is read.</p> <p>This bit will contribute to an overrun interrupt request if the MODE bit (in SEQB_CTRL) for the corresponding sequence is set to 0 (and if the overrun interrupt is enabled).</p>	0
31	DATAVALID	<p>This bit is set to 1 at the end of each conversion when a new result is loaded into the RESULT field. It is cleared whenever this register is read.</p> <p>This bit will cause a conversion-complete interrupt for the corresponding sequence if the MODE bit (in SEQB_CTRL) for that sequence is set to 0 (and if the interrupt is enabled).</p>	0

### 16.5.5 A/D Channel Data Registers 1 to 8

The A/D Channel Data Registers hold the result of the last conversion completed for each A/D channel. They also include status bits to indicate when a conversion has been completed, when a data overrun has occurred, and where the most recent conversion fits relative to the range dictated by the high and low threshold registers.

Results of A/D conversion can be read in one of two ways. One is to use the A/D Global Data Registers for each of the sequences to read data from the ADC at the end of each A/D conversion. Another is to use these individual A/D Channel Data Registers, typically after the entire sequence has completed. It is recommended to use one method consistently for a given conversion sequence.

**Remark:** The method to be employed for each sequence should be reflected in the MODE bit in the corresponding SEQ\_CTRL register since this will impact interrupt and overrun flag generation.

The information presented in the DAT registers always pertains to the most recent conversion completed on that channel regardless of what sequence requested the conversion or which trigger caused it.

The OVERRUN fields for each channel are also replicated in the FLAGS register.

Table 232. A/D Data Registers (DAT[1:8], address 0x4001 C024 (DAT1) to 0x4001 C040 (DAT8)) bit description

Bit	Symbol	Description	Reset value
3:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	RESULT	This field contains the 12-bit A/D conversion result from the last conversion performed on this channel. This will be a binary fraction representing the voltage on the AD0[n] pin, as it falls within the range of $V_{REFP}$ to $V_{REFN}$ . Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on $V_{REFN}$ , while 0xFFF indicates that the voltage on the input was close to, equal to, or greater than that on $V_{REFP}$ .	NA
17:16	THCMPRANGE	Threshold Range Comparison result. 0x0 = In Range: The last completed conversion was greater than or equal to the value programmed into the designated LOW threshold register (THRn_LOW) but less than or equal to the value programmed into the designated HIGH threshold register (THRn_HIGH). 0x1 = Below Range: The last completed conversion on was less than the value programmed into the designated LOW threshold register (THRn_LOW). 0x2 = Above Range: The last completed conversion was greater than the value programmed into the designated HIGH threshold register (THRn_HIGH). 0x3 = Reserved.	NA
19:18	THCMPCROSS	Threshold Crossing Comparison result. 0x0 = No threshold Crossing detected: The most recent completed conversion on this channel had the same relationship (above or below) to the threshold value established by the designated LOW threshold register (THRn_LOW) as did the previous conversion on this channel. 0x1 = Reserved. 0x2 = Downward Threshold Crossing Detected. Indicates that a threshold crossing in the downward direction has occurred - i.e. the previous sample on this channel was above the threshold value established by the designated LOW threshold register (THRn_LOW) and the current sample is below that threshold. 0x3 = Upward Threshold Crossing Detected. Indicates that a threshold crossing in the upward direction has occurred - i.e. the previous sample on this channel was below the threshold value established by the designated LOW threshold register (THRn_LOW) and the current sample is above that threshold.	NA
25:20	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 232. A/D Data Registers (DAT[1:8], address 0x4001 C024 (DAT1) to 0x4001 C040 (DAT8)) bit description

Bit	Symbol	Description	Reset value
29:26	CHANNEL	This field is hard-coded to contain the channel number that this particular register relates to (i.e. this field will contain 0b0001 for the DAT1 register, 0b0010 for the DAT2 register, etc)	NA
30	OVERRUN	<p>This bit will be set to a 1 if a new conversion on this channel completes and overwrites the previous contents of the RESULT field before it has been read - i.e. while the DONE bit is set.</p> <p>This bit is cleared, along with the DONE bit, whenever this register is read or when the data related to this channel is read from either of the global SEQn_GDAT registers.</p> <p>This bit (in any of the 8 registers) will cause an overrun interrupt request to be asserted if the overrun interrupt is enabled.</p> <p><b>Remark:</b> While it is allowed to include the same channels in both conversion sequences, doing so may cause erratic behavior of the DONE and OVERRUN bits in the data registers associated with any of the channels that are shared between the two sequences. Any erratic OVERRUN behavior will also affect overrun interrupt generation, if enabled.</p>	NA
31	DATAVALID	<p>This bit is set to 1 when an A/D conversion on this channel completes.</p> <p>This bit is cleared whenever this register is read or when the data related to this channel is read from either of the global SEQn_GDAT registers.</p> <p><b>Remark:</b> While it is allowed to include the same channels in both conversion sequences, doing so may cause erratic behavior of the DONE and OVERRUN bits in the data registers associated with any of the channels that are shared between the two sequences. Any erratic OVERRUN behavior will also affect overrun interrupt generation, if enabled.</p>	NA

### 16.5.6 A/D Compare Low Threshold Registers 0 and 1

These registers set the LOW threshold levels against which A/D conversions on all channels will be compared.

Each channel will either be compared to the THR0\_LOW/HIGH registers or to the THR1\_LOW/HIGH registers depending on what is specified for that channel in the CHAN\_THRSEL register.

A conversion result LESS THAN this value on any channel will cause the THCMP\_RANGE status bits for that channel to be set to 0b01. This result will also generate an interrupt request if enabled to do so via the ADCMPINTEN bits associated with each channel in the INTEN register.

If, for two successive conversions on a given channel, one result is below this threshold and the other is equal-to or above this threshold, then a threshold crossing has occurred. In this case the MSB of the THCMP\_CROSS status bits will indicate that a threshold crossing has occurred and the LSB will indicate the direction of the crossing. A threshold crossing event will also generate an interrupt request if enabled to do so via the ADCMPINTEN bits associated with each channel in the INTEN register.

**Table 233. A/D Compare Low Threshold register 0 (THR0\_LOW, address 0x4001 C050) bit description**

Bit	Symbol	Description	Reset value
3:0		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	THRLOW	Low threshold value against which A/D results will be compared	0x000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

**Table 234. A/D Compare Low Threshold register 1 (THR1\_LOW, address 0x4001 C054) bit description**

Bit	Symbol	Description	Reset value
3:0		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	THRLOW	Low threshold value against which A/D results will be compared	0x000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 16.5.7 A/D Compare High Threshold Registers 0 and 1

These registers set the HIGH threshold level against which A/D conversions on all channels will be compared.

Each channel will either be compared to the THR0\_LOW/HIGH registers or to the THR1\_LOW/HIGH registers depending on what is specified for that channel in the CHAN\_THRSEL register.

A conversion result greater than this value on any channel will cause the THCMP status bits for that channel to be set to 0b10. This result will also generate an interrupt request if enabled to do so via the ADCMPINTEN bits associated with each channel in the INTEN register.

**Table 235. Compare High Threshold register0 (THR0\_HIGH, address 0x4001 C058) bit description**

Bit	Symbol	Description	Reset value
3:0		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	THRHIGH	High threshold value against which A/D results will be compared	0x000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA



**Table 236. Compare High Threshold register 1 (THR1\_HIGH, address 0x4001 C05C) bit description**

Bit	Symbol	Description	Reset value
3:0		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:4	THRHIGH	High threshold value against which A/D results will be compared	0x000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 16.5.8 A/D Channel Threshold Select register

For each channel, this register indicates which pair of threshold registers conversion results should be compared to.

**Table 237. A/D Channel Threshold Select register (CHAN\_THRSEL, addresses 0x4001 C060) bit description**

Bit	Symbol	Value	Description	Reset value
0			Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
1	CH1_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 1 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 1 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
2	CH2_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 2 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 2 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
3	CH3_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 3 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 3 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
4	CH4_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 4 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 4 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
5	CH5_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 5 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 5 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	



Table 237. A/D Channel Threshold Select register (CHAN\_THRSEL, addresses 0x4001 C060) bit description

Bit	Symbol	Value	Description	Reset value
6	CH6_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 6 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 6 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
7	CH7_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 7 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 7 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
8	CH8_THRSEL		Threshold select by channel.	0
		0	Threshold 0. Channel 8 results will be compared against the threshold levels indicated in the THR0_LOW and THR0_HIGH registers	
		1	Threshold 1. Channel 8 results will be compared against the threshold levels indicated in the THR1_LOW and THR1_HIGH registers	
31:9			Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 16.5.9 A/D Interrupt Enable Register

There are four separate interrupt requests generated by the ADC: conversion-complete or sequence-complete interrupts for each of the two sequences, a threshold-comparison out-of-range interrupt, and a data overrun interrupt.

These interrupts may be combined into one request on some chips if there is a limited number of interrupt slots. This register contains the interrupt-enable bits for each interrupt.

In this register, threshold events selected in the ADCMPINTENn bits are described as follows:

- Disabled: Threshold comparisons on channel n will not generate an A/D threshold-compare interrupt request.
- Outside threshold: A conversion result on channel n which is outside the range specified by the designated HIGH and LOW threshold registers will set the channel n THCMP flag in the FLAGS register and generate an A/D threshold-compare interrupt request.
- Crossing threshold: Detection of a threshold crossing on channel n will set the channel n THCMP flag in the ADFLAGS register and generate an A/D threshold-compare interrupt request.

**Remark:** Overrun and threshold-compare interrupts related to a particular channel will occur regardless of which sequence was in progress at the time the conversion was performed or what trigger caused the conversion.

Table 238. A/D Interrupt Enable register (INTEN, address 0x4001 C064 ) bit description

Bit	Symbol	Value	Description	Reset value
0	SEQA_INTEN		Sequence A interrupt enable.	0
		0	Disabled. The sequence A interrupt is disabled.	
		1	Enabled. The sequence A interrupt is enabled and will be asserted either upon completion of each individual conversion performed as part of sequence A, or upon completion of the entire A sequence of conversions, depending on the MODE bit in the SEQA_CTRL register.	
1	SEQB_INTEN		Sequence B interrupt enable.	0
		0	Disabled. The sequence B interrupt is disabled.	
		1	Enabled. The sequence B interrupt is enabled and will be asserted either upon completion of each individual conversion performed as part of sequence B, or upon completion of the entire B sequence of conversions, depending on the MODE bit in the SEQB_CTRL register.	
2	OVR_INTEN		Overflow interrupt enable.	0
		0	Disabled. The overflow interrupt is disabled.	
		1	Enabled. The overflow interrupt is enabled. Detection of an overflow condition on any of the 12 channel data registers will cause an overflow interrupt request.  In addition, if the MODE bit for a particular sequence is 0, then an overflow in the global data register for that sequence will also cause this interrupt request to be asserted.	
4:3	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
6:5	ADCMPINTEN1		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved.	
8:7	ADCMPINTEN2		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	
10:9	ADCMPINTEN3		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	
12:11	ADCMPINTEN4		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	

Table 238. A/D Interrupt Enable register (INTEN, address 0x4001 C064 ) bit description

Bit	Symbol	Value	Description	Reset value
14:13	ADCMPINTEN5		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	
16:15	ADCMPINTEN6		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved.	
18:17	ADCMPINTEN7		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	
20:19	ADCMPINTEN8		Threshold comparison interrupt enable.	00
		0x0	Disabled.	
		0x1	Outside threshold.	
		0x2	Crossing threshold.	
		0x3	Reserved	
31:21	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 16.5.10 A/D Flag register

The A/D Flags registers contains the four interrupt request flags along with the individual overrun flags that contribute to an overrun interrupt and the component threshold-comparison flags that contribute to that interrupt.

The channel OVERRUN flags, mirror those in the appearing in the individual ADDAT registers for each channel, indicate a data overrun in each of those registers.

Likewise, the SEQA\_OVR and SEQB\_OVR bits mirror the OVERRUN bits in the two global data registers (SEQA\_GDAT and SEQB\_GDAT).

Table 239. A/D Flags register (FLAGS, address 0x4001 C068) bit description

Bit	Symbol	Description	Reset value
0	-	Reserved.	0
1	THCMP1	Threshold comparison event on Channel 1. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
2	THCMP2	Threshold comparison event on Channel 2. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00

Table 239. A/D Flags register (FLAGS, address 0x4001 C068) bit description

Bit	Symbol	Description	Reset value
3	THCMP3	Threshold comparison event on Channel 3. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
4	THCMP4	Threshold comparison event on Channel 4. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
5	THCMP5	Threshold comparison event on Channel 5. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
6	THCMP6	Threshold comparison event on Channel 6. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
7	THCMP7	Threshold comparison event on Channel 7. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
8	THCMP8	Threshold comparison event on Channel 8. Set to 1 upon either an out-of-range result or a threshold-crossing result if enabled to do so in the INTEN register. This bit is cleared by writing a 1.	00
9	-	Reserved.	00
10	-	Reserved.	00
11	-	Reserved.	00
12	-	Reserved.	0
13	OVERRUN1	Mirrors the OVERRRUN status flag from the result register for A/D channel 1	0
14	OVERRUN2	Mirrors the OVERRRUN status flag from the result register for A/D channel 2	0
15	OVERRUN3	Mirrors the OVERRRUN status flag from the result register for A/D channel 3	0
16	OVERRUN4	Mirrors the OVERRRUN status flag from the result register for A/D channel 4	0
17	OVERRUN5	Mirrors the OVERRRUN status flag from the result register for A/D channel 5	0
18	OVERRUN6	Mirrors the OVERRRUN status flag from the result register for A/D channel 6	0
19	OVERRUN7	Mirrors the OVERRRUN status flag from the result register for A/D channel 7	0
20	OVERRUN8	Mirrors the OVERRRUN status flag from the result register for A/D channel 8	0
21	-	Reserved.	0
22	-	Reserved.	0
23	-	Reserved.	0
24	SEQA_OVR	Mirrors the global OVERRUN status flag in the SEQA_GDAT register	0
25	SEQB_OVR	Mirrors the global OVERRUN status flag in the SEQB_GDAT register	0
27:26	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
28	SEQA_INT	Sequence A interrupt.  If the MODE bit in the SEQA_CTRL register is 0, this flag will mirror the DATAVALID bit in the sequence A global data register (SEQA_GDAT), which is set at the end of every A/D conversion performed as part of sequence A. It will be cleared automatically when the SEQA_GDAT register is read.  If the MODE bit in the SEQA_CTRL register is 1, this flag will be set upon completion of an entire A sequence. In this case it must be cleared by writing a 1 to this SEQA_INT bit.  This interrupt must be enabled in the INTEN register.	0

Table 239. A/D Flags register (FLAGS, address 0x4001 C068) bit description

Bit	Symbol	Description	Reset value
29	SEQB_INT	Sequence A interrupt. If the MODE bit in the SEQB_CTRL register is 0, this flag will mirror the DATAVALID bit in the sequence A global data register (SEQB_GDAT), which is set at the end of every A/D conversion performed as part of sequence B. It will be cleared automatically when the SEQB_GDAT register is read. If the MODE bit in the SEQB_CTRL register is 1, this flag will be set upon completion of an entire B sequence. In this case it must be cleared by writing a 1 to this SEQB_INT bit. This interrupt must be enabled in the INTEN register.	0
30	THCMP_INT	Threshold Comparison Interrupt. This bit will be set if any of the 12 THCMP flags in the lower bits of this register are set to 1 (due to an enabled out-of-range or threshold-crossing event on any channel). Each type of threshold comparison interrupt on each channel must be individually enabled in the INTEN register to cause this interrupt. This bit will be cleared when all of the component flags in bits 11:0 are cleared via writing 1s to those bits.	0
31	OVR_INT	Overflow Interrupt flag. Any overrun bit in any of the individual channel data registers will cause this interrupt. In addition, if the MODE bit in either of the SEQn_CTRL registers is 0 then the OVERRUN bit in the corresponding SEQn_GDAT register will also cause this interrupt. This interrupt must be enabled in the INTEN register. This bit will be cleared when all of the individual overrun bits have been cleared via reading the corresponding data registers.	0

### 16.5.11 A/D trim register

The A/D trim register configures the ADC for the appropriate operating range of the analog supply voltage VDDA.

**Remark:** Failure to set the VRANGE bit correctly causes the ADC to return incorrect conversion results.

Table 240. A/D Flags register (TRM, addresses 0x4001 C06C) bit description

Bit	Symbol	Value	Description	Reset value
4:0	-		Reserved.	-
5	VRANGE		Reserved.	0
		0	High voltage. VDDA = 2.7 V to 3.6 V.	
		1	Low voltage. VDDA = 1.8 V to 2.7 V.	
31:6	-		Reserved.	-

## 16.6 Functional description

### 16.6.1 Conversion Sequences

A conversion sequence is a single pass through a series of A/D conversions performed on a selected set of A/D channels. Software can set-up two independent conversion sequences, either of which can be triggered by software or by a transition on one of the

hardware triggers. Each sequence can be triggered by a different hardware trigger. One of these conversion sequences is referred to as the A sequence and the other as the B sequence. It is not necessary to employ both sequences.

An optional single-step mode allows advancing through the channels of a sequence one at a time on each successive occurrence of a trigger.

The user can select whether a trigger on the B sequence can interrupt an already-in-progress A sequence. The B sequence, however, can never be interrupted by an A trigger.

### 16.6.2 Hardware-triggered conversion

Software can select which of these hardware triggers will launch each conversion sequence and it can specify the active edge for the selected trigger independently for each conversion sequence.

For each conversion sequence, if a designated trigger event occurs, one single cycle through that conversion sequence will be launched unless:

- The BURST bit in the ADSEQn\_CTRL register for this sequence is set to 1.
- The requested conversion sequence is already in progress.
- A set of conversions for the alternate conversion sequence is already in progress except in the case of a B trigger interrupting an A sequence if the A sequence is set to LOWPRIO.

If any of these conditions is true, the new trigger event will be ignored and will have no effect.

In addition, if the single-step bit for a sequence is set, each new trigger will cause a single conversion to be performed on the next channel in the sequence rather than launching a pass through the entire sequence.

If the A sequence is enabled to be interrupted (i.e. the LOWPRIO bit in the SEQn\_CTRL register is set) and a B trigger occurs while an A sequence is in progress, then the following will occur:

- The A/D conversion which is currently in-progress will be aborted.
- The A sequence will be paused, and the B sequence will immediately commence.
- The interrupted A sequence will resume after the B sequence completes, beginning with the conversion that was aborted when the interruption occurred. The channel for that conversion will be re-sampled.

#### 16.6.2.1 Avoiding spurious hardware triggers

Care should be taken to avoid generating a spurious trigger when writing to the SEQn\_CTRL register to change the trigger selected for the sequence, switch the polarity of the selected trigger, or to enable the sequence for operation.

In general, the TRIGGER and TRIGPOL bits in the SEQn\_CTRL register should only be written to when the sequence is disabled (while the SEQn\_ENA bit is LOW). The SEQn\_ENA bit itself should only be set when the selected trigger input is in its INACTIVE

state (as designated by the TRIGPOL bit). If this condition is not met, a trigger will be generated immediately upon enabling the sequence - even though no actual transition has occurred on the trigger input.

### 16.6.3 Software-triggered conversion

There are two ways that software can trigger a conversion sequence:

1. Start Bit: The first way to software-trigger an sequence is by setting the START bit in the corresponding SEQn\_CTRL register. The response to this is identical to occurrence of a hardware trigger on that sequence. Specifically, one cycle of conversions through that conversion sequence will be immediately triggered except as indicated above.
2. Burst Mode: The other way to initiate conversions is to set the BURST bit in the SEQn\_CTRL register. As long as this bit is 1 the designated conversion sequence will be continuously and repetitively cycled through. Any new software or hardware trigger on this sequence will be ignored.

If a bursting A sequence is allowed to be interrupted (i.e. the LOWPRIO bit in its SEQA\_CTRL register is set to 1 and a software or hardware trigger for the B sequence occurs, then the burst will be immediately interrupted and a B sequence will be initiated. The interrupted A sequence will resume continuous cycling, starting with the aborted conversion, after the alternate sequence has completed.

### 16.6.4 Interrupts

There are four interrupts that can be generated by the ADC:

- Conversion-Complete or Sequence-Complete interrupts for sequences A and B
- Threshold-Compare Out-of-Range Interrupt
- Data Overrun Interrupt

Any of these interrupt requests may be individually enabled or disabled in the INTEN register.

#### 16.6.4.1 Conversion-Complete or Sequence-Complete interrupts

For each of the two sequences, an interrupt request can either be asserted at the end of each A/D conversion performed as part of that sequence or when the entire sequence of conversions is completed. The MODE bits in the SEQn\_CTRL registers select between these alternative behaviors.

If the MODE bit for a sequence is 0 (conversion-complete mode) then the interrupt flag for that sequence will reflect the state of the DATAVALID bit in the global data register (SEQn\_GDAT) for that sequence. In this case, reading the SEQn\_GDAT register will automatically clear the interrupt request.

If the MODE bit for the sequence is 1 (sequence-complete mode) then the interrupt flag must be written-to by software to clear it.



#### 16.6.4.2 Threshold-Compare Out-of-Range Interrupt

Every conversion performed on any channel is automatically compared against a designated set of low and high threshold levels specified in the `THRn_HIGH` and `THRn_LOW` registers. The results of this comparison on any individual channel(s) can be enabled to cause a threshold-compare interrupt if that result was above or below the range specified by the two thresholds or, alternatively, if the result represented a crossing of the low threshold in either direction.

This flag must be cleared by a software write to clear the individual `THCMP` flags in the `FLAGS` register.

#### 16.6.4.3 Data Overrun Interrupt

This interrupt request will be asserted if any of the `OVERRUN` bits in the individual channel data registers are set. In addition, the `OVERRUN` bits in the two sequence global data (`SEQn_GDAT`) registers will cause this interrupt request IF the `MODE` bit for that sequence is set to 0 (conversion-complete mode).

This flag will be cleared when the `OVERRUN` bit that caused it is cleared via reading the register containing it.

Note that the `OVERRUN` bits in the individual data registers are cleared when data related to that channel is read from either of the global data registers as well as when the individual data registers themselves are read.

#### 16.6.5 Optional Operating Modes

The following optional mode of A/D operation may be selected in the `CTRL` register:

Low-power mode. When this mode is selected, the analog portions of the ADC are automatically shut down when no conversions are in progress. The ADC is automatically restarted whenever any hardware or software trigger event occurs. This mode can save an appreciable amount of power when the ADC is not in continuous use, but at the expense of a delay between the trigger event and the onset of sampling and conversion.

#### 16.6.6 Self-Calibration

The A/D converter includes a built-in, self-calibration mode. In order to achieve the specified ADC accuracy, the A/D converter must be recalibrated, at a minimum, following every chip reset before initiating normal ADC operation. In applications where the chip is expected to operate over extended periods without being reset or powered-down, it may be advisable to perform calibration on a periodic basis.

**Remark:** It is strongly recommended that the provided API call be used to initiate calibration. The API routine will save any existing Control Register settings, then modify those settings as required and set the `CAL_MODE` bit to launch calibration. When calibration completes, the API routine will restore the original user settings to the Control Register.

A calibration cycle will require approximately 290  $\mu$ s to complete. Normal ADC conversions cannot be launched, and the ADC Control Register must not be written-to while calibration is in progress.



### 16.6.7 ADC vs. digital receiver

The ADC function must be selected via the IOCON registers in order to get accurate voltage readings on the monitored pin. The PINMODE should also be set to the mode for which neither pull-up nor pull-down resistor is enabled. For a pin hosting an ADC input, it is not possible to have a digital function selected and yet get valid ADC readings. An inside circuit disconnects ADC hardware from the associated pin whenever a digital function is selected on that pin.

### 16.6.8 Hardware Trigger Source Selection

Each ADC has a selection of up to eight hardware trigger sources. The trigger to be used for each conversion sequence is specified in the TRIGGER fields in the two SEQn\_CTRL registers.

### 17.1 Features

- Flash access times can be configured through a register in the flash controller block.
- Flash signature generation

### 17.2 Register description

Table 241. Register overview: FMC (base address 0x4003 C000)

Name	Access	Address offset	Description	Reset value	Reference
FLASHCFG	R/W	0x010	Flash access time configuration register	-	<a href="#">Table 242</a>
FMSSTART	R/W	0x020	Signature start address register	0	<a href="#">Table 252</a>
FMSSTOP	R/W	0x024	Signature stop-address register	0	<a href="#">Table 253</a>
FMSW0	R	0x02C	Word 0 [31:0]	-	<a href="#">Table 254</a>
FMSW1	R	0x030	Word 1 [63:32]	-	<a href="#">Table 255</a>
FMSW2	R	0x034	Word 2 [95:64]	-	<a href="#">Table 256</a>
FMSW3	R	0x038	Word 3 [127:96]	-	<a href="#">Table 257</a>
FMSTAT	R	0xFE0	Signature generation status register	0	<a href="#">Table 258</a>
FMSTATCLR	W	0xFE8	Signature generation status clear register	-	<a href="#">Table 259</a>

#### 17.2.1 Flash configuration register

Depending on the system clock frequency, access to the flash memory can be configured with various access times by writing to the FLASHCFG register at address 0x4003 C010.

**Remark:** Improper setting of this register may result in incorrect operation of the flash memory.

Table 242. Flash configuration register (FLASHCFG, address 0x4003 C010) bit description

Bit	Symbol	Value	Description	Reset value
1:0	FLASHTIM		Flash memory access time. FLASHTIM + 1 is equal to the number of system clocks used for flash access.	0b10
		0x0	1 system clock flash access time (for system clock frequencies of up to 20 MHz).	
		0x1	2 system clocks flash access time (for system clock frequencies of up to 40 MHz).	
		0x2	3 system clocks flash access time (for system clock frequencies of up to 50 MHz).	
		0x3	Reserved.	
31:2	-	-	Reserved. <b>User software must not change the value of these bits. Bits 31:2 must be written back exactly as read.</b>	-

### 17.2.2 Signature generation address and control registers

These registers control automatic signature generation. A signature can be generated for any part of the flash memory contents. The address range to be used for generation is defined by writing the start address to the signature start address register (FMSSTART) and the stop address to the signature stop address register (FMSSTOP. The start and stop addresses must be aligned to 128-bit boundaries and can be derived by dividing the byte address by 16.

Signature generation is started by setting the SIG\_START bit in the FMSSTOP register. Setting the SIG\_START bit is typically combined with the signature stop address in a single write.

[Table 252](#) and [Table 253](#) show the bit assignments in the FMSSTART and FMSSTOP registers respectively.

**Table 243. Flash Module Signature Start register (FMSSTART, address 0x4003 C020) bit description**

Bit	Symbol	Description	Reset value
16:0	START	Signature generation start address (corresponds to AHB byte address bits[20:4]).	0
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

**Table 244. Flash Module Signature Stop register (FMSSTOP, address 0x4003 C024) bit description**

Bit	Symbol	Value	Description	Reset value
16:0	STOP		BIST stop address divided by 16 (corresponds to AHB byte address [20:4]).	0
17	SIG_START		Start control bit for signature generation.	0
		0	Stop. Signature generation is stopped	
		1	Start. Initiate signature generation	
31:18	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 17.2.3 Signature generation result registers

The signature generation result registers return the flash signature produced by the embedded signature generator. The 128-bit signature is reflected by the four registers FMSW0, FMSW1, FMSW2 and FMSW3.

The generated flash signature can be used to verify the flash memory contents. The generated signature can be compared with an expected signature and thus makes saves time and code space. The method for generating the signature is described in [Section 17.3.2](#).

[Table 257](#) show bit assignment of the FMSW0 and FMSW1, FMSW2, FMSW3 registers respectively.

**Table 245. FMSW0 register (FMSW0, address 0x4003 C02C) bit description**

Bit	Symbol	Description	Reset value
31:0	SW0	Word 0 of 128-bit signature (bits 31 to 0).	-

**Table 246. FMSW1 register (FMSW1, address 0x4003 C030) bit description**

Bit	Symbol	Description	Reset value
31:0	SW1	Word 1 of 128-bit signature (bits 63 to 32).	-

**Table 247. FMSW2 register (FMSW2, address 0x4003 C034) bit description**

Bit	Symbol	Description	Reset value
31:0	SW2	Word 2 of 128-bit signature (bits 95 to 64).	-

**Table 248. FMSW3 register (FMSW3, address 0x4003 40C8) bit description**

Bit	Symbol	Description	Reset value
31:0	SW3	Word 3 of 128-bit signature (bits 127 to 96).	-

### 17.2.4 Flash Module Status register

The read-only FMSTAT register provides a means of determining when signature generation has completed. Completion of signature generation can be checked by polling the SIG\_DONE bit in FMSTAT. SIG\_DONE should be cleared via the FMSTATCLR register before starting a signature generation operation, otherwise the status might indicate completion of a previous operation.

**Table 249. Flash module Status register (FMSTAT, address 0x4003 CFE0) bit description**

Bit	Symbol	Description	Reset value
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE	When 1, a previously started signature generation has completed. See FMSTATCLR register description for clearing this flag.	0
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 17.2.5 Flash Module Status Clear register

The FMSTATCLR register is used to clear the signature generation completion flag.

**Table 250. Flash Module Status Clear register (FMSTATCLR, address 0x0x4003 CFE8) bit description**

Bit	Symbol	Description	Reset value
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE_CLR	Writing a 1 to this bits clears the signature generation completion flag (SIG_DONE) in the FMSTAT register.	0
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 17.3 Flash signature generation

The flash module contains a built-in signature generator. This generator can produce a 128-bit signature from a range of flash memory. A typical usage is to verify the flashed contents against a calculated signature (e.g. during programming).

The address range for generating a signature must be aligned on flash-word boundaries, i.e. 128-bit boundaries. Once started, signature generation completes independently. While signature generation is in progress, the flash memory cannot be accessed for other purposes, and an attempted read will cause a wait state to be asserted until signature generation is complete. Code outside of the flash (e.g. internal RAM) can be executed during signature generation. This can include interrupt services, if the interrupt vector table is re-mapped to memory other than the flash memory. The code that initiates signature generation should also be placed outside of the flash memory.

### 17.3.1 Register description for signature generation

**Table 251. Register overview: FMC (base address 0x4003 C000)**

Name	Access	Address offset	Description	Reset value	Reference
FMSSTART	R/W	0x020	Signature start address register	0	<a href="#">Table 252</a>
FMSSTOP	R/W	0x024	Signature stop-address register	0	<a href="#">Table 253</a>
FMSW0	R	0x02C	Word 0 [31:0]	-	<a href="#">Table 254</a>
FMSW1	R	0x030	Word 1 [63:32]	-	<a href="#">Table 255</a>
FMSW2	R	0x034	Word 2 [95:64]	-	<a href="#">Table 256</a>
FMSW3	R	0x038	Word 3 [127:96]	-	<a href="#">Table 257</a>
FMSTAT	R	0xFE0	Signature generation status register	0	<a href="#">Section 17.3.1.3</a>
FMSTATCLR	W	0xFE8	Signature generation status clear register	-	<a href="#">Section 17.3.1.4</a>

#### 17.3.1.1 Signature generation address and control registers

These registers control automatic signature generation. A signature can be generated for any part of the flash memory contents. The address range to be used for generation is defined by writing the start address to the signature start address register (FMSSTART) and the stop address to the signature stop address register (FMSSTOP). The start and stop addresses must be aligned to 128-bit boundaries and can be derived by dividing the byte address by 16.

Signature generation is started by setting the SIG\_START bit in the FMSSTOP register. Setting the SIG\_START bit is typically combined with the signature stop address in a single write.

[Table 252](#) and [Table 253](#) show the bit assignments in the FMSSTART and FMSSTOP registers respectively.

**Table 252. Flash Module Signature Start register (FMSSTART - 0x4003 C020) bit description**

Bit	Symbol	Description	Reset value
16:0	START	Signature generation start address (corresponds to AHB byte address bits[20:4]).	0
31:17	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

**Table 253. Flash Module Signature Stop register (FMSSTOP - 0x4003 C024) bit description**

Bit	Symbol	Value	Description	Reset value
16:0	STOP		BIST stop address divided by 16 (corresponds to AHB byte address [20:4]).	0
17	SIG_START		Start control bit for signature generation.	0
		0	Signature generation is stopped	
		1	Initiate signature generation	
31:18	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 17.3.1.2 Signature generation result registers

The signature generation result registers return the flash signature produced by the embedded signature generator. The 128-bit signature is reflected by the four registers FMSW0, FMSW1, FMSW2 and FMSW3.

The generated flash signature can be used to verify the flash memory contents. The generated signature can be compared with an expected signature and thus makes saves time and code space. The method for generating the signature is described in [Section 17.3.2](#).

[Table 257](#) show bit assignment of the FMSW0 and FMSW1, FMSW2, FMSW3 registers respectively.

**Table 254. FMSW0 register bit description (FMSW0, address: 0x4003 C02C)**

Bit	Symbol	Description	Reset value
31:0	SW0[31:0]	Word 0 of 128-bit signature (bits 31 to 0).	-

**Table 255. FMSW1 register bit description (FMSW1, address: 0x4003 C030)**

Bit	Symbol	Description	Reset value
31:0	SW1[63:32]	Word 1 of 128-bit signature (bits 63 to 32).	-

**Table 256. FMSW2 register bit description (FMSW2, address: 0x4003 C034)**

Bit	Symbol	Description	Reset value
31:0	SW2[95:64]	Word 2 of 128-bit signature (bits 95 to 64).	-

**Table 257. FMSW3 register bit description (FMSW3, address: 0x4003 40C8)**

Bit	Symbol	Description	Reset value
31:0	SW3[127:96]	Word 3 of 128-bit signature (bits 127 to 96).	-

### 17.3.1.3 Flash Module Status register

The read-only FMSTAT register provides a means of determining when signature generation has completed. Completion of signature generation can be checked by polling the SIG\_DONE bit in FMSTAT. SIG\_DONE should be cleared via the FMSTATCLR register before starting a signature generation operation, otherwise the status might indicate completion of a previous operation.

**Table 258. Flash module Status register (FMSTAT - 0x4003 CFE0) bit description**

Bit	Symbol	Description	Reset value
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE	When 1, a previously started signature generation has completed. See FMSTATCLR register description for clearing this flag.	0
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

### 17.3.1.4 Flash Module Status Clear register

The FMSTATCLR register is used to clear the signature generation completion flag.

**Table 259. Flash Module Status Clear register (FMSTATCLR - 0x0x4003 CFE8) bit description**

Bit	Symbol	Description	Reset value
1:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	SIG_DONE_CLR	Writing a 1 to this bits clears the signature generation completion flag (SIG_DONE) in the FMSTAT register.	0
31:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

## 17.3.2 Algorithm and procedure for signature generation

### Signature generation

A signature can be generated for any part of the flash contents. The address range to be used for signature generation is defined by writing the start address to the FMSSTART register, and the stop address to the FMSSTOP register.

The signature generation is started by writing a '1' to the SIG\_START bit in the FMSSTOP register. Starting the signature generation is typically combined with defining the stop address, which is done in the STOP bits of the same register.

The time that the signature generation takes is proportional to the address range for which the signature is generated. Reading of the flash memory for signature generation uses a self-timed read mechanism and does not depend on any configurable timing settings for the flash. A safe estimation for the duration of the signature generation is:

$$\text{Duration} = \text{int}((60 / t_{cy}) + 3) \times (\text{FMSSTOP} - \text{FMSSTART} + 1)$$

When signature generation is triggered via software, the duration is in AHB clock cycles, and *tcy* is the time in ns for one AHB clock. The SIG\_DONE bit in FMSTAT can be polled by software to determine when signature generation is complete.

After signature generation, a 128-bit signature can be read from the FMSW0 to FMSW3 registers. The 128-bit signature reflects the corrected data read from the flash. The 128-bit signature reflects flash parity bits and check bit values.

### Content verification

The signature as it is read from the FMSW0 to FMSW3 registers must be equal to the reference signature. The algorithms to derive the reference signature is given in [Figure 52](#).

```
int128 signature = 0
int128 nextSignature
FOR address = flashpage 0 TO address = flashpage max
{
    FOR i = 0 TO 126 {
        nextSignature[i] = flashword[i] XOR signature[i+1]}
    nextSignature[127] = flashword[127] XOR signature[0] XOR signature[2]
        XOR signature[27] XOR signature[29]
    signature = nextSignature
}
return signature
```

**Fig 52. Algorithm for generating a 128-bit signature**



### 18.1 Features

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- In-System Programming: In-System programming (ISP) is programming or reprogramming the on-chip flash memory, using the boot loader software and UART serial port. This can be done when the part resides in the end-user board.
- In-Application Programming: In-Application (IAP) programming is performing erase and write operation on the on-chip flash memory, as directed by the end-user application code.
- Flash access times can be configured through a register in the flash controller block.

### 18.2 General description

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#### 18.2.1 Boot loader

The boot loader controls initial operation after reset and also provides the means to accomplish programming of the flash memory via UART. This could be initial programming of a blank device, erasure and re-programming of a previously programmed device, or programming of the flash memory by the application program in a running system.

The boot loader code is executed every time the part is powered on or reset. The loader can execute the ISP command handler or the user application code. A LOW level after reset at the PIO0\_1 pin is considered as an external hardware request to start the ISP command handler either via UART, if present.

**Remark:** SRAM location 0x1000 0000 to 0x1000 0050 is not used by the boot loader and the memory content in this area is retained during reset. SRAM memory is not retained when the part powers down or enters Deep power-down mode.

Assuming that power supply pins are on their nominal levels when the rising edge on RESET pin is generated, it may take up to 3 ms before PIO0\_1 is sampled and the decision whether to continue with user code or ISP handler is made. If PIO0\_1 is sampled low and the watchdog overflow flag is set, the external hardware request to start the ISP command handler is ignored. If there is no request for the ISP command handler execution (PIO0\_1 is sampled HIGH after reset), a search is made for a valid user program. If a valid user program is found then the execution control is transferred to it. If a valid user program is not found, the auto-baud routine is invoked.

**Remark:** The sampling of pin PIO0\_1 can be disabled through programming flash location 0x0000 02FC (see [Section 18.2.7.1](#)).

#### 18.2.2 Memory map after any reset

The boot block is 16 kB in size. The boot block is located in the memory region starting from the address 0x1FFF 0000. The boot loader is designed to run from this memory area, but both the ISP and IAP software use parts of the on-chip RAM. The RAM usage is

described later in this chapter. The interrupt vectors residing in the boot block of the on-chip flash memory also become active after reset, i.e., the bottom 512 bytes of the boot block are also visible in the memory region starting from the address 0x0000 0000.

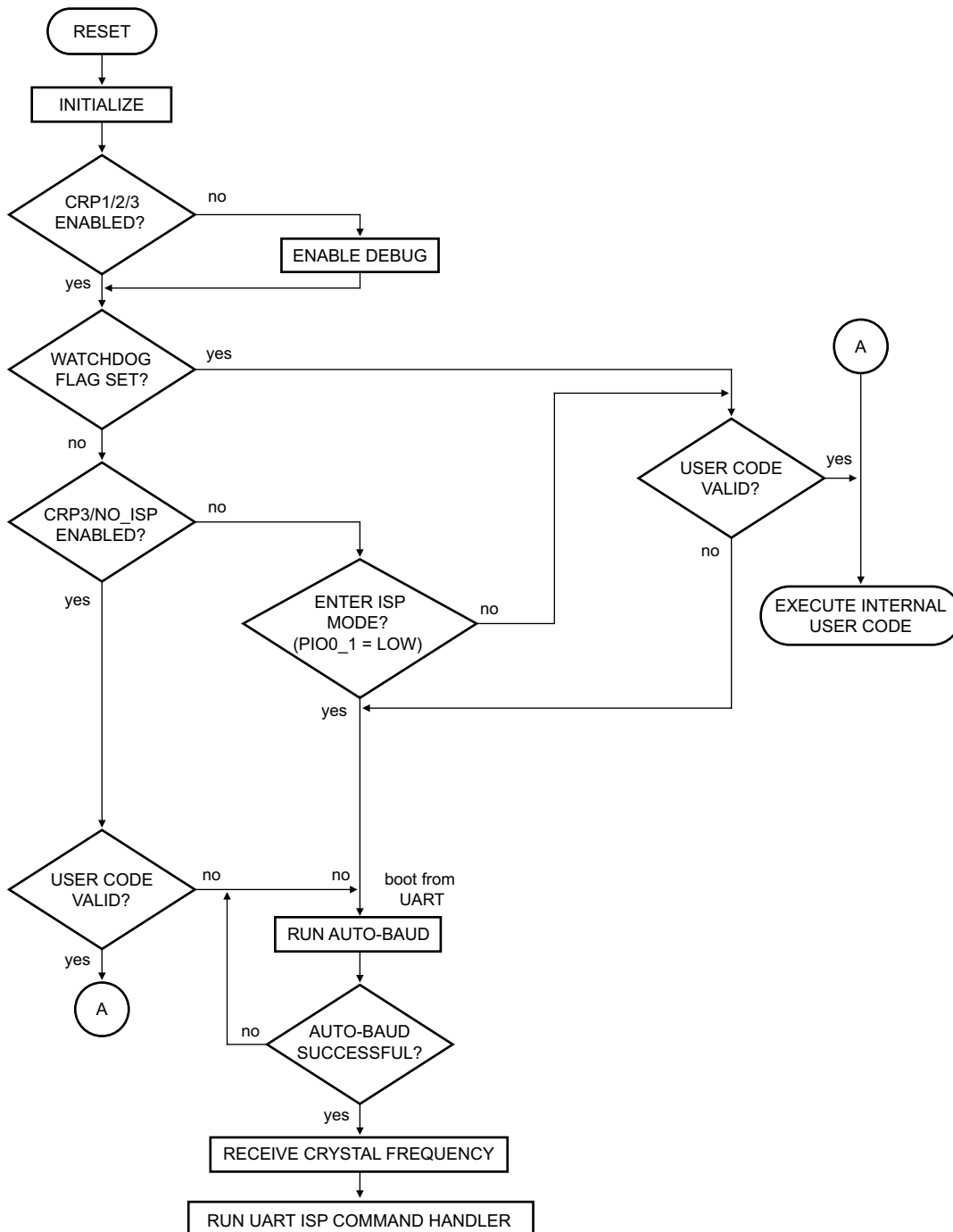
### 18.2.3 Criterion for Valid User Code

Criterion for valid user code: The reserved Cortex-M0 exception vector location 7 (offset 0x 0000 001C in the vector table) should contain the 2's complement of the check-sum of table entries 0 through 6. This causes the checksum of the first 8 table entries to be 0. The boot loader code checksums the first 8 locations in sector 0 of the flash. If the result is 0, then execution control is transferred to the user code.

If the signature is not valid, the auto-baud routine synchronizes with the host via serial port 0. The host should send a '?' (0x3F) as a synchronization character and wait for a response. The host side serial port settings should be 8 data bits, 1 stop bit and no parity. The auto-baud routine measures the bit time of the received synchronization character in terms of its own frequency and programs the baud rate generator of the serial port. It also sends an ASCII string ("Synchronized<CR><LF>") to the host. In response to this host should send the same string ("Synchronized<CR><LF>"). The auto-baud routine looks at the received characters to verify synchronization. If synchronization is verified then "OK<CR><LF>" string is sent to the host. The host should respond by sending the crystal frequency (in kHz) at which the part is running. For example, if the part is running at 10 MHz, the response from the host should be "10000<CR><LF>". "OK<CR><LF>" string is sent to the host after receiving the crystal frequency. If synchronization is not verified then the auto-baud routine waits again for a synchronization character. For auto-baud to work correctly in case of user invoked ISP, the CCLK frequency should be greater than or equal to 10 MHz.

Once the crystal frequency is received the part is initialized and the ISP command handler is invoked. For safety reasons an "Unlock" command is required before executing the commands resulting in flash erase/write operations and the "Go" command. The rest of the commands can be executed without the unlock command. The Unlock command is required to be executed once per ISP session. The Unlock command is explained in [Section 18.4 "API description \(ISP commands\)" on page 265](#).

### 18.2.4 Boot process flowchart



(1) For details on handling the crystal frequency, see [Section 18.5.8 "Reinvoke ISP \(IAP\)" on page 279](#)

**Fig 53. Boot process flowchart**

### 18.2.5 Flash configuration

Some IAP and ISP commands operate on sectors and specify sector numbers. In addition, a page erase command is supported. The following table shows the correspondence between page numbers, sector numbers, and memory addresses.

The size of a sector is 4 kB, the size of a page is 256 Byte. One sector contains 16 pages.

**Table 260. Flash configuration**

Sector number	Sector size [kB]	Page number	Address range
0	4	0 - 15	0x0000 0000 - 0x0000 0FFF
1	4	16 - 31	0x0000 1000 - 0x0000 1FFF
2	4	32 - 47	0x0000 2000 - 0x0000 2FFF
3	4	48 - 63	0x0000 3000 - 0x0000 3FFF
4	4	64 - 79	0x0000 4000 - 0x0000 4FFF
5	4	80 - 95	0x0000 5000 - 0x0000 5FFF
6	4	96 - 111	0x0000 6000 - 0x0000 6FFF
7	4	112 - 127	0x0000 7000 - 0x0000 7FFF
8	4	128 - 143	0x0000 8000 - 0x0000 8FFF
9	4	144 - 159	0x0000 9000 - 0x0000 9FFF
10	4	160 - 175	0x0000 A000 - 0x0000 AFFF
11	4	176 - 191	0x0000 B000 - 0x0000 BFFF
12	4	192 - 207	0x0000 C000 - 0x0000 CFFF
13	4	208 - 223	0x0000 D000 - 0x0000 DFFF
14	4	224 - 239	0x0000 E000 - 0x0000 EFFF
15	4	240 - 255	0x0000 F000 - 0x0000 FFFF

### 18.2.6 Flash content protection mechanism

The part is equipped with the Error Correction Code (ECC) capable Flash memory. The purpose of an error correction module is twofold. Firstly, it decodes data words read from the memory into output data words. Secondly, it encodes data words to be written to the memory. The error correction capability consists of single bit error correction with Hamming code.

The operation of ECC is transparent to the running application. The ECC content itself is stored in a flash memory not accessible by user's code to either read from it or write into it on its own. A byte of ECC corresponds to every consecutive 128 bits of the user accessible Flash. Consequently, Flash bytes from 0x0000 0000 to 0x0000 000F are protected by the first ECC byte, Flash bytes from 0x0000 0010 to 0x0000 001F are protected by the second ECC byte, etc.

Whenever the CPU requests a read from user's Flash, both 128 bits of raw data containing the specified memory location and the matching ECC byte are evaluated. If the ECC mechanism detects a single error in the fetched data, a correction will be applied before data are provided to the CPU. When a write request into the user's Flash is made, write of user specified content is accompanied by a matching ECC value calculated and stored in the ECC memory.

When a sector of Flash memory is erased, the corresponding ECC bytes are also erased. Once an ECC byte is written, it can not be updated unless it is erased first. Therefore, for the implemented ECC mechanism to perform properly, data must be written into the flash memory in groups of 16 bytes (or multiples of 16), aligned as described above.

### 18.2.7 Code Read Protection (CRP)

Code Read Protection is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the ISP can be restricted. When needed, CRP is invoked by programming a specific pattern in flash location at 0x0000 02FC. IAP commands are not affected by the code read protection.

**Important: any CRP change becomes effective only after the device has gone through a power cycle.**

**Table 261. Code Read Protection options**

Name	Pattern programmed in 0x0000 02FC	Description
NO_ISP	0x4E69 7370	Prevents sampling of pin PIO0_1 for entering ISP mode. PIO0_1 is available for other uses.

Table 261. Code Read Protection options

Name	Pattern programmed in 0x0000 02FC	Description
CRP1	0x12345678	<p>Access to chip via the SWD pins is disabled. This mode allows partial flash update using the following ISP commands and restrictions:</p> <ul style="list-style-type: none"> <li>• Write to RAM command should not access RAM below 0x1000 0300. Access to addresses below 0x1000 0200 is disabled.</li> <li>• Copy RAM to flash command can not write to Sector 0.</li> <li>• Erase command can erase Sector 0 only when all sectors are selected for erase.</li> <li>• Compare command is disabled.</li> <li>• Read Memory command is disabled.</li> </ul> <p>This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased. Since compare command is disabled in case of partial updates the secondary loader should implement checksum mechanism to verify the integrity of the flash.</p>
CRP2	0x87654321	<p>Access to chip via the SWD pins is disabled. The following ISP commands are disabled:</p> <ul style="list-style-type: none"> <li>• Read Memory</li> <li>• Write to RAM</li> <li>• Go</li> <li>• Copy RAM to flash</li> <li>• Compare</li> </ul> <p>When CRP2 is enabled the ISP erase command only allows erasure of all user sectors.</p>
CRP3	0x43218765	<p>Access to chip via the SWD pins is disabled. ISP entry by pulling PIO0_1 LOW is disabled if a valid user code is present in flash sector 0.</p> <p>This mode effectively disables ISP override using PIO0_1 pin. It is up to the user's application to provide a flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART.</p> <p><b>Caution: If CRP3 is selected, no future factory testing can be performed on the device.</b></p>

Table 262. Code Read Protection hardware/software interaction

CRP option	User Code Valid	PIO0_1 pin at reset	SWD enabled	LPC111x/ LPC11Cxx enters ISP mode	partial flash update in ISP mode
None	No	x	Yes	Yes	Yes
None	Yes	High	Yes	No	NA
None	Yes	Low	Yes	Yes	Yes
CRP1	Yes	High	No	No	NA
CRP1	Yes	Low	No	Yes	Yes
CRP2	Yes	High	No	No	NA
CRP2	Yes	Low	No	Yes	No
CRP3	Yes	x	No	No	NA

Table 262. Code Read Protection hardware/software interaction

CRP option	User Code Valid	PIO0_1 pin at reset	SWD enabled	LPC111x/ LPC11Cxx enters ISP mode	partial flash update in ISP mode
CRP1	No	x	No	Yes	Yes
CRP2	No	x	No	Yes	No
CRP3	No	x	No	Yes	No

Table 263. ISP commands allowed for different CRP levels

ISP command	CRP1	CRP2	CRP3 (no entry in ISP mode allowed)
Unlock	yes	yes	n/a
Set Baud Rate	yes	yes	n/a
Echo	yes	yes	n/a
Write to RAM	yes; above 0x1000 0300 only	no	n/a
Read Memory	no	no	n/a
Prepare sector(s) for write operation	yes	yes	n/a
Copy RAM to flash	yes; not to sector 0	no	n/a
Go	no	no	n/a
Erase sector(s)	yes; sector 0 can only be erased when all sectors are erased.	yes; all sectors only	n/a
Blank check sector(s)	no	no	n/a
Read Part ID	yes	yes	n/a
Read Boot code version	yes	yes	n/a
Compare	no	no	n/a
ReadUID	yes	yes	n/a

In case a CRP mode is enabled and access to the chip is allowed via the ISP, an unsupported or restricted ISP command will be terminated with return code `CODE_READ_PROTECTION_ENABLED`.

### 18.2.7.1 ISP entry protection

In addition to the three CRP modes, the user can prevent the sampling of pin PIO0\_1 for entering ISP mode and thereby release pin PIO0\_1 for other uses. This is called the NO\_ISP mode. The NO\_ISP mode can be entered by programming the pattern 0x4E69 7370 at location 0x0000 02FC.

## 18.2.8 Debug notes

### 18.2.8.1 Comparing flash images

Depending on the debugger used and the IDE debug settings, the memory that is visible when the debugger connects might be the boot ROM, the internal SRAM, or the flash. To help determine which memory is present in the current debug environment, check the

value contained at flash address 0x0000 0004. This address contains the entry point to the code in the ARM Cortex-M0 vector table, which is the bottom of the boot ROM, the internal SRAM, or the flash memory respectively.

**Table 264. Memory mapping in debug mode**

Memory mapping mode	Memory start address visible at 0x0000 0004
Bootloader mode	0x1FFF 0000
User flash mode	0x0000 0000
User SRAM mode	0x1000 0000

### 18.2.8.2 Serial Wire Debug (SWD) flash programming interface

Debug tools can write parts of the flash image to RAM and then execute the IAP call "Copy RAM to flash" repeatedly with proper offset.

## 18.3 UART Communication protocol

All UART ISP commands should be sent as single ASCII strings. Strings should be terminated with Carriage Return (CR) and/or Line Feed (LF) control characters. Extra <CR> and <LF> characters are ignored. All ISP responses are sent as <CR><LF> terminated ASCII strings. Data is sent and received in UU-encoded format.

### 18.3.1 UART ISP command format

"Command Parameter\_0 Parameter\_1 ... Parameter\_n<CR><LF>" "Data" (Data only for Write commands).

### 18.3.2 UART ISP response format

"Return\_Code<CR><LF>Response\_0<CR><LF>Response\_1<CR><LF> ... Response\_n<CR><LF>" "Data" (Data only for Read commands).

### 18.3.3 UART ISP data format

The data stream is in UU-encoded format. The UU-encode algorithm converts 3 bytes of binary data in to 4 bytes of printable ASCII character set. It is more efficient than Hex format which converts 1 byte of binary data in to 2 bytes of ASCII hex. The sender should send the check-sum after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. The receiver should compare it with the check-sum of the received bytes. If the check-sum matches then the receiver should respond with "OK<CR><LF>" to continue further transmission. If the check-sum does not match the receiver should respond with "RESEND<CR><LF>". In response the sender should retransmit the bytes.

### 18.3.4 UART ISP flow control

A software XON/XOFF flow control scheme is used to prevent data loss due to buffer overrun. When the data arrives rapidly, the ASCII control character DC3 (stop) is sent to stop the flow of data. Data flow is resumed by sending the ASCII control character DC1 (start). The host should also support the same flow control scheme.



### 18.3.5 UART ISP command abort

Commands can be aborted by sending the ASCII control character "ESC". This feature is not documented as a command under "ISP Commands" section. Once the escape code is received the ISP command handler waits for a new command.

### 18.3.6 Interrupts during UART ISP

The boot block interrupt vectors located in the boot block of the flash are active after any reset.

### 18.3.7 Interrupts during IAP

The on-chip flash memory is not accessible during erase/write operations. When the user application code starts executing the interrupt vectors from the user flash area are active. Before making any IAP call, either disable the interrupts or ensure that the user interrupt vectors are active in RAM and that the interrupt handlers reside in RAM. The IAP code does not use or disable interrupts.

### 18.3.8 RAM used by ISP command handler (for LPC11Cxx parts)

ISP commands use on-chip RAM from 0x1000 017C to 0x1000 025B. The user could use this area, but the contents may be lost upon reset. Flash programming commands use the top 32 bytes of on-chip RAM. The stack is located at (RAM top – 32). The maximum stack usage is 256 bytes and it grows downwards.

### 18.3.9 RAM used by ISP command handler (for LPC111x parts)

ISP commands use on-chip RAM from 0x1000 0050 to 0x1000 017F. The user could use this area, but the contents may be lost upon reset. Flash programming commands use the top 32 bytes of on-chip RAM. The stack is located at (RAM top – 32). The maximum stack usage is 256 bytes and it grows downwards.

### 18.3.10 RAM used by IAP command handler

Flash programming commands use the top 32 bytes of on-chip RAM. The maximum stack usage in the user allocated stack space is 128 bytes and it grows downwards.

## 18.4 API description (ISP commands)

---

The following commands are accepted by the ISP command handler. Detailed status codes are supported for each command. The command handler sends the return code `INVALID_COMMAND` when an undefined command is received. Commands and return codes are in ASCII format.

`CMD_SUCCESS` is sent by ISP command handler only when received ISP command has been completely executed and the new ISP command can be given by the host. Exceptions from this rule are "Set Baud Rate", "Write to RAM", "Read Memory", and "Go" commands.

Table 265. UART ISP command summary

ISP Command	Usage	Described in
Unlock	U <Unlock Code>	<a href="#">Table 266</a>
Set Baud Rate	B <Baud Rate> <stop bit>	<a href="#">Table 267</a>
Echo	A <setting>	<a href="#">Table 268</a>
Write to RAM	W <start address> <number of bytes>	<a href="#">Table 269</a>
Read Memory	R <address> <number of bytes>	<a href="#">Table 270</a>
Prepare sector(s) for write operation	P <start sector number> <end sector number>	<a href="#">Table 271</a>
Copy RAM to flash	C <Flash address> <RAM address> <number of bytes>	<a href="#">Table 272</a>
Go	G <address> <Mode>	<a href="#">Table 273</a>
Erase sector(s)	E <start sector number> <end sector number>	<a href="#">Table 274</a>
Blank check sector(s)	I <start sector number> <end sector number>	<a href="#">Table 275</a>
Read Part ID	J	<a href="#">Table 276</a>
Read Boot code version	K	<a href="#">Table 278</a>
Compare	M <address1> <address2> <number of bytes>	<a href="#">Table 279</a>
ReadUID	N	<a href="#">Table 280</a>

### 18.4.1 Unlock <Unlock code> (UART ISP)

Table 266. UART ISP Unlock command

Command	U
Input	Unlock code: 23130 <sub>10</sub>
Return Code	CMD_SUCCESS   INVALID_CODE   PARAM_ERROR
Description	This command is used to unlock Flash Write, Erase, and Go commands.
Example	"U 23130<CR><LF>" unlocks the Flash Write/Erase & Go commands.

### 18.4.2 Set Baud Rate <Baud Rate> <stop bit> (UART ISP)

Table 267. UART ISP Set Baud Rate command

Command	B
Input	Baud Rate: 9600   19200   38400   57600   115200 Stop bit: 1   2
Return Code	CMD_SUCCESS   INVALID_BAUD_RATE   INVALID_STOP_BIT   PARAM_ERROR
Description	This command is used to change the baud rate. The new baud rate is effective after the command handler sends the CMD_SUCCESS return code.
Example	"B 57600 1<CR><LF>" sets the serial port to baud rate 57600 bps and 1 stop bit.

### 18.4.3 Echo <setting> (UART ISP)

Table 268. UART ISP Echo command

Command	A
Input	Setting: ON = 1   OFF = 0
Return Code	CMD_SUCCESS   PARAM_ERROR
Description	The default setting for echo command is ON. When ON the ISP command handler sends the received serial data back to the host.
Example	"A 0<CR><LF>" turns echo off.

### 18.4.4 Write to RAM <start address> <number of bytes> (UART ISP)

The host should send the data only after receiving the CMD\_SUCCESS return code. The host should send the check-sum after transmitting 20 UU-encoded lines. The checksum is generated by adding raw data (before UU-encoding) bytes and is reset after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. When the data fits in less than 20 UU-encoded lines then the check-sum should be of the actual number of bytes sent. The ISP command handler compares it with the check-sum of the received bytes. If the check-sum matches, the ISP command handler responds with "OK<CR><LF>" to continue further transmission. If the check-sum does not match, the ISP command handler responds with "RESEND<CR><LF>". In response the host should retransmit the bytes.

Table 269. UART ISP Write to RAM command

Command	W
Input	<b>Start Address:</b> RAM address where data bytes are to be written. This address should be a word boundary. <b>Number of Bytes:</b> Number of bytes to be written. Count should be a multiple of 4
Return Code	CMD_SUCCESS   ADDR_ERROR (Address not on word boundary)   ADDR_NOT_MAPPED   COUNT_ERROR (Byte count is not multiple of 4)   PARAM_ERROR   CODE_READ_PROTECTION_ENABLED
Description	This command is used to download data to RAM. Data should be in UU-encoded format. This command is blocked when code read protection is enabled.
Example	"W 268436224 4<CR><LF>" writes 4 bytes of data to address 0x1000 0300.

### 18.4.5 Read Memory <address> <no. of bytes> (UART ISP)

The data stream is followed by the command success return code. The check-sum is sent after transmitting 20 UU-encoded lines. The checksum is generated by adding raw data (before UU-encoding) bytes and is reset after transmitting 20 UU-encoded lines. The length of any UU-encoded line should not exceed 61 characters (bytes) i.e. it can hold 45 data bytes. When the data fits in less than 20 UU-encoded lines then the check-sum is of actual number of bytes sent. The host should compare it with the checksum of the received bytes. If the check-sum matches then the host should respond with

"OK<CR><LF>" to continue further transmission. If the check-sum does not match then the host should respond with "RESEND<CR><LF>". In response the ISP command handler sends the data again.

**Table 270. UART ISP Read Memory command**

Command	R
Input	<b>Start Address:</b> Address from where data bytes are to be read. This address should be a word boundary. <b>Number of Bytes:</b> Number of bytes to be read. Count should be a multiple of 4.
Return Code	CMD_SUCCESS followed by <actual data (UU-encoded)>   ADDR_ERROR (Address not on word boundary)   ADDR_NOT_MAPPED   COUNT_ERROR (Byte count is not a multiple of 4)   PARAM_ERROR   CODE_READ_PROTECTION_ENABLED
Description	This command is used to read data from RAM or flash memory. This command is blocked when code read protection is enabled.
Example	"R 268435456 4<CR><LF>" reads 4 bytes of data from address 0x1000 0000.

#### 18.4.6 Prepare sector(s) for write operation <start sector number> <end sector number> (UART ISP)

This command makes flash write/erase operation a two step process.

**Table 271. UART ISP Prepare sector(s) for write operation command**

Command	P
Input	<b>Start Sector Number</b> <b>End Sector Number:</b> Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS   BUSY   INVALID_SECTOR   PARAM_ERROR
Description	This command must be executed before executing "Copy RAM to flash" or "Erase Sector(s)" command. Successful execution of the "Copy RAM to flash" or "Erase Sector(s)" command causes relevant sectors to be protected again. The boot block can not be prepared by this command. To prepare a single sector use the same "Start" and "End" sector numbers.
Example	"P 0 0<CR><LF>" prepares the flash sector 0.

#### 18.4.7 Copy RAM to flash <Flash address> <RAM address> <no of bytes> (UART ISP)

When writing to the flash, the following limitations apply:

1. The smallest amount of data that can be written to flash by the copy RAM to flash command is 256 byte (equal to one page).
2. One page consists of 16 flash words (lines), and the smallest amount that can be modified per flash write is one flash word (one line). This limitation follows from the application of ECC to the flash write operation, see [Section 18.2.6](#).

3. To avoid write disturbance (a mechanism intrinsic to flash memories), an erase should be performed after following 16 consecutive writes inside the same page. Note that the erase operation then erases the entire sector.

**Remark:** Once a page has been written to 16 times, it is still possible to write to other pages within the same sector without performing a sector erase (assuming that those pages have been erased previously).

**Table 272. UART ISP Copy RAM to flash command**

Command	C
Input	<b>Flash Address (DST):</b> Destination flash address where data bytes are to be written. The destination address should be a 256 byte boundary. <b>RAM Address (SRC):</b> Source RAM address from where data bytes are to be read. <b>Number of Bytes:</b> Number of bytes to be written. Should be 256   512   1024   4096. <b>Remark:</b> In parts with less than 4 kB SRAM, the number of bytes is limited to 1024.
Return Code	CMD_SUCCESS   SRC_ADDR_ERROR (Address not on word boundary)   DST_ADDR_ERROR (Address not on correct boundary)   SRC_ADDR_NOT_MAPPED   DST_ADDR_NOT_MAPPED   COUNT_ERROR (Byte count is not 256   512   1024   4096)   SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION   BUSY   CMD_LOCKED   PARAM_ERROR   CODE_READ_PROTECTION_ENABLED
Description	This command is used to program the flash memory. The "Prepare Sector(s) for Write Operation" command should precede this command. The affected sectors are automatically protected again once the copy command is successfully executed. The boot block cannot be written by this command. This command is blocked when code read protection is enabled.
Example	"C 0 268467504 512<CR><LF>" copies 512 bytes from the RAM address 0x1000 0800 to the flash address 0.

### 18.4.8 Go <address> <mode> (UART ISP)

Table 273. UART ISP Go command

Command	G
Input	<b>Address:</b> Flash or RAM address from which the code execution is to be started. This address should be on a word boundary. <b>Mode:</b> T (Execute program in Thumb Mode).
Return Code	CMD_SUCCESS   ADDR_ERROR   ADDR_NOT_MAPPED   CMD_LOCKED   PARAM_ERROR   CODE_READ_PROTECTION_ENABLED
Description	This command is used to execute a program residing in RAM or flash memory. It may not be possible to return to the ISP command handler once this command is successfully executed. This command is blocked when code read protection is enabled. The command must be used with an address of 0x0000 0200 or greater.
Example	"G 512 T<CR><LF>" branches to address 0x0000 0200 in Thumb mode.

### 18.4.9 Erase sector(s) <start sector number> <end sector number> (UART ISP)

Table 274. UART ISP Erase sector command

Command	E
Input	<b>Start Sector Number</b> <b>End Sector Number:</b> Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS   BUSY   INVALID_SECTOR   SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION   CMD_LOCKED   PARAM_ERROR   CODE_READ_PROTECTION_ENABLED
Description	This command is used to erase one or more sector(s) of on-chip flash memory. The boot block can not be erased using this command. This command only allows erasure of all user sectors when the code read protection is enabled.
Example	"E 2 3<CR><LF>" erases the flash sectors 2 and 3.

### 18.4.10 Blank check sector(s) <sector number> <end sector number> (UART ISP)

Table 275. UART ISP Blank check sector command

Command	I
Input	<b>Start Sector Number:</b> <b>End Sector Number:</b> Should be greater than or equal to start sector number.
Return Code	CMD_SUCCESS   SECTOR_NOT_BLANK (followed by <Offset of the first non blank word location> <Contents of non blank word location>)   INVALID_SECTOR   PARAM_ERROR
Description	This command is used to blank check one or more sectors of on-chip flash memory. Blank check on sector 0 always fails as first 64 bytes are re-mapped to flash boot block.  When CRP is enabled, the blank check command returns 0 for the offset and value of sectors which are not blank. Blank sectors are correctly reported irrespective of the CRP setting.
Example	"I 2 3<CR><LF>" blank checks the flash sectors 2 and 3.

### 18.4.11 Read Part Identification number (UART ISP)

Table 276. UART ISP Read Part Identification command

Command	J
Input	None.
Return Code	CMD_SUCCESS followed by part identification number in ASCII (see <a href="#">Table 277</a> ).
Description	This command is used to read the part identification number.

Table 277. Part identification numbers

Device	Hex coding
LPC1125	0x00150080
LPC1124	0x00140040

### 18.4.12 Read Boot code version number (UART ISP)

Table 278. UART ISP Read Boot Code version number command

Command	K
Input	None
Return Code	CMD_SUCCESS followed by 2 bytes of boot code version number in ASCII format. It is to be interpreted as <byte1(Major)>.<byte0(Minor)>.
Description	This command is used to read the boot code version number.

### 18.4.13 Compare <address1> <address2> <no of bytes> (UART ISP)

Table 279. UART ISP Compare command

Command	M
Input	<b>Address1 (DST):</b> Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. <b>Address2 (SRC):</b> Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. <b>Number of Bytes:</b> Number of bytes to be compared; should be a multiple of 4.
Return Code	CMD_SUCCESS   (Source and destination data are equal) COMPARE_ERROR   (Followed by the offset of first mismatch) COUNT_ERROR (Byte count is not a multiple of 4)   ADDR_ERROR   ADDR_NOT_MAPPED   PARAM_ERROR
Description	This command is used to compare the memory contents at two locations. Compare result may not be correct when source or destination address contains any of the first 512 bytes starting from address zero. First 512 bytes are re-mapped to boot ROM
Example	"M 8192 268468224 4<CR><LF>" compares 4 bytes from the RAM address 0x1000 8000 to the 4 bytes from the flash address 0x2000.

### 18.4.14 ReadUID (UART ISP)

Table 280. UART ISP ReadUID command

Command	N
Input	None
Return Code	CMD_SUCCESS followed by four 32-bit words of E-sort test information in ASCII format. The word sent at the lowest address is sent first.
Description	This command is used to read the unique ID.

### 18.4.15 UART ISP Return Codes

Table 281. UART ISP Return Codes Summary

Return Code	Mnemonic	Description
0	CMD_SUCCESS	Command is executed successfully. Sent by ISP handler only when command given by the host has been completely and successfully executed.
1	INVALID_COMMAND	Invalid command.
2	SRC_ADDR_ERROR	Source address is not on word boundary.
3	DST_ADDR_ERROR	Destination address is not on a correct boundary.
4	SRC_ADDR_NOT_MAPPED	Source address is not mapped in the memory map. Count value is taken in to consideration where applicable.
5	DST_ADDR_NOT_MAPPED	Destination address is not mapped in the memory map. Count value is taken in to consideration where applicable.



Table 281. UART ISP Return Codes Summary

Return Code	Mnemonic	Description
6	COUNT_ERROR	Byte count is not multiple of 4 or is not a permitted value.
7	INVALID_SECTOR	Sector number is invalid or end sector number is greater than start sector number.
8	SECTOR_NOT_BLANK	Sector is not blank.
9	SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION	Command to prepare sector for write operation was not executed.
10	COMPARE_ERROR	Source and destination data not equal.
11	BUSY	Flash programming hardware interface is busy.
12	PARAM_ERROR	Insufficient number of parameters or invalid parameter.
13	ADDR_ERROR	Address is not on word boundary.
14	ADDR_NOT_MAPPED	Address is not mapped in the memory map. Count value is taken in to consideration where applicable.
15	CMD_LOCKED	Command is locked.
16	INVALID_CODE	Unlock code is invalid.
17	INVALID_BAUD_RATE	Invalid baud rate setting.
18	INVALID_STOP_BIT	Invalid stop bit setting.
19	CODE_READ_PROTECTION_ENABLED	Code read protection enabled.

## 18.5 API description (IAP commands)

For in application programming the IAP routine should be called with a word pointer in register r0 pointing to memory (RAM) containing command code and parameters. Result of the IAP command is returned in the result table pointed to by register r1. The user can reuse the command table for result by passing the same pointer in registers r0 and r1. The parameter table should be big enough to hold all the results in case the number of results are more than number of parameters. Parameter passing is illustrated in the [Figure 54](#). The number of parameters and results vary according to the IAP command. The maximum number of parameters is 5, passed to the "Copy RAM to FLASH" command. The maximum number of results is 4, returned by the "ReadUID" command. The command handler sends the status code INVALID\_COMMAND when an undefined command is received. The IAP routine resides at 0x1FFF 1FF0 location and it is thumb code.

The IAP function could be called in the following way using C:

Define the IAP location entry point. Since the 0th bit of the IAP location is set there will be a change to Thumb instruction set when the program counter branches to this address.

```
#define IAP_LOCATION 0x1fff1ff1
```

Define data structure or pointers to pass IAP command table and result table to the IAP function:

```
unsigned int command_param[5];
```

```
unsigned int status_result[4];
```

or

```
unsigned int * command_param;
unsigned int * status_result;
command_param = (unsigned int *) 0x...
status_result =(unsigned int *) 0x...
```

Define pointer to function type, which takes two parameters and returns void. Note the IAP returns the result with the base address of the table residing in R1.

```
typedef void (*IAP)(unsigned int [],unsigned int[]);
IAP iap_entry;
```

Setting the function pointer:

```
iap_entry=(IAP) IAP_LOCATION;
```

To call the IAP, use the following statement.

```
iap_entry (command_param,status_result);
```

As per the ARM specification (The ARM Thumb Procedure Call Standard SWS ESPC 0002 A-05) up to 4 parameters can be passed in the r0, r1, r2 and r3 registers respectively. Additional parameters are passed on the stack. Up to 4 parameters can be returned in the r0, r1, r2 and r3 registers respectively. Additional parameters are returned indirectly via memory. Some of the IAP calls require more than 4 parameters. If the ARM suggested scheme is used for the parameter passing/returning then it might create problems due to difference in the C compiler implementation from different vendors. The suggested parameter passing scheme reduces such risk.

The flash memory is not accessible during a write or erase operation. IAP commands, which results in a flash write/erase operation, use 32 bytes of space in the top portion of the on-chip RAM for execution. The user program should not be use this space if IAP flash programming is permitted in the application.

**Table 282. IAP Command Summary**

IAP Command	Command Code	Described in
Prepare sector(s) for write operation	50 (decimal)	<a href="#">Table 283</a>
Copy RAM to flash	51 (decimal)	<a href="#">Table 284</a>
Erase sector(s)	52 (decimal)	<a href="#">Table 285</a>
Blank check sector(s)	53 (decimal)	<a href="#">Table 286</a>
Read Part ID	54 (decimal)	<a href="#">Table 287</a>
Read Boot code version	55 (decimal)	<a href="#">Table 288</a>
Compare	56 (decimal)	<a href="#">Table 289</a>
Reinvoke ISP	57 (decimal)	<a href="#">Table 290</a>
Read UID	58 (decimal)	<a href="#">Table 291</a>
Erase page	59 (decimal)	<a href="#">Table 292</a>

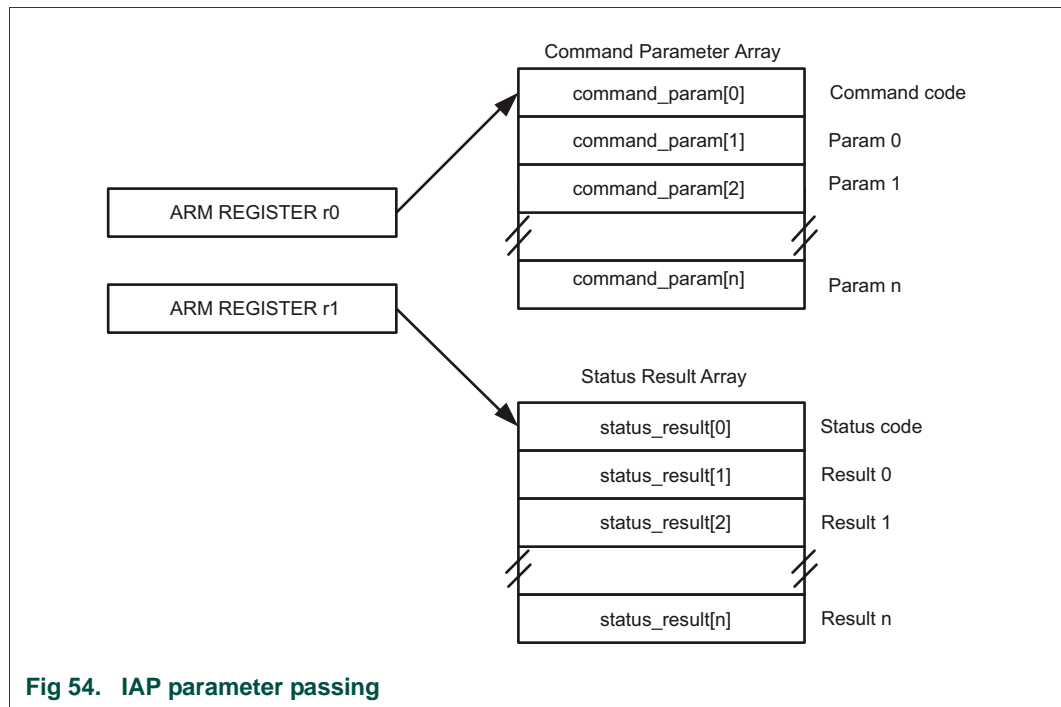


Fig 54. IAP parameter passing

### 18.5.1 Prepare sector(s) for write operation (IAP)

This command makes flash write/erase operation a two step process.

Table 283. IAP Prepare sector(s) for write operation command

Command	Prepare sector(s) for write operation
Input	<b>Command code:</b> 50 (decimal) <b>Param0:</b> Start Sector Number <b>Param1:</b> End Sector Number (should be greater than or equal to start sector number).
Status code	CMD_SUCCESS   BUSY   INVALID_SECTOR
Result	None
Description	This command must be executed before executing "Copy RAM to flash" or "Erase Sector(s)" command. Successful execution of the "Copy RAM to flash" or "Erase Sector(s)" command causes relevant sectors to be protected again. The boot sector can not be prepared by this command. To prepare a single sector use the same "Start" and "End" sector numbers.

### 18.5.2 Copy RAM to flash (IAP)

See [Section 18.4.4](#) for limitations on the write-to-flash process.

Table 284. IAP Copy RAM to flash command

Command	Copy RAM to flash
Input	<p><b>Command code:</b> 51 (decimal)</p> <p><b>Param0(DST):</b> Destination flash address where data bytes are to be written. This address should be a 256 byte boundary.</p> <p><b>Param1(SRC):</b> Source RAM address from which data bytes are to be read. This address should be a word boundary.</p> <p><b>Param2:</b> Number of bytes to be written. Should be 256   512   1024   4096.</p> <p><b>Param3:</b> System Clock Frequency (CCLK) in kHz.</p> <p><b>Remark:</b> In parts with less than 4 kB SRAM, Param2 is limited to 1024.</p>
Status code	CMD_SUCCESS   SRC_ADDR_ERROR (Address not a word boundary)   DST_ADDR_ERROR (Address not on correct boundary)   SRC_ADDR_NOT_MAPPED   DST_ADDR_NOT_MAPPED   COUNT_ERROR (Byte count is not 256   512   1024   4096)   SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION   BUSY
Result	None
Description	This command is used to program the flash memory. The affected sectors should be prepared first by calling "Prepare Sector for Write Operation" command. The affected sectors are automatically protected again once the copy command is successfully executed. The boot sector can not be written by this command.

### 18.5.3 Erase Sector(s) (IAP)

Table 285. IAP Erase Sector(s) command

Command	Erase Sector(s)
Input	<p><b>Command code:</b> 52 (decimal)</p> <p><b>Param0:</b> Start Sector Number</p> <p><b>Param1:</b> End Sector Number (should be greater than or equal to start sector number).</p> <p><b>Param2:</b> System Clock Frequency (CCLK) in kHz.</p>
Status code	CMD_SUCCESS   BUSY   SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION   INVALID_SECTOR
Result	None
Description	This command is used to erase a sector or multiple sectors of on-chip flash memory. The boot sector can not be erased by this command. To erase a single sector use the same "Start" and "End" sector numbers.

### 18.5.4 Blank check sector(s) (IAP)

Table 286. IAP Blank check sector(s) command

Command	Blank check sector(s)
Input	<b>Command code: 53</b> (decimal) <b>Param0:</b> Start Sector Number <b>Param1:</b> End Sector Number (should be greater than or equal to start sector number).
Status code	CMD_SUCCESS   BUSY   SECTOR_NOT_BLANK   INVALID_SECTOR
Result	<b>Result0:</b> Offset of the first non blank word location if the Status Code is SECTOR_NOT_BLANK. <b>Result1:</b> Contents of non blank word location.
Description	This command is used to blank check a sector or multiple sectors of on-chip flash memory. To blank check a single sector use the same "Start" and "End" sector numbers.

### 18.5.5 Read Part Identification number (IAP)

Table 287. IAP Read Part Identification command

Command	Read part identification number
Input	<b>Command code: 54</b> (decimal) <b>Parameters:</b> None
Status code	CMD_SUCCESS
Result	<b>Result0:</b> Part Identification Number.
Description	This command is used to read the part identification number.

### 18.5.6 Read Boot code version number (IAP)

Table 288. IAP Read Boot Code version number command

Command	Read boot code version number
Input	<b>Command code: 55</b> (decimal) <b>Parameters:</b> None
Status code	CMD_SUCCESS
Result	<b>Result0:</b> 2 bytes of boot code version number. Read as <byte1(Major)>.<byte0(Minor)>
Description	This command is used to read the boot code version number.

### 18.5.7 Compare <address1> <address2> <no of bytes> (IAP)

Table 289. IAP Compare command

Command	Compare
Input	<b>Command code:</b> 56 <sub>(decimal)</sub> <b>Param0(DST):</b> Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. <b>Param1(SRC):</b> Starting flash or RAM address of data bytes to be compared. This address should be a word boundary. <b>Param2:</b> Number of bytes to be compared; should be a multiple of 4.
Status code	CMD_SUCCESS   COMPARE_ERROR   COUNT_ERROR (Byte count is not a multiple of 4)   ADDR_ERROR   ADDR_NOT_MAPPED
Result	<b>Result0:</b> Offset of the first mismatch if the Status Code is COMPARE_ERROR.
Description	This command is used to compare the memory contents at two locations. <b>The result may not be correct when the source or destination includes any of the first 512 bytes starting from address zero. The first 512 bytes can be re-mapped to RAM.</b>

### 18.5.8 Reinvoke ISP (IAP)

Table 290. IAP Reinvoke ISP

Command	Compare
Input	<b>Command code: 57</b> (decimal)
Status code	None
Result	None.
Description	This command is used to invoke the boot loader in ISP mode. It maps boot vectors, sets PCLK = CCLK, configures UART pins U0_RXD and U0_TXD, resets counter/timer CT32B1 and resets the FDR. This command may be used when a valid user program is present in the internal flash memory and the PIO0_1 pin is not accessible to force the ISP mode.

### 18.5.9 ReadUID (IAP)

Table 291. IAP ReadUID command

Command	Compare
Input	<b>Command code: 58</b> (decimal)
Status code	CMD_SUCCESS
Result	<b>Result0:</b> The first 32-bit word (at the lowest address). <b>Result1:</b> The second 32-bit word. <b>Result2:</b> The third 32-bit word. <b>Result3:</b> The fourth 32-bit word.
Description	This command is used to read the unique ID.

### 18.5.10 Erase page

Table 292. IAP Erase page command

Command	Erase page
Input	<b>Command code: 59</b> (decimal) <b>Param0:</b> Start page number. <b>Param1:</b> End page number (should be greater than or equal to start page) <b>Param2:</b> System Clock Frequency (CCLK) in kHz.
Return Code	CMD_SUCCESS   BUSY   SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION   INVALID_SECTOR
Result	None
Description	This command is used to erase a page or multiple pages of on-chip flash memory. To erase a single page use the same "start" and "end" page numbers.

### 18.5.11 IAP Status Codes

Table 293. IAP Status Codes Summary

Status code	Mnemonic	Description
0	CMD_SUCCESS	Command is executed successfully.
1	INVALID_COMMAND	Invalid command.
2	SRC_ADDR_ERROR	Source address is not on a word boundary.
3	DST_ADDR_ERROR	Destination address is not on a correct boundary.
4	SRC_ADDR_NOT_MAPPED	Source address is not mapped in the memory map. Count value is taken in to consideration where applicable.
5	DST_ADDR_NOT_MAPPED	Destination address is not mapped in the memory map. Count value is taken in to consideration where applicable.
6	COUNT_ERROR	Byte count is not multiple of 4 or is not a permitted value.
7	INVALID_SECTOR	Sector number is invalid.
8	SECTOR_NOT_BLANK	Sector is not blank.
9	SECTOR_NOT_PREPARED_FOR_WRITE_OPERATION	Command to prepare sector for write operation was not executed.
10	COMPARE_ERROR	Source and destination data is not same.
11	BUSY	Flash programming hardware interface is busy.



### 19.1 How to read this chapter

---

The power profiles are available for the part LPC1125.

### 19.2 Basic configuration

---

Specific power profile settings are required in the following situation: When using IAP commands, configure the power profiles in Default mode.

Disable all interrupts before making calls to the power profile API. You can re-enable the interrupts after the power profile API calls have completed.

### 19.3 Features

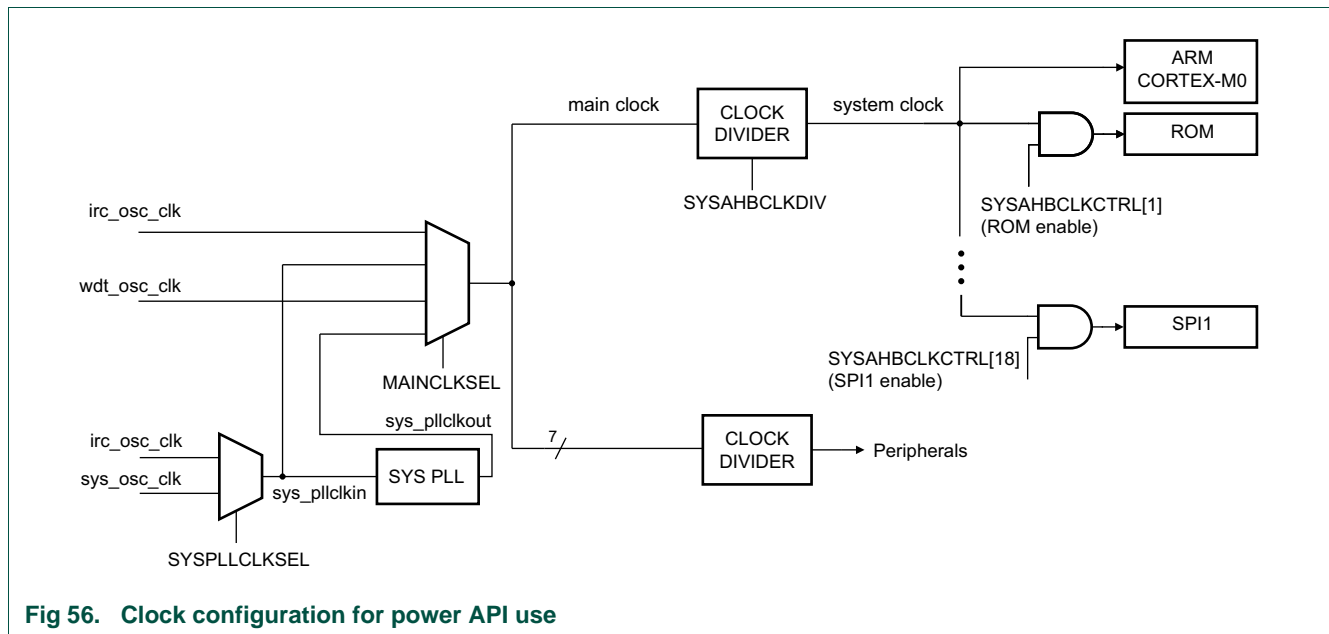
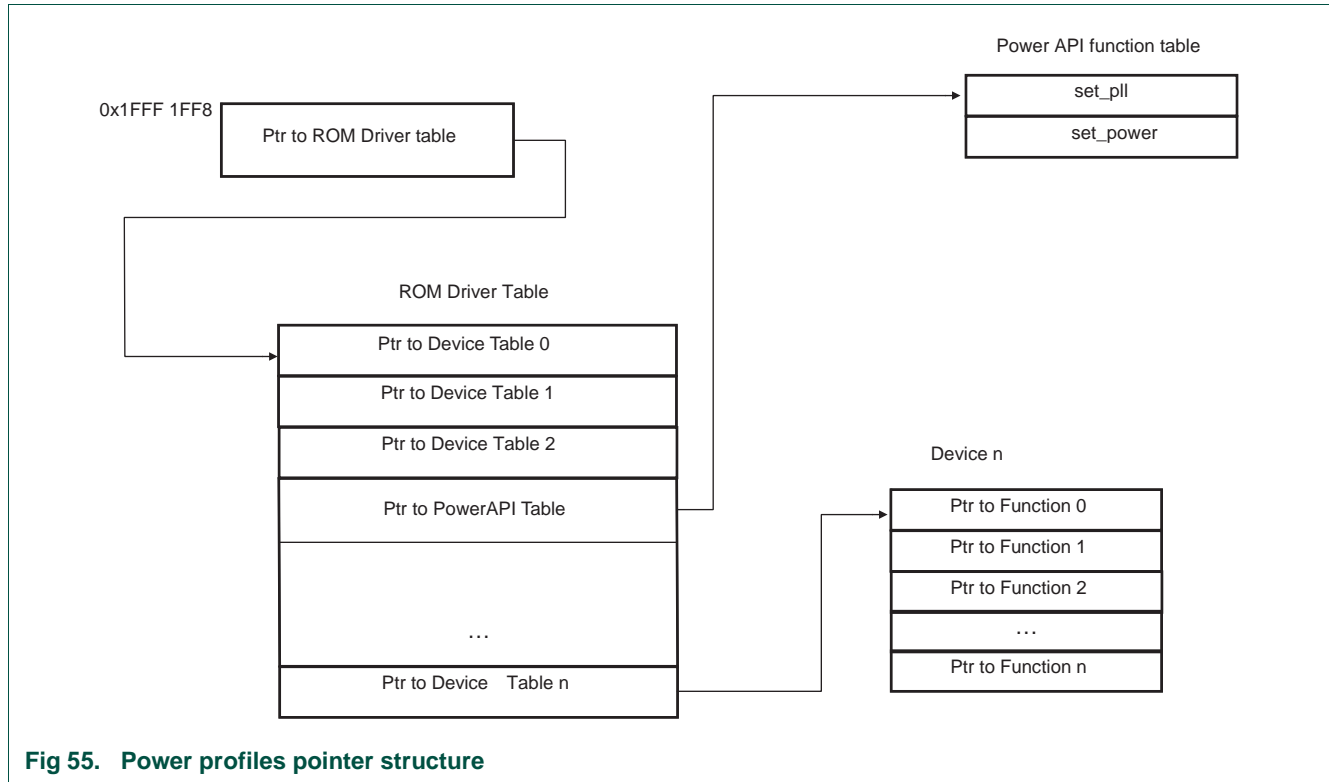
---

- ROM-based application for power and clocking management.
- Four power modes: Default, performance, efficiency, low-current.

### 19.4 Description

---

The API calls to the ROM are performed by executing functions which are pointed by a pointer within the ROM Driver Table. [Figure 55](#) shows the pointer structure used to call the Power Profiles API.



## 19.5 Definitions

The following elements have to be defined in an application that uses the power profiles:

```
typedef struct _PWRD {
    void (*set_pll)(unsigned int cmd[], unsigned int resp[]);
```

```

        void (*set_power)(unsigned int cmd[], unsigned int resp[]);
    } PWRD;
    typedef struct _ROM {
        const PWRD * pWRD;
    } ROM;
    ROM ** rom = (ROM **) (0xFFFF1FF8 + 3 * sizeof(ROM**));
    unsigned int command[4], result[2];
    // Power API (power profiles) struct definition
    typedef const struct _PWRD {
        void (*set_pll)(unsigned int cmd[], unsigned int resp[]);
        void (*set_power)(unsigned int cmd[], unsigned int resp[]);
    } PWRD;
    typedef struct _ROM {
        uint32_t *devTbl0;
        uint32_t *devTbl1;
        uint32_t *devTbl2;
        const PWRD * pWRD;
    } ROM;

```

## 19.6 Clocking routine

### 19.6.1 set\_pll

This routine sets up the system PLL according to the calling arguments. If the expected clock can be obtained by simply dividing the system PLL input, set\_pll bypasses the PLL to lower system power consumption.

**Remark:** Before this routine is invoked, the PLL clock source (IRC/system oscillator) must be selected ([Table 14](#)), the main clock source must be set to the input clock to the system PLL ([Table 16](#)) and the system/AHB clock divider must be set to 1 ([Table 18](#)).

set\_pll attempts to find a PLL setup that matches the calling parameters. Once a combination of a feedback divider value (SYSPLLCTRL, M), a post divider ratio (SYSPLLCTRL, P) and the system/AHB clock divider (SYSAHBCLKDIV) is found, set\_pll applies the selected values and switches the main clock source selection to the system PLL clock out (if necessary).

The routine returns a result code that indicates if the system PLL was successfully set (PLL\_CMD\_SUCCESS) or not (in which case the result code identifies what went wrong). The current system frequency value is also returned. The application should use this information to adjust other clocks in the device (the SSP, UART, and WDT clocks, and/or CLOCKOUT).

Table 294. set\_pll routine

Routine	set_pll
Input	<b>Param0:</b> system PLL input frequency (in kHz) <b>Param1:</b> expected system clock (in kHz) <b>Param2:</b> mode (CPU_FREQ_EQU, CPU_FREQ_LTE, CPU_FREQ_GTE, CPU_FREQ_APPROX) <b>Param3:</b> system PLL lock time-out
Result	<b>Result0:</b> PLL_CMD_SUCCESS   PLL_INVALID_FREQ   PLL_INVALID_MODE   PLL_FREQ_NOT_FOUND   PLL_NOT_LOCKED <b>Result1:</b> system clock (in kHz)

The following definitions are needed when making set\_pll power routine calls:

```

/* set_pll mode options */
#define CPU_FREQ_EQU      0
#define CPU_FREQ_LTE     1
#define CPU_FREQ_GTE     2
#define CPU_FREQ_APPROX  3
/* set_pll result0 options */
#define PLL_CMD_SUCCESS   0
#define PLL_INVALID_FREQ  1
#define PLL_INVALID_MODE  2
#define PLL_FREQ_NOT_FOUND 3
#define PLL_NOT_LOCKED   4

```

For a simplified clock configuration scheme see [Figure 56](#). For more details see [Figure 3](#).

#### 19.6.1.1 Param0: system PLL input frequency and Param1: expected system clock

set\_pll looks for a setup in which the system PLL clock does not exceed 50 MHz. It easily finds a solution when the ratio between the expected system clock and the system PLL input frequency is an integer value, but it can also find solutions in other cases.

The system PLL input frequency (Param0) must be between 10000 to 25000 kHz (10 MHz to 25 MHz) inclusive. The expected system clock (Param1) must be between 1 and 50000 kHz inclusive. If either of these requirements is not met, set\_pll returns PLL\_INVALID\_FREQ and returns Param0 as Result1 since the PLL setting is unchanged.

#### 19.6.1.2 Param2: mode

The first priority of set\_pll is to find a setup that generates the system clock at exactly the rate specified in Param1. If it is unlikely that an exact match can be found, input parameter mode (Param2) should be used to specify if the actual system clock can be less than or equal, greater than or equal or approximately the value specified as the expected system clock (Param1).

A call specifying CPU\_FREQ\_EQU will only succeed if the PLL can output exactly the frequency requested in Param1.

CPU\_FREQ\_LTE can be used if the requested frequency should not be exceeded (such as overall current consumption and/or power budget reasons).

CPU\_FREQ\_GTE helps applications that need a minimum level of CPU processing capabilities.

CPU\_FREQ\_APPROX results in a system clock that is as close as possible to the requested value (it may be greater than or less than the requested value).

If an illegal mode is specified, set\_pll returns PLL\_INVALID\_MODE. If the expected system clock is out of the range supported by this routine, set\_pll returns PLL\_FREQ\_NOT\_FOUND. In these cases the current PLL setting is not changed and Param0 is returned as Result1.

### 19.6.1.3 Param3: system PLL lock time-out

It should take no more than 100  $\mu$ s for the system PLL to lock if a valid configuration is selected. If Param3 is zero, set\_pll will wait indefinitely for the PLL to lock. A non-zero value indicates how many times the code will check for a successful PLL lock event before it returns PLL\_NOT\_LOCKED. In this case the PLL settings are unchanged and Param0 is returned as Result1.

**Remark:** The time it takes the PLL to lock depends on the selected PLL input clock source (IRC/system oscillator) and its characteristics. The selected source can experience more or less jitter depending on the operating conditions such as power supply and/or ambient temperature. This is why it is suggested that when a good known clock source is used and a PLL\_NOT\_LOCKED response is received, the set\_pll routine should be invoked several times before declaring the selected PLL clock source invalid.

Hint: setting Param3 equal to the system PLL frequency [Hz] divided by 10000 will provide more than enough PLL lock-polling cycles.

### 19.6.1.4 Code examples

The following examples illustrate some of the features of set\_pll discussed above.

#### 19.6.1.4.1 Invalid frequency (device maximum clock rate exceeded)

```
command[0] = 12000;  
command[1] = 60000;  
command[2] = CPU_FREQ_EQU;  
command[3] = 0;  
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock and a system clock of exactly 60 MHz. The application was ready to infinitely wait for the PLL to lock. But the expected system clock of 60 MHz exceeds the maximum of 50 MHz. Therefore set\_pll returns PLL\_INVALID\_FREQ in result[0] and 12000 in result[1] without changing the PLL settings.

#### 19.6.1.4.2 Invalid frequency selection (system clock divider restrictions)

```
command[0] = 12000;  
command[1] = 40;  
command[2] = CPU_FREQ_LTE;  
command[3] = 0;  
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock, a system clock of no more than 40 kHz and no time-out while waiting for the PLL to lock. Since the maximum divider value for the system clock is 255 and running at 40 kHz would need a divide by value of 300, `set_pll` returns `PLL_INVALID_FREQ` in `result[0]` and 12000 in `result[1]` without changing the PLL settings.

#### 19.6.1.4.3 Exact solution cannot be found (PLL)

```
command[0] = 12000;
command[1] = 25000;
command[2] = CPU_FREQ_EQU;
command[3] = 0;
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock and a system clock of exactly 25 MHz. The application was ready to infinitely wait for the PLL to lock. Since there is no valid PLL setup within earlier mentioned restrictions, `set_pll` returns `PLL_FREQ_NOT_FOUND` in `result[0]` and 12000 in `result[1]` without changing the PLL settings.

#### 19.6.1.4.4 System clock less than or equal to the expected value

```
command[0] = 12000;
command[1] = 25000;
command[2] = CPU_FREQ_LTE;
command[3] = 0;
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock, a system clock of no more than 25 MHz and no locking time-out. `set_pll` returns `PLL_CMD_SUCCESS` in `result[0]` and 24000 in `result[1]`. The new system clock is 24 MHz.

#### 19.6.1.4.5 System clock greater than or equal to the expected value

```
command[0] = 12000;
command[1] = 25000;
command[2] = CPU_FREQ_GTE;
command[3] = 0;
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock, a system clock of at least 25 MHz and no locking time-out. `set_pll` returns `PLL_CMD_SUCCESS` in `result[0]` and 36000 in `result[1]`. The new system clock is 36 MHz.

#### 19.6.1.4.6 System clock approximately equal to the expected value

```
command[0] = 12000;
command[1] = 16500;
command[2] = CPU_FREQ_APPROX;
command[3] = 0;
(*rom)->pWRD->set_pll(command, result);
```

The above code specifies a 12 MHz PLL input clock, a system clock of approximately 16.5 MHz and no locking time-out. `set_pll` returns `PLL_CMD_SUCCESS` in `result[0]` and 16000 in `result[1]`. The new system clock is 16 MHz.

## 19.7 Power routine

### 19.7.1 set\_power

This routine configures the device's internal power control settings according to the calling arguments. The goal is to reduce active power consumption while maintaining the feature of interest to the application close to its optimum.

**Remark:** The set\_power routine was designed for systems employing the configuration of SYSAHBCLKDIV = 1 (System clock divider register, see [Table 18](#) and [Figure 56](#)). Using this routine in an application with the system clock divider not equal to 1 might not improve microcontroller's performance as much as in setups when the main clock and the system clock are running at the same rate.

set\_power returns a result code that reports whether the power setting was successfully changed or not.

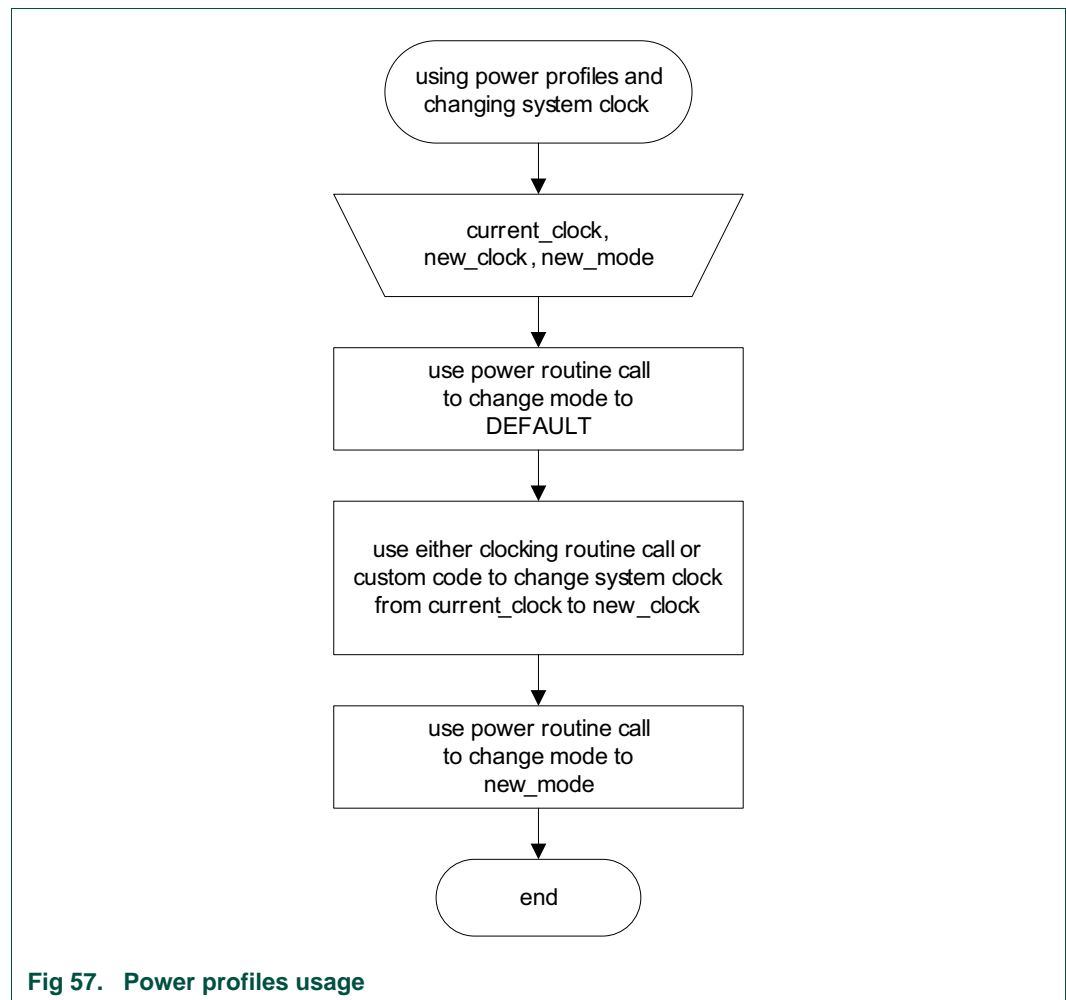


Table 295. set\_power routine

Routine	set_power
Input	<b>Param0:</b> main clock (in MHz) <b>Param1:</b> mode (PWR_DEFAULT, PWR_CPU_PERFORMANCE, PWR_EFFICIENCY, PWR_LOW_CURRENT) <b>Param2:</b> system clock (in MHz)
Result	<b>Result0:</b> PWR_CMD_SUCCESS   PWR_INVALID_FREQ   PWR_INVALID_MODE

The following definitions are needed for set\_power routine calls:

```

/* set_power mode options */
#define PWR_DEFAULT 0
#define PWR_CPU_PERFORMANCE 1
#define PWR_EFFICIENCY 2
#define PWR_LOW_CURRENT 3
/* set_power result0 options */
#define PWR_CMD_SUCCESS 0
#define PWR_INVALID_FREQ 1
#define PWR_INVALID_MODE 2

```

For a simplified clock configuration scheme see [Figure 56](#). For more details see [Figure 3](#).

#### 19.7.1.1 Param0: main clock

The main clock is the clock rate the microcontroller uses to source the system's and the peripherals' clock. It is configured by either a successful execution of the clocking routine call or a similar code provided by the user. This operand must be an integer between 1 to 50 MHz inclusive. If a value out of this range is supplied, set\_power returns PWR\_INVALID\_FREQ and does not change the power control system.

#### 19.7.1.2 Param1: mode

The input parameter mode (Param1) specifies one of four available power settings. If an illegal selection is provided, set\_power returns PWR\_INVALID\_MODE and does not change the power control system.

PWR\_DEFAULT keeps the device in a baseline power setting similar to its reset state.

PWR\_CPU\_PERFORMANCE configures the microcontroller so that it can provide more processing capability to the application. CPU performance is 30% better than the default option.

PWR\_EFFICIENCY setting was designed to find a balance between active current and the CPU's ability to execute code and process data. In this mode the device outperforms the default mode both in terms of providing higher CPU performance and lowering active current.

PWR\_LOW\_CURRENT is intended for those solutions that focus on lowering power consumption rather than CPU performance.

#### 19.7.1.3 Param2: system clock

The system clock is the clock rate at which the microcontroller core is running when set\_power is called. This parameter is an integer between from 1 and 50 MHz inclusive.



#### 19.7.1.4 Code examples

The following examples illustrate some of the set\_power features discussed above.

##### 19.7.1.4.1 Invalid frequency (device maximum clock rate exceeded)

```
command[0] = 60;  
command[1] = PWR_CPU_PERFORMANCE;  
command[2] = 60;  
(*rom)->pWRD->set_power(command, result);
```

The above setup would be used in a system running at the main and system clock of 60 MHz, with a need for maximum CPU processing power. Since the specified 60 MHz clock is above the 50 MHz maximum, set\_power returns PWR\_INVALID\_FREQ in result[0] without changing anything in the existing power setup.

##### 19.7.1.4.2 An applicable power setup

```
command[0] = 24;  
command[1] = PWR_CPU_EFFICIENCY;  
command[2] = 24;  
(*rom)->pWRD->set_power(command, result);
```

The above code specifies that an application is running at the main and system clock of 24 MHz with emphasis on efficiency. set\_power returns PWR\_CMD\_SUCCESS in result[0] after configuring the microcontroller's internal power control features.

## 20.1 Features

- Supports ARM Serial Wire Debug mode.
- Direct debug access to all memories, registers, and peripherals.
- No target resources are required for the debugging session.
- Four breakpoints.
- Two data watchpoints that can also be used as triggers.

## 20.2 General description

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported. The ARM Cortex-M0 is configured to support up to four breakpoints and two watchpoints.

Debugging uses the Serial Wire Debug mode.

## 20.3 Pin description

The tables below indicate the various pin functions related to debug. Some of these functions share pins with other functions which therefore may not be used at the same time.

**Table 296. Serial Wire Debug pin description**

Pin Name	Type	Description
SWCLK	Input	Serial Wire <b>Clock</b> . This pin is the clock for debug logic when in the Serial Wire Debug mode (SWCLK). This pin is pulled up internally.
SWDIO	Input / Output	<b>Serial wire debug data input/output</b> . The SWDIO pin is used by an external debug tool to communicate with and control the part. This pin is pulled up internally.

## 20.4 Debug notes

### 20.4.1 Debug limitations

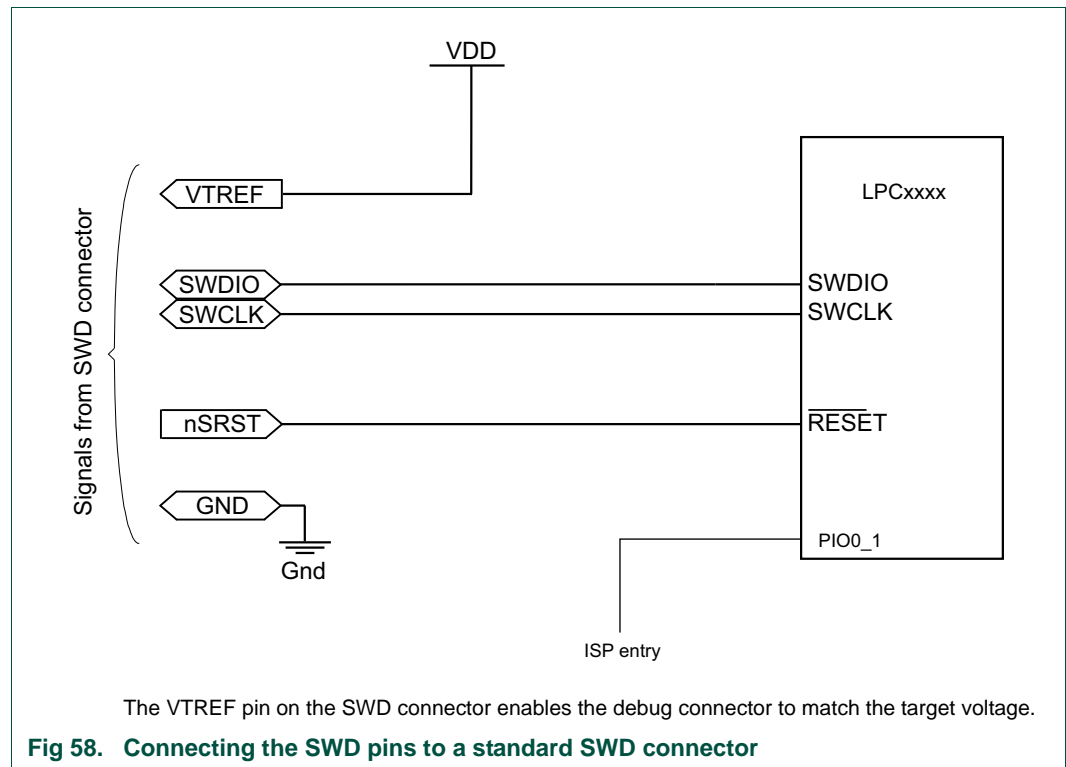
**Important:** The user should be aware of certain limitations during debugging. The most important is that, due to limitations of the ARM Cortex-M0 integration, the part cannot wake up in the usual manner from Deep-sleep mode. It is recommended not to use this mode during debug.

Another issue is that debug mode changes the way in which reduced power modes work internal to the ARM Cortex-M0 CPU, and this ripples through the entire system. These differences mean that power measurements should not be made while debugging, the results will be higher than during normal operation in an application.

During a debugging session, the System Tick Timer is automatically stopped whenever the CPU is stopped. Other peripherals are not affected.

### 20.4.2 Debug connections

For debugging purposes, it is useful to provide access to the ISP entry pin PIO0\_1. This pin can be used to recover the part from configurations which would disable the SWD port such as improper PLL configuration, reconfiguration of SWD pins as ADC inputs, entry into Deep power-down mode out of reset, etc. This pin can be used for other functions such as GPIO, but it should not be held low on power-up or reset.



### 21.1 Introduction

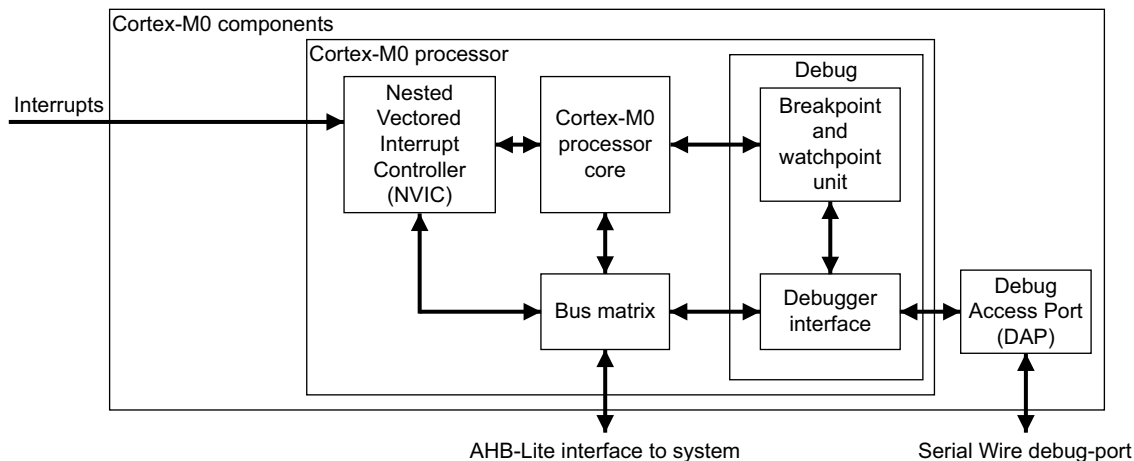
The following material is using the ARM *Cortex-M0 User Guide*. Minor changes have been made regarding the specific implementation of the Cortex-M0 for the LPC111x, LPC11D14, and LPC11Cxx parts.

The ARM Cortex-M0 documentation is also available in [Ref. 1](#) and [Ref. 2](#).

### 21.2 About the Cortex-M0 processor and core peripherals

The Cortex-M0 processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture that is easy to learn and program.
- Ultra-low power, energy efficient operation.
- Excellent code density.
- Deterministic, high-performance interrupt handling.
- Upward compatibility with Cortex-M processor family.



**Fig 59. Cortex-M0 implementation**

The Cortex-M0 processor is built on a highly area and power optimized 32-bit processor core, with a 3-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0 processor implements the ARMv6-M architecture, which is based on the 16-bit Thumb instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex-M0 processor closely integrates a configurable **Nested Vectored Interrupt Controller** (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- Includes a **non-maskable interrupt** (NMI).
- Provides zero jitter interrupt option.
- Provides four interrupt priority levels.

The tight integration of the processor core and NVIC provides fast execution of **interrupt service routines** (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a Deep-sleep function that enables the entire device to be rapidly powered down.

### 21.2.1 System-level interface

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

### 21.2.2 Integrated configurable debug

The Cortex-M0 processor implements a complete hardware debug solution, with extensive hardware breakpoint and watchpoint options. This provides high system visibility of the processor, memory and peripherals through a 2-pin **Serial Wire Debug** (SWD) port that is ideal for microcontrollers and other small package devices.

### 21.2.3 Cortex-M0 processor features summary

- High code density with 32-bit performance.
- Tools and binary upwards compatible with Cortex-M processor family.
- Integrated ultra low-power sleep modes.
- Efficient code execution permits slower processor clock or increases sleep mode time.
- Single-cycle 32-bit hardware multiplier.
- Zero jitter interrupt handling.
- Extensive debug capabilities.

### 21.2.4 Cortex-M0 core peripherals

These are:

**NVIC** — The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

**System Control Block** — The **System Control Block** (SCB) is the programmers model interface to the processor. It provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

**System timer** — The system timer, SysTick, is a 24-bit count-down timer. Use this as a Real Time Operating System (RTOS) tick timer or as a simple counter.

## 21.3 Processor

### 21.3.1 Programmers model

This section describes the Cortex-M0 programmers model. In addition to the individual core register descriptions, it contains information about the processor modes and stacks.

#### 21.3.1.1 Processor modes

The processor **modes** are:

**Thread mode** — Used to execute application software. The processor enters Thread mode when it comes out of reset.

**Handler mode** — Used to handle exceptions. The processor returns to Thread mode when it has finished all exception processing.

#### 21.3.1.2 Stacks

The processor uses a full descending stack. This means the stack pointer indicates the last stacked item on the stack memory. When the processor pushes a new item onto the stack, it decrements the stack pointer and then writes the item to the new memory location. The processor implements two stacks, the main stack and the process stack, with independent copies of the stack pointer, see [Section 21.3.1.3.2](#).

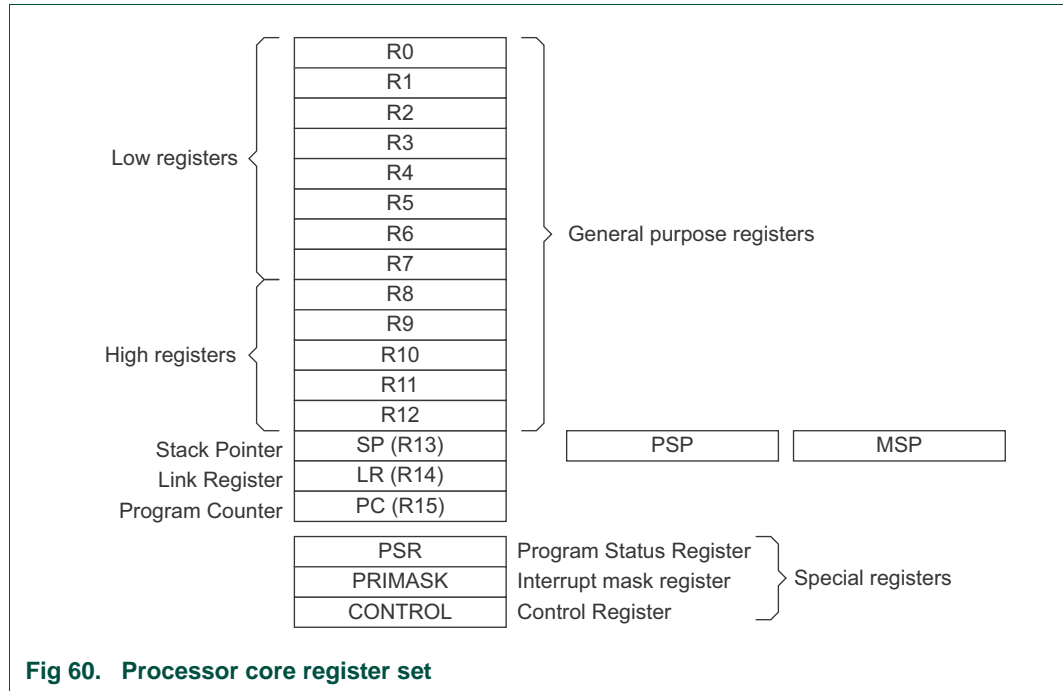
In Thread mode, the CONTROL register controls whether the processor uses the main stack or the process stack, see [Section 21–21.3.1.3.7](#). In Handler mode, the processor always uses the main stack. The options for processor operations are:

**Table 297. Summary of processor mode and stack use options**

Processor mode	Used to execute	Stack used
Thread	Applications	Main stack or process stack See <a href="#">Section 21–21.3.1.3.7</a>
Handler	Exception handlers	Main stack

#### 21.3.1.3 Core registers

The processor core registers are:



**Fig 60. Processor core register set**

**Table 298. Core register set summary**

Name	Type <sup>[1]</sup>	Reset value	Description
R0-R12	RW	Unknown	<a href="#">Section 21–21.3.1.3.1</a>
MSP	RW	See description	<a href="#">Section 21–21.3.1.3.2</a>
PSP	RW	Unknown	<a href="#">Section 21–21.3.1.3.2</a>
LR	RW	Unknown	<a href="#">Section 21–21.3.1.3.3</a>
PC	RW	See description	<a href="#">Section 21–21.3.1.3.4</a>
PSR	RW	Unknown <sup>[2]</sup>	<a href="#">Table 21–299</a>
APSR	RW	Unknown	<a href="#">Table 21–300</a>
IPSR	RO	0x00000000	<a href="#">Table 301</a>
EPSR	RO	Unknown <sup>[2]</sup>	<a href="#">Table 21–302</a>
PRIMASK	RW	0x00000000	<a href="#">Table 21–303</a>
CONTROL	RW	0x00000000	<a href="#">Table 21–304</a>

[1] Describes access type during program execution in thread mode and Handler mode. Debug access can differ.

[2] Bit[24] is the T-bit and is loaded from bit[0] of the reset vector.

### 21.3.1.3.1 General-purpose registers

R0-R12 are 32-bit general-purpose registers for data operations.

### 21.3.1.3.2 Stack Pointer

The Stack Pointer (SP) is register R13. In Thread mode, bit[1] of the CONTROL register indicates the stack pointer to use:

- 0 = **Main Stack Pointer** (MSP). This is the reset value.
- 1 = **Process Stack Pointer** (PSP).

On reset, the processor loads the MSP with the value from address 0x00000000.

### 21.3.1.3.3 Link Register

The **Link Register** (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions. On reset, the LR value is Unknown.

#### 21.3.1.3.4 Program Counter

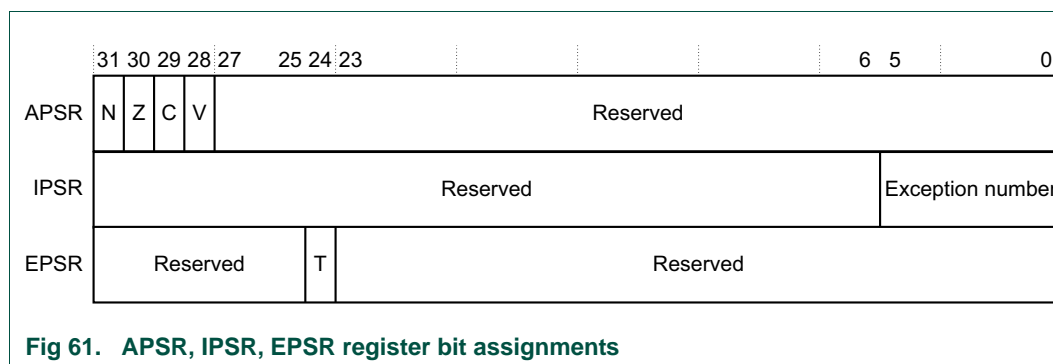
The **Program Counter** (PC) is register R15. It contains the current program address. On reset, the processor loads the PC with the value of the reset vector, which is at address 0x00000004. Bit[0] of the value is loaded into the EPSR T-bit at reset and must be 1.

### 21.3.1.3.5 Program Status Register

The **Program Status Register** (PSR) combines:

- **Application Program Status Register (APSR)**
- **Interrupt Program Status Register (IPSR)**
- **Execution Program Status Register (EPSR).**

These registers are mutually exclusive bitfields in the 32-bit PSR. The PSR bit assignments are:



Access these registers individually or as a combination of any two or all three registers, using the register name as an argument to the **MSR** or **MRS** instructions. For example:

- read all of the registers using `PSR` with the `MRS` instruction
- write to the `APSR` using `APSR` with the `MSR` instruction.

The PSR combinations and attributes are:

### Table 299. PSR register combinations

Register	Type	Combination
PSR	RW <sup>[1]</sup> <sup>[2]</sup>	APSR, EPSR, and IPSR
IEPSR	RO	EPSR and IPSR
IAPSR	RW <sup>[1]</sup>	APSR and IPSR
EAPSR	RW <sup>[2]</sup>	APSR and EPSR

[1] The processor ignores writes to the IPSR bits.

[2] Reads of the EPSR bits return zero, and the processor ignores writes to the these bits



See the instruction descriptions [Section 21–21.4.7.6](#) and [Section 21–21.4.7.7](#) for more information about how to access the program status registers.

**Application Program Status Register:** The APSR contains the current state of the condition flags, from previous instruction executions. See the register summary in [Table 21–298](#) for its attributes. The bit assignments are:

**Table 300. APSR bit assignments**

Bits	Name	Function
[31]	N	Negative flag
[30]	Z	Zero flag
[29]	C	Carry or borrow flag
[28]	V	Overflow flag
[27:0]	-	Reserved

See [Section 21.4.4.1.4](#) for more information about the APSR negative, zero, carry or borrow, and overflow flags.

**Interrupt Program Status Register:** The IPSR contains the exception number of the current **Interrupt Service Routine** (ISR). See the register summary in [Table 21–298](#) for its attributes. The bit assignments are:

**Table 301. IPSR bit assignments**

Bits	Name	Function
[31:6]	-	Reserved
[5:0]	Exception number	This is the number of the current exception: 0 = Thread mode 1 = Reserved 2 = NMI 3 = HardFault 4-10 = Reserved 11 = SVCall 12, 13 = Reserved 14 = PendSV 15 = SysTick 16 = IRQ0 . . . 47 = IRQ31 48-63 = Reserved. see <a href="#">Section 21–21.3.3.2</a> for more information.

**Execution Program Status Register:** The EPSR contains the Thumb state bit.

See the register summary in [Table 21–298](#) for the EPSR attributes. The bit assignments are:

Table 302. EPSR bit assignments

Bits	Name	Function
[31:25]	-	Reserved
[24]	T	Thumb state bit
[23:0]	-	Reserved

Attempts by application software to read the EPSR directly using the `MRS` instruction always return zero. Attempts to write the EPSR using the `MSR` instruction are ignored. Fault handlers can examine the EPSR value in the stacked PSR to determine the cause of the fault. See [Section 21–21.3.3.6](#). The following can clear the T bit to 0:

- instructions `BLX`, `BX` and `POP{PC}`
- restoration from the stacked xPSR value on an exception return
- bit[0] of the vector value on an exception entry.

Attempting to execute instructions when the T bit is 0 results in a HardFault or lockup. See [Section 21–21.3.4.1](#) for more information.

**Interruptible-restartable instructions:** The interruptible-restartable instructions are `LDM` and `STM`. When an interrupt occurs during the execution of one of these instructions, the processor abandons execution of the instruction.

After servicing the interrupt, the processor restarts execution of the instruction from the beginning.

#### 21.3.1.3.6 Exception mask register

The exception mask register disables the handling of exceptions by the processor. Disable exceptions where they might impact on timing critical tasks or code sequences requiring atomicity.

To disable or re-enable exceptions, use the `MSR` and `MRS` instructions, or the `CPS` instruction, to change the value of PRIMASK. See [Section 21–21.4.7.6](#), [Section 21–21.4.7.7](#), and [Section 21–21.4.7.2](#) for more information.

**Priority Mask Register:** The PRIMASK register prevents activation of all exceptions with configurable priority. See the register summary in [Table 21–298](#) for its attributes. The bit assignments are:

Table 303. PRIMASK register bit assignments

Bits	Name	Function
[31:1]	-	Reserved
[0]	PRIMASK	0 = no effect 1 = prevents the activation of all exceptions with configurable priority.

#### 21.3.1.3.7 CONTROL register

The CONTROL register controls the stack used when the processor is in Thread mode. See the register summary in [Table 21–298](#) for its attributes. The bit assignments are:

Table 304. CONTROL register bit assignments

Bits	Name	Function
[31:2]	-	Reserved
[1]	Active stack pointer	Defines the current stack: 0 = MSP is the current stack pointer 1 = PSP is the current stack pointer. In Handler mode this bit reads as zero and ignores writes.
[0]	-	Reserved.

Handler mode always uses the MSP, so the processor ignores explicit writes to the active stack pointer bit of the CONTROL register when in Handler mode. The exception entry and return mechanisms update the CONTROL register.

In an OS environment, it is recommended that threads running in Thread mode use the process stack and the kernel and exception handlers use the main stack.

By default, Thread mode uses the MSP. To switch the stack pointer used in Thread mode to the PSP, use the `MSR` instruction to set the Active stack pointer bit to 1, see [Section 21–21.4.7.6](#).

**Remark:** When changing the stack pointer, software must use an `ISB` instruction immediately after the `MSR` instruction. This ensures that instructions after the `ISB` execute using the new stack pointer. See [Section 21–21.4.7.5](#).

### 21.3.1.4 Exceptions and interrupts

The Cortex-M0 processor supports interrupts and system exceptions. The processor and the **Nested Vectored Interrupt Controller** (NVIC) prioritize and handle all exceptions. An interrupt or exception changes the normal flow of software control. The processor uses handler mode to handle all exceptions except for reset. See [Section 21–21.3.3.6.1](#) and [Section 21–21.3.3.6.2](#) for more information.

The NVIC registers control interrupt handling. See [Section 21–21.5.2](#) for more information.

### 21.3.1.5 Data types

The processor:

- supports the following data types:
  - 32-bit words
  - 16-bit halfwords
  - 8-bit bytes
- manages all data memory accesses as little-endian. Instruction memory and **Private Peripheral Bus** (PPB) accesses are always little-endian. See [Section 21–21.3.2.1](#) for more information.

### 21.3.1.6 The Cortex Microcontroller Software Interface Standard

ARM provides the **Cortex Microcontroller Software Interface Standard** (CMSIS) for programming Cortex-M0 microcontrollers. The CMSIS is an integrated part of the device driver library.

For a Cortex-M0 microcontroller system, CMSIS defines:

- a common way to:
  - access peripheral registers
  - define exception vectors
- the names of:
  - the registers of the core peripherals
  - the core exception vectors
- a device-independent interface for RTOS kernels.

The CMSIS includes address definitions and data structures for the core peripherals in the Cortex-M0 processor. It also includes optional interfaces for middleware components comprising a TCP/IP stack and a Flash file system.

The CMSIS simplifies software development by enabling the reuse of template code, and the combination of CMSIS-compliant software components from various middleware vendors. Software vendors can expand the CMSIS to include their peripheral definitions and access functions for those peripherals.

This document includes the register names defined by the CMSIS, and gives short descriptions of the CMSIS functions that address the processor core and the core peripherals.

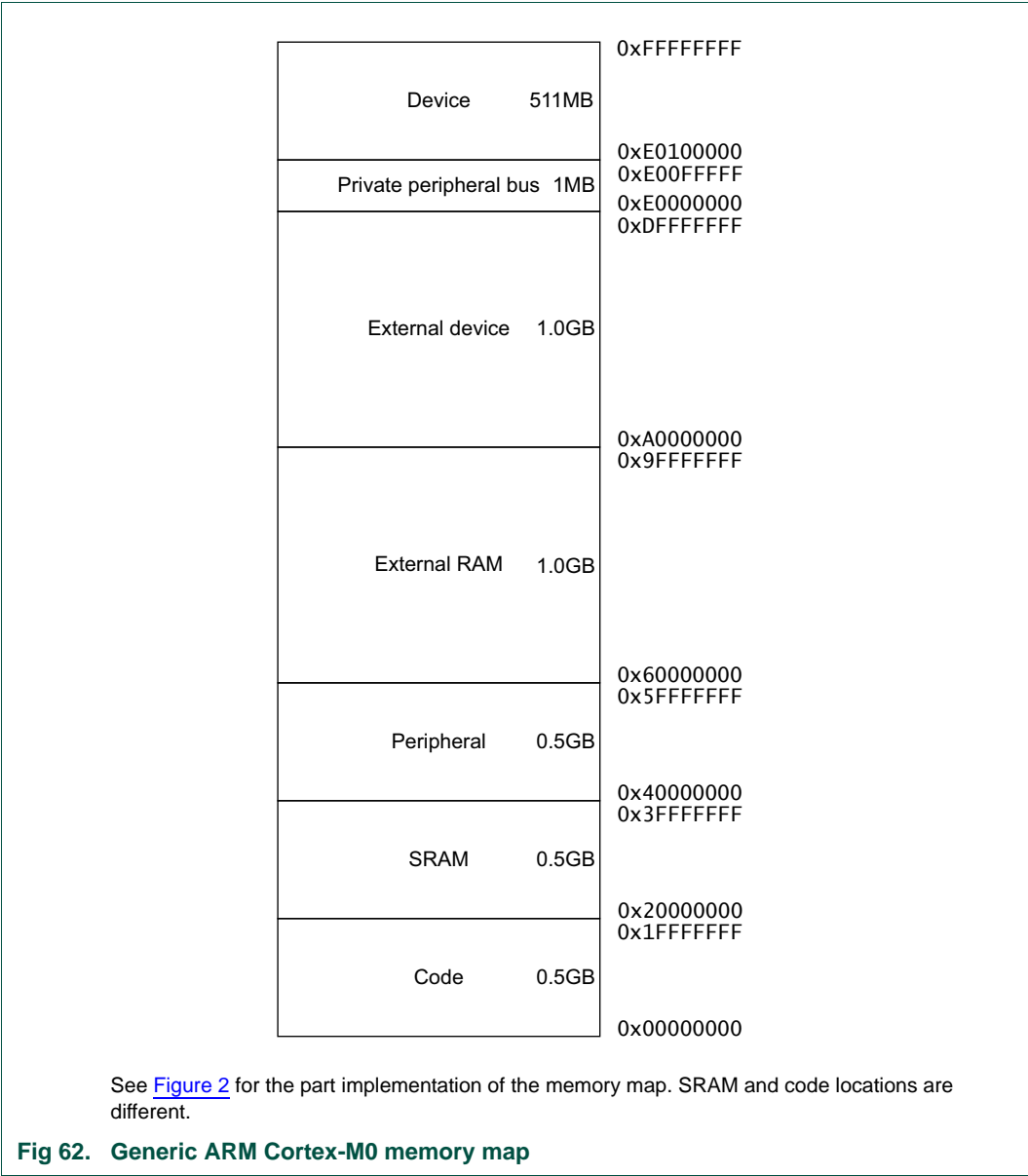
**Remark:** This document uses the register short names defined by the CMSIS. In a few cases these differ from the architectural short names that might be used in other documents.

The following sections give more information about the CMSIS:

- [Section 21.3.5.3 “Power management programming hints”](#)
- [Section 21.4.2 “Intrinsic functions”](#)
- [Section 21.5.2.1 “Accessing the Cortex-M0 NVIC registers using CMSIS”](#)
- [Section 21.5.2.8.1 “NVIC programming hints”](#).

### 21.3.2 Memory model

This section describes the processor memory map and the behavior of memory accesses. The processor has a fixed memory map that provides up to 4GB of addressable memory. The memory map is:



The processor reserves regions of the **Private peripheral bus** (PPB) address range for core peripheral registers, see [Section 21–21.2](#).

21.3.2.1 Memory regions, types and attributes

The memory map is split into regions. Each region has a defined memory type, and some regions have additional memory attributes. The memory type and attributes determine the behavior of accesses to the region.

The memory types are:

- Normal** — The processor can re-order transactions for efficiency, or perform speculative reads.
- Device** — The processor preserves transaction order relative to other transactions to Device or Strongly-ordered memory.

**Strongly-ordered** — The processor preserves transaction order relative to all other transactions.

The different ordering requirements for Device and Strongly-ordered memory mean that the memory system can buffer a write to Device memory, but must not buffer a write to Strongly-ordered memory.

The additional memory attributes include.

**Execute Never (XN)** — Means the processor prevents instruction accesses. A HardFault exception is generated on executing an instruction fetched from an XN region of memory.

### 21.3.2.2 Memory system ordering of memory accesses

For most memory accesses caused by explicit memory access instructions, the memory system does not guarantee that the order in which the accesses complete matches the program order of the instructions, providing any re-ordering does not affect the behavior of the instruction sequence. Normally, if correct program execution depends on two memory accesses completing in program order, software must insert a memory barrier instruction between the memory access instructions, see [Section 21–21.3.2.4](#).

However, the memory system does guarantee some ordering of accesses to Device and Strongly-ordered memory. For two memory access instructions A1 and A2, if A1 occurs before A2 in program order, the ordering of the memory accesses caused by two instructions is:

A1 \ A2		Normal access	Device access		Strongly-ordered access
			Non-shareable	Shareable	
Normal access		-	-	-	-
Device access, non-shareable		-	<	-	<
Device access, shareable		-	-	<	<
Strongly-ordered access		-	<	<	<

**Fig 63. Memory ordering restrictions**

Where:

- — Means that the memory system does not guarantee the ordering of the accesses.

< — Means that accesses are observed in program order, that is, A1 is always observed before A2.

### 21.3.2.3 Behavior of memory accesses

The behavior of accesses to each region in the memory map is:

Table 305. Memory access behavior

Address range	Memory region	Memory type <sup>[1]</sup>	XN <sup>[1]</sup>	Description
0x00000000-0x1FFFFFFF	Code	Normal	-	Executable region for program code. You can also put data here.
0x20000000-0x3FFFFFFF	SRAM	Normal	-	Executable region for data. You can also put code here.
0x40000000-0x5FFFFFFF	Peripheral	Device	XN	External device memory.
0x60000000-0x9FFFFFFF	External RAM	Normal	-	Executable region for data.
0xA0000000-0xDFFFFFFF	External device	Device	XN	External device memory.
0xE0000000-0xE00FFFFF	Private Peripheral Bus	Strongly-ordered	XN	This region includes the NVIC, System timer, and System Control Block. Only word accesses can be used in this region.
0xE0100000-0xFFFFFFFF	Device	Device	XN	Vendor specific.

[1] See [Section 21–21.3.2.1](#) for more information.

The Code, SRAM, and external RAM regions can hold programs.

#### 21.3.2.4 Software ordering of memory accesses

The order of instructions in the program flow does not always guarantee the order of the corresponding memory transactions. This is because:

- the processor can reorder some memory accesses to improve efficiency, providing this does not affect the behavior of the instruction sequence
- memory or devices in the memory map might have different wait states
- some memory accesses are buffered or speculative.

[Section 21–21.3.2.2](#) describes the cases where the memory system guarantees the order of memory accesses. Otherwise, if the order of memory accesses is critical, software must include memory barrier instructions to force that ordering. The processor provides the following memory barrier instructions:

**DMB** — The **Data Memory Barrier** (DMB) instruction ensures that outstanding memory transactions complete before subsequent memory transactions. See [Section 21–21.4.7.3](#).

**DSB** — The **Data Synchronization Barrier** (DSB) instruction ensures that outstanding memory transactions complete before subsequent instructions execute. See [Section 21–21.4.7.4](#).

**ISB** — The **Instruction Synchronization Barrier** (ISB) ensures that the effect of all completed memory transactions is recognizable by subsequent instructions. See [Section 21–21.4.7.5](#).

The following are examples of using memory barrier instructions:

**Vector table** — If the program changes an entry in the vector table, and then enables the corresponding exception, use a `DMB` instruction between the operations. This ensures that if the exception is taken immediately after being enabled the processor uses the new exception vector.

**Self-modifying code** — If a program contains self-modifying code, use an `ISB` instruction immediately after the code modification in the program. This ensures subsequent instruction execution uses the updated program.

**Memory map switching** — If the system contains a memory map switching mechanism, use a `DSB` instruction after switching the memory map. This ensures subsequent instruction execution uses the updated memory map.

Memory accesses to Strongly-ordered memory, such as the System Control Block, do not require the use of `DMB` instructions.

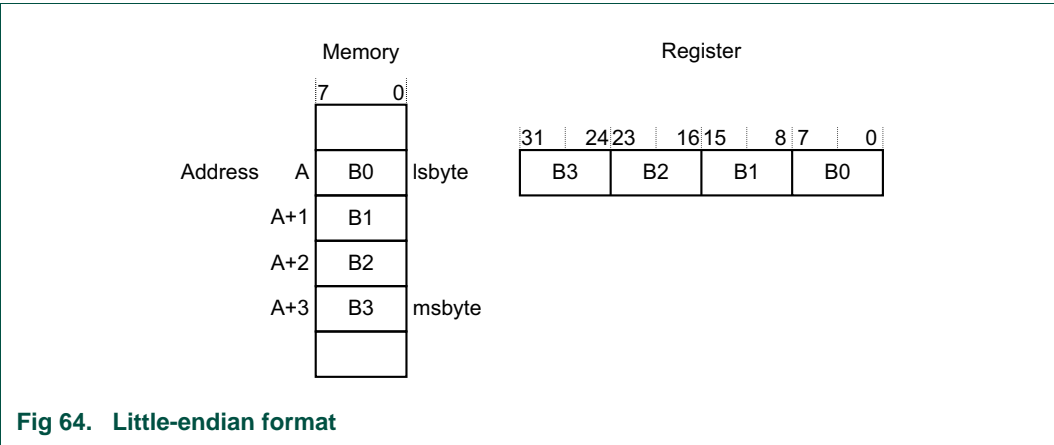
The processor preserves transaction order relative to all other transactions.

21.3.2.5 Memory endianness

The processor views memory as a linear collection of bytes numbered in ascending order from zero. For example, bytes 0-3 hold the first stored word, and bytes 4-7 hold the second stored word. [Section 21–21.3.2.5.1](#) describes how words of data are stored in memory.

21.3.2.5.1 Little-endian format

In little-endian format, the processor stores the **least significant byte** (lsbyte) of a word at the lowest-numbered byte, and the **most significant byte** (msbyte) at the highest-numbered byte. For example:



21.3.3 Exception model

This section describes the exception model.

21.3.3.1 Exception states

Each exception is in one of the following states:

**Inactive** — The exception is not active and not pending.

**Pending** — The exception is waiting to be serviced by the processor.



An interrupt request from a peripheral or from software can change the state of the corresponding interrupt to pending.

**Active** — An exception that is being serviced by the processor but has not completed.

An exception handler can interrupt the execution of another exception handler. In this case both exceptions are in the active state.

**Active and pending** — The exception is being serviced by the processor and there is a pending exception from the same source.

### 21.3.3.2 Exception types

The exception types are:

**Reset** — Reset is invoked on power up or a warm reset. The exception model treats reset as a special form of exception. When reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When reset is deasserted, execution restarts from the address provided by the reset entry in the vector table. Execution restarts in Thread mode.

**NMI** — A **NonMaskable Interrupt** (NMI) can be signalled by a peripheral or triggered by software. This is the highest priority exception other than reset. It is permanently enabled and has a fixed priority of -2. NMIs cannot be:

- masked or prevented from activation by any other exception
- preempted by any exception other than Reset.

**HardFault** — A HardFault is an exception that occurs because of an error during normal or exception processing. HardFaults have a fixed priority of -1, meaning they have higher priority than any exception with configurable priority.

**SVC** — A **supervisor call** (SVC) is an exception that is triggered by the `SVC` instruction. In an OS environment, applications can use `SVC` instructions to access OS kernel functions and device drivers.

**PendSV** — PendSV is an interrupt-driven request for system-level service. In an OS environment, use PendSV for context switching when no other exception is active.

**SysTick** — A SysTick exception is an exception the system timer generates when it reaches zero. Software can also generate a SysTick exception. In an OS environment, the processor can use this exception as system tick.

**Interrupt (IRQ)** — An interrupt, or IRQ, is an exception signalled by a peripheral, or generated by a software request. All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor.

**Table 306. Properties of different exception types**

Exception number <sup>[1]</sup>	IRQ number <sup>[1]</sup>	Exception type	Priority	Vector address <sup>[2]</sup>
1	-	Reset	-3, the highest	0x00000004
2	-14	NMI	-2	0x00000008
3	-13	HardFault	-1	0x0000000C
4-10	-	Reserved	-	-
11	-5	SVC	Configurable <sup>[3]</sup>	0x0000002C
12-13	-	Reserved	-	-

Table 306. Properties of different exception types

Exception number <sup>[1]</sup>	IRQ number <sup>[1]</sup>	Exception type	Priority	Vector address <sup>[2]</sup>
14	-2	PendSV	Configurable <sup>[3]</sup>	0x00000038
15	-1	SysTick	Configurable <sup>[3]</sup>	0x0000003C
16 and above	0 and above	Interrupt (IRQ)	Configurable <sup>[3]</sup>	0x00000040 and above <sup>[4]</sup>

[1] To simplify the software layer, the CMSIS only uses IRQ numbers and therefore uses negative values for exceptions other than interrupts. The IPSR returns the Exception number, see [Table 21–301](#).

[2] See [Section 21.3.3.4](#) for more information.

[3] See [Section 21–21.5.2.6](#).

[4] Increasing in steps of 4.

For an asynchronous exception, other than reset, the processor can execute additional instructions between when the exception is triggered and when the processor enters the exception handler.

Privileged software can disable the exceptions that [Table 21–306](#) shows as having configurable priority, see [Section 21–21.5.2.3](#).

For more information about HardFaults, see [Section 21–21.3.4](#).

### 21.3.3.3 Exception handlers

The processor handles exceptions using:

**Interrupt Service Routines (ISRs)** — Interrupts IRQ0 to IRQ31 are the exceptions handled by ISRs.

**Fault handler** — HardFault is the only exception handled by the fault handler.

**System handlers** — NMI, PendSV, SVCall SysTick, and HardFault are all system exceptions handled by system handlers.

### 21.3.3.4 Vector table

The vector table contains the reset value of the stack pointer, and the start addresses, also called exception vectors, for all exception handlers. [Figure 21–65](#) shows the order of the exception vectors in the vector table. The least-significant bit of each vector must be 1, indicating that the exception handler is written in Thumb code.

Exception number	IRQ number	Vector	Offset
47	31	IRQ31	0xBC
.		.	.
.		.	.
.		.	.
18	2	IRQ2	0x48
17	1	IRQ1	0x44
16	0	IRQ0	0x40
15	-1	SysTick	0x3C
14	-2	PendSV	0x38
13		Reserved	
12			
11	-5	SVCall	0x2C
10			
9			
8			
7		Reserved	
6			
5			
4			
3	-13	HardFault	0x10
2	-14	NMI	0x0C
1		Reset	0x08
		Initial SP value	0x04
			0x00

**Fig 65. Vector table**

The vector table is fixed at address 0x00000000.

21.3.3.5 Exception priorities

As [Table 21–306](#) shows, all exceptions have an associated priority, with:

- a lower priority value indicating a higher priority
- configurable priorities for all exceptions except Reset, HardFault, and NMI.

If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0. For information about configuring exception priorities see

- [Section 21–21.5.3.7](#)
- [Section 21–21.5.2.6](#).

**Remark:** Configurable priority values are in the range 0-3. The Reset, HardFault, and NMI exceptions, with fixed negative priority values, always have higher priority than any other exception.

Assigning a higher priority value to IRQ[0] and a lower priority value to IRQ[1] means that IRQ[1] has higher priority than IRQ[0]. If both IRQ[1] and IRQ[0] are asserted, IRQ[1] is processed before IRQ[0].

If multiple pending exceptions have the same priority, the pending exception with the lowest exception number takes precedence. For example, if both IRQ[0] and IRQ[1] are pending and have the same priority, then IRQ[0] is processed before IRQ[1].

When the processor is executing an exception handler, the exception handler is preempted if a higher priority exception occurs. If an exception occurs with the same priority as the exception being handled, the handler is not preempted, irrespective of the exception number. However, the status of the new interrupt changes to pending.

### 21.3.3.6 Exception entry and return

Descriptions of exception handling use the following terms:

**Preemption** — When the processor is executing an exception handler, an exception can preempt the exception handler if its priority is higher than the priority of the exception being handled.

When one exception preempts another, the exceptions are called nested exceptions. See [Section 21–21.3.3.6.1](#) for more information.

**Return** — This occurs when the exception handler is completed, and:

- there is no pending exception with sufficient priority to be serviced
- the completed exception handler was not handling a late-arriving exception.

The processor pops the stack and restores the processor state to the state it had before the interrupt occurred. See [Section 21–21.3.3.6.2](#) for more information.

**Tail-chaining** — This mechanism speeds up exception servicing. On completion of an exception handler, if there is a pending exception that meets the requirements for exception entry, the stack pop is skipped and control transfers to the new exception handler.

**Late-arriving** — This mechanism speeds up preemption. If a higher priority exception occurs during state saving for a previous exception, the processor switches to handle the higher priority exception and initiates the vector fetch for that exception. State saving is not affected by late arrival because the state saved would be the same for both exceptions. On return from the exception handler of the late-arriving exception, the normal tail-chaining rules apply.

#### 21.3.3.6.1 Exception entry

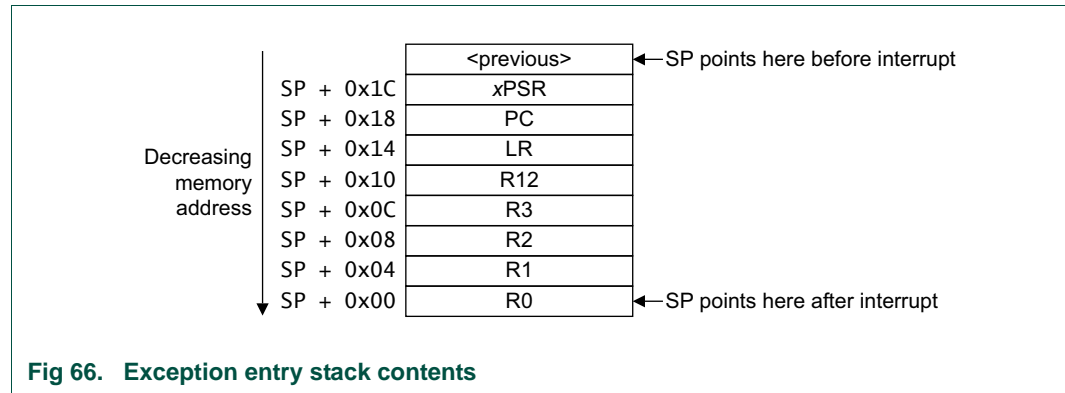
Exception entry occurs when there is a pending exception with sufficient priority and either:

- the processor is in Thread mode
- the new exception is of higher priority than the exception being handled, in which case the new exception preempts the exception being handled.

When one exception preempts another, the exceptions are nested.

Sufficient priority means the exception has greater priority than any limit set by the mask register, see [Section 21–21.3.1.3.6](#). An exception with less priority than this is pending but is not handled by the processor.

When the processor takes an exception, unless the exception is a tail-chained or a late-arriving exception, the processor pushes information onto the current stack. This operation is referred to as **stacking** and the structure of eight data words is referred to as a **stack frame**. The stack frame contains the following information:



Immediately after stacking, the stack pointer indicates the lowest address in the stack frame. The stack frame is aligned to a double-word address.

The stack frame includes the return address. This is the address of the next instruction in the interrupted program. This value is restored to the PC at exception return so that the interrupted program resumes.

The processor performs a vector fetch that reads the exception handler start address from the vector table. When stacking is complete, the processor starts executing the exception handler. At the same time, the processor writes an EXC\_RETURN value to the LR. This indicates which stack pointer corresponds to the stack frame and what operation mode the processor was in before the entry occurred.

If no higher priority exception occurs during exception entry, the processor starts executing the exception handler and automatically changes the status of the corresponding pending interrupt to active.

If another higher priority exception occurs during exception entry, the processor starts executing the exception handler for this exception and does not change the pending status of the earlier exception. This is the late arrival case.

#### 21.3.3.6.2 Exception return

Exception return occurs when the processor is in Handler mode and execution of one of the following instructions attempts to set the PC to an EXC\_RETURN value:

- a **POP** instruction that loads the PC
- a **BX** instruction using any register.

The processor saves an EXC\_RETURN value to the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. Bits[31:4] of an EXC\_RETURN value are 0xFFFFFFFF. When the processor loads a value matching this pattern to the PC it detects that the operation is a

not a normal branch operation and, instead, that the exception is complete. Therefore, it starts the exception return sequence. Bits[3:0] of the EXC\_RETURN value indicate the required return stack and processor mode, as [Table 21–307](#) shows.

**Table 307. Exception return behavior**

EXC_RETURN	Description
0xFFFFFFFF1	Return to Handler mode. Exception return gets state from the main stack. Execution uses MSP after return.
0xFFFFFFFF9	Return to Thread mode. Exception return gets state from MSP. Execution uses MSP after return.
0xFFFFFFFDD	Return to Thread mode. Exception return gets state from PSP. Execution uses PSP after return.
All other values	Reserved.

### 21.3.4 Fault handling

Faults are a subset of exceptions, see [Section 21–21.3.3](#). All faults result in the HardFault exception being taken or cause lockup if they occur in the NMI or HardFault handler. The faults are:

- execution of an SVC instruction at a priority equal or higher than SVCall
- execution of a BKPT instruction without a debugger attached
- a system-generated bus error on a load or store
- execution of an instruction from an XN memory address
- execution of an instruction from a location for which the system generates a bus fault
- a system-generated bus error on a vector fetch
- execution of an Undefined instruction
- execution of an instruction when not in Thumb-State as a result of the T-bit being previously cleared to 0
- an attempted load or store to an unaligned address.

**Remark:** Only Reset and NMI can preempt the fixed priority HardFault handler. A HardFault can preempt any exception other than Reset, NMI, or another hard fault.

#### 21.3.4.1 Lockup

The processor enters a lockup state if a fault occurs when executing the NMI or HardFault handlers, or if the system generates a bus error when unstacking the PSR on an exception return using the MSP. When the processor is in lockup state it does not execute any instructions. The processor remains in lockup state until one of the following occurs:

- it is reset
- a debugger halts it
- an NMI occurs and the current lockup is in the HardFault handler.

**Remark:** If lockup state occurs in the NMI handler a subsequent NMI does not cause the processor to leave lockup state.

### 21.3.5 Power management

The Cortex-M0 processor sleep modes reduce power consumption:

- a sleep mode, that stops the processor clock
- a Deep-sleep mode.

The SLEEPDEEP bit of the SCR selects which sleep mode is used, see [Section 21–21.5.3.5](#).

This section describes the mechanisms for entering sleep mode and the conditions for waking up from sleep mode.

#### 21.3.5.1 Entering sleep mode

This section describes the mechanisms software can use to put the processor into sleep mode.

The system can generate spurious wake-up events, for example a debug operation wakes up the processor. Therefore software must be able to put the processor back into sleep mode after such an event. A program might have an idle loop to put the processor back in to sleep mode.

##### 21.3.5.1.1 Wait for interrupt

The Wait For Interrupt instruction, `WFI`, causes immediate entry to sleep mode. When the processor executes a `WFI` instruction it stops executing instructions and enters sleep mode. See [Section 21–21.4.7.12](#) for more information.

##### 21.3.5.1.2 Wait for event

**Remark:** The WFE instruction is not implemented on the LPC111x/LPC11Cxx.

The Wait For Event instruction, `WFE`, causes entry to sleep mode conditional on the value of a one-bit event register. When the processor executes a `WFE` instruction, it checks the value of the event register:

**0** — The processor stops executing instructions and enters sleep mode

**1** — The processor sets the register to zero and continues executing instructions without entering sleep mode.

See [Section 21–21.4.7.11](#) for more information.

If the event register is 1, this indicates that the processor must not enter sleep mode on execution of a `WFE` instruction. Typically, this is because of the assertion of an external event, or because another processor in the system has executed a `SEV` instruction, see [Section 21–21.4.7.9](#). Software cannot access this register directly.

#### 21.3.5.1.3 Sleep-on-exit

If the SLEEPONEXIT bit of the SCR is set to 1, when the processor completes the execution of an exception handler and returns to Thread mode it immediately enters sleep mode. Use this mechanism in applications that only require the processor to run when an interrupt occurs.

#### 21.3.5.2 Wake-up from sleep mode

The conditions for the processor to wake-up depend on the mechanism that caused it to enter sleep mode.

##### 21.3.5.2.1 Wake-up from WFI or sleep-on-exit

Normally, the processor wakes up only when it detects an exception with sufficient priority to cause exception entry.

Some embedded systems might have to execute system restore tasks after the processor wakes up, and before it executes an interrupt handler. To achieve this set the PRIMASK bit to 1. If an interrupt arrives that is enabled and has a higher priority than current exception priority, the processor wakes up but does not execute the interrupt handler until the processor sets PRIMASK to zero. For more information about PRIMASK, see [Section 21–21.3.1.3.6](#).

##### 21.3.5.2.2 Wake-up from WFE

The processor wakes up if:

- it detects an exception with sufficient priority to cause exception entry
- in a multiprocessor system, another processor in the system executes a `SEV` instruction.

In addition, if the SEVONPEND bit in the SCR is set to 1, any new pending interrupt triggers an event and wakes up the processor, even if the interrupt is disabled or has insufficient priority to cause exception entry. For more information about the SCR see [Section 21–21.5.3.5](#).

#### 21.3.5.3 Power management programming hints

ISO/IEC C cannot directly generate the `WFI`, `WFE`, and `SEV` instructions. The CMSIS provides the following intrinsic functions for these instructions:

```
void __WFE(void) // Wait for Event

void __WFI(void) // Wait for Interrupt

void __SEV(void) // Send Event
```

## 21.4 Instruction set

### 21.4.1 Instruction set summary

The processor implements a version of the Thumb instruction set. [Table 308](#) lists the supported instructions.

**Remark:** In [Table 308](#)



- angle brackets, <>, enclose alternative forms of the operand
- braces, {}, enclose optional operands and mnemonic parts
- the Operands column is not exhaustive.

For more information on the instructions and operands, see the instruction descriptions.

**Table 308. Cortex-M0 instructions**

Mnemonic	Operands	Brief description	Flags	Reference
ADCS	{Rd,} Rn, Rm	Add with Carry	N,Z,C,V	<a href="#">Section 21–21.4.5.1</a>
ADD{S}	{Rd,} Rn, <Rm #imm>	Add	N,Z,C,V	<a href="#">Section 21–21.4.5.1</a>
ADR	Rd, label	PC-relative Address to Register	-	<a href="#">Section 21–21.4.4.1</a>
ANDS	{Rd,} Rn, Rm	Bitwise AND	N,Z	<a href="#">Section 21–21.4.5.1</a>
ASRS	{Rd,} Rm, <Rs #imm>	Arithmetic Shift Right	N,Z,C	<a href="#">Section 21–21.4.5.3</a>
B{cc}	label	Branch {conditionally}	-	<a href="#">Section 21–21.4.6.1</a>
BICS	{Rd,} Rn, Rm	Bit Clear	N,Z	<a href="#">Section 21–21.4.5.2</a>
BKPT	#imm	Breakpoint	-	<a href="#">Section 21–21.4.7.1</a>
BL	label	Branch with Link	-	<a href="#">Section 21–21.4.6.1</a>
BLX	Rm	Branch indirect with Link	-	<a href="#">Section 21–21.4.6.1</a>
BX	Rm	Branch indirect	-	<a href="#">Section 21–21.4.6.1</a>
CMN	Rn, Rm	Compare Negative	N,Z,C,V	<a href="#">Section 21–21.4.5.4</a>
CMP	Rn, <Rm #imm>	Compare	N,Z,C,V	<a href="#">Section 21–21.4.5.4</a>
CPSID	i	Change Processor State, Disable Interrupts	-	<a href="#">Section 21–21.4.7.2</a>
CPSIE	i	Change Processor State, Enable Interrupts	-	<a href="#">Section 21–21.4.7.2</a>
DMB	-	Data Memory Barrier	-	<a href="#">Section 21–21.4.7.3</a>
DSB	-	Data Synchronization Barrier	-	<a href="#">Section 21–21.4.7.4</a>
EORS	{Rd,} Rn, Rm	Exclusive OR	N,Z	<a href="#">Section 21–21.4.5.2</a>
ISB	-	Instruction Synchronization Barrier	-	<a href="#">Section 21–21.4.7.5</a>
LDM	Rn{!}, reglist	Load Multiple registers, increment after	-	<a href="#">Section 21–21.4.4.5</a>
LDR	Rt, label	Load Register from PC-relative address	-	<a href="#">Section 21–21.4.4</a>
LDR	Rt, [Rn, <Rm #imm>]	Load Register with word	-	<a href="#">Section 21–21.4.4</a>
LDRB	Rt, [Rn, <Rm #imm>]	Load Register with byte	-	<a href="#">Section 21–21.4.4</a>
LDRH	Rt, [Rn, <Rm #imm>]	Load Register with halfword	-	<a href="#">Section 21–21.4.4</a>
LDRSB	Rt, [Rn, <Rm #imm>]	Load Register with signed byte	-	<a href="#">Section 21–21.4.4</a>
LDRSH	Rt, [Rn, <Rm #imm>]	Load Register with signed halfword	-	<a href="#">Section 21–21.4.4</a>
LSLS	{Rd,} Rn, <Rs #imm>	Logical Shift Left	N,Z,C	<a href="#">Section 21–21.4.5.3</a>
U	{Rd,} Rn, <Rs #imm>	Logical Shift Right	N,Z,C	<a href="#">Section 21–21.4.5.3</a>
MOV{S}	Rd, Rm	Move	N,Z	<a href="#">Section 21–21.4.5.5</a>
MRS	Rd, spec_reg	Move to general register from special register	-	<a href="#">Section 21–21.4.7.6</a>
MSR	spec_reg, Rm	Move to special register from general register	N,Z,C,V	<a href="#">Section 21–21.4.7.7</a>
MULS	Rd, Rn, Rm	Multiply, 32-bit result	N,Z	<a href="#">Section 21–21.4.5.6</a>
MVNS	Rd, Rm	Bitwise NOT	N,Z	<a href="#">Section 21–21.4.5.5</a>

Table 308. Cortex-M0 instructions

Mnemonic	Operands	Brief description	Flags	Reference
NOP	-	No Operation	-	<a href="#">Section 21–21.4.7.8</a>
ORRS	{Rd,} Rn, Rm	Logical OR	N,Z	<a href="#">Section 21–21.4.5.2</a>
POP	reglist	Pop registers from stack	-	<a href="#">Section 21–21.4.4.6</a>
PUSH	reglist	Push registers onto stack	-	<a href="#">Section 21–21.4.4.6</a>
REV	Rd, Rm	Byte-Reverse word	-	<a href="#">Section 21–21.4.5.7</a>
REV16	Rd, Rm	Byte-Reverse packed halfwords	-	<a href="#">Section 21–21.4.5.7</a>
REVSH	Rd, Rm	Byte-Reverse signed halfword	-	<a href="#">Section 21–21.4.5.7</a>
RORS	{Rd,} Rn, Rs	Rotate Right	N,Z,C	<a href="#">Section 21–21.4.5.3</a>
RSBS	{Rd,} Rn, #0	Reverse Subtract	N,Z,C,V	<a href="#">Section 21–21.4.5.1</a>
SBCS	{Rd,} Rn, Rm	Subtract with Carry	N,Z,C,V	<a href="#">Section 21–21.4.5.1</a>
SEV	-	Send Event	-	<a href="#">Section 21–21.4.7.9</a>
STM	Rn!, reglist	Store Multiple registers, increment after	-	<a href="#">Section 21–21.4.4.5</a>
STR	Rt, [Rn, <Rm #imm>]	Store Register as word	-	<a href="#">Section 21–21.4.4</a>
STRB	Rt, [Rn, <Rm #imm>]	Store Register as byte	-	<a href="#">Section 21–21.4.4</a>
STRH	Rt, [Rn, <Rm #imm>]	Store Register as halfword	-	<a href="#">Section 21–21.4.4</a>
SUB{S}	{Rd,} Rn, <Rm #imm>	Subtract	N,Z,C,V	<a href="#">Section 21–21.4.5.1</a>
SVC	#imm	Supervisor Call	-	<a href="#">Section 21–21.4.7.10</a>
SXTB	Rd, Rm	Sign extend byte	-	<a href="#">Section 21–21.4.5.8</a>
SXTH	Rd, Rm	Sign extend halfword	-	<a href="#">Section 21–21.4.5.8</a>
TST	Rn, Rm	Logical AND based test	N,Z	<a href="#">Section 21–21.4.5.9</a>
UXTB	Rd, Rm	Zero extend a byte	-	<a href="#">Section 21–21.4.5.8</a>
UXTH	Rd, Rm	Zero extend a halfword	-	<a href="#">Section 21–21.4.5.8</a>
WFE	-	Wait For Event	-	<a href="#">Section 21–21.4.7.11</a>
WFI	-	Wait For Interrupt	-	<a href="#">Section 21–21.4.7.12</a>

## 21.4.2 Intrinsic functions

ISO/IEC C code cannot directly access some Cortex-M0 instructions. This section describes intrinsic functions that can generate these instructions, provided by the CMSIS and that might be provided by a C compiler. If a C compiler does not support an appropriate intrinsic function, you might have to use inline assembler to access the relevant instruction.

The CMSIS provides the following intrinsic functions to generate instructions that ISO/IEC C code cannot directly access:

Table 309. CMSIS intrinsic functions to generate some Cortex-M0 instructions

Instruction	CMSIS intrinsic function
CPSIE i	void __enable_irq(void)
CPSID i	void __disable_irq(void)
ISB	void __ISB(void)
DSB	void __DSB(void)
DMB	void __DMB(void)
NOP	void __NOP(void)

**Table 309. CMSIS intrinsic functions to generate some Cortex-M0 instructions**

Instruction	CMSIS intrinsic function
REV	uint32_t __REV(uint32_t int value)
REV16	uint32_t __REV16(uint32_t int value)
REVSH	uint32_t __REVSH(uint32_t int value)
SEV	void __SEV(void)
WFE	void __WFE(void)
WFI	void __WFI(void)

The CMSIS also provides a number of functions for accessing the special registers using MRS and MSR instructions:

**Table 310. CMSIS intrinsic functions to access the special registers**

Special register	Access	CMSIS function
PRIMASK	Read	uint32_t __get_PRIMASK (void)
	Write	void __set_PRIMASK (uint32_t value)
CONTROL	Read	uint32_t __get_CONTROL (void)
	Write	void __set_CONTROL (uint32_t value)
MSP	Read	uint32_t __get_MSP (void)
	Write	void __set_MSP (uint32_t TopOfMainStack)
PSP	Read	uint32_t __get_PSP (void)
	Write	void __set_PSP (uint32_t TopOfProcStack)

### 21.4.3 About the instruction descriptions

The following sections give more information about using the instructions:

- [Section 21.4.3.1 “Operands”](#)
- [Section 21.4.3.2 “Restrictions when using PC or SP”](#)
- [Section 21.4.3.3 “Shift Operations”](#)
- [Section 21.4.3.4 “Address alignment”](#)
- [Section 21.4.3.5 “PC-relative expressions”](#)
- [Section 21.4.3.6 “Conditional execution”](#).

#### 21.4.3.1 Operands

An instruction operand can be an ARM register, a constant, or another instruction-specific parameter. Instructions act on the operands and often store the result in a destination register. When there is a destination register in the instruction, it is usually specified before the other operands.

#### 21.4.3.2 Restrictions when using PC or SP

Many instructions are unable to use, or have restrictions on whether you can use, the **Program Counter** (PC) or **Stack Pointer** (SP) for the operands or destination register. See instruction descriptions for more information.

**Remark:** When you update the PC with a BX, BLX, or POP instruction, bit[0] of any address must be 1 for correct execution. This is because this bit indicates the destination instruction set, and the Cortex-M0 processor only supports Thumb instructions. When a BL or BLX instruction writes the value of bit[0] into the LR it is automatically assigned the value 1.

### 21.4.3.3 Shift Operations

Register shift operations move the bits in a register left or right by a specified number of bits, the **shift length**. Register shift can be performed directly by the instructions ASR, LSR, LSL, and ROR and the result is written to a destination register. The permitted shift lengths depend on the shift type and the instruction, see the individual instruction description. If the shift length is 0, no shift occurs. Register shift operations update the carry flag except when the specified shift length is 0. The following sub-sections describe the various shift operations and how they affect the carry flag. In these descriptions, *Rm* is the register containing the value to be shifted, and *n* is the shift length.

#### 21.4.3.3.1 ASR

Arithmetic shift right by *n* bits moves the left-hand 32 - *n* bits of the register *Rm*, to the right by *n* places, into the right-hand 32 - *n* bits of the result, and it copies the original bit[31] of the register into the left-hand *n* bits of the result. See [Figure 21–67](#).

You can use the ASR operation to divide the signed value in the register *Rm* by  $2^n$ , with the result being rounded towards negative-infinity.

When the instruction is ASRS the carry flag is updated to the last bit shifted out, bit[*n*-1], of the register *Rm*.

**Remark:**

- If *n* is 32 or more, then all the bits in the result are set to the value of bit[31] of *Rm*.
- If *n* is 32 or more and the carry flag is updated, it is updated to the value of bit[31] of *Rm*.

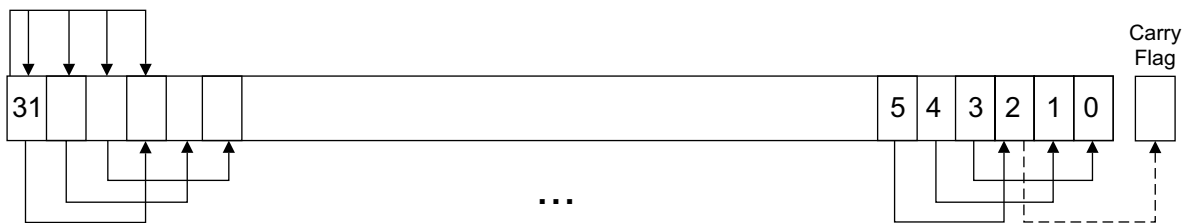


Fig 67. ASR #3

#### 21.4.3.3.2 LSR

Logical shift right by *n* bits moves the left-hand 32 - *n* bits of the register *Rm*, to the right by *n* places, into the right-hand 32 - *n* bits of the result, and it sets the left-hand *n* bits of the result to 0. See [Figure 68](#).

You can use the LSR operation to divide the value in the register  $Rm$  by  $2^n$ , if the value is regarded as an unsigned integer.

When the instruction is LSRS, the carry flag is updated to the last bit shifted out, bit[ $n-1$ ], of the register  $Rm$ .

**Remark:**

- If  $n$  is 32 or more, then all the bits in the result are cleared to 0.
- If  $n$  is 33 or more and the carry flag is updated, it is updated to 0.

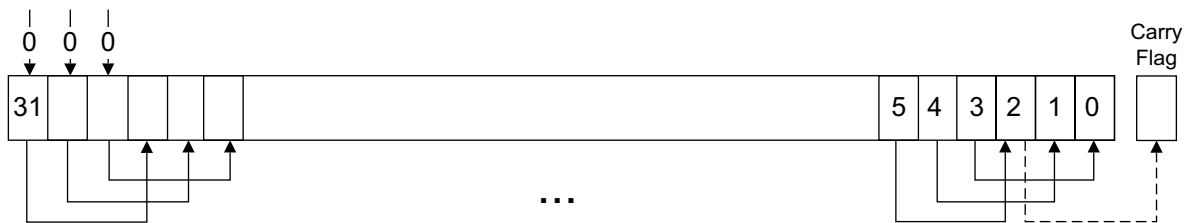


Fig 68. LSR #3

#### 21.4.3.3.3 LSL

Logical shift left by  $n$  bits moves the right-hand  $32-n$  bits of the register  $Rm$ , to the left by  $n$  places, into the left-hand  $32-n$  bits of the result, and it sets the right-hand  $n$  bits of the result to 0. See [Figure 69](#).

You can use the LSL operation to multiply the value in the register  $Rm$  by  $2^n$ , if the value is regarded as an unsigned integer or a two's complement signed integer. Overflow can occur without warning.

When the instruction is LSLS the carry flag is updated to the last bit shifted out, bit[ $32-n$ ], of the register  $Rm$ . These instructions do not affect the carry flag when used with LSL #0.

**Remark:**

- If  $n$  is 32 or more, then all the bits in the result are cleared to 0.
- If  $n$  is 33 or more and the carry flag is updated, it is updated to 0.

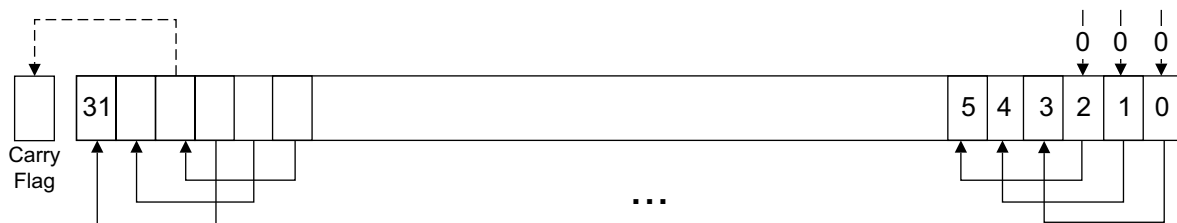


Fig 69. LSL #3

#### 21.4.3.3.4 ROR

Rotate right by  $n$  bits moves the left-hand  $32-n$  bits of the register  $Rm$ , to the right by  $n$  places, into the right-hand  $32-n$  bits of the result, and it moves the right-hand  $n$  bits of the register into the left-hand  $n$  bits of the result. See [Figure 21–70](#).

When the instruction is RORS the carry flag is updated to the last bit rotation, bit[ $n-1$ ], of the register  $Rm$ .

**Remark:**

- If  $n$  is 32, then the value of the result is same as the value in  $Rm$ , and if the carry flag is updated, it is updated to bit[31] of  $Rm$ .
- ROR  
with shift length,  $n$ , greater than 32 is the same as  
ROR  
with shift length  $n-32$ .

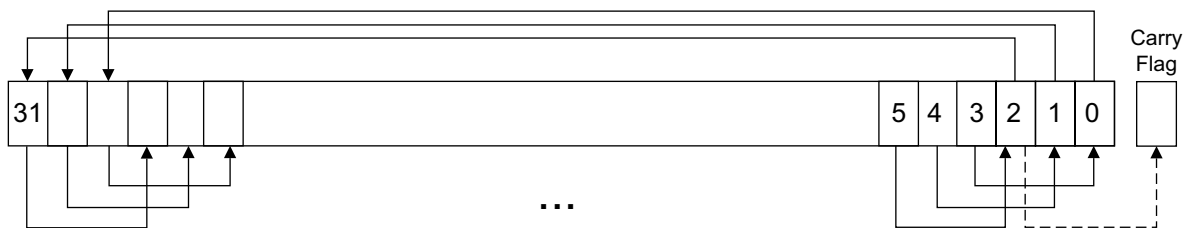


Fig 70. ROR #3

#### 21.4.3.4 Address alignment

An aligned access is an operation where a word-aligned address is used for a word, or multiple word access, or where a halfword-aligned address is used for a halfword access. Byte accesses are always aligned.

There is no support for unaligned accesses on the Cortex-M0 processor. Any attempt to perform an unaligned memory access operation results in a HardFault exception.

#### 21.4.3.5 PC-relative expressions

A PC-relative expression or **label** is a symbol that represents the address of an instruction or literal data. It is represented in the instruction as the PC value plus or minus a numeric offset. The assembler calculates the required offset from the label and the address of the current instruction. If the offset is too big, the assembler produces an error.

**Remark:**

- For most instructions, the value of the PC is the address of the current instruction plus 4 bytes.
- Your assembler might permit other syntaxes for PC-relative expressions, such as a label plus or minus a number, or an expression of the form [PC, #imm].

### 21.4.3.6 Conditional execution

Most data processing instructions update the condition flags in the **Application Program Status Register** (APSR) according to the result of the operation, see [Section](#) . Some instructions update all flags, and some only update a subset. If a flag is not updated, the original value is preserved. See the instruction descriptions for the flags they affect.

You can execute a conditional branch instruction, based on the condition flags set in another instruction, either:

- immediately after the instruction that updated the flags
- after any number of intervening instructions that have not updated the flags.

On the Cortex-M0 processor, conditional execution is available by using conditional branches.

This section describes:

- [Section 21.4.3.6.1 “The condition flags”](#)
- [Section 21.4.3.6.2 “Condition code suffixes”](#).

#### 21.4.3.6.1 The condition flags

The APSR contains the following condition flags:

**N** — Set to 1 when the result of the operation was negative, cleared to 0 otherwise.

**Z** — Set to 1 when the result of the operation was zero, cleared to 0 otherwise.

**C** — Set to 1 when the operation resulted in a carry, cleared to 0 otherwise.

**V** — Set to 1 when the operation caused overflow, cleared to 0 otherwise.

For more information about the APSR see [Section 21–21.3.1.3.5](#).

A carry occurs:

- if the result of an addition is greater than or equal to  $2^{32}$
- if the result of a subtraction is positive or zero
- as the result of a shift or rotate instruction.

Overflow occurs when the sign of the result, in bit[31], does not match the sign of the result had the operation been performed at infinite precision, for example:

- if adding two negative values results in a positive value
- if adding two positive values results in a negative value
- if subtracting a positive value from a negative value generates a positive value
- if subtracting a negative value from a positive value generates a negative value.

The Compare operations are identical to subtracting, for CMP, or adding, for CMN, except that the result is discarded. See the instruction descriptions for more information.

#### 21.4.3.6.2 Condition code suffixes

Conditional branch is shown in syntax descriptions as B{cond}. A branch instruction with a condition code is only taken if the condition code flags in the APSR meet the specified condition, otherwise the branch instruction is ignored. shows the condition codes to use.

[Table 311](#) also shows the relationship between condition code suffixes and the N, Z, C, and V flags.

**Table 311. Condition code suffixes**

Suffix	Flags	Meaning
EQ	Z = 1	Equal, last flag setting result was zero
NE	Z = 0	Not equal, last flag setting result was non-zero
CS or HS	C = 1	Higher or same, unsigned
CC or LO	C = 0	Lower, unsigned
MI	N = 1	Negative
PL	N = 0	Positive or zero
VS	V = 1	Overflow
VC	V = 0	No overflow
HI	C = 1 and Z = 0	Higher, unsigned
LS	C = 0 or Z = 1	Lower or same, unsigned
GE	N = V	Greater than or equal, signed
LT	N != V	Less than, signed
GT	Z = 0 and N = V	Greater than, signed
LE	Z = 1 and N != V	Less than or equal, signed
AL	Can have any value	Always. This is the default when no suffix is specified.

## 21.4.4 Memory access instructions

[Table 312](#) shows the memory access instructions:

**Table 312. Access instructions**

Mnemonic	Brief description	See
LDR{type}	Load Register using register offset	<a href="#">Section 21–21.4.4.3</a>
LDR	Load Register from PC-relative address	<a href="#">Section 21–21.4.4.4</a>
POP	Pop registers from stack	<a href="#">Section 21–21.4.4.6</a>
PUSH	Push registers onto stack	<a href="#">Section 21–21.4.4.6</a>
STM	Store Multiple registers	<a href="#">Section 21–21.4.4.5</a>
STR{type}	Store Register using immediate offset	<a href="#">Section 21–21.4.4.2</a>
STR{type}	Store Register using register offset	<a href="#">Section 21–21.4.4.3</a>

### 21.4.4.1 ADR

Generates a PC-relative address.

#### 21.4.4.1.1 Syntax

ADR *Rd*, *label*



where:

*Rd* is the destination register.

*label* is a PC-relative expression. See [Section 21–21.4.3.5](#).

#### 21.4.4.1.2 Operation

ADR generates an address by adding an immediate value to the PC, and writes the result to the destination register.

ADR facilitates the generation of position-independent code, because the address is PC-relative.

If you use ADR to generate a target address for a BX or BLX instruction, you must ensure that bit[0] of the address you generate is set to 1 for correct execution.

#### 21.4.4.1.3 Restrictions

In this instruction *Rd* must specify R0-R7. The data-value addressed must be word aligned and within 1020 bytes of the current PC.

#### 21.4.4.1.4 Condition flags

This instruction does not change the flags.

#### 21.4.4.1.5 Examples

```
ADR    R1, TextMessage    ; Write address value of a location labelled as
                           ; TextMessage to R1

ADR    R3, [PC,#996]      ; Set R3 to value of PC + 996.
```

### 21.4.4.2 LDR and STR, immediate offset

Load and Store with immediate offset.

#### 21.4.4.2.1 Syntax

LDR *Rt*, [<*Rn* | SP> {, #*imm*}]

LDR<B|H> *Rt*, [*Rn* {, #*imm*}]

STR *Rt*, [<*Rn* | SP>, {, #*imm*}]

STR<B|H> *Rt*, [*Rn* {, #*imm*}]

where:

*Rt* is the register to load or store.

*Rn* is the register on which the memory address is based.

*imm* is an offset from *Rn*. If *imm* is omitted, it is assumed to be zero.

#### 21.4.4.2.2 Operation

LDR, LDRB and LDRH instructions load the register specified by *Rt* with either a word, byte or halfword data value from memory. Sizes less than word are zero extended to 32-bits before being written to the register specified by *Rt*.

STR, STRB and STRH instructions store the word, least-significant byte or lower halfword contained in the single register specified by *Rt* in to memory. The memory address to load from or store to is the sum of the value in the register specified by either *Rn* or SP and the immediate value *imm*.

#### 21.4.4.2.3 Restrictions

In these instructions:

- *Rt* and *Rn* must only specify R0-R7.
- *imm* must be between:
  - 0 and 1020 and an integer multiple of four for LDR and STR using SP as the base register
  - 0 and 124 and an integer multiple of four for LDR and STR using R0-R7 as the base register
  - 0 and 62 and an integer multiple of two for LDRH and STRH
  - 0 and 31 for LDRB and STRB.
- The computed address must be divisible by the number of bytes in the transaction, see [Section 21–21.4.3.4](#).

#### 21.4.4.2.4 Condition flags

These instructions do not change the flags.

#### 21.4.4.2.5 Examples

```
LDR    R4, [R7                ; Loads R4 from the address in R7.
STR    R2, [R0,#const-struct ; const-struct is an expression evaluating
                                ; to a constant in the range 0-1020.
```

#### 21.4.4.3 LDR and STR, register offset

Load and Store with register offset.

##### 21.4.4.3.1 Syntax

LDR *Rt*, [*Rn*, *Rm*]

LDR<B|H> *Rt*, [*Rn*, *Rm*]

LDR<SB|SH> *Rt*, [*Rn*, *Rm*]

STR *Rt*, [*Rn*, *Rm*]

STR<B|H> *Rt*, [*Rn*, *Rm*]

where:

*Rt* is the register to load or store.

*Rn* is the register on which the memory address is based.

*Rm* is a register containing a value to be used as the offset.

#### 21.4.4.3.2 Operation

LDR, LDRB, U, LDRSB and LDRSH load the register specified by *Rt* with either a word, zero extended byte, zero extended halfword, sign extended byte or sign extended halfword value from memory.

STR, STRB and STRH store the word, least-significant byte or lower halfword contained in the single register specified by *Rt* into memory.

The memory address to load from or store to is the sum of the values in the registers specified by *Rn* and *Rm*.

#### 21.4.4.3.3 Restrictions

In these instructions:

- *Rt*, *Rn*, and *Rm* must only specify R0-R7.
- the computed memory address must be divisible by the number of bytes in the load or store, see [Section 21–21.4.3.4](#).

#### 21.4.4.3.4 Condition flags

These instructions do not change the flags.

#### 21.4.4.3.5 Examples

```
STR    R0, [R5, R1]      ; Store value of R0 into an address equal to
                          ; sum of R5 and R1

LDRSH  R1, [R2, R3]      ; Load a halfword from the memory address
                          ; specified by (R2 + R3), sign extend to 32-bits
                          ; and write to R1.
```

#### 21.4.4.4 LDR, PC-relative

Load register (literal) from memory.

##### 21.4.4.4.1 Syntax

LDR *Rt*, *label*

where:

*Rt* is the register to load.

*label* is a PC-relative expression. See [Section 21–21.4.3.5](#).

##### 21.4.4.4.2 Operation

Loads the register specified by *Rt* from the word in memory specified by *label*.

##### 21.4.4.4.3 Restrictions

In these instructions, *label* must be within 1020 bytes of the current PC and word aligned.

##### 21.4.4.4.4 Condition flags

These instructions do not change the flags.

#### 21.4.4.4.5 Examples

```
LDR    R0, LookUpTable    ; Load R0 with a word of data from an address  
                                ; labelled as LookUpTable.
```

```
LDR    R3, [PC, #100]     ; Load R3 with memory word at (PC + 100).
```

#### 21.4.4.5 LDM and STM

Load and Store Multiple registers.

##### 21.4.4.5.1 Syntax

LDM *Rn{!}*, *reglist*

STM *Rn!*, *reglist*

where:

*Rn* is the register on which the memory addresses are based.

! writeback suffix.

*reglist* is a list of one or more registers to be loaded or stored, enclosed in braces. It can contain register ranges. It must be comma separated if it contains more than one register or register range, see [Section 21–21.4.4.5.5](#).

LDMIA and LDMFD are synonyms for LDM. LDMIA refers to the base register being Incremented After each access. LDMFD refers to its use for popping data from Full Descending stacks.

STMIA and STMEA are synonyms for STM. STMIA refers to the base register being Incremented After each access. STMEA refers to its use for pushing data onto Empty Ascending stacks.

##### 21.4.4.5.2 Operation

LDM instructions load the registers in *reglist* with word values from memory addresses based on *Rn*.

STM instructions store the word values in the registers in *reglist* to memory addresses based on *Rn*.

The memory addresses used for the accesses are at 4-byte intervals ranging from the value in the register specified by *Rn* to the value in the register specified by  $Rn + 4 * (n-1)$ , where *n* is the number of registers in *reglist*. The accesses happens in order of increasing register numbers, with the lowest numbered register using the lowest memory address and the highest number register using the highest memory address. If the writeback suffix is specified, the value in the register specified by  $Rn + 4 * n$  is written back to the register specified by *Rn*.

##### 21.4.4.5.3 Restrictions

In these instructions:

- *reglist* and *Rn* are limited to R0-R7.
- the writeback suffix must always be used unless the instruction is an LDM where *reglist* also contains *Rn*, in which case the writeback suffix must not be used.

- the value in the register specified by *Rn* must be word aligned. See [Section 21–21.4.3.4](#) for more information.
- for STM, if *Rn* appears in *reglist*, then it must be the first register in the list.

#### 21.4.4.5.4 Condition flags

These instructions do not change the flags.

#### 21.4.4.5.5 Examples

```
LDM      R0, {R0,R3,R4}      ; LDMIA is a synonym for LDM
STMIA    R1!, {R2-R4,R6}
```

#### 21.4.4.5.6 Incorrect examples

```
STM      R5!, {R4,R5,R6} ; Value stored for R5 is unpredictable
LDM      R2, {}           ; There must be at least one register in the list
```

### 21.4.4.6 PUSH and POP

Push registers onto, and pop registers off a full-descending stack.

#### 21.4.4.6.1 Syntax

PUSH *reglist*

POP *reglist*

where:

*reglist* is a non-empty list of registers, enclosed in braces. It can contain register ranges. It must be comma separated if it contains more than one register or register range.

#### 21.4.4.6.2 Operation

PUSH stores registers on the stack, with the lowest numbered register using the lowest memory address and the highest numbered register using the highest memory address.

POP loads registers from the stack, with the lowest numbered register using the lowest memory address and the highest numbered register using the highest memory address.

PUSH uses the value in the SP register minus four as the highest memory address,

POP uses the value in the SP register as the lowest memory address, implementing a full-descending stack. On completion,

PUSH updates the SP register to point to the location of the lowest store value,

POP updates the SP register to point to the location above the highest location loaded.

If a POP instruction includes PC in its *reglist*, a branch to this location is performed when the POP instruction has completed. Bit[0] of the value read for the PC is used to update the APSR T-bit. This bit must be 1 to ensure correct operation.

#### 21.4.4.6.3 Restrictions

In these instructions:

- *reglist* must use only R0-R7.

- The exception is LR for a PUSH and PC for a POP.

#### 21.4.4.6.4 Condition flags

These instructions do not change the flags.

#### 21.4.4.6.5 Examples

```
PUSH    {R0,R4-R7}      ; Push R0,R4,R5,R6,R7 onto the stack
PUSH    {R2,LR}          ; Push R2 and the link-register onto the stack
POP     {R0,R6,PC}       ; Pop r0,r6 and PC from the stack, then branch to
                        ; the new PC.
```

### 21.4.5 General data processing instructions

[Table 313](#) shows the data processing instructions:

**Table 313. Data processing instructions**

Mnemonic	Brief description	See
ADCS	Add with Carry	<a href="#">Section 21–21.4.5.1</a>
ADD{S}	Add	<a href="#">Section 21–21.4.5.1</a>
ANDS	Logical AND	<a href="#">Section 21–21.4.5.2</a>
ASRS	Arithmetic Shift Right	<a href="#">Section 21–21.4.5.3</a>
BICS	Bit Clear	<a href="#">Section 21–21.4.5.2</a>
CMN	Compare Negative	<a href="#">Section 21–21.4.5.4</a>
CMP	Compare	<a href="#">Section 21–21.4.5.4</a>
EORS	Exclusive OR	<a href="#">Section 21–21.4.5.2</a>
LSLS	Logical Shift Left	<a href="#">Section 21–21.4.5.3</a>
LSRS	Logical Shift Right	<a href="#">Section 21–21.4.5.3</a>
MOV{S}	Move	<a href="#">Section 21–21.4.5.5</a>
MULS	Multiply	<a href="#">Section 21–21.4.5.6</a>
MVNS	Move NOT	<a href="#">Section 21–21.4.5.5</a>
ORRS	Logical OR	<a href="#">Section 21–21.4.5.2</a>
REV	Reverse byte order in a word	<a href="#">Section 21–21.4.5.7</a>
REV16	Reverse byte order in each halfword	<a href="#">Section 21–21.4.5.7</a>
REVSH	Reverse byte order in bottom halfword and sign extend	<a href="#">Section 21–21.4.5.7</a>
RORS	Rotate Right	<a href="#">Section 21–21.4.5.3</a>
RSBS	Reverse Subtract	<a href="#">Section 21–21.4.5.1</a>
SBCS	Subtract with Carry	<a href="#">Section 21–21.4.5.1</a>
SUBS	Subtract	<a href="#">Section 21–21.4.5.1</a>
SXTB	Sign extend a byte	<a href="#">Section 21–21.4.5.8</a>
SXTH	Sign extend a halfword	<a href="#">Section 21–21.4.5.8</a>
UXTB	Zero extend a byte	<a href="#">Section 21–21.4.5.8</a>
UXTH	Zero extend a halfword	<a href="#">Section 21–21.4.5.8</a>
TST	Test	<a href="#">Section 21–21.4.5.9</a>

### 21.4.5.1 ADC, ADD, RSB, SBC, and SUB

Add with carry, Add, Reverse Subtract, Subtract with carry, and Subtract.

#### 21.4.5.1.1 Syntax

ADCS {*Rd*,} *Rn*, *Rm*

ADD{S} {*Rd*,} *Rn*, <*Rm*|#*imm*>

RSBS {*Rd*,} *Rn*, *Rm*, #0

SBCS {*Rd*,} *Rn*, *Rm*

SUB{S} {*Rd*,} *Rn*,

<*Rm*|#*imm*>

Where:

*S* causes an ADD or SUB instruction to update flags

*Rd* specifies the result register

*Rn* specifies the first source register

*Rm* specifies the second source register

*imm* specifies a constant immediate value.

When the optional *Rd* register specifier is omitted, it is assumed to take the same value as *Rn*, for example ADDS R1,R2 is identical to ADDS R1,R1,R2.

#### 21.4.5.1.2 Operation

The ADCS instruction adds the value in *Rn* to the value in *Rm*, adding a further one if the carry flag is set, places the result in the register specified by *Rd* and updates the N, Z, C, and V flags.

The ADD instruction adds the value in *Rn* to the value in *Rm* or an immediate value specified by *imm* and places the result in the register specified by *Rd*.

The ADDS instruction performs the same operation as ADD and also updates the N, Z, C and V flags.

The RSBS instruction subtracts the value in *Rn* from zero, producing the arithmetic negative of the value, and places the result in the register specified by *Rd* and updates the N, Z, C and V flags.

The SBCS instruction subtracts the value of *Rm* from the value in *Rn*, deducts a further one if the carry flag is set. It places the result in the register specified by *Rd* and updates the N, Z, C and V flags.

The SUB instruction subtracts the value in *Rm* or the immediate specified by *imm*. It places the result in the register specified by *Rd*.

The SUBS instruction performs the same operation as SUB and also updates the N, Z, C and V flags.

Use ADC and SBC to synthesize multiword arithmetic, see [Section 21.4.5.1.4](#).

See also [Section 21–21.4.4.1](#).

### 21.4.5.1.3 Restrictions

[Table 314](#) lists the legal combinations of register specifiers and immediate values that can be used with each instruction.

**Table 314. ADC, ADD, RSB, SBC and SUB operand restrictions**

Instruction	Rd	Rn	Rm	imm	Restrictions
ADCS	R0-R7	R0-R7	R0-R7	-	<i>Rd</i> and <i>Rn</i> must specify the same register.
ADD	R0-R15	R0-R15	R0-PC	-	<i>Rd</i> and <i>Rn</i> must specify the same register. <i>Rn</i> and <i>Rm</i> must not both specify PC.
	R0-R7	SP or PC	-	0-1020	Immediate value must be an integer multiple of four.
	SP	SP	-	0-508	Immediate value must be an integer multiple of four.
ADDS	R0-R7	R0-R7	-	0-7	-
	R0-R7	R0-R7	-	0-255	<i>Rd</i> and <i>Rn</i> must specify the same register.
	R0-R7	R0-R7	R0-R7	-	-
RSBS	R0-R7	R0-R7	-	-	-
SBCS	R0-R7	R0-R7	R0-R7	-	<i>Rd</i> and <i>Rn</i> must specify the same register.
SUB	SP	SP	-	0-508	Immediate value must be an integer multiple of four.
SUBS	R0-R7	R0-R7	-	0-7	-
	R0-R7	R0-R7	-	0-255	<i>Rd</i> and <i>Rn</i> must specify the same register.
	R0-R7	R0-R7	R0-R7	-	-

### 21.4.5.1.4 Examples

The following shows two instructions that add a 64-bit integer contained in R0 and R1 to another 64-bit integer contained in R2 and R3, and place the result in R0 and R1.

#### 64-bit addition:

```
ADDS    R0, R0, R2    ; add the least significant words
ADCS    R1, R1, R3    ; add the most significant words with carry
```

Multiword values do not have to use consecutive registers. The following shows instructions that subtract a 96-bit integer contained in R1, R2, and R3 from another contained in R4, R5, and R6. The example stores the result in R4, R5, and R6.

#### 96-bit subtraction:

```
SUBS    R4, R4, R1    ; subtract the least significant words
SBCS    R5, R5, R2    ; subtract the middle words with carry
SBCS    R6, R6, R3    ; subtract the most significant words with carry
```

The following shows the RSBS instruction used to perform a 1's complement of a single register.

**Arithmetic negation:**     RSBS     R7, R7, #0     ; subtract R7 from zero

### 21.4.5.2 AND, ORR, EOR, and BIC

Logical AND, OR, Exclusive OR, and Bit Clear.



**21.4.5.2.1 Syntax**

ANDS {*Rd*,} *Rn*, *Rm*

ORRS {*Rd*,} *Rn*, *Rm*

EORS {*Rd*,} *Rn*, *Rm*

BICS {*Rd*,} *Rn*, *Rm*

where:

*Rd* is the destination register.

*Rn* is the register holding the first operand and is the same as the destination register.

*Rm* second register.

**21.4.5.2.2 Operation**

The AND, EOR, and ORR instructions perform bitwise AND, exclusive OR, and inclusive OR operations on the values in *Rn* and *Rm*.

The BIC instruction performs an AND operation on the bits in *Rn* with the logical negation of the corresponding bits in the value of *Rm*.

The condition code flags are updated on the result of the operation, see [Section 21.4.3.6.1](#).

**21.4.5.2.3 Restrictions**

In these instructions, *Rd*, *Rn*, and *Rm* must only specify R0-R7.

**21.4.5.2.4 Condition flags**

These instructions:

- update the N and Z flags according to the result
- do not affect the C or V flag.

**21.4.5.2.5 Examples**

```
ANDS    R2, R2, R1
ORRS    R2, R2, R5
ANDS    R5, R5, R8
EORS    R7, R7, R6
BICS    R0, R0, R1
```

**21.4.5.3 ASR, LSL, LSR, and ROR**

Arithmetic Shift Right, Logical Shift Left, Logical Shift Right, and Rotate Right.

**21.4.5.3.1 Syntax**

ASRS {*Rd*,} *Rm*, *Rs*

ASRS {*Rd*,} *Rm*, #*imm*

LSLS {*Rd*,} *Rm*, *Rs*

LSLS {*Rd*,} *Rm*, #*imm*

LSRS {Rd,} *Rm*, *Rs*

LSRS {Rd,} *Rm*, #*imm*

RORS {Rd,} *Rm*, *Rs*

where:

*Rd* is the destination register. If *Rd* is omitted, it is assumed to take the same value as *Rm*.

*Rm* is the register holding the value to be shifted.

*Rs* is the register holding the shift length to apply to the value in *Rm*.

*imm* is the shift length.

The range of shift length depends on the instruction:

**ASR** — shift length from 1 to 32

**LSL** — shift length from 0 to 31

**LSR** — shift length from 1 to 32.

**Remark:** MOVS *Rd*, *Rm* is a pseudonym for LSLS *Rd*, *Rm*, #0.

#### 21.4.5.3.2 Operation

ASR, LSL, LSR, and ROR perform an arithmetic-shift-left, logical-shift-left, logical-shift-right or a right-rotation of the bits in the register *Rm* by the number of places specified by the immediate *imm* or the value in the least-significant byte of the register specified by *Rs*.

For details on what result is generated by the different instructions, see [Section 21–21.4.3.3](#).

#### 21.4.5.3.3 Restrictions

In these instructions, *Rd*, *Rm*, and *Rs* must only specify R0-R7. For non-immediate instructions, *Rd* and *Rm* must specify the same register.

#### 21.4.5.3.4 Condition flags

These instructions update the N and Z flags according to the result.

The C flag is updated to the last bit shifted out, except when the shift length is 0, see [Section 21–21.4.3.3](#). The V flag is left unmodified.

#### 21.4.5.3.5 Examples

```
ASRS    R7, R5, #9 ; Arithmetic shift right by 9 bits
LSLS    R1, R2, #3 ; Logical shift left by 3 bits with flag update
LSRS    R4, R5, #6 ; Logical shift right by 6 bits
RORS    R4, R4, R6 ; Rotate right by the value in the bottom byte of R6.
```

#### 21.4.5.4 CMP and CMN

Compare and Compare Negative.

#### 21.4.5.4.1 Syntax

CMN *Rn*, *Rm*

CMP *Rn*, #*imm*

CMP *Rn*, *Rm*

where:

*Rn* is the register holding the first operand.

*Rm* is the register to compare with.

*imm* is the immediate value to compare with.

#### 21.4.5.4.2 Operation

These instructions compare the value in a register with either the value in another register or an immediate value. They update the condition flags on the result, but do not write the result to a register.

The CMP instruction subtracts either the value in the register specified by *Rm*, or the immediate *imm* from the value in *Rn* and updates the flags. This is the same as a SUBS instruction, except that the result is discarded.

The CMN instruction adds the value of *Rm* to the value in *Rn* and updates the flags. This is the same as an ADDS instruction, except that the result is discarded.

#### 21.4.5.4.3 Restrictions

For the:

- CMN  
instruction *Rn*, and *Rm* must only specify R0-R7.
- CMP instruction:
  - *Rn* and *Rm* can specify R0-R14
  - immediate must be in the range 0-255.

#### 21.4.5.4.4 Condition flags

These instructions update the N, Z, C and V flags according to the result.

#### 21.4.5.4.5 Examples

```
CMP    R2, R9
CMN    R0, R2
```

#### 21.4.5.5 MOV and MVN

Move and Move NOT.

##### 21.4.5.5.1 Syntax

MOV{S} *Rd*, *Rm*

MOVS *Rd*, #*imm*

MVNS *Rd*, *Rm*

where:

*S* is an optional suffix. If *S* is specified, the condition code flags are updated on the result of the operation, see [Section 21–21.4.3.6](#).

*Rd* is the destination register.

*Rm* is a register.

*imm* is any value in the range 0-255.

#### 21.4.5.5.2 Operation

The MOV instruction copies the value of *Rm* into *Rd*.

The MOVS instruction performs the same operation as the MOV instruction, but also updates the N and Z flags.

The MVNS instruction takes the value of *Rm*, performs a bitwise logical negate operation on the value, and places the result into *Rd*.

#### 21.4.5.5.3 Restrictions

In these instructions, *Rd*, and *Rm* must only specify R0-R7.

When *Rd* is the PC in a MOV instruction:

- Bit[0] of the result is discarded.
- A branch occurs to the address created by forcing bit[0] of the result to 0. The T-bit remains unmodified.

**Remark:** Though it is possible to use MOV as a branch instruction, ARM strongly recommends the use of a BX or BLX instruction to branch for software portability.

#### 21.4.5.5.4 Condition flags

If *S* is specified, these instructions:

- update the N and Z flags according to the result
- do not affect the C or V flags.

#### 21.4.5.5.5 Example

```
MOVS R0, #0x000B    ; Write value of 0x000B to R0, flags get updated
MOVS R1, #0x0        ; Write value of zero to R1, flags are updated
MOV  R10, R12        ; Write value in R12 to R10, flags are not updated
MOVS R3, #23         ; Write value of 23 to R3
MOV  R8, SP          ; Write value of stack pointer to R8
MVNS R2, R0          ; Write inverse of R0 to the R2 and update flags
```

#### 21.4.5.6 MULS

Multiply using 32-bit operands, and producing a 32-bit result.

##### 21.4.5.6.1 Syntax

MULS *Rd*, *Rn*, *Rm*

where:

*Rd* is the destination register.

*Rn*, *Rm* are registers holding the values to be multiplied.

#### 21.4.5.6.2 Operation

The MUL instruction multiplies the values in the registers specified by *Rn* and *Rm*, and places the least significant 32 bits of the result in *Rd*. The condition code flags are updated on the result of the operation, see [Section 21–21.4.3.6](#).

The results of this instruction does not depend on whether the operands are signed or unsigned.

#### 21.4.5.6.3 Restrictions

In this instruction:

- *Rd*, *Rn*, and *Rm* must only specify R0-R7
- *Rd* must be the same as *Rm*.

#### 21.4.5.6.4 Condition flags

This instruction:

- updates the N and Z flags according to the result
- does not affect the C or V flags.

#### 21.4.5.6.5 Examples

```
MULS    R0, R2, R0    ; Multiply with flag update, R0 = R0 x R2
```

### 21.4.5.7 REV, REV16, and REVSH

Reverse bytes.

#### 21.4.5.7.1 Syntax

REV *Rd*, *Rn*

REV16 *Rd*, *Rn*

REVSH *Rd*, *Rn*

where:

*Rd* is the destination register.

*Rn* is the source register.

#### 21.4.5.7.2 Operation

Use these instructions to change endianness of data:

**REV** — converts 32-bit big-endian data into little-endian data or 32-bit little-endian data into big-endian data.

**REV16** — converts two packed 16-bit big-endian data into little-endian data or two packed 16-bit little-endian data into big-endian data.

**REVSH** — converts 16-bit signed big-endian data into 32-bit signed little-endian data or 16-bit signed little-endian data into 32-bit signed big-endian data.

#### 21.4.5.7.3 Restrictions

In these instructions, *Rd*, and *Rn* must only specify R0-R7.

#### 21.4.5.7.4 Condition flags

These instructions do not change the flags.

#### 21.4.5.7.5 Examples

```
REV    R3, R7 ; Reverse byte order of value in R7 and write it to R3
REV16  R0, R0 ; Reverse byte order of each 16-bit halfword in R0
REVSH  R0, R5 ; Reverse signed halfword
```

#### 21.4.5.8 SXT and UXT

Sign extend and Zero extend.

##### 21.4.5.8.1 Syntax

SXTB *Rd*, *Rm*

SXTH *Rd*, *Rm*

UXTB *Rd*, *Rm*

UXTH *Rd*, *Rm*

where:

*Rd* is the destination register.

*Rm* is the register holding the value to be extended.

##### 21.4.5.8.2 Operation

These instructions extract bits from the resulting value:

- SXTB extracts bits[7:0] and sign extends to 32 bits
- UXTB extracts bits[7:0] and zero extends to 32 bits
- SXTH extracts bits[15:0] and sign extends to 32 bits
- UXTH extracts bits[15:0] and zero extends to 32 bits.

##### 21.4.5.8.3 Restrictions

In these instructions, *Rd* and *Rm* must only specify R0-R7.

##### 21.4.5.8.4 Condition flags

These instructions do not affect the flags.

#### 21.4.5.8.5 Examples

```

        SXTB  R4, R6          ; Obtain the lower halfword of the
                               ; value in R6 and then sign extend to
                               ; 32 bits and write the result to R4.
        UXTB  R3, R1          ; Extract lowest byte of the value in R10 and zero
                               ; extend it, and write the result to R3

```

#### 21.4.5.9 TST

Test bits.

##### 21.4.5.9.1 Syntax

TST *Rn*, *Rm*

where:

*Rn* is the register holding the first operand.

*Rm* the register to test against.

##### 21.4.5.9.2 Operation

This instruction tests the value in a register against another register. It updates the condition flags based on the result, but does not write the result to a register.

The TST instruction performs a bitwise AND operation on the value in *Rn* and the value in *Rm*. This is the same as the ANDS instruction, except that it discards the result.

To test whether a bit of *Rn* is 0 or 1, use the TST instruction with a register that has that bit set to 1 and all other bits cleared to 0.

##### 21.4.5.9.3 Restrictions

In these instructions, *Rn* and *Rm* must only specify R0-R7.

##### 21.4.5.9.4 Condition flags

This instruction:

- updates the N and Z flags according to the result
- does not affect the C or V flags.

##### 21.4.5.9.5 Examples

```

        TST   R0, R1          ; Perform bitwise AND of R0 value and R1 value,
                               ; condition code flags are updated but result is discarded

```

### 21.4.6 Branch and control instructions

[Table 315](#) shows the branch and control instructions:

**Table 315. Branch and control instructions**

Mnemonic	Brief description	See
B{cc}	Branch {conditionally}	<a href="#">Section 21–21.4.6.1</a>

Table 315. Branch and control instructions

Mnemonic	Brief description	See
BL	Branch with Link	<a href="#">Section 21–21.4.6.1</a>
BLX	Branch indirect with Link	<a href="#">Section 21–21.4.6.1</a>
BX	Branch indirect	<a href="#">Section 21–21.4.6.1</a>

### 21.4.6.1 B, BL, BX, and BLX

Branch instructions.

#### 21.4.6.1.1 Syntax

*B{cond} label*

*BL label*

*BX Rm*

*BLX Rm*

where:

*cond* is an optional condition code, see [Section 21–21.4.3.6](#).

*label* is a PC-relative expression. See [Section 21–21.4.3.5](#).

*Rm* is a register providing the address to branch to.

#### 21.4.6.1.2 Operation

All these instructions cause a branch to the address indicated by *label* or contained in the register specified by *Rm*. In addition:

- The BL and BLX instructions write the address of the next instruction to LR, the link register R14.
- The BX and BLX instructions result in a HardFault exception if bit[0] of *Rm* is 0.

BL and BLX instructions also set bit[0] of the LR to 1. This ensures that the value is suitable for use by a subsequent POP {PC} or BX instruction to perform a successful return branch.

[Table 316](#) shows the ranges for the various branch instructions.

Table 316. Branch ranges

Instruction	Branch range
<i>B label</i>	–2 KB to +2 KB
<i>Bcond label</i>	–256 bytes to +254 bytes
<i>BL label</i>	–16 MB to +16 MB
<i>BX Rm</i>	Any value in register
<i>BLX Rm</i>	Any value in register

#### 21.4.6.1.3 Restrictions

In these instructions:

- Do not use SP or PC in the BX or BLX instruction.



- For BX and BLX, bit[0] of *Rm* must be 1 for correct execution. Bit[0] is used to update the EPSR T-bit and is discarded from the target address.

**Remark:** *Bcond* is the only conditional instruction on the Cortex-M0 processor.

#### 21.4.6.1.4 Condition flags

These instructions do not change the flags.

#### 21.4.6.1.5 Examples

```

B      loopA ; Branch to loopA
BL     funC  ; Branch with link (Call) to function funC, return address
          ; stored in LR
BX     LR    ; Return from function call
BLX    R0    ; Branch with link and exchange (Call) to a address stored
          ; in R0

BEQ     labelD ; Conditionally branch to labelD if last flag setting
          ; instruction set the Z flag, else do not branch.

```

### 21.4.7 Miscellaneous instructions

[Table 317](#) shows the remaining Cortex-M0 instructions:

**Table 317. Miscellaneous instructions**

Mnemonic	Brief description	See
BKPT	Breakpoint	<a href="#">Section 21–21.4.7.1</a>
CPSID	Change Processor State, Disable Interrupts	<a href="#">Section 21–21.4.7.2</a>
CPSIE	Change Processor State, Enable Interrupts	<a href="#">Section 21–21.4.7.2</a>
DMB	Data Memory Barrier	<a href="#">Section 21–21.4.7.3</a>
DSB	Data Synchronization Barrier	<a href="#">Section 21–21.4.7.4</a>
ISB	Instruction Synchronization Barrier	<a href="#">Section 21–21.4.7.5</a>
MRS	Move from special register to register	<a href="#">Section 21–21.4.7.6</a>
MSR	Move from register to special register	<a href="#">Section 21–21.4.7.7</a>
NOP	No Operation	<a href="#">Section 21–21.4.7.8</a>
SEV	Send Event	<a href="#">Section 21–21.4.7.9</a>

Table 317. Miscellaneous instructions

Mnemonic	Brief description	See
SVC	Supervisor Call	<a href="#">Section 21–21.4.7.10</a>
WFE	Wait For Event	<a href="#">Section 21–21.4.7.11</a>
WFI	Wait For Interrupt	<a href="#">Section 21–21.4.7.12</a>

**21.4.7.1 BKPT**

Breakpoint.

**21.4.7.1.1 Syntax**

BKPT #*imm*

where:

*imm* is an integer in the range 0-255.

**21.4.7.1.2 Operation**

The BKPT instruction causes the processor to enter Debug state. Debug tools can use this to investigate system state when the instruction at a particular address is reached. *imm* is ignored by the processor. If required, a debugger can use it to store additional information about the breakpoint.

The processor might also produce a HardFault or go in to lockup if a debugger is not attached when a BKPT instruction is executed. See [Section 21–21.3.4.1](#) for more information.

**21.4.7.1.3 Restrictions**

There are no restrictions.

**21.4.7.1.4 Condition flags**

This instruction does not change the flags.

**21.4.7.1.5 Examples**

```
BKPT #0 ; Breakpoint with immediate value set to 0x0.
```

**21.4.7.2 CPS**

Change Processor State.

**21.4.7.2.1 Syntax**

CPSID *i*

CPSIE *i*

**21.4.7.2.2 Operation**

CPS changes the PRIMASK special register values. CPSID causes interrupts to be disabled by setting PRIMASK. CPSIE cause interrupts to be enabled by clearing PRIMASK. See [Section 21–21.3.1.3.6](#) for more information about these registers.

**21.4.7.2.3 Restrictions**

There are no restrictions.

**21.4.7.2.4 Condition flags**

This instruction does not change the condition flags.

**21.4.7.2.5 Examples**

```
CPSID i ; Disable all interrupts except NMI (set PRIMASK)
```

```
CPSIE i ; Enable interrupts (clear PRIMASK)
```

**21.4.7.3 DMB**

Data Memory Barrier.

**21.4.7.3.1 Syntax**

DMB

**21.4.7.3.2 Operation**

DMB acts as a data memory barrier. It ensures that all explicit memory accesses that appear in program order before the DMB instruction are observed before any explicit memory accesses that appear in program order after the DMB instruction. DMB does not affect the ordering of instructions that do not access memory.

**21.4.7.3.3 Restrictions**

There are no restrictions.

**21.4.7.3.4 Condition flags**

This instruction does not change the flags.

**21.4.7.3.5 Examples**

```
DMB ; Data Memory Barrier
```

**21.4.7.4 DSB**

Data Synchronization Barrier.

**21.4.7.4.1 Syntax**

DSB

**21.4.7.4.2 Operation**

DSB acts as a special data synchronization memory barrier. Instructions that come after the DSB, in program order, do not execute until the DSB instruction completes. The DSB instruction completes when all explicit memory accesses before it complete.

**21.4.7.4.3 Restrictions**

There are no restrictions.

#### 21.4.7.4.4 Condition flags

This instruction does not change the flags.

#### 21.4.7.4.5 Examples

```
DSB ; Data Synchronisation Barrier
```

### 21.4.7.5 ISB

Instruction Synchronization Barrier.

#### 21.4.7.5.1 Syntax

ISB

#### 21.4.7.5.2 Operation

ISB acts as an instruction synchronization barrier. It flushes the pipeline of the processor, so that all instructions following the ISB are fetched from cache or memory again, after the ISB instruction has been completed.

#### 21.4.7.5.3 Restrictions

There are no restrictions.

#### 21.4.7.5.4 Condition flags

This instruction does not change the flags.

#### 21.4.7.5.5 Examples

```
ISB ; Instruction Synchronisation Barrier
```

### 21.4.7.6 MRS

Move the contents of a special register to a general-purpose register.

#### 21.4.7.6.1 Syntax

MRS *Rd*, *spec\_reg*

where:

*Rd* is the general-purpose destination register.

*spec\_reg* is one of the special-purpose registers: APSR, IPSR, EPSR, IEPSR, IAPSR, EAPSR, PSR, MSP, PSP, PRIMASK, or CONTROL.

#### 21.4.7.6.2 Operation

MRS stores the contents of a special-purpose register to a general-purpose register. The MRS instruction can be combined with the MR instruction to produce read-modify-write sequences, which are suitable for modifying a specific flag in the PSR.

See [Section 21–21.4.7.7](#).

#### 21.4.7.6.3 Restrictions

In this instruction, *Rd* must not be SP or PC.

#### 21.4.7.6.4 Condition flags

This instruction does not change the flags.

#### 21.4.7.6.5 Examples

```
MRS R0, PRIMASK ; Read PRIMASK value and write it to R0
```

#### 21.4.7.7 MSR

Move the contents of a general-purpose register into the specified special register.

##### 21.4.7.7.1 Syntax

MSR *spec\_reg*, *Rn*

where:

*Rn* is the general-purpose source register.

*spec\_reg* is the special-purpose destination register: APSR, IPSR, EPSR, IEPSR, IAPSR, EAPSR, PSR, MSP, PSP, PRIMASK, or CONTROL.

##### 21.4.7.7.2 Operation

MSR updates one of the special registers with the value from the register specified by *Rn*.

See [Section 21–21.4.7.6](#).

##### 21.4.7.7.3 Restrictions

In this instruction, *Rn* must not be SP and must not be PC.

##### 21.4.7.7.4 Condition flags

This instruction updates the flags explicitly based on the value in *Rn*.

##### 21.4.7.7.5 Examples

```
MSR CONTROL, R1 ; Read R1 value and write it to the CONTROL register
```

#### 21.4.7.8 NOP

No Operation.

##### 21.4.7.8.1 Syntax

NOP

##### 21.4.7.8.2 Operation

NOP performs no operation and is not guaranteed to be time consuming. The processor might remove it from the pipeline before it reaches the execution stage.

Use NOP for padding, for example to place the subsequent instructions on a 64-bit boundary.

##### 21.4.7.8.3 Restrictions

There are no restrictions.

#### 21.4.7.8.4 Condition flags

This instruction does not change the flags.

#### 21.4.7.8.5 Examples

```
NOP ; No operation
```

#### 21.4.7.9 SEV

Send Event.

##### 21.4.7.9.1 Syntax

SEV

##### 21.4.7.9.2 Operation

SEV causes an event to be signaled to all processors within a multiprocessor system. It also sets the local event register, see [Section 21–21.3.5](#).

See also [Section 21–21.4.7.11](#).

##### 21.4.7.9.3 Restrictions

There are no restrictions.

##### 21.4.7.9.4 Condition flags

This instruction does not change the flags.

##### 21.4.7.9.5 Examples

```
SEV ; Send Event
```

#### 21.4.7.10 SVC

Supervisor Call.

##### 21.4.7.10.1 Syntax

SVC #*imm*

where:

*imm* is an integer in the range 0-255.

##### 21.4.7.10.2 Operation

The SVC instruction causes the SVC exception.

*imm* is ignored by the processor. If required, it can be retrieved by the exception handler to determine what service is being requested.

##### 21.4.7.10.3 Restrictions

There are no restrictions.

##### 21.4.7.10.4 Condition flags

This instruction does not change the flags.

#### 21.4.7.10.5 Examples

```
SVC #0x32 ; Supervisor Call (SVC handler can extract the immediate value  
; by locating it via the stacked PC)
```

#### 21.4.7.11 WFE

Wait For Event.

**Remark:** The WFE instruction is not implemented on the LPC111x/LPC11Cxx

##### 21.4.7.11.1 Syntax

WFE

##### 21.4.7.11.2 Operation

If the event register is 0, WFE suspends execution until one of the following events occurs:

- an exception, unless masked by the exception mask registers or the current priority level
- an exception enters the Pending state, if SEVONPEND in the System Control Register is set
- a Debug Entry request, if debug is enabled
- an event signaled by a peripheral or another processor in a multiprocessor system using the SEV instruction.

If the event register is 1, WFE clears it to 0 and completes immediately.

For more information see [Section 21–21.3.5](#).

**Remark:** WFE is intended for power saving only. When writing software assume that WFE might behave as NOP.

##### 21.4.7.11.3 Restrictions

There are no restrictions.

##### 21.4.7.11.4 Condition flags

This instruction does not change the flags.

##### 21.4.7.11.5 Examples

```
WFE ; Wait for event
```

#### 21.4.7.12 WFI

Wait for Interrupt.

##### 21.4.7.12.1 Syntax

WFI

**21.4.7.12.2 Operation**

WFI

suspends execution until one of the following events occurs:

- an exception
- an interrupt becomes pending which would preempt if PRIMASK was clear
- a Debug Entry request, regardless of whether debug is enabled.

**Remark:** WFI is intended for power saving only. When writing software assume that WFI might behave as a NOP operation.

**21.4.7.12.3 Restrictions**

There are no restrictions.

**21.4.7.12.4 Condition flags**

This instruction does not change the flags.

**21.4.7.12.5 Examples**

```
WFI ; Wait for interrupt
```

## 21.5 Peripherals

**21.5.1 About the ARM Cortex-M0**

The address map of the **Private peripheral bus** (PPB) is:

**Table 318. Core peripheral register regions**

Address	Core peripheral	Description
0xE000E008-0xE000E00F	System Control Block	<a href="#">Table 21–327</a>
0xE000E010-0xE000E01F	System timer	<a href="#">Table 21–336</a>
0xE000E100-0xE000E4EF	Nested Vectored Interrupt Controller	<a href="#">Table 21–319</a>
0xE000ED00-0xE000ED3F	System Control Block	<a href="#">Table 21–327</a>
0xE000EF00-0xE000EF03	Nested Vectored Interrupt Controller	<a href="#">Table 21–319</a>

In register descriptions, the register **type** is described as follows:

**RW** — Read and write.

**RO** — Read-only.

**WO** — Write-only.

**21.5.2 Nested Vectored Interrupt Controller**

This section describes the **Nested Vectored Interrupt Controller** (NVIC) and the registers it uses. The NVIC supports:

- 32 interrupts.



- A programmable priority level of 0-3 for each interrupt. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Interrupt tail-chaining.
- An external **Non-Maskable Interrupt** (NMI).

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling. The hardware implementation of the NVIC registers is:

**Table 319. NVIC register summary**

Address	Name	Type	Reset value	Description
0xE000E100	ISER	RW	0x00000000	<a href="#">Section 21–21.5.2.2</a>
0xE000E180	ICER	RW	0x00000000	<a href="#">Section 21–21.5.2.3</a>
0xE000E200	ISPR	RW	0x00000000	<a href="#">Section 21–21.5.2.4</a>
0xE000E280	ICPR	RW	0x00000000	<a href="#">Section 21–21.5.2.5</a>
0xE000E400–0xE000E41C	IPR0-7	RW	0x00000000	<a href="#">Section 21–21.5.2.6</a>

### 21.5.2.1 Accessing the Cortex-M0 NVIC registers using CMSIS

CMSIS functions enable software portability between different Cortex-M profile processors.

To access the NVIC registers when using CMSIS, use the following functions:

**Table 320. CMSIS access NVIC functions**

CMSIS function	Description
void NVIC_EnableIRQ(IRQn_Type IRQn) <sup>[1]</sup>	Enables an interrupt or exception.
void NVIC_DisableIRQ(IRQn_Type IRQn) <sup>[1]</sup>	Disables an interrupt or exception.
void NVIC_SetPendingIRQ(IRQn_Type IRQn) <sup>[1]</sup>	Sets the pending status of interrupt or exception to 1.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn) <sup>[1]</sup>	Clears the pending status of interrupt or exception to 0.
uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn) <sup>[1]</sup>	Reads the pending status of interrupt or exception. This function returns non-zero value if the pending status is set to 1.
void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority) <sup>[1]</sup>	Sets the priority of an interrupt or exception with configurable priority level to 1.
uint32_t NVIC_GetPriority(IRQn_Type IRQn) <sup>[1]</sup>	Reads the priority of an interrupt or exception with configurable priority level. This function returns the current priority level.

[1] The input parameter IRQn is the IRQ number, see [Table 306](#) for more information.

### 21.5.2.2 Interrupt Set-enable Register

The ISER enables interrupts, and shows which interrupts are enabled. See the register summary in [Table 319](#) for the register attributes.

The bit assignments are:

Table 321. ISER bit assignments

Bits	Name	Function
[31:0]	SETENA	Interrupt set-enable bits. Write: 0 = no effect 1 = enable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

### 21.5.2.3 Interrupt Clear-enable Register

The ICER disables interrupts, and show which interrupts are enabled. See the register summary in [Table 21–319](#) for the register attributes.

The bit assignments are:

Table 322. ICER bit assignments

Bits	Name	Function
[31:0]	CLRENA	Interrupt clear-enable bits. Write: 0 = no effect 1 = disable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.

### 21.5.2.4 Interrupt Set-pending Register

The ISPR forces interrupts into the pending state, and shows which interrupts are pending. See the register summary in [Table 21–319](#) for the register attributes.

The bit assignments are:

Table 323. ISPR bit assignments

Bits	Name	Function
[31:0]	SETPEND	Interrupt set-pending bits. Write: 0 = no effect 1 = changes interrupt state to pending. Read: 0 = interrupt is not pending 1 = interrupt is pending.

**Remark:** Writing 1 to the ISPR bit corresponding to:

- an interrupt that is pending has no effect

- a disabled interrupt sets the state of that interrupt to pending.

21.5.2.5 Interrupt Clear-pending Register

The ICPR removes the pending state from interrupts, and shows which interrupts are pending. See the register summary in [Table 21–319](#) for the register attributes.

The bit assignments are:

Table 324. ICPR bit assignments

Bits	Name	Function
[31:0]	CLRPEND	Interrupt clear-pending bits. Write: 0 = no effect 1 = removes pending state an interrupt. Read: 0 = interrupt is not pending 1 = interrupt is pending.

**Remark:** Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt.

21.5.2.6 Interrupt Priority Registers

The IPR0-IPR7 registers provide an 2-bit priority field for each interrupt. These registers are only word-accessible. See the register summary in [Table 21–319](#) for their attributes. Each register holds four priority fields as shown:

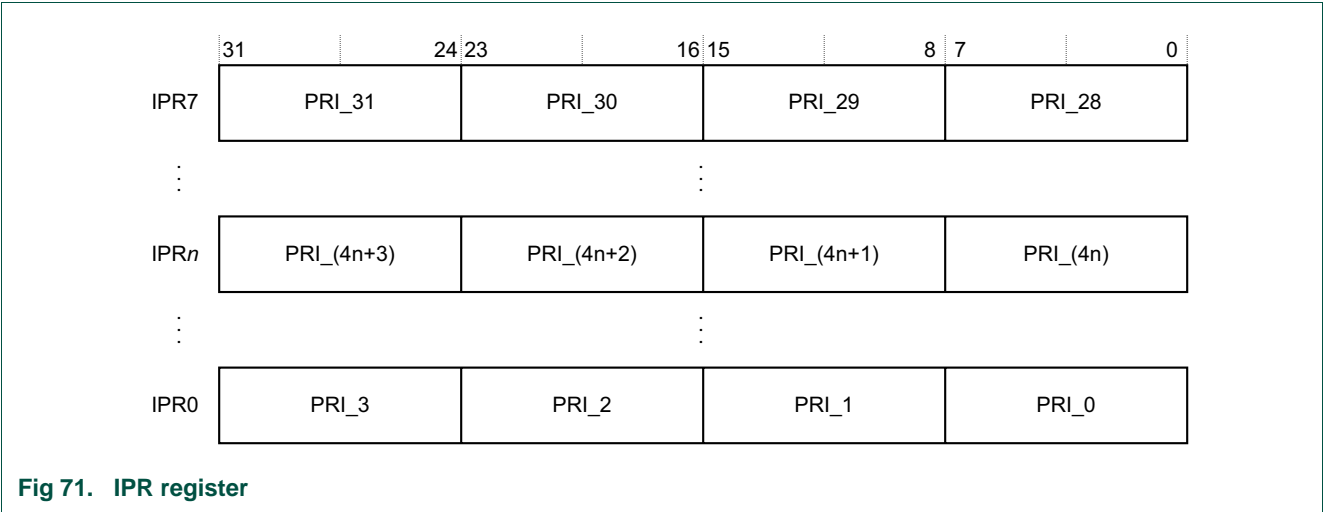


Fig 71. IPR register

Table 325. IPR bit assignments

Bits	Name	Function
[31:24]	Priority, byte offset 3	Each priority field holds a priority value, 0-3. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[7:6] of each field, bits [5:0] read as zero and ignore writes.
[23:16]	Priority, byte offset 2	
[15:8]	Priority, byte offset 1	
[7:0]	Priority, byte offset 0	

See [Section 21–21.5.2.1](#) for more information about the access to the interrupt priority array, which provides the software view of the interrupt priorities.

Find the IPR number and byte offset for interrupt **M** as follows:

- the corresponding IPR number, **N**, is given by  $N = M \text{ DIV } 4$
- the byte offset of the required Priority field in this register is  $M \text{ MOD } 4$ , where:
  - byte offset 0 refers to register bits[7:0]
  - byte offset 1 refers to register bits[15:8]
  - byte offset 2 refers to register bits[23:16]
  - byte offset 3 refers to register bits[31:24].

### 21.5.2.7 Level-sensitive and pulse interrupts

The processor supports both level-sensitive and pulse interrupts. Pulse interrupts are also described as edge-triggered interrupts.

A level-sensitive interrupt is held asserted until the peripheral deasserts the interrupt signal. Typically this happens because the ISR accesses the peripheral, causing it to clear the interrupt request. A pulse interrupt is an interrupt signal sampled synchronously on the rising edge of the processor clock. To ensure the NVIC detects the interrupt, the peripheral must assert the interrupt signal for at least one clock cycle, during which the NVIC detects the pulse and latches the interrupt.

When the processor enters the ISR, it automatically removes the pending state from the interrupt, see [Section 21.5.2.7.1](#). For a level-sensitive interrupt, if the signal is not deasserted before the processor returns from the ISR, the interrupt becomes pending again, and the processor must execute its ISR again. This means that the peripheral can hold the interrupt signal asserted until it no longer needs servicing.

#### 21.5.2.7.1 Hardware and software control of interrupts

The Cortex-M0 latches all interrupts. A peripheral interrupt becomes pending for one of the following reasons:

- the NVIC detects that the interrupt signal is active and the corresponding interrupt is not active
- the NVIC detects a rising edge on the interrupt signal
- software writes to the corresponding interrupt set-pending register bit, see [Section 21–21.5.2.4](#).

A pending interrupt remains pending until one of the following:

- The processor enters the ISR for the interrupt. This changes the state of the interrupt from pending to active. Then:
  - For a level-sensitive interrupt, when the processor returns from the ISR, the NVIC samples the interrupt signal. If the signal is asserted, the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR. Otherwise, the state of the interrupt changes to inactive.

- For a pulse interrupt, the NVIC continues to monitor the interrupt signal, and if this is pulsed the state of the interrupt changes to pending and active. In this case, when the processor returns from the ISR the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR.  
If the interrupt signal is not pulsed while the processor is in the ISR, when the processor returns from the ISR the state of the interrupt changes to inactive.
- Software writes to the corresponding interrupt clear-pending register bit.  
For a level-sensitive interrupt, if the interrupt signal is still asserted, the state of the interrupt does not change. Otherwise, the state of the interrupt changes to inactive.  
For a pulse interrupt, state of the interrupt changes to:
  - inactive, if the state was pending
  - active, if the state was active and pending.

### 21.5.2.8 NVIC usage hints and tips

Ensure software uses correctly aligned register accesses. The processor does not support unaligned accesses to NVIC registers.

An interrupt can enter pending state even if it is disabled. Disabling an interrupt only prevents the processor from taking that interrupt.

### 21.5.2.8.1 NVIC programming hints

Software uses the `CPSIE i` and `CPSID i` instructions to enable and disable interrupts. The CMSIS provides the following intrinsic functions for these instructions:

```
void __disable_irq(void) // Disable Interrupts

void __enable_irq(void) // Enable Interrupts
```

In addition, the CMSIS provides a number of functions for NVIC control, including:

**Table 326. CMSIS functions for NVIC control**

CMSIS interrupt control function	Description
<code>void NVIC_EnableIRQ(IRQn_t IRQn)</code>	Enable IRQn
<code>void NVIC_DisableIRQ(IRQn_t IRQn)</code>	Disable IRQn
<code>uint32_t NVIC_GetPendingIRQ (IRQn_t IRQn)</code>	Return true (1) if IRQn is pending
<code>void NVIC_SetPendingIRQ (IRQn_t IRQn)</code>	Set IRQn pending
<code>void NVIC_ClearPendingIRQ (IRQn_t IRQn)</code>	Clear IRQn pending status
<code>void NVIC_SetPriority (IRQn_t IRQn, uint32_t priority)</code>	Set priority for IRQn
<code>uint32_t NVIC_GetPriority (IRQn_t IRQn)</code>	Read priority of IRQn
<code>void NVIC_SystemReset (void)</code>	Reset the system

The input parameter `IRQn` is the IRQ number, see [Table 21–306](#) for more information. For more information about these functions, see the CMSIS documentation.

## 21.5.3 System Control Block

The **System Control Block** (SCB) provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. The SCB registers are:

**Table 327. Summary of the SCB registers**

Address	Name	Type	Reset value	Description
0xE00ED00	CPUID	RO	0x410CC200	<a href="#">Section 21.5.3.2</a>
0xE00ED04	ICSR	RW <sup>[1]</sup>	0x00000000	<a href="#">Section 21–21.5.3.3</a>
0xE00ED0C	AIRCR	RW <sup>[1]</sup>	0xFA050000	<a href="#">Section 21–21.5.3.4</a>
0xE00ED10	SCR	RW	0x00000000	<a href="#">Section 21–21.5.3.5</a>
0xE00ED14	CCR	RO	0x00000204	<a href="#">Section 21–21.5.3.6</a>
0xE00ED1C	SHPR2	RW	0x00000000	<a href="#">Section 21–21.5.3.7.1</a>
0xE00ED20	SHPR3	RW	0x00000000	<a href="#">Section 21–21.5.3.7.2</a>

[1] See the register description for more information.

### 21.5.3.1 The CMSIS mapping of the Cortex-M0 SCB registers

To improve software efficiency, the CMSIS simplifies the SCB register presentation. In the CMSIS, the array `SHP[1]` corresponds to the registers SHPR2-SHPR3.

### 21.5.3.2 CPUID Register

The CPUID register contains the processor part number, version, and implementation information. See the register summary in for its attributes. The bit assignments are:

**Table 328. CPUID register bit assignments**

Bits	Name	Function
[31:24]	Implementer	Implementer code: 0x41 = ARM
[23:20]	Variant	Variant number, the r value in the <b>mpn</b> product revision identifier: 0x0 = Revision 0
[19:16]	Constant	Constant that defines the architecture of the processor:, reads as 0xC = ARMv6-M architecture
[15:4]	Partno	Part number of the processor: 0xC20 = Cortex-M0
[3:0]	Revision	Revision number, the p value in the <b>mpn</b> product revision identifier: 0x0 = Patch 0

### 21.5.3.3 Interrupt Control and State Register

The ICSR:

- provides:
  - a set-pending bit for the **Non-Maskable Interrupt** (NMI) exception
  - set-pending and clear-pending bits for the PendSV and SysTick exceptions
- indicates:
  - the exception number of the exception being processed
  - whether there are preempted active exceptions
  - the exception number of the highest priority pending exception

- whether any interrupts are pending.

See the register summary in [Table 21–327](#) for the ICSR attributes. The bit assignments are:

**Table 329. ICSR bit assignments**

Bits	Name	Type	Function
[31]	NMIPENDSET	RW	NMI set-pending bit. Write: 0 = no effect 1 = changes NMI exception state to pending. Read: 0 = NMI exception is not pending 1 = NMI exception is pending. Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30:29]	-	-	Reserved.
[28]	PENDSVSET	RW	PendSV set-pending bit. Write: 0 = no effect 1 = changes PendSV exception state to pending. Read: 0 = PendSV exception is not pending 1 = PendSV exception is pending. Writing 1 to this bit is the only way to set the PendSV exception state to pending.
[27]	PENDSVCLR	WO	PendSV clear-pending bit. Write: 0 = no effect 1 = removes the pending state from the PendSV exception.
[26]	PENDSTSET	RW	SysTick exception set-pending bit. Write: 0 = no effect 1 = changes SysTick exception state to pending. Read: 0 = SysTick exception is not pending 1 = SysTick exception is pending.

Table 329. ICSR bit assignments

Bits	Name	Type	Function
[25]	PENDSTCLR	WO	SysTick exception clear-pending bit. Write: 0 = no effect 1 = removes the pending state from the SysTick exception. This bit is WO. On a register read its value is Unknown.
[24:23]	-	-	Reserved.
[22]	ISRPENDING	RO	Interrupt pending flag, excluding NMI and Faults: 0 = interrupt not pending 1 = interrupt pending.
[21:18]	-	-	Reserved.
[17:12]	VECTPENDING	RO	Indicates the exception number of the highest priority pending enabled exception: 0 = no pending exceptions Nonzero = the exception number of the highest priority pending enabled exception.
[11:6]	-	-	Reserved.
[5:0]	VECTACTIVE <sup>[1]</sup>	RO	Contains the active exception number: 0 = Thread mode Nonzero = The exception number <sup>[1]</sup> of the currently active exception. <b>Remark:</b> Subtract 16 from this value to obtain the CMSIS IRQ number that identifies the corresponding bit in the Interrupt Clear-Enable, Set-Enable, Clear-Pending, Set-pending, and Priority Register, see <a href="#">Table 21–301</a> .

[1] This is the same value as IPSR bits[5:0], see [Table 21–301](#).

When you write to the ICSR, the effect is Unpredictable if you:

- write 1 to the PENDSVSET bit and write 1 to the PENDSVCLR bit
- write 1 to the PENDSTSET bit and write 1 to the PENDSTCLR bit.

#### 21.5.3.4 Application Interrupt and Reset Control Register

The AIRCR provides endian status for data accesses and reset control of the system. See the register summary in [Table 21–327](#) and [Table 21–330](#) for its attributes.

To write to this register, you must write 0x05FA to the VECTKEY field, otherwise the processor ignores the write.

The bit assignments are:



Table 330. AIRCR bit assignments

Bits	Name	Type	Function
[31:16]	Read: Reserved Write: VECTKEY	RW	Register key: Reads as Unknown On writes, write 0x05FA to VECTKEY, otherwise the write is ignored.
[15]	ENDIANESS	RO	Data endianness implemented: 0 = Little-endian 1 = Big-endian.
[14:3]	-	-	Reserved
[2]	SYSRESETREQ	WO	System reset request: 0 = no effect 1 = requests a system level reset. This bit reads as 0.
[1]	VECTCLRACTIVE	WO	Reserved for debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.
[0]	-	-	Reserved.

### 21.5.3.5 System Control Register

The SCR controls features of entry to and exit from low power state. See the register summary in [Table 21–327](#) for its attributes. The bit assignments are:

Table 331. SCR bit assignments

Bits	Name	Function
[31:5]	-	Reserved.
[4]	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wake-up the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wake-up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an <code>SEV</code> instruction.
[3]	-	Reserved.
[2]	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep.
[1]	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	-	Reserved.

### 21.5.3.6 Configuration and Control Register

The CCR is a read-only register and indicates some aspects of the behavior of the Cortex-M0 processor. See the register summary in [Table 21–327](#) for the CCR attributes.

The bit assignments are:

**Table 332. CCR bit assignments**

Bits	Name	Function
[31:10]	-	Reserved.
[9]	STKALIGN	Always reads as one, indicates 8-byte stack alignment on exception entry. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception it uses this stacked bit to restore the correct stack alignment.
[8:4]	-	Reserved.
[3]	UNALIGN_TRP	Always reads as one, indicates that all unaligned accesses generate a HardFault.
[2:0]	-	Reserved.

### 21.5.3.7 System Handler Priority Registers

The SHPR2-SHPR3 registers set the priority level, 0 to 3, of the exception handlers that have configurable priority.

SHPR2-SHPR3 are word accessible. See the register summary in [Table 21–327](#) for their attributes.

To access to the system exception priority level using CMSIS, use the following CMSIS functions:

- `uint32_t NVIC_GetPriority(IRQn_Type IRQn)`
- `void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority)`

The input parameter `IRQn` is the IRQ number, see [Table 21–306](#) for more information.

The system fault handlers, and the priority field and register for each handler are:

**Table 333. System fault handler priority fields**

Handler	Field	Register description
SVCall	PRI_11	<a href="#">Section 21–21.5.3.7.1</a>
PendSV	PRI_14	<a href="#">Section 21–21.5.3.7.2</a>
SysTick	PRI_15	

Each PRI\_N field is 8 bits wide, but the processor implements only bits[7:6] of each field, and bits[5:0] read as zero and ignore writes.

#### 21.5.3.7.1 System Handler Priority Register 2

The bit assignments are:

Table 334. SHPR2 register bit assignments

Bits	Name	Function
[31:24]	PRI_11	Priority of system handler 11, SVCall
[23:0]	-	Reserved

### 21.5.3.7.2 System Handler Priority Register 3

The bit assignments are:

Table 335. SHPR3 register bit assignments

Bits	Name	Function
[31:24]	PRI_15	Priority of system handler 15, SysTick exception
[23:16]	PRI_14	Priority of system handler 14, PendSV
[15:0]	-	Reserved

### 21.5.3.8 SCB usage hints and tips

Ensure software uses aligned 32-bit word size transactions to access all the SCB registers.

### 21.5.4 System timer, SysTick

When enabled, the timer counts down from the current value (SYST\_CVR) to zero, reloads (wraps) to the value in the SysTick Reload Value Register (SYST\_RVR) on the next clock edge, then decrements on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set to 1. The COUNTFLAG bit clears on reads.

**Remark:** The SYST\_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST\_RVR value rather than an arbitrary value when it is enabled.

**Remark:** If the SYST\_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

A write to the SYST\_CVR will clear the register and the COUNTFLAG status bit. The write causes the SYST\_CVR to reload from the SYST\_RVR on the next timer clock, however, it does not trigger the SysTick exception logic. On a read, the current value is the value of the register at the time the register is accessed.

**Remark:** When the processor is halted for debugging the counter does not decrement.

The system timer registers are:

Table 336. System timer registers summary

Address	Name	Type	Reset value	Description
0xE000E010	SYST_CSR	RW	0x00000000	<a href="#">Section 21.5.4.1</a>
0xE000E014	SYST_RVR	RW	Unknown	<a href="#">Section 21–21.5.4.2</a>
0xE000E018	SYST_CVR	RW	Unknown	<a href="#">Section 21–21.5.4.3</a>
0xE000E01C	SYST_CALIB	RO	0x00000004 <sup>[1]</sup>	<a href="#">Section 21–21.5.4.4</a>

[1] SysTick calibration value.

#### 21.5.4.1 SysTick Control and Status Register

The SYST\_CSR enables the SysTick features. See the register summary in [Table 21–336](#) for its attributes. The bit assignments are:

**Table 337. SYST\_CSR bit assignments**

Bits	Name	Function
[31:17]	-	Reserved.
[16]	COUNTFLAG	Returns 1 if timer counted to 0 since the last read of this register.
[15:3]	-	Reserved.
[2]	CLKSOURCE	Selects the SysTick timer clock source: 0 = external reference clock. 1 = processor clock.
[1]	TICKINT	Enables SysTick exception request: 0 = counting down to zero does not assert the SysTick exception request. 1 = counting down to zero asserts the SysTick exception request.
[0]	ENABLE	Enables the counter: 0 = counter disabled. 1 = counter enabled.

#### 21.5.4.2 SysTick Reload Value Register

The SYST\_RVR specifies the start value to load into the SYST\_CVR. See the register summary in [Table 21–336](#) for its attributes. The bit assignments are:

**Table 338. SYST\_RVR bit assignments**

Bits	Name	Function
[31:24]	-	Reserved.
[23:0]	RELOAD	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0, see <a href="#">Section 21.5.4.2.1</a> .

##### 21.5.4.2.1 Calculating the RELOAD value

The RELOAD value can be any value in the range 0x00000001-0x00FFFFFF. You can program a value of 0, but this has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

To generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. For example, if the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.

#### 21.5.4.3 SysTick Current Value Register

The SYST\_CVR contains the current value of the SysTick counter. See the register summary in [Table 21–336](#) for its attributes. The bit assignments are:

Table 339. SYST\_CVR bit assignments

Bits	Name	Function
[31:24]	-	Reserved.
[23:0]	CURRENT	Reads return the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

#### 21.5.4.4 SysTick Calibration Value Register

The SYST\_CALIB register indicates the SysTick calibration properties. See the register summary in [Table 21–336](#) for its attributes. The bit assignments are:

Table 340. SYST\_CALIB register bit assignments

Bits	Name	Function
[31]	NOREF	Reads as one. Indicates that no separate reference clock is provided.
[30]	SKEW	Reads as one. Calibration value for the 10ms inexact timing is not known because TENMS is not known. This can affect the suitability of SysTick as a software real time clock.
[29:24]	-	Reserved.
[23:0]	TENMS	Reads as zero. Indicates calibration value is not known.

If calibration information is not known, calculate the calibration value required from the frequency of the processor clock or external clock.

#### 21.5.4.5 SysTick usage hints and tips

The interrupt controller clock updates the SysTick counter. If this clock signal is stopped for low power mode, the SysTick counter stops.

Ensure software uses word accesses to access the SysTick registers.

If the SysTick counter reload and current value are undefined at reset, the correct initialization sequence for the SysTick counter is:

1. Program reload value.
2. Clear current value.
3. Program Control and Status register.

## 21.6 Cortex-M0 instruction summary

Table 341. Cortex M0- instruction summary

Operation	Description	Assembler	Cycles
Move	8-bit immediate	MOVS Rd, #<imm>	1
	Lo to Lo	MOVS Rd, Rm	1
	Any to Any	MOV Rd, Rm	1
	Any to PC	MOV PC, Rm	3
Add	3-bit immediate	ADDS Rd, Rn, #<imm>	1
	All registers Lo	ADDS Rd, Rn, Rm	1
	Any to Any	ADD Rd, Rd, Rm	1
	Any to PC	ADD PC, PC, Rm	3
Add	8-bit immediate	ADDS Rd, Rd, #<imm>	1
	With carry	ADCS Rd, Rd, Rm	1
	Immediate to SP	ADD SP, SP, #<imm>	1
	Form address from SP	ADD Rd, SP, #<imm>	1
	Form address from PC	ADR Rd, <label>	1
Subtract	Lo and Lo	SUBS Rd, Rn, Rm	1
	3-bit immediate	SUBS Rd, Rn, #<imm>	1
	8-bit immediate	SUBS Rd, Rd, #<imm>	1
	With carry	SBCS Rd, Rd, Rm	1
	Immediate from SP	SUB SP, SP, #<imm>	1
	Negate	RSBS Rd, Rn, #0	1
Multiply	Multiply	MULS Rd, Rm, Rd	1
Compare	Compare	CMP Rn, Rm	1
	Negative	CMN Rn, Rm	1
	Immediate	CMP Rn, #<imm>	1
Logical	AND	ANDS Rd, Rd, Rm	1
	Exclusive OR	EORS Rd, Rd, Rm	1
	OR	ORRS Rd, Rd, Rm	1
	Bit clear	BICS Rd, Rd, Rm	1
	Move NOT	MVNS Rd, Rm	1
	AND test	TST Rn, Rm	1
Shift	Logical shift left by immediate	LSLS Rd, Rm, #<shift>	1
	Logical shift left by register	LSLS Rd, Rd, Rs	1
	Logical shift right by immediate	LSRS Rd, Rm, #<shift>	1
	Logical shift right by register	LSRS Rd, Rd, Rs	1
	Arithmetic shift right	ASRS Rd, Rm, #<shift>	1
	Arithmetic shift right by register	ASRS Rd, Rd, Rs	1
Rotate	Rotate right by register	RORS Rd, Rd, Rs	1

Table 341. Cortex M0- instruction summary

Operation	Description	Assembler	Cycles
Load	Word, immediate offset	LDR Rd, [Rn, #<imm>]	2
	Halfword, immediate offset	LDRH Rd, [Rn, #<imm>]	2
	Byte, immediate offset	LDRB Rd, [Rn, #<imm>]	2
	Word, register offset	LDR Rd, [Rn, Rm]	2
	Halfword, register offset	LDRH Rd, [Rn, Rm]	2
	Signed halfword, register offset	LDRSH Rd, [Rn, Rm]	2
	Byte, register offset	LDRB Rd, [Rn, Rm]	2
	Signed byte, register offset	LDRSB Rd, [Rn, Rm]	2
	PC-relative	LDR Rd, <label>	2
	SP-relative	LDR Rd, [SP, #<imm>]	2
	Multiple, excluding base	LDM Rn!, {<loreglist>}	1 + N <sup>[1]</sup>
	Multiple, including base	LDM Rn, {<loreglist>}	1 + N <sup>[1]</sup>
Store	Word, immediate offset	STR Rd, [Rn, #<imm>]	2
Store	Halfword, immediate offset	STRH Rd, [Rn, #<imm>]	2
	Byte, immediate offset	STRB Rd, [Rn, #<imm>]	2
	Word, register offset	STR Rd, [Rn, Rm]	2
	Halfword, register offset	STRH Rd, [Rn, Rm]	2
	Byte, register offset	STRB Rd, [Rn, Rm]	2
	SP-relative	STR Rd, [SP, #<imm>]	2
	Multiple	STM Rn!, {<loreglist>}	1 + N <sup>[1]</sup>
Push	Push	PUSH {<loreglist>}	1 + N <sup>[1]</sup>
	Push with link register	PUSH {<loreglist>, LR}	1 + N <sup>[1]</sup>
Pop	Pop	POP {<loreglist>}	1 + N <sup>[1]</sup>
	Pop and return	POP {<loreglist>, PC}	4 + N <sup>[2]</sup>
Branch	Conditional	B<cc> <label>	1 or 3 <sup>[3]</sup>
	Unconditional	B <label>	3
	With link	BL <label>	4
	With exchange	BX Rm	3
	With link and exchange	BLX Rm	3
Extend	Signed halfword to word	SXTH Rd, Rm	1
	Signed byte to word	SXTB Rd, Rm	1
	Unsigned halfword	UXTH Rd, Rm	1
	Unsigned byte	UXTB Rd, Rm	1
Reverse	Bytes in word	REV Rd, Rm	1
	Bytes in both halfwords	REV16 Rd, Rm	1
	Signed bottom half word	REVSH Rd, Rm	1
State change	Supervisor Call	SVC <imm>	- <sup>[4]</sup>
	Disable interrupts	CPSID i	1
	Enable interrupts	CPSIE i	1
	Read special register	MRS Rd, <specreg>	4
	Write special register	MSR <specreg>, Rn	4

Table 341. Cortex M0- instruction summary

Operation	Description	Assembler	Cycles
Hint	Send event	SEV	1
	Wait for event	WFE	2 <sup>[5]</sup>
	Wait for interrupt	WFI	2 <sup>[5]</sup>
	Yield	YIELD <sup>[6]</sup>	1
	No operation	NOP	1
Barriers	Instruction synchronization	ISB	4
	Data memory	DMB	4
	Data synchronization	DSB	4

[1] N is the number of elements.

[2] N is the number of elements in the stack-pop list including PC and assumes load or store does not generate a HardFault exception.

[3] 3 if taken, 1 if not taken.

[4] Cycle count depends on core and debug configuration.

[5] Excludes time spend waiting for an interrupt or event.

[6] Executes as NOP.



## 22.1 Abbreviations

Table 342. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

## 22.2 References

- [1] **ARM DUI 0497A** — Cortex-M0 Devices Generic User Guide
- [2] **ARM DDI 0432C** — Cortex-M0 Revision r0p0 Technical Reference Manual

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