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# Multichannel, True-Differential, Serial, 14-Bit ADCs

## General Description

The MAX1146–MAX1149 low-power, 14-bit, multichannel, analog-to-digital converters (ADCs) feature an internal track/hold (T/H), voltage reference, and clock. The MAX1146/MAX1148 operate from a single +4.75V to +5.25V supply, and the MAX1147/MAX1149 operate from a single +2.7V to +3.6V supply. All analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™/MICROWIRE™ devices without external logic. The serial strobe output (SSTRB) allows convenient connection to digital signal processors. The MAX1146–MAX1149 use an internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX1146/MAX1148 include an internal +4.096V reference, while the MAX1147/MAX1149 include an internal +2.500V reference. All devices accept an external reference from 1.5V to V<sub>DD</sub>.

The MAX1146–MAX1149 provide a hardware shutdown and two software power-down modes. Using the software power-down modes allows the devices to be powered down between conversions. When powered down, accessing the serial interface automatically powers up the devices. The quick turn-on time allows power-down between all conversions. This technique reduces supply current to under 120µA for quick turn-on.

The MAX1146–MAX1149 are available in a 20-pin TSSOP package.

## Applications

Portable Data Logging

Data Acquisition

Medical Instruments

Battery-Powered Instruments

Process Control

## Features

- ◆ 8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1148/MAX1149)
- ◆ 4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1146/MAX1147)
- ◆ Internal Multiplexer and T/H
- ◆ Single-Supply Operation
  - 4.75V to 5.25V Supply (MAX1146/MAX1148)
  - 2.7V to 3.6V Supply (MAX1147/MAX1149)
- ◆ Internal Reference
  - +4.096V (MAX1146/MAX1148)
  - +2.500V (MAX1147/MAX1149)
- ◆ 116ksps Sampling Rate
- ◆ Low Power
  - 1.1mA (116ksps)
  - 120µA (10ksps)
  - 12µA (1ksps)
  - 300nA (Power-Down Mode)
- ◆ SPI-/QSPI-/MICROWIRE Compatible
- ◆ 20-Pin TSSOP

*Pin Configurations appear at end of data sheet.*

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

**MAX1146–MAX1149**

## Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)	INPUT CHANNELS	INTERNAL REFERENCE (V)
MAX1146BCUP	0°C to +70°C	20 TSSOP	±2	4	+4.096
MAX1146BEUP	-40°C to +85°C	20 TSSOP	±2	4	+4.096
MAX1147BCUP	0°C to +70°C	20 TSSOP	±2	4	+2.500
MAX1147BEUP	-40°C to +85°C	20 TSSOP	±2	4	+2.500
MAX1148BCUP	0°C to +70°C	20 TSSOP	±2	8	+4.096
MAX1148BEUP	-40°C to +85°C	20 TSSOP	±2	8	+4.096
MAX1149BCUP	0°C to +70°C	20 TSSOP	±2	8	+2.500
MAX1149BEUP	-40°C to +85°C	20 TSSOP	±2	8	+2.500

**MAXIM**

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

# Multichannel, True-Differential, Serial, 14-Bit ADCs

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to AGND, DGND	-0.3V to +6.0V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
AGND to DGND	-0.3V to +0.3V	20 TSSOP (derate 10.9mW/°C above +70°C) .....879mW
CH0-CH7, COM to AGND	-0.3V to (V <sub>DD</sub> + 0.3V)	Operating Temperature Ranges
REF, REFADJ to AGND	-0.3V to (V <sub>DD</sub> + 0.3V)	MAX114 <sub>—</sub> BC <sub>—</sub> .....0°C to +70°C
Digital Inputs to DGND	-0.3V to (V <sub>DD</sub> + 0.3V)	MAX114 <sub>—</sub> BE <sub>—</sub> .....-40°C to +85°C
Digital Outputs to DGND	-0.3V to (V <sub>DD</sub> + 0.3V)	Storage Temperature Range .....-60°C to +150°C
Digital Output Sink Current	25mA	Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 5V (MAX1146/MAX1148), V<sub>DD</sub> = 3.3V (MAX1147/MAX1149),  $\overline{\text{SHDN}} = \text{V}_{\text{DD}}$ , V<sub>COM</sub> = 0, f<sub>SCLK</sub> = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V<sub>REFADJ</sub> = V<sub>DD</sub>, C<sub>REF</sub> = 2.2 $\mu$ F, external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY (Note 1)</b>						
Resolution			14			Bits
Relative Accuracy (Note 2)	INL			$\pm 0.7$	$\pm 2$	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-1.0	$\pm 0.5$	$+1.5$	LSB
Offset Error					$\pm 10$	LSB
Offset Temperature Coefficient				0.3		ppm/°C
Gain Error		(Note 3)			$\pm 20$	LSB
Gain Temperature Coefficient				$\pm 0.8$		ppm/°C
Channel-to-Channel Offset Matching				$\pm 1$		LSB
Channel-to-Channel Gain Matching				$\pm 1$		LSB
<b>DYNAMIC SPECIFICATIONS (1kHz sine-wave input, 2.5Vp-p, full-scale analog input, 116ksps, 2.1MHz external clock)</b>						
Signal-to-Noise Plus Distortion Ratio	SINAD		77	81		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-96	-88	dB
Spurious-Free Dynamic Range	SFDR		84	98		dB
Channel-to-Channel Crosstalk		(Note 4)		-85		dB
Small-Signal Bandwidth	SSBW	-3dB point		3.0		MHz
Full-Power Bandwidth	FPBW	SINAD > 68dB		2.0		MHz
<b>CONVERSION RATE</b>						
Conversion Time (Note 5)	t <sub>CONV</sub>	External clock, 2.1MHz 15 SCLK cycles	7.2			$\mu$ s
		Internal clock	6	8		

# Multichannel, True-Differential, Serial, 14-Bit ADCs

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 5V (MAX1146/MAX1148), V<sub>DD</sub> = 3.3V (MAX1147/MAX1149),  $\overline{\text{SHDN}} = \text{V}_{\text{DD}}$ , V<sub>COM</sub> = 0, f<sub>SCLK</sub> = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V<sub>REFADJ</sub> = V<sub>DD</sub>, C<sub>REF</sub> = 2.2 $\mu$ F, external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Throughput Rate	f <sub>SAMPLE</sub>	Internal clock mode, f <sub>SCLK</sub> = 2.1MHz	18 clocks/conversion	60.3		ksps
			24 clocks/conversion	51.5		
		External clock mode, f <sub>SCLK</sub> = 2.1MHz	18 clocks/conversion	116.66		
			24 clocks/conversion	87.50		
T/H Acquisition Time	t <sub>ACQ</sub>		1.4			$\mu$ s
Aperture Delay	t <sub>AD</sub>			20		ns
Aperture Jitter	t <sub>AJ</sub>			<50		ps
Serial Clock Frequency	f <sub>SCLK</sub>	External clock mode	0.1	2.1		MHz
		Internal clock mode	0	2.1		
Internal Clock Frequency				2.1		MHz
<b>ANALOG INPUTS (CH0–CH7, COM)</b>						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0	0	V <sub>REF</sub>		V
		Bipolar, COM = V <sub>REF</sub> / 2, single-ended		$\pm V_{\text{REF}} / 2$		
Multiplexer Leakage Current		On/off-leakage current, V <sub>CH</sub> = 0 to V <sub>DD</sub>		$\pm 0.01$	$\pm 1$	$\mu$ A
Input Capacitance				18		pF
<b>INTERNAL REFERENCE (C<sub>REF</sub> = 2.2<math>\mu</math>F, C<sub>REFADJ</sub> = 0.01<math>\mu</math>F)</b>						
REF Output Voltage	V <sub>REF</sub>	MAX1147/MAX1149, T <sub>A</sub> = +25°C	2.480	2.500	2.520	V
		MAX1146/MAX1148, T <sub>A</sub> = +25°C	4.076	4.096	4.116	
REF Short-Circuit Current	I <sub>REFSC</sub>	REF = DGND		20		mA
V <sub>REF</sub> Tempco (Note 7)		MAX114_BC __		$\pm 30$	$\pm 50$	ppm/°C
		MAX114_BE __		$\pm 40$	$\pm 60$	
Load Regulation		0 to 0.2mA output load (Note 8)		2.0		mV
Capacitive Bypass at REF			2			$\mu$ F
Capacitive Bypass at REFADJ			0.01			$\mu$ F
REFADJ Output Voltage				1.250		V
REFADJ Input Range				$\pm 18$		mV
REFADJ Logic High		Pull REFADJ high to disable the internal bandgap reference and reference buffer	V <sub>DD</sub> - 0.25V			V
Reference Buffer Voltage Gain		MAX1147/MAX1149	2.000			V/V
		MAX1146/MAX1148	3.277			

**MAX1146–MAX1149**

# Multichannel, True-Differential, Serial, 14-Bit ADCs

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 5V$  (MAX1146/MAX1148),  $V_{DD} = 3.3V$  (MAX1147/MAX1149),  $\overline{SHDN} = V_{DD}$ ,  $V_{COM} = 0$ ,  $f_{SCLK} = 2.1MHz$ , external clock (50% duty cycle), 18 clocks/conversion (116ksps),  $V_{REFADJ} = V_{DD}$ ,  $C_{REF} = 2.2\mu F$ , external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
<b>EXTERNAL REFERENCE AT REF</b>								
REF Input Voltage Range	$V_{REF}$		1.5	$V_{DD} + 50mV$		V		
REF Input Current	$I_{REF}$		125	450		$\mu A$		
		Shutdown	0.01	10				
REF Input Resistance			6	8		$k\Omega$		
<b>DIGITAL INPUTS (DIN, SCLK, CS, SHDN)</b>								
Input High Voltage	$V_{IH}$	$V_{DD} < 3.6V$	2.0			V		
		$V_{DD} > 3.6V$	3.0					
Input Low Voltage	$V_{IL}$			0.8		V		
Input Hysteresis	$V_{HYST}$			0.2		V		
Input Leakage	$I_{IN}$			$\pm 1$		$\mu A$		
Input Capacitance	$C_{IN}$			10		pF		
<b>DIGITAL OUTPUT (DOUT, SSTRB)</b>								
Output-Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$		0.4		V		
Output-Voltage High	$V_{OH}$	$I_{SOURCE} = 2mA$		$V_{DD} - 0.5$		V		
Tri-State Leakage Current	$I_L$	$CS = V_{DD}$		$\pm 10$		$\mu A$		
Tri-State Output Capacitance	$C_{OUT}$	$CS = V_{DD}$		10		pF		
<b>POWER REQUIREMENTS</b>								
Positive Supply Voltage	$V_{DD}$	MAX1147/MAX1149			2.7	3.6		
		MAX1146/MAX1148			4.75	5.25		
Supply Current (Note 8)	$I_{DD}$	Normal operation, full-scale input	External reference	116ksps	1.1	1.5		
				10ksps	0.12			
				1ksps	0.012			
			Internal reference at 116ksps		1.9	2.4		
Shutdown Supply Current (Note 8)		Fast power-down			120			
		Full power-down			0.3			
		$SHDN = DGND$			0.3	10		
Power-Supply Rejection (Note 9)	$PSR$	External reference		$\pm 0.2$		mV		

# Multichannel, True-Differential, Serial, 14-Bit ADCs

**MAX1146-MAX1149**

## TIMING CHARACTERISTICS

(V<sub>DD</sub> = 4.75V to 5.25V (MAX1146/MAX1148), V<sub>DD</sub> = 2.7V to 3.6V (MAX1147/MAX1149),  $\overline{\text{SHDN}} = \text{V}_{\text{DD}}$ , V<sub>COM</sub> = 0, f<sub>SCLK</sub> = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V<sub>REFADJ</sub> = V<sub>DD</sub>, C<sub>REF</sub> = 2.2 $\mu$ F, external +4.096V reference at REF for the MAX1146/MAX1148, external 2.500V reference at REF for the MAX1147/MAX1149, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Figures 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to SCLK Setup Time	t <sub>D5</sub>		50			ns
DIN to SCLK Hold Time	t <sub>DH</sub>		0			ns
SCLK Fall to Output Data Valid	t <sub>D OV</sub>	C <sub>LOAD</sub> = 50pF	10	80		ns
$\overline{\text{CS}}$ Fall to DOUT Enable	t <sub>D OE</sub>	C <sub>LOAD</sub> = 50pF		120		ns
$\overline{\text{CS}}$ Rise to DOUT Disable	t <sub>D OD</sub>	C <sub>LOAD</sub> = 50pF		120		ns
SHDN Rise $\overline{\text{CS}}$ Fall to SCLK Rise Time	t <sub>CSS</sub>		50			ns
SHDN Rise $\overline{\text{CS}}$ Fall to SCLK Rise Hold Time	t <sub>CSH</sub>		50			ns
SCLK Clock Frequency	f <sub>SCLK</sub>	External clock mode	0.1	2.1		MHz
		Internal clock mode	0	2.1		
SCLK Pulse-Width High	t <sub>CH</sub>	Internal clock mode	100			ns
SCLK Pulse-Width Low	t <sub>CL</sub>	Internal clock mode	100			ns
$\overline{\text{CS}}$ Fall to SSTRB Output Enable	t <sub>STE</sub>	External clock mode only		120		ns
$\overline{\text{CS}}$ Rise to SSTRB Output Disable	t <sub>STD</sub>	External clock mode only		120		ns
SSTRB Rise to SCLK Rise	t <sub>SCK</sub>	Internal clock mode only		0		ns
SCLK Fall to SSTRB Edge	t <sub>SCST</sub>			80		ns
$\overline{\text{CS}}$ Pulse Width	t <sub>CSW</sub>		100			ns

**Note 1:** Tested at V<sub>DD</sub> = 3.0V (MAX1147/MAX1149) or 5.0V(MAX1146/MAX1148); V<sub>COM</sub> = 0; unipolar single-ended input mode.

**Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

**Note 3:** Offset nulled. Measured with external reference.

**Note 4:** "On" channel grounded; full-scale 1kHz sine wave applied to all "off" channels.

**Note 5:** Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle. (See Figures 8-11.)

**Note 6:** The common-mode range for the analog inputs is from AGND to V<sub>DD</sub>.

**Note 7:** Digital inputs equal V<sub>DD</sub> or DGND.

**Note 8:** External load should not change during conversion for specified accuracy.

**Note 9:** Measured as (V<sub>FS</sub> x 3.6V) - (V<sub>FS</sub> x 2.7V) for the MAX1147/MAX1149 and (V<sub>FS</sub> x 5.25V) - (V<sub>FS</sub> x 4.75V) for the MAX1146/MAX1148. V<sub>DD</sub> = 3.6V to 2.7V for MAX1147/MAX1149 and V<sub>DD</sub> = 5.25V to 4.75V for the MAX1146/MAX1148.

## Multichannel, True-Differential, Serial, 14-Bit ADCs

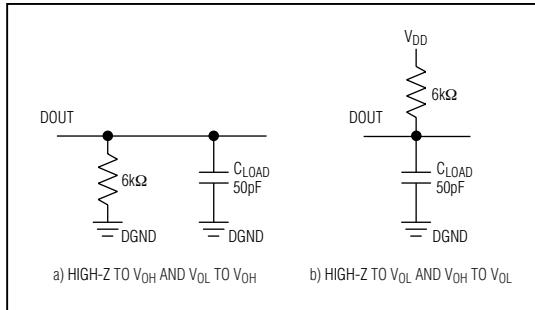


Figure 1. Load Circuits for Enable Time

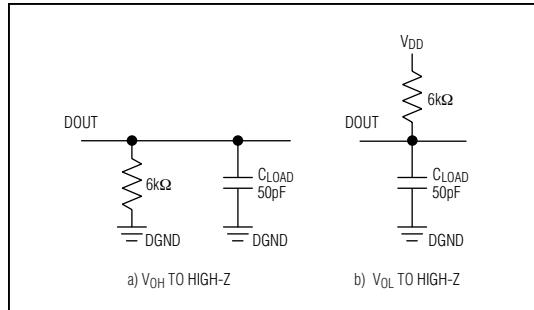


Figure 2. Load Circuits for Disable Time

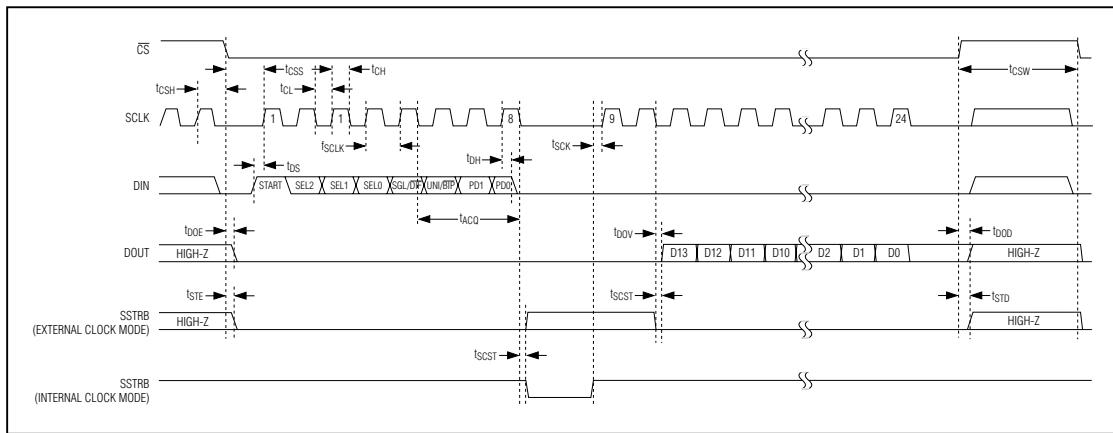


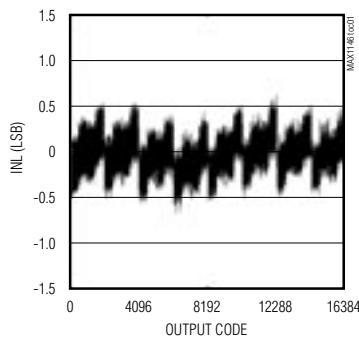
Figure 3. Detailed Operating Characteristics

# Multichannel, True-Differential, Serial, 14-Bit ADCs

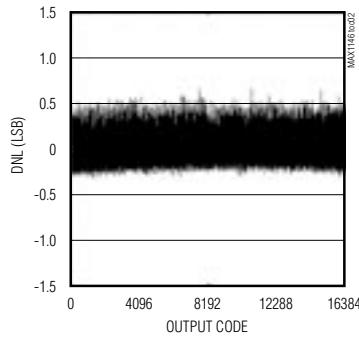
## Typical Operating Characteristics

( $V_{DD} = +5.0\text{V}$  (MAX1146/MAX1148),  $V_{DD} = +3.3\text{V}$  (MAX1147/MAX1149),  $\text{SHDN} = V_{DD}$ ,  $V_{COM} = 0$ ,  $f_{SCLK} = 2.1\text{MHz}$ , external clock (50% duty cycle), 18 clocks/conversion (116ksps),  $V_{REFADJ} = V_{DD}$ , external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149),  $C_{REF} = 2.2\mu\text{F}$ ,  $C_{LOAD} = 50\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

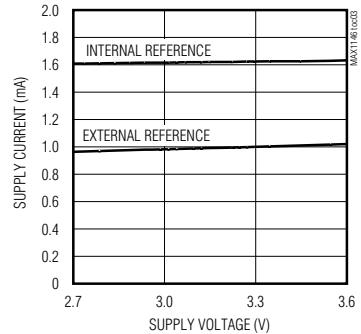
INL vs. OUTPUT CODE



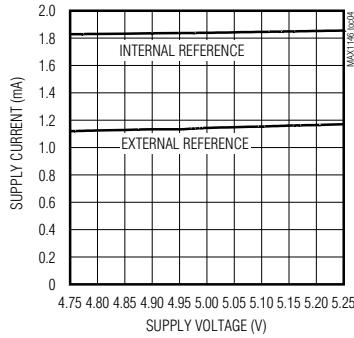
DNL vs. OUTPUT CODE



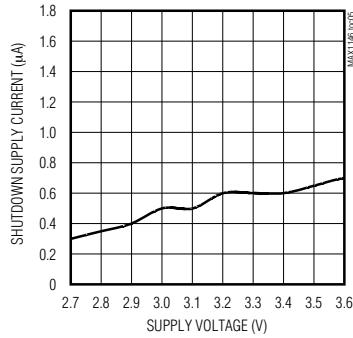
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
(MAX1147/MAX1149)



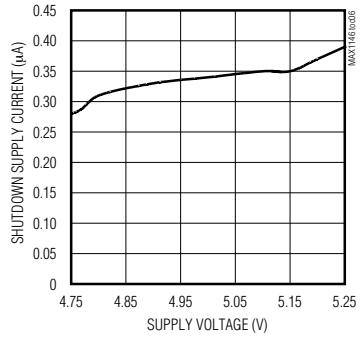
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
(MAX1146/MAX1148)



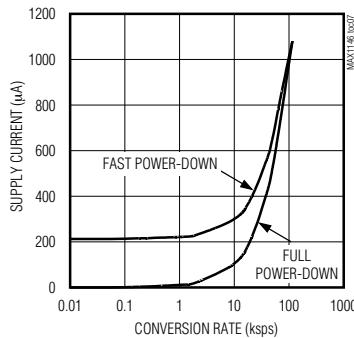
SHUTDOWN SUPPLY CURRENT  
vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



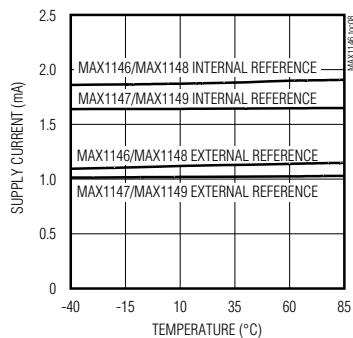
SHUTDOWN SUPPLY CURRENT  
vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



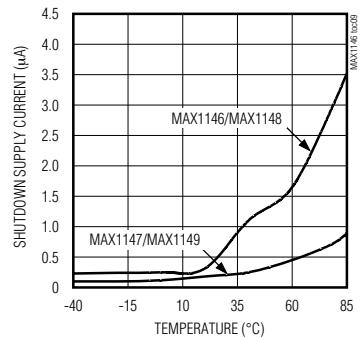
SUPPLY CURRENT  
vs. CONVERSION RATE



SUPPLY CURRENT vs. TEMPERATURE



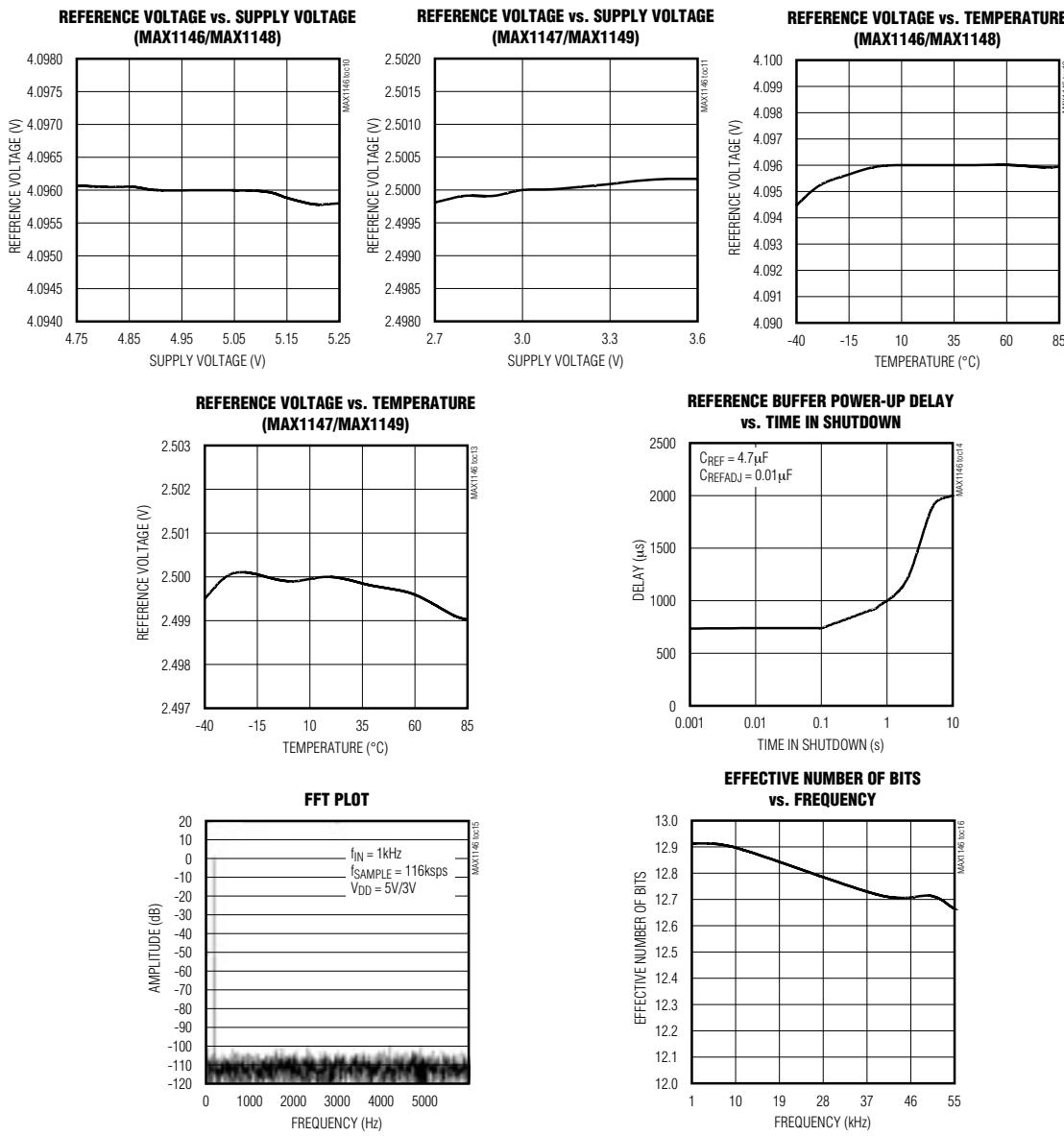
SHUTDOWN SUPPLY CURRENT  
vs. TEMPERATURE



# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Typical Operating Characteristics (continued)

( $V_{DD} = +5.0V$  (MAX1146/MAX1148),  $V_{DD} = +3.3V$  (MAX1147/MAX1149),  $SHDN = V_{DD}$ ,  $V_{COM} = 0$ ,  $f_{SCLK} = 2.1MHz$ , external clock (50% duty cycle), 18 clocks/conversion (116ksps),  $V_{REFADJ} = V_{DD}$ , external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149),  $C_{REF} = 2.2\mu F$ ,  $C_{LOAD} = 50pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

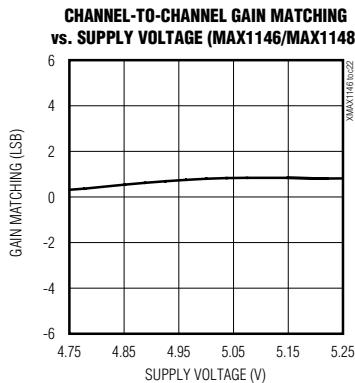
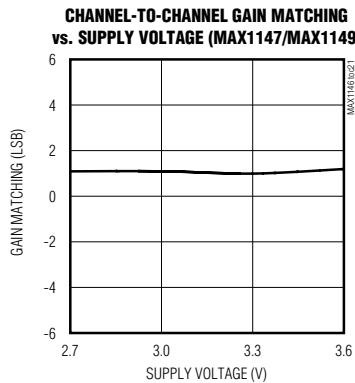
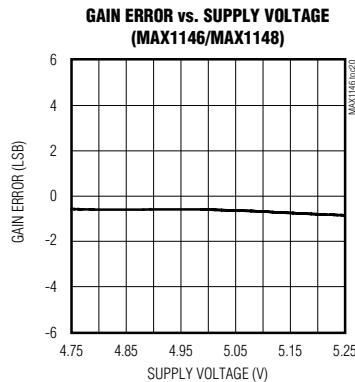
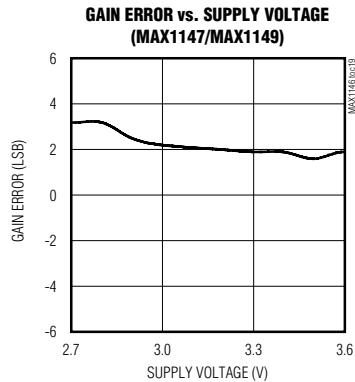
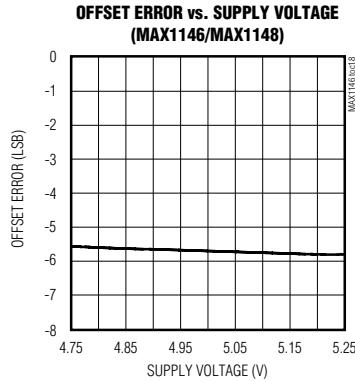
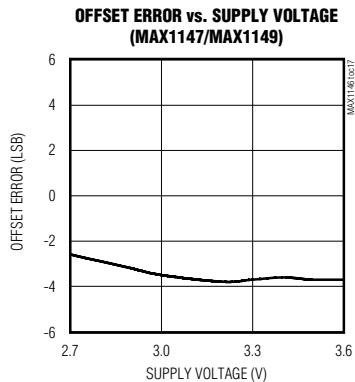


# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Typical Operating Characteristics (continued)

( $V_{DD} = +5.0\text{V}$  (MAX1146/MAX1148),  $V_{DD} = +3.3\text{V}$  (MAX1147/MAX1149),  $\overline{SHDN} = V_{DD}$ ,  $V_{COM} = 0$ ,  $f_{SCLK} = 2.1\text{MHz}$ , external clock (50% duty cycle), 18 clocks/conversion (116ksps),  $V_{REFADJ} = V_{DD}$ , external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149),  $C_{REF} = 2.2\mu\text{F}$ ,  $C_{LOAD} = 50\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

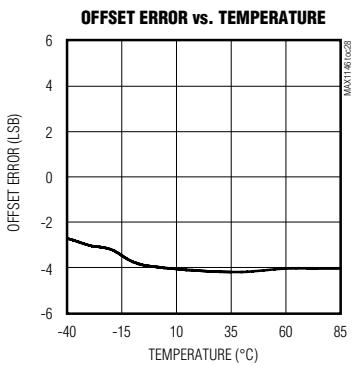
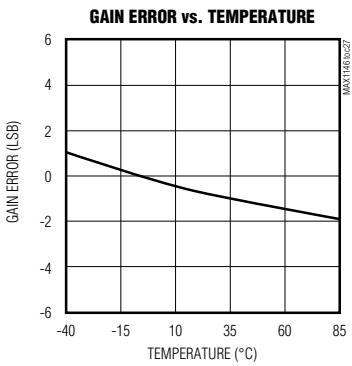
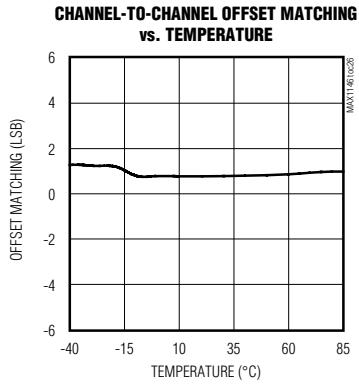
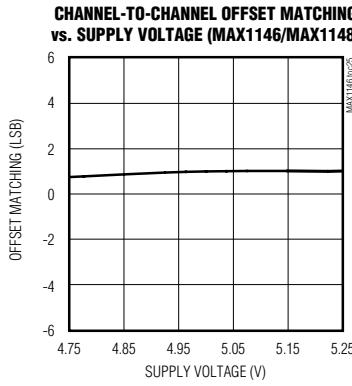
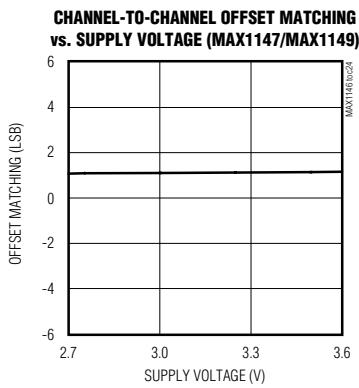
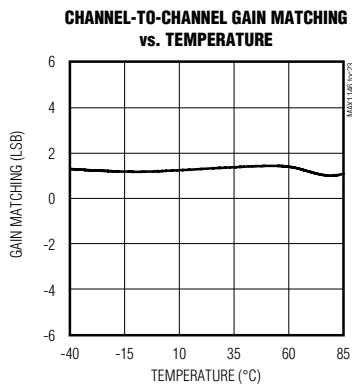
**MAX1146-MAX1149**



# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Typical Operating Characteristics (continued)

( $V_{DD} = +5.0V$  (MAX1146/MAX1148),  $V_{DD} = +3.3V$  (MAX1147/MAX1149),  $SHDN = V_{DD}$ ,  $V_{COM} = 0$ ,  $f_{SCLK} = 2.1MHz$ , external clock (50% duty cycle), 18 clocks/conversion (116ksps),  $V_{REFADJ} = V_{DD}$ , external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149),  $C_{REF} = 2.2\mu F$ ,  $C_{LOAD} = 50pF$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Multichannel, True-Differential, Serial, 14-Bit ADCs

**MAX1146–MAX1149**

## Pin Description

PIN		NAME	FUNCTION
MAX1148 MAX1149	MAX1146 MAX1147		
1	1	CH0	Analog Inputs
2	2	CH1	
3	3	CH2	
4	4	CH3	
5	—	CH4	
6	—	CH5	
7	—	CH6	
8	—	CH7	
9	9	COM	Common Input. Negative analog input in single-ended mode. COM sets zero-code voltage in unipolar and bipolar mode.
10	10	SHDN	Active-Low Shutdown Input. Pulling SHDN low shuts down the device reducing supply current to $0.2\mu\text{A}$ . Driving shutdown high enables the devices.
11	11	REF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the MAX1146/MAX1148 VREF is $+4.096\text{V}$ , and the MAX1147/MAX1149 VREF is $+2.500\text{V}$ .
12	12	REFADJ	Bandgap Reference Output and Reference Buffer Input. Bypass to AGND with a $0.01\mu\text{F}$ capacitor. Connect REFADJ to $\text{V}_{\text{DD}}$ to disable the internal bandgap reference and reference-buffer amplifier.
13	13	AGND	Analog Ground
14	14	DGND	Digital Ground
15	15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK when $\overline{\text{CS}}$ is low. DOUT is high impedance when $\overline{\text{CS}}$ is high.
16	16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the ADC conversion begins, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for two clock periods before the MSB decision. SSTRB is high impedance when $\overline{\text{CS}}$ is high (external clock mode).
17	17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK when $\overline{\text{CS}}$ is low. DIN is high impedance when CS is high.
18	18	$\overline{\text{CS}}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT is high impedance.
19	19	SCLK	Serial Clock Input. Clocks data in and out of the serial interface and sets the conversion speed in external clock mode. (Duty cycle must be 40% to 60%.)
20	20	$\text{V}_{\text{DD}}$	Positive Supply Voltage. Bypass to AGND with a $0.1\mu\text{F}$ capacitor.
—	5–8	N.C.	No Connection. Not internally connected.

# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Detailed Description

The MAX1146–MAX1149 ADCs use a successive-approximation conversion technique and input T/H circuitry to convert an analog signal to a 14-bit digital output. A flexible serial interface provides easy interface to microprocessors ( $\mu$ Ps). Figure 4 shows the typical application circuit and Figure 5 shows a functional diagram of the MAX1148/MAX1149.

### True-Differential Analog Input and Track/Hold

The MAX1146–MAX1149 analog input architecture contains an analog input multiplexer (MUX), two T/H capacitors, T/H switches, a comparator, and two switched capacitor digital-to-analog converters (DACs) (Figure 6).

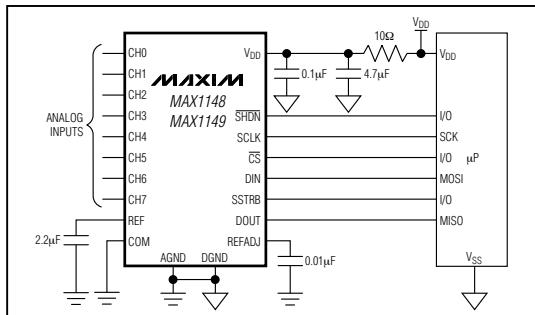


Figure 4. Typical Application Circuit

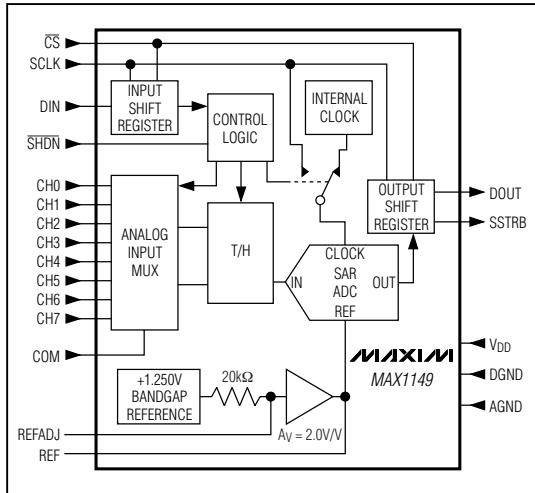


Figure 5. Functional Diagram

In single-ended mode, the analog input MUX connects IN+ to the selected input channel and IN- to COM. In differential mode, IN+ and IN- are connected to the selected analog input pairs such as CH0/CH1. Select the analog input channels according to Tables 1–5.

The analog input multiplexer switches to the selected channel on the control byte's fifth SCLK falling edge. At this time, the T/H switches are in the track position and  $C_{T/H+}$  and  $C_{T/H-}$  track the analog input signal. At the control byte's eighth SCLK falling edge, the MUX opens and the T/H switches move to the hold position, retaining the charge on  $C_{T/H+}$  and  $C_{T/H-}$  as a sample of the input signal. See Figures 8–11 for input MUX and T/H switch positioning.

During the conversion interval, the switched capacitive DAC adjusts to restore the comparator-input voltage to 0 within the limits of 14-bit resolution. This action requires 15 conversion clock cycles and is equivalent to transferring a charge of  $18pF \times (V_{IN+} - V_{IN-})$  from  $C_{T/H+}$  and  $C_{T/H-}$  to the binary-weighted capacitive DAC, forming a digital representation of the analog input signal.

After conversion, the T/H switches move from the hold position to the track position and the MUX switches back to the last specified position. In internal clock mode, the conversion is complete on the rising edge of SSTRB. In external clock mode, the conversion is complete on the eighteenth SCLK falling edge.

The time required for the T/H to acquire an input signal is a function of the analog input source impedance. If the input signal source impedance is high, the acquisition time lengthens. The MAX1146–MAX1149 provide three SCLK cycles (tACQ) in which the T/H capacitance must acquire a charge representing the input signal, typically the last three SCLKs of the control word. The input source impedance (R<sub>SOURCE</sub>) should be minimized to allow the T/H capacitance to charge within this allotted time.

$$t_{ACQ} = 11.5 \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

where R<sub>SOURCE</sub> is the analog input source impedance, R<sub>IN</sub> is 2.6kΩ (which is the sum of the analog input MUX and T/H switch resistances), and C<sub>IN</sub> is 18pF (which is the sum of  $C_{T/H+}$ ,  $C_{T/H-}$ , and input stray capacitance).

To minimize sampling errors with higher source impedances, connect a 100pF capacitor from the analog input to AGND. This input capacitor reduces the input's AC impedance but forms an RC filter with the source impedance, limiting the analog input bandwidth. For larger source impedance, use a buffer amplifier such as the MAX4430 to maintain analog input signal integrity.

# Multichannel, True-Differential, Serial, 14-Bit ADCs

**MAX1146–MAX1149**

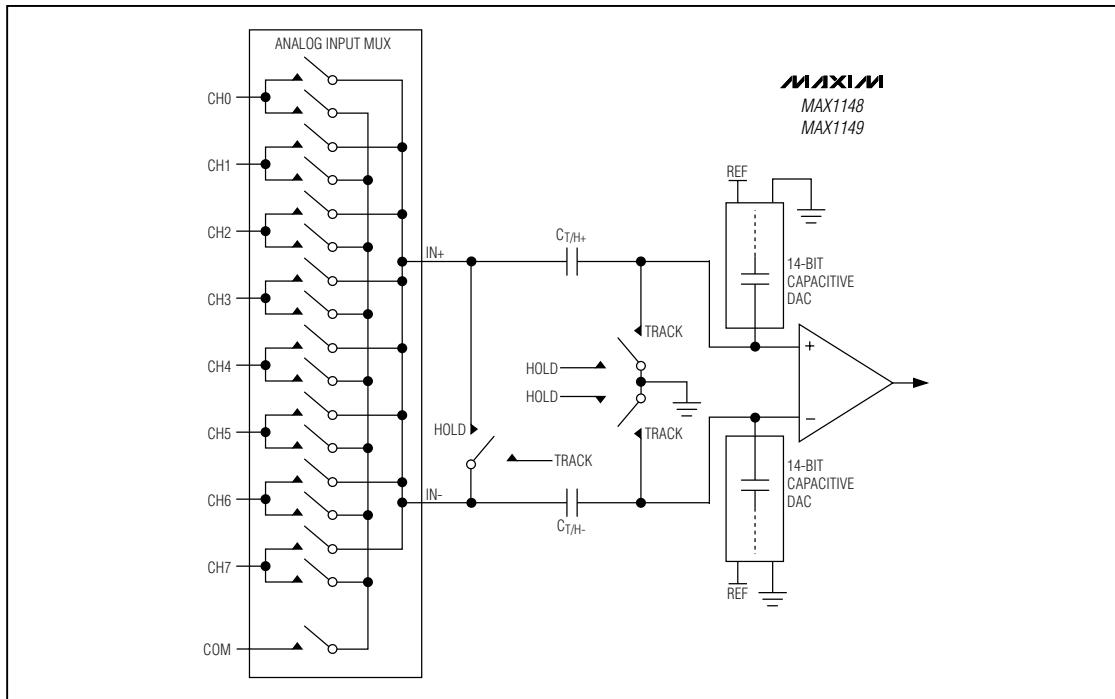


Figure 6. Equivalent Input Circuit

## Input Bandwidth

The MAX1146–MAX1149 feature input tracking circuitry with a 3.0MHz small-signal bandwidth. The 3.0MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

## Analog Input Protection

Internal protection diodes clamp the analog input to VDD and AGND. These diodes allow the analog inputs to swing from (AGND - 0.3V) to (VDD + 0.3V) without causing damage to the device. For accurate conversions, the inputs must not go more than 50mV below AGND or above VDD.

**Note:** If the analog input exceeds 50mV beyond the supply rails, limit the current to 2mA.

## Quick Look

Use the circuit of Figure 7 to quickly evaluate the MAX1148/MAX1149. The MAX1148/MAX1149 require a control byte to be written to DIN using SCLK before each conversion. Connecting DIN to VDD and clocking SCLK feeds in a control byte of \$FF HEX (see Table 1). Trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the MSB of the 14-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 18 clock cycles are required per conversion (Figure 10). All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

## Multichannel, True-Differential, Serial, 14-Bit ADCs

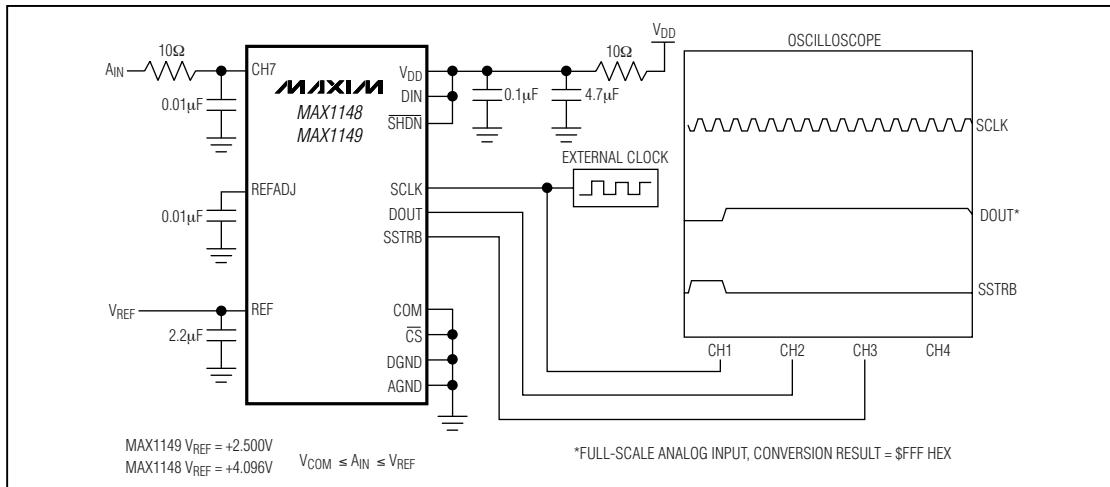


Figure 7. Quick-Look Circuit

Table 1. Control Byte Format

BIT	NAME	DESCRIPTION
7 (MSB)	START	Start bit. The first logic 1 bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6	SEL2	
5	SEL1	Channel-select bits. The channel-select bits select which of the eight channels are used for the conversion (Tables 2, 3, 4, and 5).
4	SEL0	
3	SGL/DIF	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured.
2	UNI/BIP	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, connect COM to AGND to perform conversion from 0 to $V_{REF}$ . In bipolar mode, connect COM to $V_{REF}/2$ to perform conversion from 0 to $V_{REF}$ . See Table 7.
1	PD1	Selects clock and power-down modes. PD1 = 0 and PDO = 0 selects full power-down mode*. PD1 = 0 and PDO = 1 selects fast power-down mode*. PD1 = 1 and PDO = 0 selects internal clock mode. PD1 = 1 and PDO = 1 selects external clock mode.
0 (LSB)	PDO	

\*The start bit resets power-down modes.

# Multichannel, True-Differential, Serial, 14-Bit ADCs

MAX1146–MAX1149

**Table 2. MAX1148/MAX1149 Channel Selection in Single-Ended Mode (SGL/DIF = 1)**

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								-
1	0	0		+							-
0	0	1			+						-
1	0	1				+					-
0	1	0					+				-
1	1	0						+			-
0	1	1						+			-
1	1	1							+		-

**Table 3. MAX1148/MAX1149 Channel Selection in Differential Mode (SGL/DIF = 0)**

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	-						
0	0	1			+	-				
0	1	0				+	-			
0	1	1					+	-		
1	0	0	-	+						
1	0	1			-	+				
1	1	0					-	+		
1	1	1						-	+	

**Table 4. MAX1146/MAX1147 Channel Selection in Single-Ended Mode (SGL/DIF = 1)**

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	0	+				-
1	0	0		+			-
0	0	1			+	-	
1	0	1				+	-

### Power-On Reset

When power is first applied, internal power-on reset circuitry activates the MAX1146–MAX1149 in internal clock mode, making the MAX1146–MAX1149 ready to convert with SSTRB high. No conversions should be performed until the power supply is stable. The first logical 1 on DIN with CS low is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

### Starting a Conversion

Start a conversion by clocking a control byte into DIN. With CS low, a rising edge on SCLK latches a bit from DIN into the MAX1146–MAX1149 internal shift register. After CS falls, the first logic 1 bit defines the control

**Table 5. MAX1146/MAX1147 Channel Selection in Differential Mode (SGL/DIF = 0)**

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	0	+	-		
0	0	1			+	-
1	0	0	-	+		
1	0	1			-	+

byte's MSB. Until this start bit arrives, any number of logic 0 bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1146–MAX1149 are compatible with SPI/QSPI and MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers. Set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI transmit a byte and receive a byte at the same time. Using the *Typical Application Circuit* (Figure 4), the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 14-bit conversion result).

# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Digital Output

In unipolar input mode, the digital output is straight binary (Figure 14). For bipolar input mode, the digital output is two's complement binary (Figure 15). Data is clocked out on the falling edge of SCLK in MSB-first format.

## Clock Modes

The MAX1146–MAX1149 can use either the external serial clock or the internal clock to drive the successive-approximation conversion. The external clock shifts data in and out of the MAX1146–MAX1149.

External clock mode allows the fastest throughput rate (116ksps) and serial clock frequencies from 0.1MHz to 2.1MHz. Internal clock mode provides the best noise performance because the digital interface can be idle during conversion. The internal clock mode serial clock frequency can range from 0 to 2.1MHz. Internal clock mode allows the CPU to request a conversion and clock back the results.

Bits PD1 and PD0 of the control byte program the clock and power-down modes. The MAX1146–MAX1149 power up in internal clock mode with all circuits activated. Figures 8–11 illustrate the available clocking modes.

## External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and the results appear at DOUT on each of the next 14 SCLK falling edges (Figures 8 and 10). SSTRB and DOUT go into a high-impedance state when CS is high.

Use internal clock mode if the serial clock frequency is less than 100kHz or if serial clock interruptions could cause the conversion interval to exceed 140 $\mu$ s. The conversion must complete in 140 $\mu$ s, or droop on the T/H capacitors can degrade conversion results.

## Internal Clock

When configured for internal clock mode, the MAX1146–MAX1149 generate an internal conversion clock. This frees the  $\mu$ P from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2.1MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 8.0 $\mu$ s, during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling SCLK clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figures 9 and 11).

For the most accurate conversion, the MAX1146–MAX1149 digital I/O should remain inactive during the internal clock conversion interval ( $t_{CONV}$ ). Do not pull CS high during conversion. Pulling CS high aborts the current conversion. To ensure that the next start bit is recognized, clock in 18 zeros at DIN. When internal clock mode is selected, SSTRB does not go into a high-impedance state when CS goes high. A rising edge on SSTRB indicates that the MAX1146–MAX1149 have finished the conversion. The  $\mu$ P can then read the conversion results at its convenience.

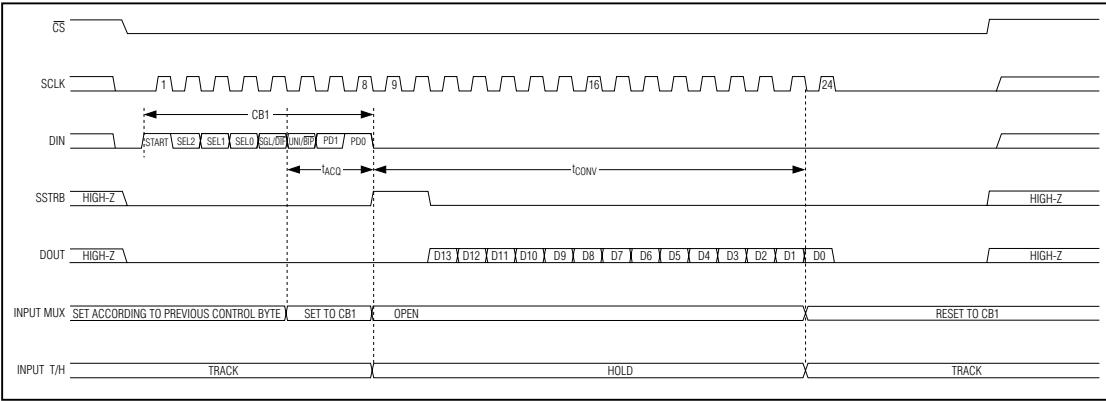


Figure 8. External Clock Mode—24 Clocks/Conversion Timing

# Multichannel, True-Differential, Serial, 14-Bit ADCs

MAX1146–MAX1149

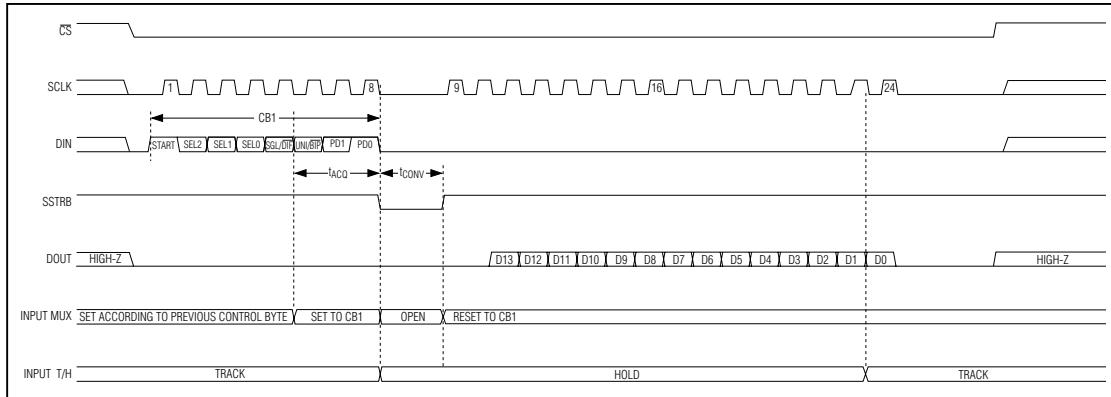


Figure 9. Internal Clock Mode Timing—24 Clocks/Conversion Timing

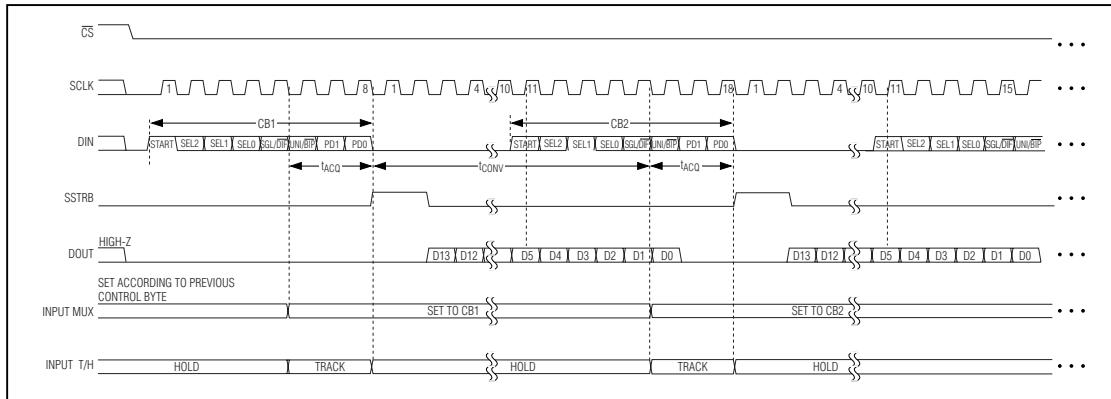


Figure 10. External Clock Mode—18 Clocks/Conversion Timing

## Applications Information

### Idle Mode

The device is considered idle when all the bits have been clocked out or 18 zeros have been clocked in on DIN.

### Start Bit

The falling edge of  $\overline{CS}$  alone does not start a conversion. The first logic high clocked into DIN with  $\overline{CS}$  low is interpreted as a start bit and defines the first bit of the control byte. The device begins to track on the fifth falling edge of SCLK after a start bit has been recognized. A conversion starts on the eighth falling edge of SCLK as the last bit of the control byte is being clocked in. The start bit is defined as follows:

- 1) The first high bit clocked into DIN with  $\overline{CS}$  low any time the converter is idle.
- or
- 2) The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto DOUT (Figures 10 and 11).

Toggle  $\overline{CS}$  before the current conversion is complete aborts the conversion and clears the output register.

The fastest the MAX1146–MAX1149 can run with  $\overline{CS}$  held low between conversions is 18 clocks per conversion. Figures 10 and 11 show the serial-interface timing necessary to perform a conversion every 18 SCLK cycles.

# Multichannel, True-Differential, Serial, 14-Bit ADCs

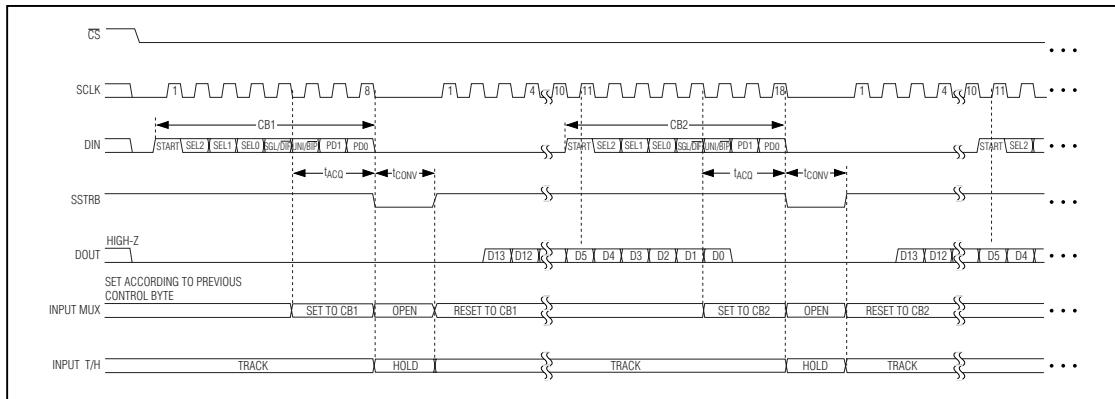


Figure 11. Internal Clock Mode—18 Clocks/Conversion Timing

### Shutdown and Power-Down Modes

The MAX1146–MAX1149 provide a hardware shutdown and two software power-down modes.

Pulling SHDN low places the converter in hardware shutdown. The conversion is immediately terminated and the supply current is reduced to 300nA. Allow 2ms for the device to power-up when the internal reference buffer is used with CREFADJ = 0.01 $\mu$ F and CREF = 2.2 $\mu$ F. Larger capacitors on CREFADJ and CREF increase the power-up time (Table 6). No wake-up time is needed for the device to power-up from fast power-down when using an external reference.

Select a software power-down mode through the PD1 and PDO bits of the control byte (Table 1). When the conversion in progress is complete, software power-down is initiated. The serial interface remains active and the last conversion result can be clocked out. In full power-down mode, only the serial interface remains operational and the supply current is reduced to 300nA. In fast power-down mode, only the bandgap reference and the serial interface remain operational, and the supply current is reduced to 600 $\mu$ A.

Table 6. Internal Reference Buffer Power-Up Times vs. Bypass Capacitors

CREFADJ*	CREF	POWER-UP TIMES FROM AN EXTENDED POWER-DOWN
0.01 $\mu$ F	4.7 $\mu$ F	2ms
0.1 $\mu$ F	10 $\mu$ F	25ms

\*Power-up times are dominated by CREFADJ.

The MAX1146–MAX1149 automatically wake up from software power-down when they receive the control byte's start bit (Table 1). Allow 2ms for the device to power-up when the internal reference buffer is used with CREFADJ = 0.01 $\mu$ F and CREF = 2.2 $\mu$ F. Larger capacitors on CREFADJ and CREF increase the power-up time (Table 6). No wake-up time is needed for the device to power-up from fast power-down when using an external reference.

### Reference Voltage

The MAX1146–MAX1149 can be used with an internal or external reference voltage. The reference voltage determines the ADC input range. The reference determines the full-scale output value (Table 7).

#### Internal Reference

The MAX1146–MAX1149 contain an internal 1.250V bandgap reference. This bandgap reference is connected to REFADJ through a 20k $\Omega$  resistor. Bypass REFADJ with a 0.01 $\mu$ F capacitor to AGND. The MAX1146/MAX1148 reference buffer has a 3.277V/V gain to provide +4.096V at REF. The MAX1147/MAX1149 reference buffer has a 2.000V/V gain to provide +2.500V at REF. Bypass REF with a minimum 2.2 $\mu$ F capacitor to AGND when using the internal reference.

#### External Reference

An external reference can be applied to the MAX1146–MAX1149 in two ways:

- 1) Disable the internal reference buffer by connecting REFADJ to VDD and apply the external reference to REF (Figure 12).
- 2) Utilize the internal reference buffer by applying an external reference to REFADJ (Figure 13).

# Multichannel, True-Differential, Serial, 14-Bit ADCs

**MAX1146–MAX1149**

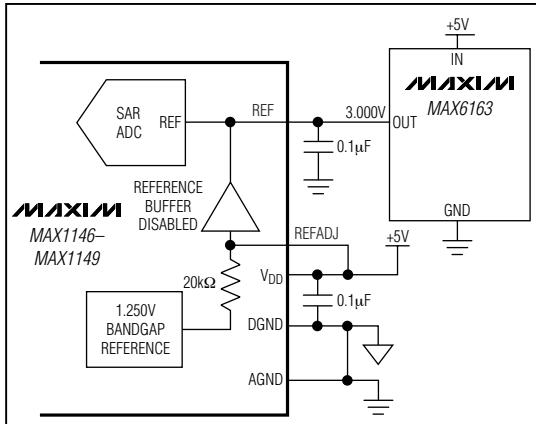


Figure 12. External Reference Applied to REF

Method 1 allows the direct application of an external reference from 1.5V to  $V_{DD} + 50\text{mV}$ . The REF input impedance is typically  $10\text{k}\Omega$ . During conversion, an external reference at REF must deliver up to  $210\mu\text{A}$  and have an output impedance less than  $10\Omega$ . Bypass REF with a  $0.1\mu\text{F}$  capacitor to AGND to improve its output impedance.

Method 2 utilizes the internal reference buffer to reduce the external reference load. The REFADJ input impedance is typically  $20\text{k}\Omega$ . During a conversion, an external reference at REFADJ must deliver at least  $100\mu\text{A}$  and have an output impedance less than  $100\Omega$ . The MAX1146/MAX1148 reference buffer has a  $3.277\text{V/V}$  gain and the MAX1147/MAX1149 has a gain of  $2.000\text{V/V}$ . The external reference voltage at REFADJ multiplied by the reference buffer gain is the SAR ADC reference voltage. This reference appears at REF and must be from 1.5V to  $V_{DD} + 50\text{mV}$ . Bypass REFADJ with a  $0.01\mu\text{F}$  capacitor and bypass REF with a  $2.2\mu\text{F}$  capacitor to AGND.

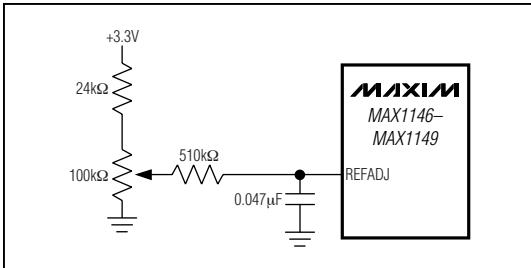


Figure 13. Reference Adjust Circuit

with a  $0.01\mu\text{F}$  capacitor and bypass REF with a  $2.2\mu\text{F}$  capacitor to AGND.

## Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

Output data coding for the MAX1146–MAX1149 is binary in unipolar mode and two's complement binary in bipolar mode with  $1 \text{ LSB} = (V_{REF}/2^N)$ , where  $N$  is the number of bits (14). Code transitions occur halfway between successive-integer LSB values. Figure 14 and Figure 15 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

## Serial Interfaces

The MAX1146–MAX1149 feature a serial interface that is fully compatible with SPI, QSPI, and MICROWIRE. If a serial interface is available, establish the CPU's serial interface as a master, so that the CPU generates the serial clock for the ADCs. Select a clock frequency up to  $2.1\text{MHz}$ .

### SPI and MICROWIRE Interface

When using an SPI (Figure 16a) or MICROWIRE interface (Figure 16b), set  $\text{CPOL} = \text{CPHA} = 0$ . Two 8-bit readings are necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling

Table 7. Full Scale and Zero Scale

INPUT AND OUTPUT MODES	UNIPOLAR MODE		BIPOLAR MODE		
	ZERO SCALE	FULL SCALE	NEGATIVE FULL SCALE	ZERO SCALE	POSITIVE FULL SCALE
Single-Ended Mode	$V_{COM}$	$V_{REF} + V_{COM}$	$\frac{-V_{REF}}{2} + V_{COM}$	$V_{COM}$	$\frac{+V_{REF}}{2} + V_{COM}$
Differential Mode	$V_{IN-}$	$V_{REF} + V_{IN-}$	$\frac{-V_{REF}}{2} + V_{IN-}$	$V_{IN-}$	$\frac{+V_{REF}}{2} + V_{IN-}$

**Note:** The common mode range for the analog inputs is from AGND to  $V_{DD}$ .

## Multichannel, True-Differential, Serial, 14-Bit ADCs

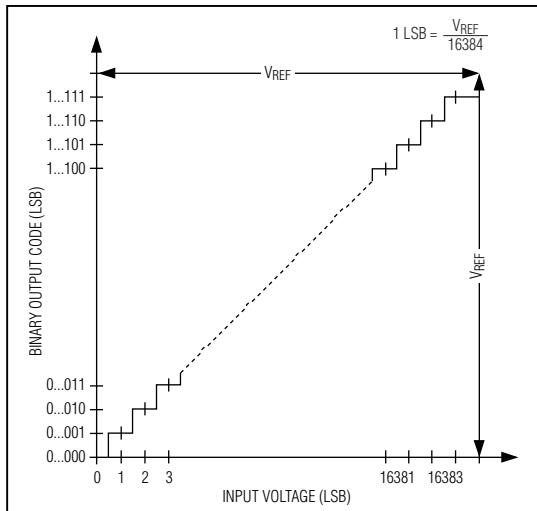


Figure 14. Unipolar Transfer Function

edge and is clocked into the  $\mu$ P on SCLK's rising edge. The first 8-bit data stream contains the first 8-bits of DOUT starting with the MSB. The second 8-bit data stream contains the remaining 6 result bits.

### QSPI Interface

Using the high-speed QSPI interface (Figure 17) with CPOL = 0 and CPHA = 0, the MAX1146–MAX1149 support a maximum fSCLK of 2.1MHz. One 16-bit reading is necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the  $\mu$ P on SCLK's rising edge. The first 14 bits are the data.

### PIC16/PIC17 SSP Module Interface

The MAX1146–MAX1149 are compatible with a PIC16/PIC17 microcontroller ( $\mu$ C), using the synchronous serial-port (SSP) module. To establish SPI com-

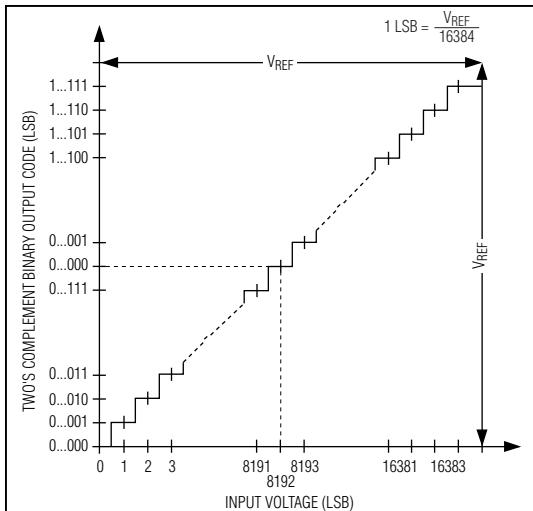


Figure 15. Bipolar Transfer Function

munication, connect the controller as shown in Figure 18 and configure the PIC16/PIC17 as system master. Initialize the synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 8 and 9. In SPI mode, the PIC16/PIC17  $\mu$ Cs allow 8 bits of data to be synchronously transmitted and received simultaneously. Two consecutive 8-bit readings are necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the  $\mu$ C on SCLK's rising edge. The first 8-bit data stream contains the first 8 data bits starting with the MSB. The second data stream contains the remaining bits, D5 through D0.

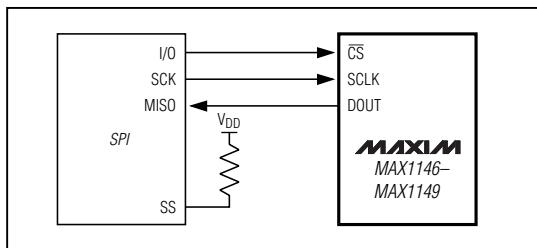


Figure 16a. SPI Connections

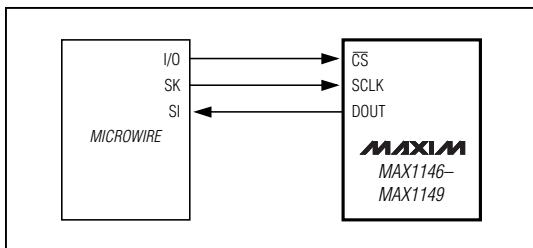


Figure 16b. MICROWIRE Connections

# Multichannel, True-Differential, Serial, 14-Bit ADCs

**MAX1146–MAX1149**

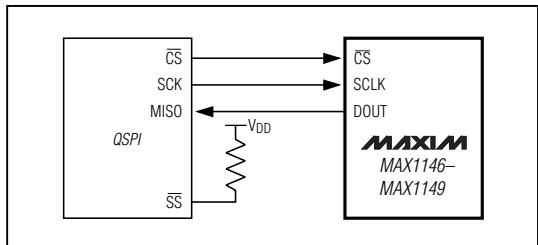


Figure 17. QSPI Connections

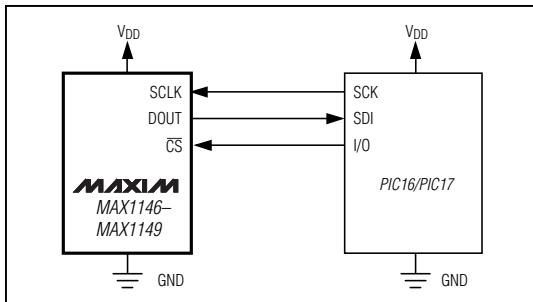


Figure 18. SPI Interface Connection for a PIC16/PIC17 Controller

**Table 8. Detailed SSPCON Register Content**

CONTROL BIT	PIC16/PIC17 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	Bit 7	X
SSPOV	Bit 6	X
SSPEN	Bit 5	1
CKP	Bit 4	0
SSPM3	Bit 3	0
SSPM2	Bit 2	0
SSPM1	Bit 1	0
SSPM0	Bit 0	1

**Table 9. Detailed SSPSTAT Register Content**

CONTROL BIT	MAX1146–MAX1149 SETTINGS	SYNCHRONOUS SERIAL-PORT STATUS REGISTER (SSPSTAT)
SMP	Bit 7	0
CKE	Bit 6	1
D/A	Bit 5	X
P	Bit 4	X
S	Bit 3	X
R/W	Bit 2	X
UA	Bit 1	X
BF	Bit 0	X

## Multichannel, True-Differential, Serial, 14-Bit ADCs

### TMS320LC3x Interface

Figure 19 shows an application circuit to interface the MAX1146–MAX1149 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 20. Use the following steps to initiate a conversion in the MAX1146–MAX1149 and to read the results:

- 1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are connected together with the MAX1146–MAX1149 SCLK input.
- 2) Drive the  $\overline{CS}$  of the MAX1146–MAX1149 low through the XF\_I/O port of the TMS320 to clock data into the MAX1146–MAX1149 DIN.
- 3) Write an 8-bit word (1XXXXX11) to the MAX1146–MAX1149 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
- 4) The MAX1146–MAX1149 SSTRB output is monitored by the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1146–MAX1149.
- 5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 14-bit conversion result followed by 2 trailing bits, which should be ignored.
- 6) Pull  $\overline{CS}$  high to disable the MAX1146–MAX1149 until the next conversion is initiated.

### Layout, Grounding, and Bypassing

Careful PC board layout is essential for best system performance. Boards should have separate analog and digital ground planes. Ensure that digital and analog signals are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the device package.

Figure 4 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all analog grounds to the star analog ground. Connect the digital grounds to the star digital ground. Connect the digital ground point to the analog ground point directly at the device. For lowest noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

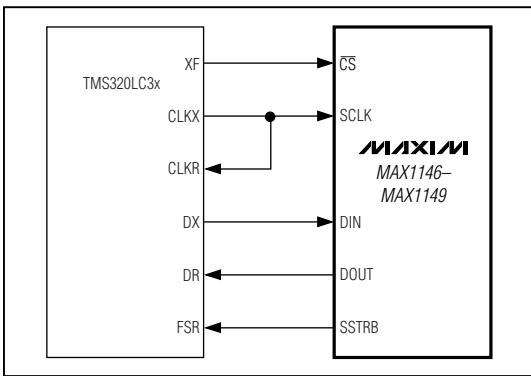


Figure 19. MAX1146-MAX1149-to-TMS320 Serial Interface

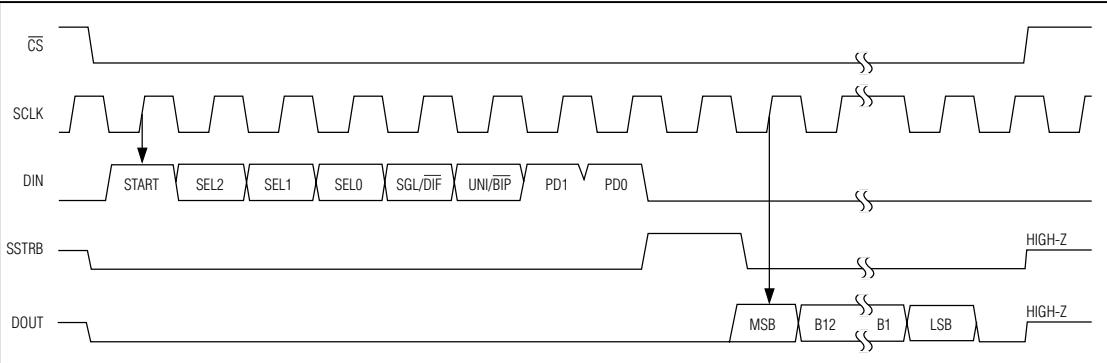


Figure 20. TMS320 Serial-Interface Timing Diagram

# Multichannel, True-Differential, Serial, 14-Bit ADCs

High-frequency noise in the  $V_{DD}$  power supply degrades the device's high-speed performance. Bypass the supply to the digital ground with  $0.1\mu F$  and  $4.7\mu F$  capacitors. Minimize capacitor lead lengths for best supply-noise rejection. Connect a  $10\Omega$  resistor in series with the  $0.1\mu F$  capacitor to form a lowpass filter when the power supply is noisy.

## Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1146–MAX1149 are measured using the end-point method.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

### Aperture Definitions

Aperture jitter ( $t_{AJ}$ ) is the sample-to-sample variation in the time between the samples. Aperture delay ( $t_{AD}$ ) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

### Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

### Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD(dB) = 20 \times \log (SignalRMS / NoiseRMS)$$

### Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left( \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2}{V_1^2}} \right)$$

where  $V_1$  is the fundamental amplitude, and  $V_2$  through  $V_5$  are the amplitudes of the 2nd- through 5th-order harmonics.

### Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

## Chip Information

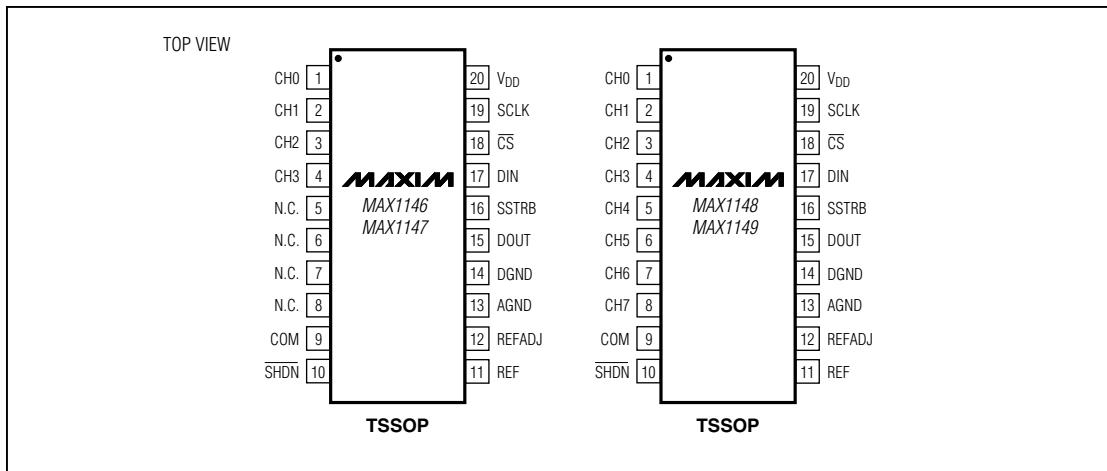
TRANSISTOR COUNT: 5589

PROCESS: BiCMOS

**MAX1146–MAX1149**

## **Multichannel, True-Differential, Serial, 14-Bit ADCs**

### **Pin Configurations**



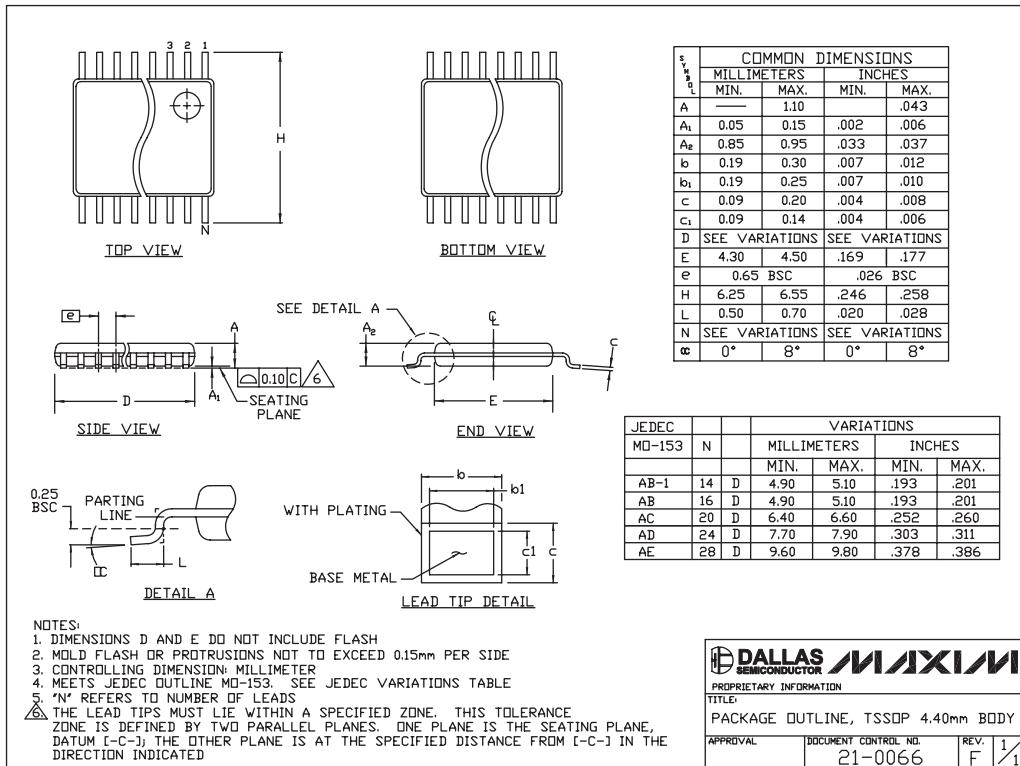
# Multichannel, True-Differential, Serial, 14-Bit ADCs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**MAX1146-MAX1149**

TSSOP4.40mm.EPS



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