TMP8085AP-2/TMP8085AHP-2
8-BIT MICROPROCESSOR

1. GENERAL DESCRIPTION

The TMP8085AP-2/TMP8085AHP-2, hereafter on referred to as TMP8085A, is a 8 bit micro processing unit (MPU). TMP8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of TMP8155P-2/TMP8156P-2 allow a direct interface with TMP8085A.

2. FEATURES

- 0.8μSec Instruction Cycle (CLK Cycle Period @200nSec)
- Single +5V Power Supply
  (TMP8085AP-2: 5V ± 5%, TMP8085AHP-2: 5V ± 10%)
- On-Chip Clock Generator (with External Crystal or RC Network)
- On-Chip System Controller; Cycle status information available for Large System Control
- 4 Vectored Interrupts (One is Non-Maskable)
- Decimal, Binary and Double Precision Arithmetic
- Serial In/Serial Out Port
- Direct Addressing Capability up to 64K Byte Memory Space
- Compatible with Intel's 8085A
- Low Power Consumption (TMP8085AHP-2: Icc max = 135mA)

3. PIN CONNECTION (TOP VIEW)

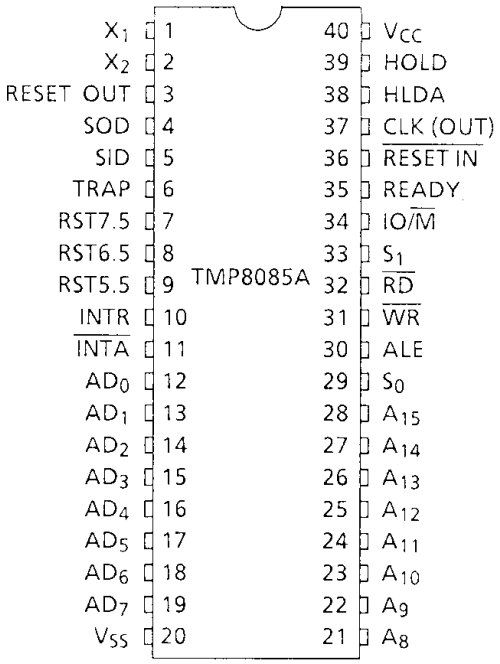

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Figure 3.1

4. BLOCK DIAGRAM

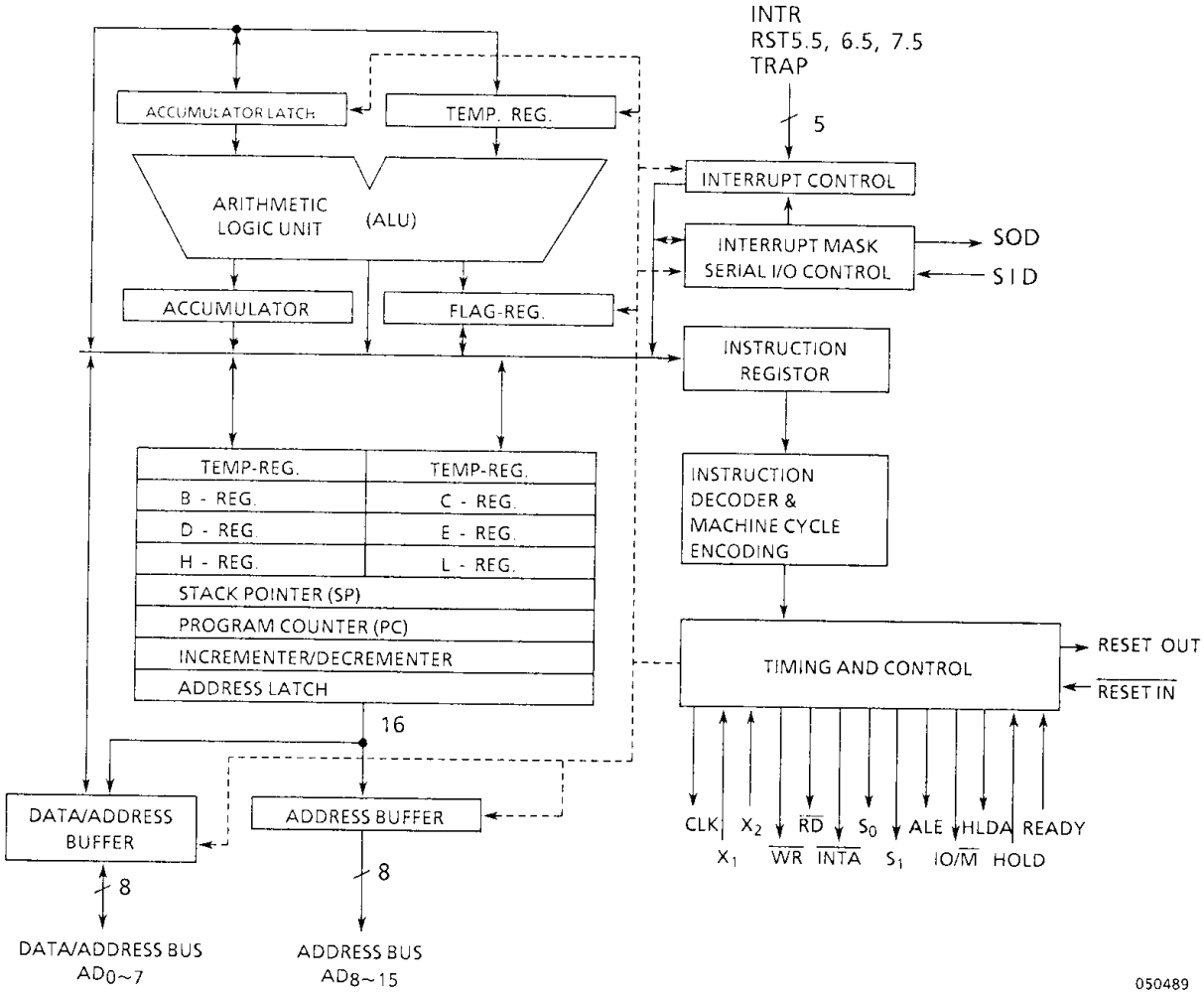

Figure 4.1

5. PIN NAME AND PIN DESCRIPTION

- X_1, X_2 (Input)

  Crystal, LC, or RC network are connected to X_1 and X_2 to drive the internal clock generator. X_1 and X_2 can also be driven by an external clock source. The input frequency is devided by 2 to give the processor's internal operating frequency.

- CLK(Output)

  Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.

- $\overline{\text{RESETIN}}$ (Input)

  The $\overline{\text{RESETIN}}$ Input initializes the processor by clearing the program counter, instruction register, SOD latch, Interrupt Enable flip-flop and HLDA flip-flop. The address and data buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESETIN}}$ is a Schmitttriggered input, allowing connection to an RC network for power on RESET delay. The TMP8085A is held in the reset condition as long as $\overline{\text{RESETIN}}$ is applied.

- RESET OUT (Output)

  The RESET OUT signal indicates that the TMP8085A is being reset. It can be used as a system reset. It is synchronized to the processor clock and lasts an integral number of clock periods.

- SOD (Output)

  Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

- SID (Input)

  Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

- INTR (Input)

  INTERRUPT REQUEST signal provides a mechanism for external devices to modify the instruction flow of the program in progress. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is recognized, the processor will complete the execution of the current instruction, and then the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by RESET and immediately after an interrupt is accepted.

- $\overline{INTA}$ (Output)

  INTERRUPT ACKNOWLEDGE: Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus. It is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.

RST 5.5
RST 6.5 } (Inputs)
RST 7.5

RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. These interrupts have a higher priority than INTR. The priority of these interrupts is ordered as shown Table 1. These interrupts are maskable using the SIM instruction.

- TRAP (Input)

  Trap interrupt is a nonmaskable RESTART interrupt. It is sampled at the same timing as INTR or RST 5.5-7.5. It is unaffected by SIM or Enable/Disable Interrupt instruction. It has the highest priority of any interrupt.

- AD_0-AD_7 (Input/Output, 3-state)

  Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T_1 state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

- A_8-A_{15} (Output, 3-state)

  Upper 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

- S_0, S_1, and IO/$\overline{M}$ (Output)

  Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt Acknowledge
TS	0	0	Halt
TS	X	X	Hold
TS	X	X	Reset

  Note : TS = 3-state (high impedance)
  X = unspecified

- ALE (Output)

  Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the external latch or the on-chip latch of peripherals. The falling edge of ALE can be used to strobe the status information. ALE never goes 3-stated.

- $\overline{WR}$ (Output, 3-state)

  WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. It is 3-stated during Hold and Halt modes and during RESET.

- $\overline{RD}$ (Output, 3-state)

  READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

- READY (Input)

  When READY is inactive (low), indicating the external operation has not been complete yet, the processor will enter the Wait state. It will wait for an integral number of clock cycles until READY goes high before completing the read or write cycle.

- HOLD (Input)

  The HOLD input cause TMP8085A to release the control over the address bus and the data bus. When HOLD goes active, the processor completes its current operation, activates the HLDA output, and puts the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines into high-impedance state. Internal processing can continue. The Holding device can then utilize the address and data buses instead of TMP8085A. TMP8085A can regain the bus only after the HOLD goes inactive (low).

- HLDA (Output)

  The Hold Acknowledge output, HLDA signal is a response to a HOLD input. It indicates that TMP8085A has received the HOLD request and HOLD will release the bus control in the next cycle. HLDA goes low after the HOLD goes inactive (low). TMP8085A takes over the bus control one half clock after HDLA goes low.

- V_{CC}

  +5 volt supply

- V_{SS}

  Ground Reference

6. FUNCTIONAL DESCRIPTION

TMP8085A is a 8-bit central processor.

TMP8085A is provided with internal 8-bit registers and 16-bit registers. TMP8085A has eight addressable 8-bit registers. Six of them can be used either as 8-bit registers or as 16-bit register pairs. In addition to the register pairs, the TMP8085A contains two additional 16-bit registers. TMP8085A register set is as follows:

- The acccumulator (A Register) is the focus of all of the accumulator instructions, which include arithmetic, logic, load and store, and I/O instructions.
- The program counter (PC) always points to the memory location of the next instruction to be executed.
- General-purpose registers BC, DE, and HL may be used as 8-bit registers or as three 16-bit registers, interchangeably, depending on the instruction being performed.
- The stack pointer (SP) is a special data pointer that always points to the stack top (next available stack address).
- The flag register contains five one-bit flags, each of which records processor status information and may also control processor operation.

The five flags in TMP8085A are shown below:

(MSB)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		C

- The carry flag (C) is set and reset by arithmetic operations. An additional operation that resutls in an overflow out of the high-order bit of the accumulator sets the carry flag. The carry flag also acts as a "borrow" flag for subtract instruction.
- The auxiliary carry flag (AC) indicates overflow out of bit 3 of the accumulator in the same way that C flag indicates overflow out of bit 7. This flag is commonly used in BCD arithmetic.
- The sign flag (S) is set to the condition of the most significant (MSB) bit of the accumulator following the execution of arithmetic or logic instructions.
- The zero flag (Z) is set if the result generated by certain instructions is zero. The zero flag is cleared if the result is not zero.
- The parity flag (P) is set to 1 if the parity (number of 1-bits) of the accumulator is even. If odd, it is cleared. TMP8085A offers the functions of clock generation,

system bus control, and interrupt priority selection as well as execution of the instruction set. TMP8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (T_1 clock cycle) of a machine cycle the lower order address is sent out on the Address/Data Bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle, the data bus is used for memory or I/O data transferring.

7. INTERRUPT AND SERIAL I/O

TMP8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to 8080A INT. Each of three RESTART inputs 5.5, 6.5, 7.5, has a programmable mask. TRAP is also one of RESTART interrupts but it is nonmaskable.

The three RESTART interrupts cause the internal execution of RESTART if the interrupts are enabled and if the corresponding interrupt mask is not set. The nonmaskable TRAP always causes internal interrupt execution whether INTR, RST 5.5, RST 6.5 and RST 7.5 interrupts are enable or not.

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high-level sensitive like INTR and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESETIN}}$ to TMP8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending: TRAP-highest priority. RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were reenabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

Table 7.1 Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address branched to When Interrupt Occurs	Type Trigger
TRAP	1	24 (Hex.)	Rising edge and high level until sampled.
RST 7.5	2	3C (Hex.)	Rising edge (latched) .
RST 6.5	3	34 (Hex.)	High level until sampled.
RST 5.5	4	2C (Hex.)	High level until sampled.
INTR	5	See Note (2)	High level until sampled.

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Notes : (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to TMP8085A when the interrupt is acknowledged.

The TRAP interrupt is special in that it disables all other interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instruction provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current interrupt enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD date.

8. BASIC TIMING

The execution of each instruction by the TMP8085A consists of a sequence of from one to five machine cycles, and cach machine cycle consists of a minimum of from three to six clock cycles. Most machine cycles consist of three T states, (cycles of the CLK output) with the exception of opecode fetch, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

At the beginning of every machine cycle, TMP8085A sends out three status signals ($IO/\overline{M}$, S_1, S_0) that define what type of machine cycle is about to take place. TMP8085A also sends out a 16-bit address at the beginning of every machine cycle to identify the particular memory location or I/O port that the machine cycle applies to.

The special timing signal, ADDRESS LATCH ENABLE (ALE), is used a strobe to sample the lower 8-bits of address on the AD_0-AD_7 lines. ALE is present during T_1 of every machine cycle. Control lines $\overline{RD}$ ($\overline{INTA}$) and $\overline{WR}$ become active later, at the time when the transfer of data is to take plece.

Figure 3 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction).

Table 8.1 TMP8085 Machine Cycle Chart

MACHINE CYCLE	$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	0	1	1	0	1	1
MEMORY READ	0	1	0	0	1	1
MEMORY WRITE	0	0	1	1	0	1
I/O READ	1	1	0	0	1	1
I/O WRITE	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	1	1	1	1	1	0
BUS IDLE: DAD	0	1	0	1	1	1
ACK. OF RST, TRAP	1	1	1	1	1	1
HALT	TS	0	0	TS	TS	1

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Notes : 0 = Logic "0", 1 = Logic "1", TS = High Impedance

Table 8.2 TMP8085 Machine State Chart

MACHINE STATE	S_1, S_0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1°
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 +	X	TS	1	1	0
T_5	1	0 +	X	TS	1	1	0
T_6	1	0 +	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

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Notes : (1) 0 = LOGIC "0", 1 = Logic "1", TS = High Impedance, X = Unspecified
(2) °ALE not generated during 2nd and 3rd machine cycles of DAD instruction
(3) + IO/$\overline{M}$ = 1 during T_4-T_6 of INA maachine cycle

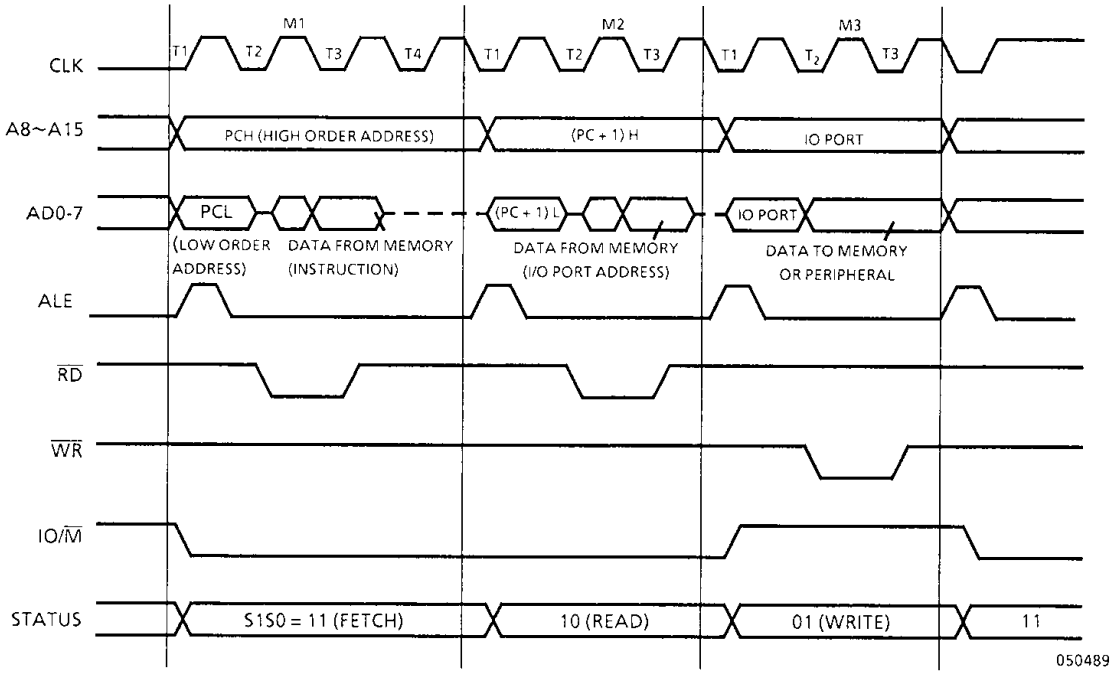

Figure 8.1 TMP8085A Basic System Timing

9. DRIVING THE X1 AND X2 INPUTS

The clock inputs of TMP8085A may be driven by a crystal oscilator, an LC tuned circuit, an RC network or an external clock source. The Minimum driving frequency must be 1 MHz, and must be twice as much as the desired internal clock frequency.

(1) Quartz Crystal Clock Driver

If a crystal used, it must have the following characteristics.

- Parallel resonance at twice the clock frequency desired
- C_S (shunt capacitance) $\leqq$ 7 pF
- R_S (equivalent shunt resistance) $\leqq$ 75 Ohms

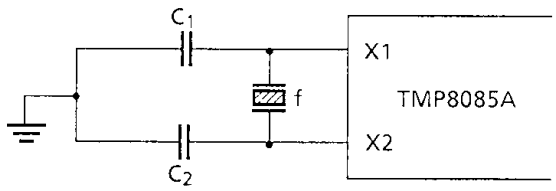

Figure 9.1

Note : A value of the external capacitors C_1 and C_2 between X1, X2 and ground.
The following values are recommended
1MHz $\leqq$ f < 4MHz : C_1 = 20pF, C_2 = 20pF
4MHz $\leqq$ f $\leqq$ 8MHz : C_1 = 10pF, C_2 = 10pF
8MHz < f $\leqq$ 10MHz : C_1 = 0, C_2 = 0

(2) LC Turned Circuit Clock Driver

A parallel-resonant LC circuit may be used as the frequency-determining network for TMP8085A, providing that its frequency tolerance of approximately 10% is acceptable. The components are chosen from the formula.

$$f = \frac{1}{2\pi\sqrt{L\,(C_{ext} + C_{int})}}$$

The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

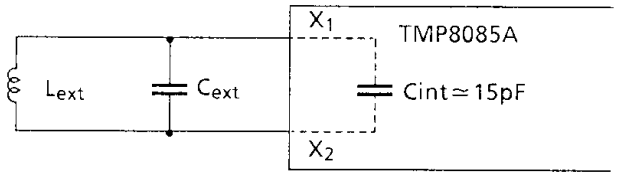

Figure 9.2

(3) RC Circuit Clock Driver

An RC circuit may be used in the case without precise clock frequency stability. Variations in the on-chip timing generation can cause a wide variation in frequency when using RC circuit. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

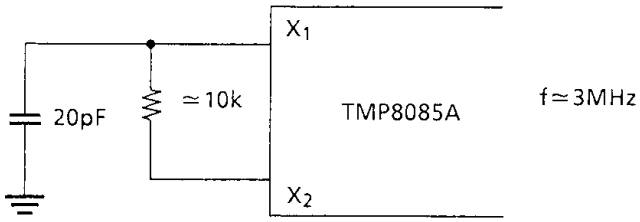

Figure 9.3

(4) External clock Driver Circuit

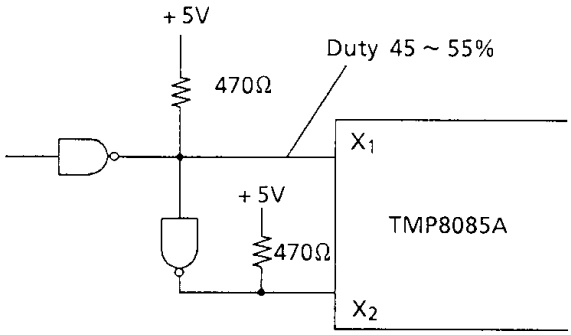

Figure 9.4

10. POWER-ON-RESET

The TMP8085A is not guaranteed to work until 10 ms after V_{CC} reaches 4.75V. It is suggested that $\overline{\text{RESETIN}}$ be kept low during this period. Note that the 10 ms period does not include the time it takes for the power supply to reach its 4.75V level.

For the TMP8085AHP-2, Power-on-reset can be performed when the supply voltage reaches 4.50V.

11. INSTRUCION SET

The code and function of machine instructions are shown as following table. In this table the symbols and abbreviated symbols are used for describing the instructions. However, the symbols required for special attention are explained on the page using them.

Explanation of Symbols

Division	Symbol	Description	
Register	r, g	Register	B, C, D, E, H, L, A
	t	Register pair	BC, DE, HL
		Stack pointer	SP
	q	Register pair	BC, DE, HL
		Program status word	PSW
Memory	mn	Memory address or immediate data indicated by 16 bits	
		m expresses higher 8 bits and n expresses lower 8 bits	
	(mn)	Contents of memory address indicated by mn	
	(HL)	Contents of memory address indicated by register pair	
		Contents of memory address indicated by register pair BC, DE and SP	
Flag status	0	Be reset to 0	
	1	Be set to 1	
	-	No change	
	*	Be affected by operation (be set to 0 or 1.)	
Operation symbol	←	Transfer	
	↔	Exchange	
	+	Addition	
	-	Subtraction	
	∧	Logical AND for every bit	
	∨	Logical OR for every bit	
	∀	Exclusive OR for every bit	
Other	IM	Interrupt mask register	
	CY	Carry flag	

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TLCS-85 List of Machine Instruction (1/2)

CLASS / ITEM	ASSEMBLER MNEMONIC	OBJECT CODE BIN (76 543 210)	OBJECT CODE HEX	FUNCTION	FLAGS CY	Z	S	P	AC	CYCL	STAT
8bit load	MOV g, r	01 ggg rrr	40 + g×8 + r	g ← r	–	–	–	–	–	1	4
	MOV g, M	01 ggg 110	46 + g×8	g ← (HL)	–	–	–	–	–	2	7
	MOV M, r	01 110 rrr	70 + r	(HL) ← r	–	–	–	–	–	2	7
	MVI g, n	00 ggg 110 nn nnn nnn	06 + g×8 n	g ← n	–	–	–	–	–	2	7
	MVI M, n	00 110 110 nn nnn nnn	36 n	(HL) ← n	–	–	–	–	–	3	10
	LDAX B	00 001 010	0A	A ← (BC)	–	–	–	–	–	2	7
	LDAX D	00 011 010	1A	A ← (DE)	–	–	–	–	–	2	7
	LDA mn	00 111 010 nn nnn nnn mm mmm mmm	3A n m	A ← (mn)	–	–	–	–	–	4	13
	STAX B	00 000 010	02	(BC) ← A	–	–	–	–	–	2	7
	STAX D	00 010 010	12	(DE) ← A	–	–	–	–	–	2	7
	STA mn	00 110 010 nn nnn nnn mm mmm mmm	32 n m	(mn) ← A	–	–	–	–	–	4	13
16bit load	LXI t, mn	00 tt0 001 nn nnn nnn mm mmm mmm	01 + t×16 n m	t ← mn	–	–	–	–	–	3	10
	LHLD mn	00 101 010 nn nnn nnn mm mmm mmm	2A n m	H ← (mn + 1) L ← (mn)	–	–	–	–	–	5	16
	SHLD mn	00 100 010 nn nnn nnn mm mmm mmm	22 n m	(mn + 1) ← H (mn) ← L	–	–	–	–	–	5	16
	SPHL	11 111 001	F9	SP ← HL	–	–	–	–	–	1	6
	PUSH q	11 qq0 101	C5 + q×6	(SP – 1)(SP – 2) ← q SP ← SP – 2	–	–	–	–	–	3	12
	POP q	11 qq0 001	C1 + q×6	q ← (SP + 1)(SP) SP ← SP + 2	– *	– *	– *	– *	– *	3	10
(a)	XCHG	11 101 011	EB	DE ↔ HL	–	–	–	–	–	1	4
	XTHL	11 100 011	E3	H ↔ (SP + 1), L ↔ (SP)	–	–	–	–	–	5	16
8bit arithmetic and logical	ADD r	10 000 rrr	80 + r	A ← A + r	*	*	*	*	*	1	4
	ADD M	10 000 110	86	A ← A + (HL)	*	*	*	*	*	2	7
	ADI n	11 000 110 nn nnn nnn	C6 n	A ← A + n	*	*	*	*	*	2	7
	ADC r	10 001 rrr	88 + r	A ← A + r + CY	*	*	*	*	*	1	4
	ADC M	10 001 110	8E	A ← A + (HL) + CY	*	*	*	*	*	2	7
	ACI n	11 001 110 nn nnn nnn	CE n	A ← A + n + CY	*	*	*	*	*	2	7
	SUB r	10 010 rrr	90 + r	A ← A – r	*	*	*	*	*	1	4
	SUB M	10 010 110	96	A ← A – (HL)	*	*	*	*	*	2	7
	SUI n	11 010 110 nn nnn nnn	D6 n	A ← A – n	*	*	*	*	*	2	7
	SBB r	10 011 rrr	98 + r	A ← A – r – CY	*	*	*	*	*	1	4
	SBB M	10 011 110	9E	A ← A – (HL) – CY	*	*	*	*	*	2	7
	SBI n	11 011 110 nn nnn nnn	DE n	A ← A – n – CY	*	*	*	*	*	2	7
	ANA r	10 100 rrr	A0 + r	A ← A ∧ r	0	*	*	*	1	1	4
	ANA M	10 100 110	A6	A ← A ∧ (HL)	0	*	*	*	1	2	7
	ANI n	11 100 110 nn nnn nnn	E6 n	A ← A ∧ n	0	*	*	*	1	2	7
	ORA r	10 110 rrr	B0 + r	A ← A ∨ r	0	*	*	*	0	1	4
	ORA M	10 110 110	B6	A ← A ∨ (HL)	0	*	*	*	0	2	7
	ORI n	11 110 110 nn nnn nnn	F6 n	A ← A ∨ n	0	*	*	*	0	2	7
	XRA r	10 101 rrr	A8 + r	A ← A ∀ r	0	*	*	*	0	1	4
	XRA M	10 101 110	AE	A ← A ∀ (HL)	0	*	*	*	0	2	7

rrr / ggg	Register
000	B
001	C
010	D
011	E
100	H
101	L
111	A

tt	Register
00	BC
01	DE
10	HL
11	SP

qq	Register
00	BC
01	DE
10	HL
11	PSW

PSW only

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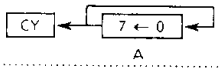
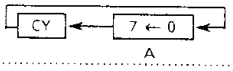
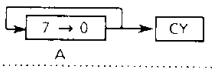
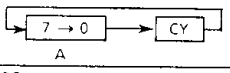
TLCS-85 List of Machine Instruction (2/2)

CLASS	ASSEMBLER MNEMONIC	OBJECT CODE BIN (76 543 210)	OBJECT CODE HEX	FUNCTION	FLAGS CY	Z	S	P	AC	CYCL	STAT
8bit arithmetic and logical	XRI n	11 101 110 nn nnn nnn	EE n	A←A∀n	0	*	*	*	0	2	7
	CMP r	10 111 rrr	B8+r	A-r	*	*	*	*	*	1	4
	CPM M	10 111 110	BE	A-(HL)	*	*	*	*	*	2	7
	CPI n	11 111 110 nn nnn nnn	FE n	A-n	*	*	*	*	*	2	7
	INR g	00 ggg 100	04+g×8	g ←g+1	–	*	*	*	*	1	4
	INR M	00 110 100	34	(HL)←(HL)+1	–	*	*	*	*	3	10
	DCR g	00 ggg 101	05+g×8	g ←g-1	–	*	*	*	*	1	4
	DCR M	00 110 101	35	(HL)←(HL)-1	–	*	*	*	*	3	10
(b)	DAA	00 100 111	27	Decimal adjust accumulator	*	*	*	*	*	1	4
	CMA	00 101 111	2F	A←NOT A	–	–	–	–	–	1	4
	CMC	00 111 111	3F	CY←NOT CY	*	–	–	–	–	1	4
	STC	00 110 111	37	CY←1	1	–	–	–	–	1	4
	NOP	00 000 000	00	no operation	–	–	–	–	–	1	4
	HLT	01 110 110	76	MPU halt	–	–	–	–	–	1	5
	DI	11 110 011	F3	INTE F/F Reset	–	–	–	–	–	1	4
	EI	11 111 011	FB	INTE F/F Set	–	–	–	–	–	1	4
(c)	DAD t	00 tt1 001	09+t×10	HL←HL+t	*	–	–	–	–	3	10
	INX t	00 tt0 011	03+t×10	t ←t+1	–	–	–	–	–	1	6
	DCX t	00 tt1 011	0B+t×10	t ←t+1	–	–	–	–	–	1	6
Rotate and sift	RLC	00 000 111	07		*	–	–	–	–	1	4
	RAL	00 010 111	17		*	–	–	–	–	1	4
	RRC	00 001 111	0F		*	–	–	–	–	1	4
	RAR	00 011 111	1F		*	–	–	–	–	1	4
Jump and call and return	JMP mn	11 000 011 nn nnn nnn mmmmmmmm	C3 n m	PC ←mn	–	–	–	–	–	3	10
	Jc mn	11 ccc 010 nn nnn nnn mmmmmmmm	C2+C×8 n m	IF cc is true, PC←mn otherwise, PC←PC+3	–	–	–	–	–	3 2	10 7
	PCHL	11 101 001	E9	PC ←HL	–	–	–	–	–	1	6
	CALL mn	11 001 101 nn nnn nnn mmmmmmmm	CD n m	(SP-1)(SP-2)←PC, SP ←SP-2, PC ←mn	–	–	–	–	–	5	18
	Cc mn	11 ccc 100 nn nnn nnn mmmmmmmm	C4+c×8 n m	IF c is ture, (SP-1)(SP-2) ←PC, SP←SP-2, PC←mn otherwise, PC←PC+3	–	–	–	–	–	5 2	18 9
	RET	11 001 001	C9	PC←(SP+1)(SP), SP←SP+2	–	–	–	–	–	3	10
	Rc	11 ccc 000	C0+C×8	IF c is true, PC←(SP+1)(SP), SP←SP+2 otherwise, PC←PC+1	–	–	–	–	–	3 1	12 6
	RST j	11 kkk 111	C7+k×8	(SP-1)(SP-2)←PC, SP←SP-2, PC←kkk×8	–	–	–	–	–	3	12
(d)	IN n	11 011 011 nn nnn nnn	DB n	A ←(n)	–	–	–	–	–	3	10
	OUT n	11 010 011 nn nnn nnn	D3 n	(n) ←A	–	–	–	–	–	3	10
(e)	RIM	00 100 000	20	A ←IM	–	–	–	–	–	1	4
	SIM	00 110 000	30	IM ←A	–	–	–	–	–	1	4

ccc	c	Condition
000	NZ	no zero
001	Z	zero
010	NC	no carry
011	C	carry
100	PO	parity odd
101	PE	parity even
110	P	sign positive
111	M	sign negative

kkk	j
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

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Note : "POP PSW" instruction changes state of flags.

(a) Exechange (b) General purpose arithmetic and MPU control
(c) 16bit arithmetic (d) Input and output (e) Interrupt

12. ELECTRICAL CARACTERISTICS

12.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Units
VCC	VCC Supply voltage	− 0.5 to + 7.0	V
PD	Power Dissipation	1.5	W
Tsolder	Soldering Temperature	260 (10 sec)	°C
Tstg	Storage Temperature	− 55 to 150	°C
Topr	Operating Temperature	0 to 70	°C

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12.2 DC CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5V ± 5% : TMP8085AP-2
VCC = 5V ± 10% : TMP8085AHP-2

Symbol	Parameter	Test Conditions	Min.	Max.	Units
VIL	Input Low Voltage		− 0.5	0.8	V
VIH	Input High Voltage		2.0	VCC + 0.5	V
VOL	Output Low Voltage	IOL = 2mA		0.45	V
VOH	Output High Voltage	IOH = − 400μA	2.4		V
ICC	Power Supply Current	TMP8085AP/AP-2		170	mA
		TMP8085AHP/AHP-2		135	
IIL	Input Leakage	0 ≦ VIN ≦ VCC		± 10	μA
ILO	Output Leakage	0.45 ≦ VOUT ≦ VCC		± 10	μA
VILR	Input Low Level (RESET)		− 0.5	0.8	V
VIHR	Input High Level (RESET)		2.4	VCC + 0.5	V
VHY	Hysteresis (RESET)		0.25		V

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12.3 AC CHARACTERISTICS

TA = 0°C to 70°C, V_{CC} = 5V ± 5% : TMP8085AP-2
VCC = 5V ± 10% : TMP8085AHP-2
Vss = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Units
tCYC	CLK Cycle Period	200	2000	ns
tL	CLK Low Time	40		ns
		50*		ns
tH	CLK High Time	70		ns
		80*		ns
tr, tf	CLK Rise and Fall Time		30	ns
tXKR	X1 Rising to CLK Rising	30	100	ns
tXKF	X1 Rising to CLK Falling	30	110	ns
tAC	A8-15 Valid to Leading Edge of Control [1]	115		ns
tACL	A0-7 Valid to Leading of Control	115		ns
tAD	A0-15 Valid to Valid Data In		350	ns
tAFR	Address Float after Leading Edge of ALE READ (INT)		0	ns
tAL	A8-15 Valid before Trailing Edge of ALE [1]	50		ns
tALL	A0-7 Valid before Trailing Edge of ALE	50		ns
tARY	READY Valid from Address Valid		100	ns
tCA	Address (A8-15) Valid after Control	60		ns
tCC	Width of Control Low (RD, WR, INTA) Edge of ALE	230		ns
tCL	Trailing Edge of Control to Leading Edge of ALE	25		ns
tDW	Data Valid to Trailing Edge of WRITE	230		ns
tHABE	HLDA to Bus Enable		150	ns
tHABF	Bus Float after HLDA		150	ns
tHACK	HLDA Valid to Trailing Edge of CLK	40		ns
tHDH	HOLD Hold Time	0		ns
tHDS	HOLD Setup Time to Trailing Edge of CLK	120		ns
tINH	INTR Hold Time	0		ns
tINS	INTR, RST and TRAP Setup Time to Falling	150		ns
tLA	Edge of CLK Address Hold Time after ALE	50		ns
tLC	Trailing Edge of ALE to Leading Edge of Control	60		ns

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Symbol	Parameter	Min.	Max.	Units
tLCK	ALE Low during CLK High	50		ns
tLDR	ALE to Valid Data during Read		270	ns
tLDW	ALE to Valid Data during Write		120	ns
tLL	ALE Width	80		ns
tLRY	ALE to READY Stable		30	ns
tRAE	Trailing Edge of READ to Re-Enabling of Address	90		ns
tRD	READ (or INTA) to Valid Data		150	ns
tRV	Control Trailing Edge of Leading Edge of Next Control	220		ns
tRDH	Data Hold Time After READ INTA	0		ns
tRYH	READY Hold Time	0		ns
tRYS	READY Setup Time to Leading Edge of CLK	100		ns
tWD	Data Valid After Trailing Edge of WRITE	60		ns
tWDL	LEADING Edge of WRITE to Data Valid		20	ns

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Test conditions CL = 150pF (*: CL = 50pF + 1TTL)
tcyc = 200ns

Notes : 1. A8-15 address specs apply to IO/M, S0 and S1 expect A8-15 are undifiend during T4-T6 of Cycle whereas IO/M, S0, and S1 are stable.
2. Timing defining signal voltage are;
Output High level = 2.0V, Low level = 0.8V
3. To calculate timing specifications at other value of tCYC use Table 12.1.

12.4 TIMING WAVEFORMS

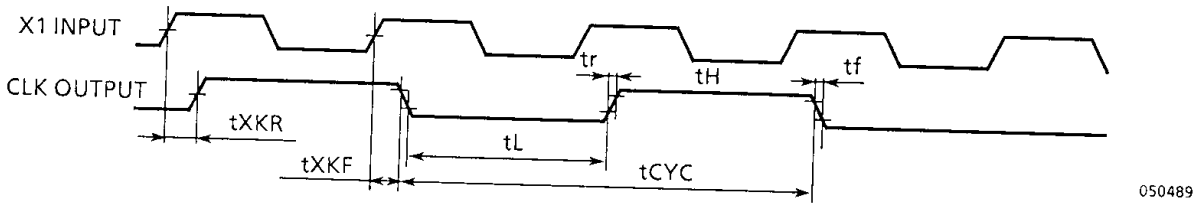


Figure 12.1 Clock Timing Waveform

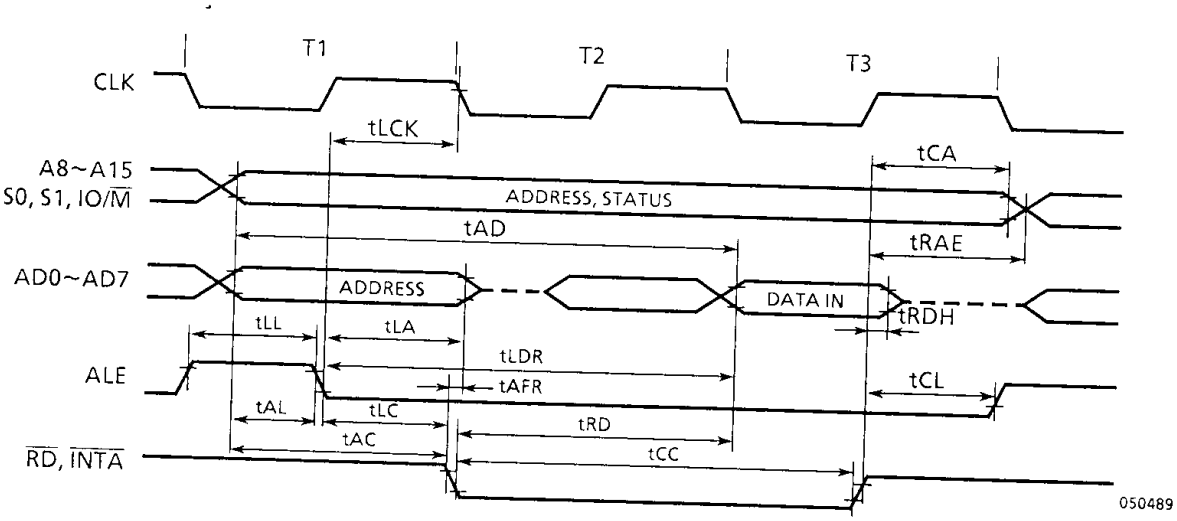


Figure 12.2 Read Operation

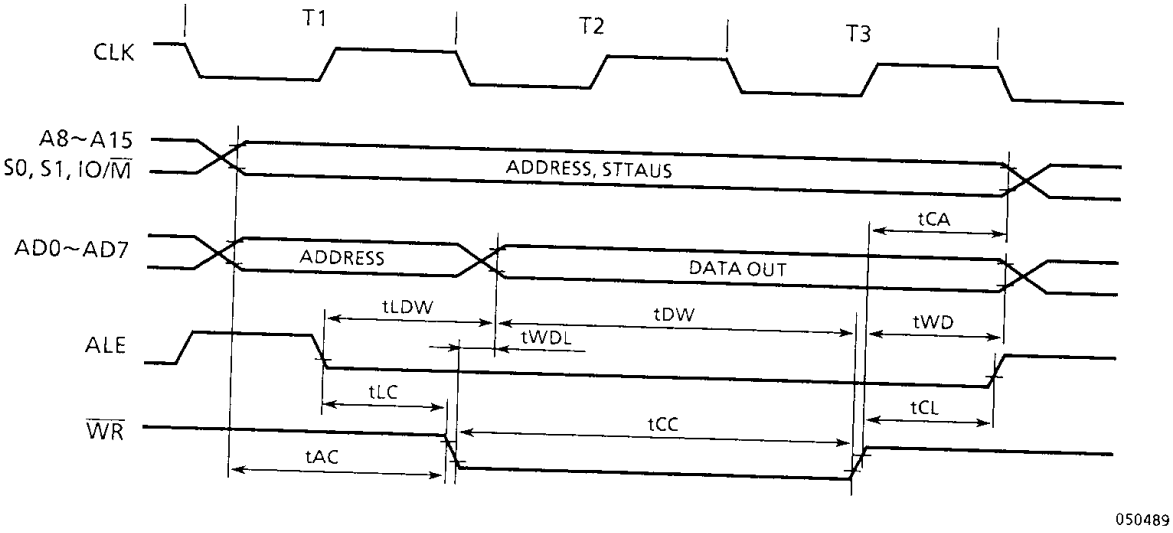


Figure 12.3 Write Operation

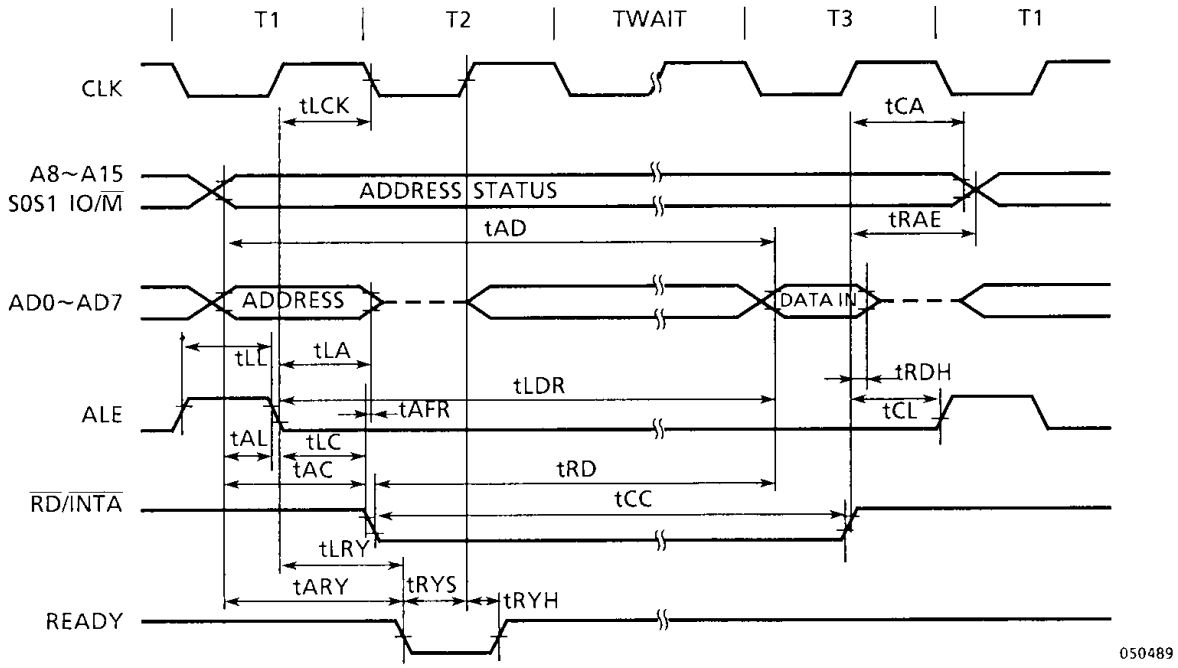


Figure 12.4 Read Operation with Wait Cycle (Typical)
- Same Ready Timing Applied to Write Operation

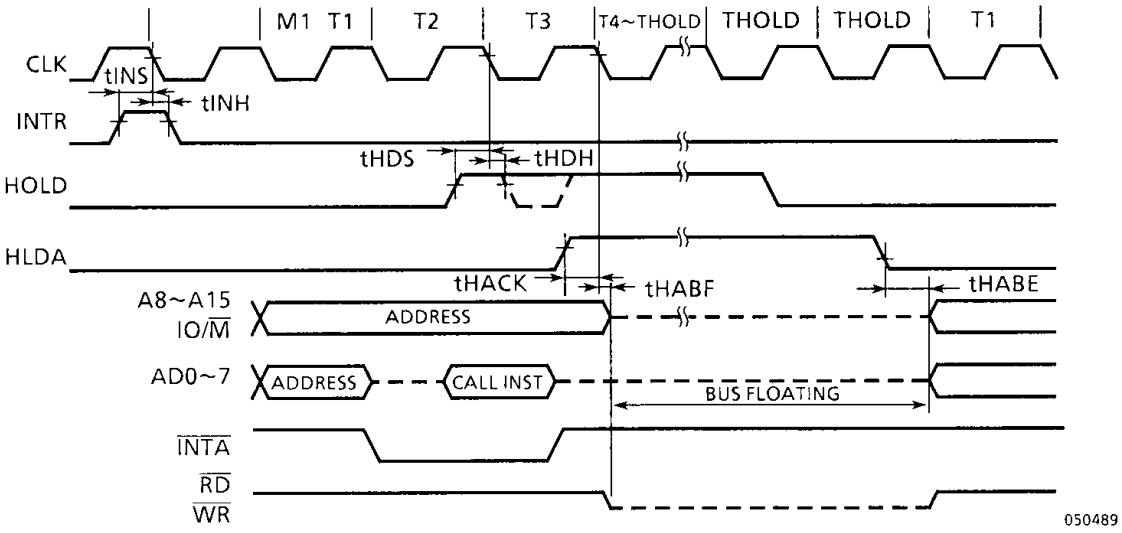
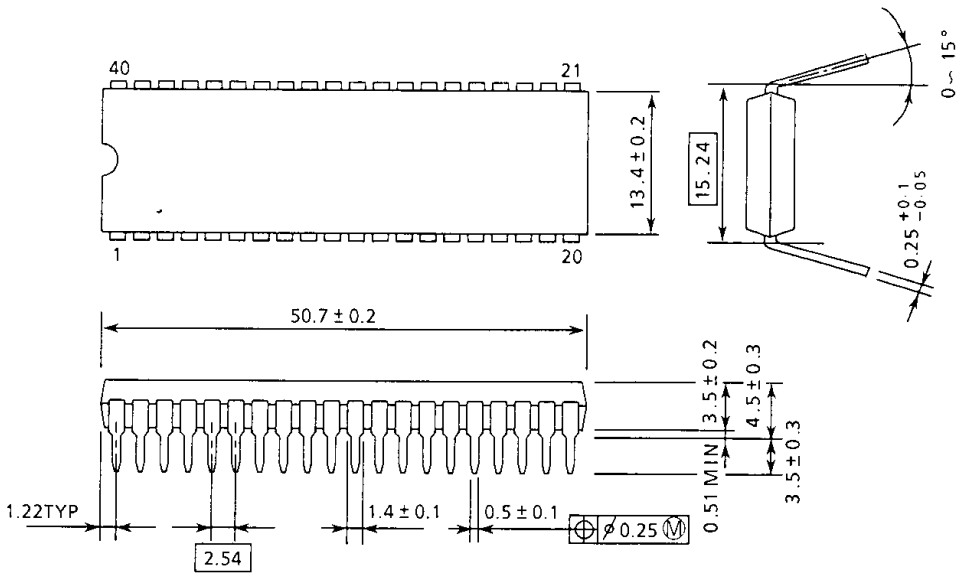


Figure 12.5 Interrupt and Hold Timing

13. OUTLINE DRAWING (40PINS PLASTIC PACKAGE)

DIP40-P-600

Unit : mm



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Note : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.