

1.2V Drive Pch MOSFET

EM6J1

● Structure

Silicon P-channel MOSFET

● Features

- 1) Two Pch MOSFET are put in EMT6 package.
- 2) High-speed switching.
- 3) Ultra low voltage drive (1.2V drive).
- 4) Built-in G-S Protection Diode.

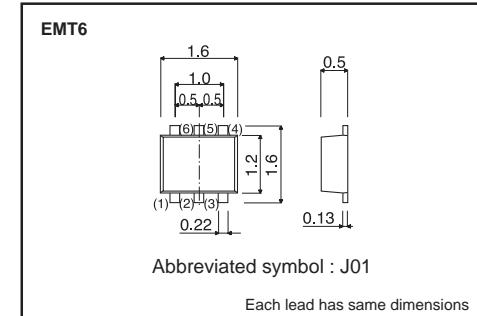
● Applications

Switching

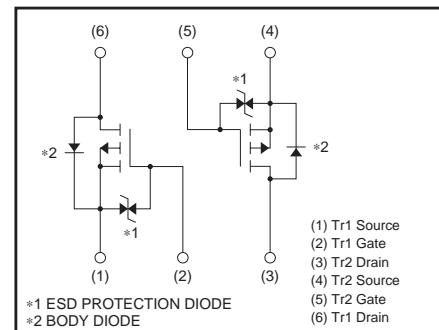
●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6J1		○

●Dimensions (Unit : mm)



● Inner circuit



● Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	-20	V	
Gate-source voltage	V _{GSS}	±10	V	
Drain current	Continuous	I _D	±200	mA
	Pulsed	I _{D^p} ^{*1}	±800	mA
Source current (Body Diode)	Continuous	I _S	-100	mA
	Pulsed	I _{S^p} ^{*1}	-800	mA
Total power dissipation		P _D ^{*2}	150	mW / TOTAL
			120	mW / ELEMENT
Channel temperature	T _{CH}	150	°C	
Range of storage temperature	T _{STG}	-55 to +150	°C	

*1 $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$

*2 Each terminal mounted on a recommended land

● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a)*	833	°C / W / TOTAL
		1042	°C / W / ELEMENT

* Each terminal mounted on a recommended land

●Electrical characteristics (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	—20	—	—	V	I _D =—1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	—	—	—1	μA	V _{DS} =—20V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	—0.3	—	—1.0	V	V _{DS} =—10V, I _D =—100μA
Static drain-source on-state resistance	R _{DS (on)} *	—	0.8	1.2	Ω	I _D =—200mA, V _{GS} =—4.5V
		—	1.0	1.5	Ω	I _D =—100mA, V _{GS} =—2.5V
		—	1.3	2.2	Ω	I _D =—100mA, V _{GS} =—1.8V
		—	1.6	3.5	Ω	I _D =—40mA, V _{GS} =—1.5V
		—	2.4	9.6	Ω	I _D =—10mA, V _{GS} =—1.2V
Forward transfer admittance	Y _{fs} *	0.2	—	—	S	V _{DS} =—10V, I _D =—200mA
Input capacitance	C _{iss}	—	115	—	pF	V _{DS} =—10V
Output capacitance	C _{oss}	—	10	—	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	—	6	—	pF	f=1MHz
Turn-on delay time	t _{d (on)} *	—	6	—	ns	V _{DD} =—10V I _D =—100mA
Rise time	t _r *	—	4	—	ns	V _{GS} =—4.5V
Turn-off delay time	t _{d (off)} *	—	17	—	ns	R _L =100Ω R _G =10Ω
Fall time	t _f *	—	17	—	ns	
Total gate charge	Q _g *	—	1.4	—	nC	V _{DD} =—10V, I _D =—200mA
Gate-source charge	Q _{gs} *	—	0.3	—	nC	V _{GS} =—4.5V
Gate-drain charge	Q _{gd} *	—	0.3	—	nC	R _L =50Ω, R _G =10Ω

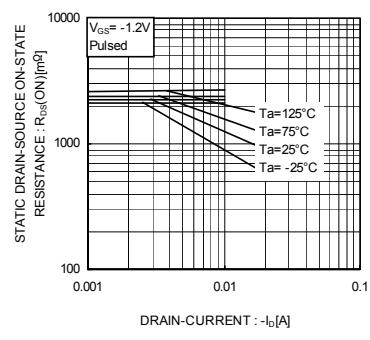
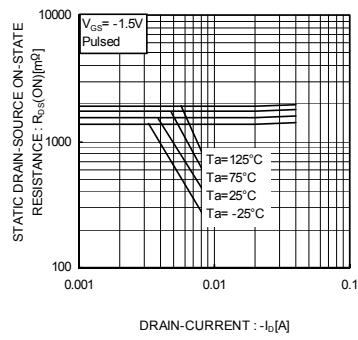
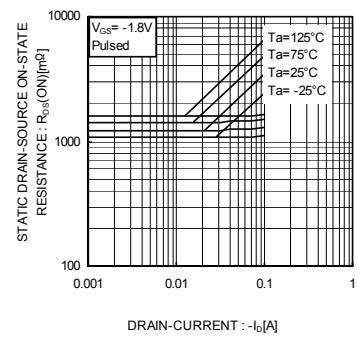
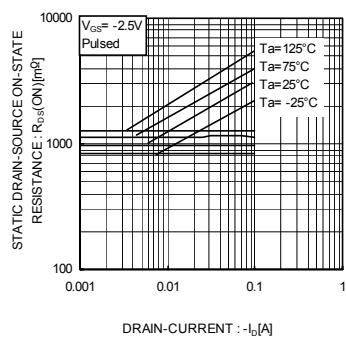
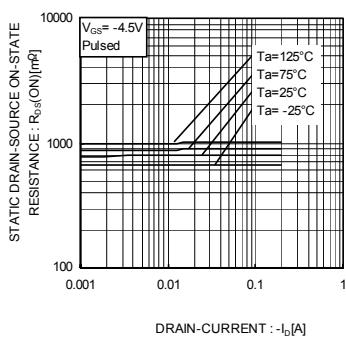
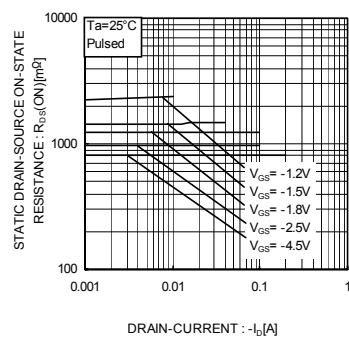
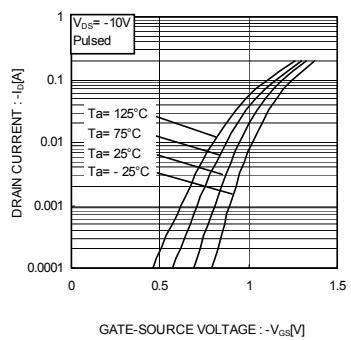
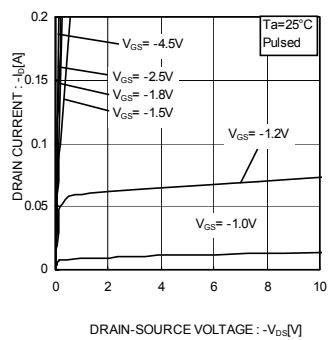
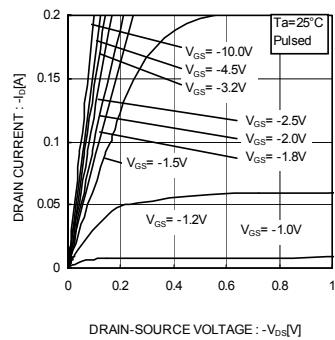
*Pulsed

●Body diode characteristics (Source-drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	—	—	—1.2	V	I _S =—200mA, V _{GS} =0V

*Pulsed

●Electrical characteristics curves



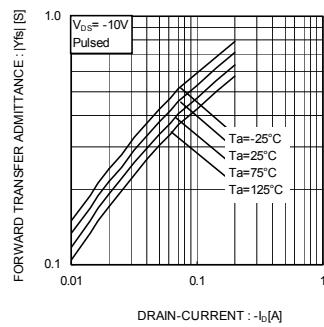


Fig.10 Forward Transfer Admittance vs. Drain Current

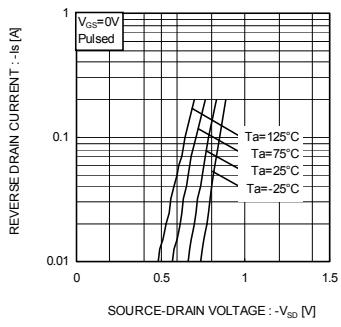


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

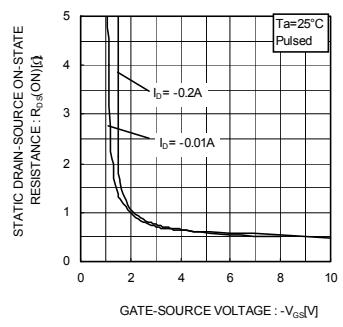


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

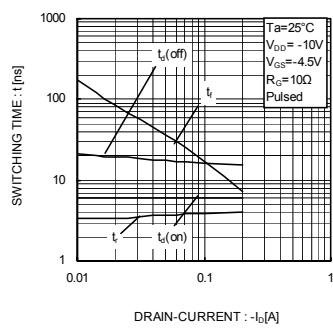


Fig.13 Switching Characteristics

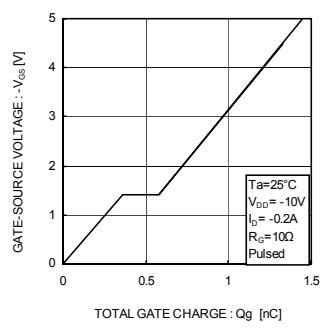


Fig.14 Dynamic Input Characteristics

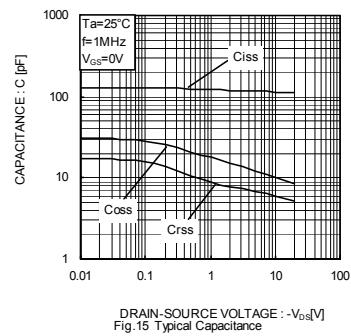


Fig.15 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

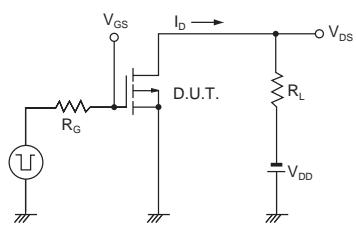


Fig.1-1 Switching Time Measurement Circuit

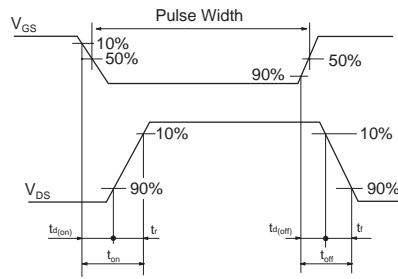


Fig.1-2 Switching Waveforms

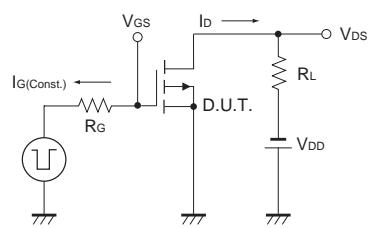


Fig.2-1 Gate Charge Measurement Circuit

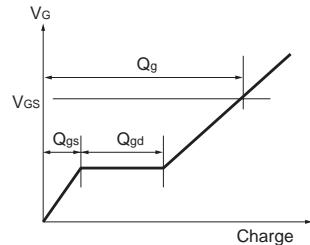


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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