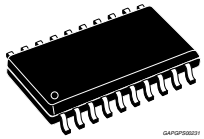
RL9904

Motor bridge controller

Datasheet - production data



SO-20

Features

- Operating supply voltage 8 V to 28 V, overvoltage max. 40 V
- Operating supply voltage 6 V with implemented step up converter
- Quiescent current in standby mode less than 50 µA
- ISO 9141 compatible interface
- Charge pump for driving a PowerMOS as reverse battery protection
- PWM operation frequency up to 30 kHz
- Programmable cross conduction protection time
- Overvoltage, undervoltage, short circuit and thermal protection
- Real time diagnostic
- Aerospace and Defense features
  - Dedicated traceability and part marking
  - Production parts approval documents available
  - Adapted Extended life time and obsolescence management
  - Extended Product Change Notification process
  - Designed and manufactured to meet sub ppm quality goals
  - Advanced mold and frame designs for Superior resilience to harsh environment (acceleration, EMI, thermal, humidity)
  - Single Fabrication, Assembly and Test site
  - Dual internal production source capability

Description

RL9904 is a control circuit for PowerMOS bridge driver with ISO 9141 bus interface.

Table 1. Device summary

Order code	Package	Packing
RL9904	SO-20	Tube
RL9904TR		Tape and reel

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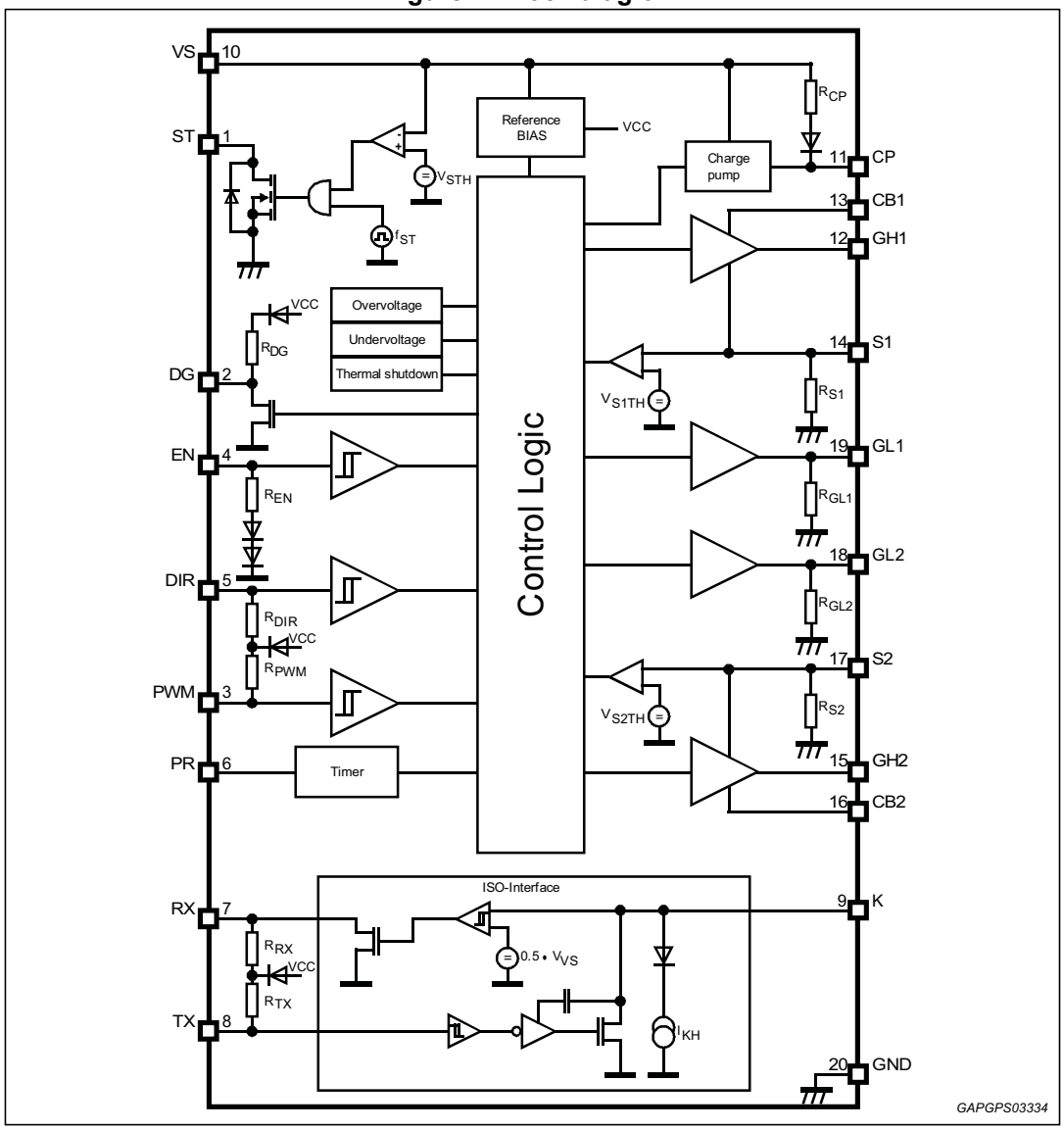
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection diagram (top view)

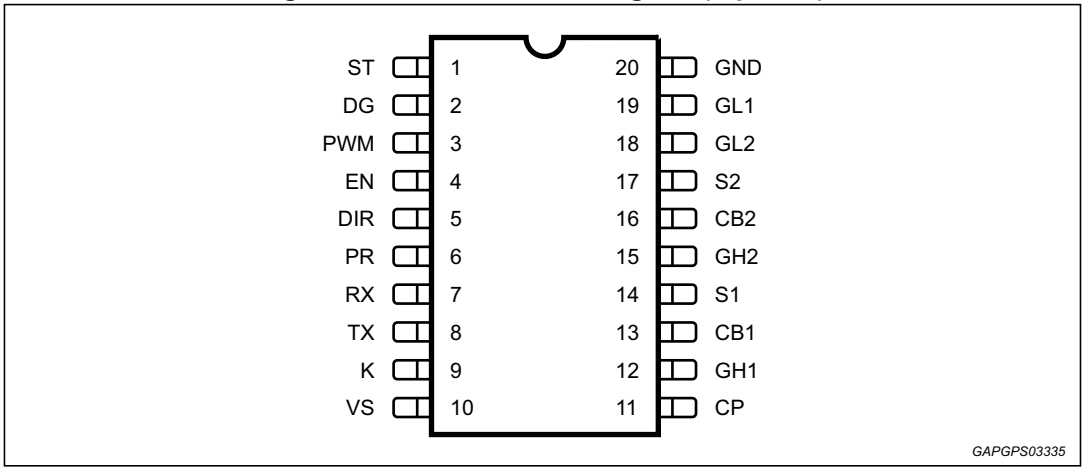


Table 2. Pins description

N#	Pin	Description
1	ST	Open Drain Switch for step up converter
2	DG	Open drain diagnostic output
3	PWM	PWM input for H-bridge control
4	EN	Enable input
5	DIR	Direction select input for H-bridge control
6	PR	Programmable cross conduction protection time
7	RX	ISO 9141 interface, receiver output
8	TX	ISO 9141 interface, transmitter input
9	K	ISO 9141 Interface, bidirectional communication K-line
10	VS	Supply voltage
11	CP	Charge pump for driving a PowerMOS as reverse battery protection
12	GH1	Gate driver for PowerMOS high side switch in half bridge 1
13	CB1	External bootstrap capacitor
14	S1	Source/drain of half bridge 1
15	GH2	Gate driver for PowerMOS high side switch in half bridge 2
16	CB2	External bootstrap capacitor
17	S2	Source/drain of half bridge 2
18	GL2	Gate driver for PowerMOS low side switch in half bridge 2
19	GL1	Gate driver for PowerMOS low side switch in half bridge 1
20	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CB1}, V_{CB2}	Bootstrap voltage	-0.3 to 40	V
I_{CB1}, I_{CB2}	Bootstrap current	-100	mA
V_{CP}	Charge pump voltage	-0.3 to 40	V
I_{CP}	Charge pump current	-1	mA
V_{DIR}, V_{EN}, V_{PWM}, V_{TX}	Logic input voltage	-0.3 to 7	V
I_{DIR}, I_{EN}, I_{PWM}, I_{TX}	Logic input current	±1	mA
V_{DG}, V_{RX}	Logic output voltage	-0.3 to 7	V
I_{DG}, I_{RX}	Logic output current	-1	mA
V_{GH1}, V_{GH2}	Gate driver voltage	-0.3 to V_{SX} + 10	V
I_{GH1}, I_{GH2}	Gate driver current	-1	mA
V_{GL1}, V_{GL2}	Gate driver voltage	-0.3 to 10	V
I_{GL1}, I_{GL2}	Gate driver current	-10	mA
V_K	K-line voltage	-20 to V_S	V
V_{PR}	Programming input voltage	-0.3 to 7	V
I_{PR}	Programming input current	-1	mA
V_{S1}, V_{S2}	Source/drain voltage	-2 to V_{VS} + 2	V
I_{S1}, I_{S2}	Source/drain current	-10	mA
V_{ST}	Output voltage	-0.3 to 40	V
I_{ST}	Step up output current	-1	mA
V_{VSDC}	DC supply voltage	-0.3 to 28	V
V_{VSP}	Pulse supply voltage (T < 500ms)	40	V
I_{VS}	DC supply current	-100	mA

Warning: **For externally applied voltages or currents exceeding these limits damage of the device may occur!**
All pins of the IC are protected against ESD. The verification is performed according to MIL883C, human body model with R = 1.5 kΩ, C = 100 pF and discharge voltage ±2 kV, corresponding to a maximum discharge energy of 0.2 mJ.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
T_J	Operating junction temperature	-40 to 150	°C
T_{JSD}	Junction temperature thermal shutdown threshold	min 150	°C
T_{JSDH}	Junction thermal shutdown hysteresis	typ 15	°C
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	85	°C/W

3.3 Electrical characteristics

8 V < V_{VS} < 20 V, V_{EN} = HIGH, -40°C ≤ T_J ≤ 150 °C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when current flows into the pin.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply (VS)						
$V_{VS\ OVH}$	Overvoltage disable HIGH threshold	-	28	33	36	V
$V_{VS\ OVh}$	Overvoltage threshold hysteresis (1)	-	-	1.6	-	V
$V_{VS\ UVH}$	Undervoltage disable HIGH threshold	-	6	-	7	V
$V_{VS\ UVh}$	Undervoltage threshold hysteresis (1)	-	-	0.66	-	V
I_{VSL}	Supply current	V_{EN} = 0; V_{VS} = 13.5 V; T_J< 85 °C	-	-	50	µA
I_{VSH}	Supply current, PWM-mode	V_{VS} = 13.5 V; V_{EN} = HIGH; V_{DIR} = LOW; S1 = S2 = GND f_{PWM} = 20 kHz; C_{CBX} = 0.1 µF; C_{GLX} = 4.7 nF; C_{GHX} = 4.7 nF; R_{PR} = 10 kΩ; C_{PR} = 150 pF	-	8.1	13	mA
I_{VSD}	Supply current, DC-mode	V_{VS} = 13.5 V; V_{EN} = HIGH; V_{DIR} = LOW; S1 = S2 = GND V_{PWM} = LOW; C_{GHX} = 4.7nF R_{PR} = 10 kΩ; C_{PR} = 150 pF	-	5.8	10	mA
Enable input (EN)						
V_{ENL}	Low level	-	-	-	1.5	V
V_{ENH}	High level	-	3.5	-	-	V
V_{ENh}	Hysteresis threshold (1)	-	-	1	-	V
R_{EN}	Input pull down resistance	V_{EN} = 5 V	16	50	100	kΩ
H-bridge control inputs (DIR, PWM)						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DIRL} V_{PWML}	Input low level	-	-	-	1.5	V
V_{DIRH} V_{PWMH}	Input high level	-	3.5	-	-	V
V_{DIRh} V_{PWMh}	Input threshold hysteresis (1)	-	-	1	-	V
R_{DIR} R_{PWM}	Internal pull up resistance to internal VCC(2)	V_{DIR} = 0; V_{PWM} = 0	16	50	100	kΩ
DIAGNOSTIC output (DG)						
V_{DG}	Output drop	I_{DG} = 1 mA	-	-	0.6	V
R_{DG}	Internal pull up resistance to internal VCC (2)	V_{DG} = 0 V	10	20	40	kΩ
Programmable cross conduction protection(3)						
N_{PR}	Threshold voltage ratio V_{PRH}/V_{PRL}	R_{PR} = 10 kΩ	1.8	2	2.2	-
I_{PR}	Current capability	V_{PR} = 2 V	-0.5	-	-	mA
ISO interface, transmission input (TX)						
V_{TXL}	Input low level	-	-	-	1.5	V
V_{TXH}	Input high level	-	3.5	-	-	V
V_{TXh}	Input hysteresis voltage (1)	-	-	1	-	V
R_{TX}	Internal pull up resistance to internal VCC (2)	V_{TX} = 0	10	20	40	kΩ
ISO interface, receiver output (RX)						
V_{RXL}	Output voltage high stage	TX = HIGH; I_{RX} = 0; V_K = V_{VS}	4.5	-	5.5	V
R_{RX}	Internal pull up resistance to internal VCC (2)	TX = HIGH; V_{RX} = 0V	5	10	20	kΩ
R_{RXON}	ON resistance to ground	TX = LOW; I_{RX} = 1mA	-	40	90	Ω
t_{RXH}	Output high delay time	See *Figure 3 on page 13*	-	0.5	-	µs
t_{RXL}	Output low delay time	-	-	0.5	-	µs
ISO interface, K-line (K)						
V_{KL}	Input low level	-	-20 V	-	0.45 · V_{VS}	-
V_{KH}	Input high level	-	0.55 · V_{VS}	-	V_{VS}	-
V_{Kh}	Input hysteresis voltage (1)	-	-	0.025· V_{VS}	0.8V	-
I_{KH}	Input current	V_{TX} = HIGH	-5	-	25	µA
R_{KON}	ON resistance to ground	V_{TX} = LOW; I_K = 10 mA	-	10	30	Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{KSC}	Short circuit current	V_{TX} = LOW	40	-	130	mA
f_K	Transmission frequency	-	60	100		kHz
t_{Kr}	Rise time	V_{VS} = 13.5 V; See *Figure 3 on page 13* External loads at K-line: R_K = 510 Ω pull up to V_{VS} C_K = 2.2 nF to GND	-	2	6	µs
t_{Kf}	Fall time	-	-	2	6	µs
t_{KH}	Switch high delay time	-	-	4	17	µs
t_{KL}	Switch low delay time	-	-	4	17	µs
t_{SH}	Short circuit detection time	V_{VS} = 13.5 V; TX = LOW $V_K > 0.55 \cdot V_{VS}$	10	-	40	µs
Charge pump						
V_{CP}	Charge pump voltage	V_{VS} = 8 V	V_{VS}+ 7 V	-	V_{VS}+ 14 V	-
		V_{VS} = 13.5 V	V_{VS}+ 10 V	-	V_{VS}+ 14 V	-
		V_{VS} = 20 V	V_{VS}+ 10 V	-	V_{VS} +14 V	-
I_{CP}	Charging current $V_{CP} = V_{VS}$ + 8 V	V_{VS} = 13.5 V	-50	-75	-	µA
t_{CP}	Charging time (1) $V_{CP} = V_{VS}$ + 8 V	V_{VS} = 13.5V C_{CP} = 10 nF	-	1.2	4	ms
f_{CP}	Charge pump frequency	V_{VS} = 13.5 V	250	500	750	kHz
Drivers for external high side PowerMOS						
V_{CB1} V_{CB2}	Bootstrap voltage	V_{VS} = 8 V; I_{CBX} = 0; V_{SX} = 0 V_{VS} = 13.5 V; I_{CBX} = 0; V_{SX} = 0 V_{VS} = 20 V; I_{CBX} = 0; V_{SX} = 0	7.5 10 10	-	14 14 14	V V V
R_{GH1L} R_{GH2L}	ON-resistance of SINK stage	V_{CBX} = 8 V; V_{SX} = 0 I_{GHX} = 50 mA; T_J = 25 °C	-	-	10	Ω
		V_{CBX} = 8 V; V_{SX} = 0 I_{GHX} = 50 mA; T_J = 125 °C	-	-	20	Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{GH1H} R_{GH2H}	ON-resistance of SOURCE stage	I_{GHX} = -50 mA; T_J = 25 °C	-	-	10	Ω
		I_{GHX} = -50 mA; T_J = 125 °C	-	-	20	Ω
V_{GH1H} V_{GH2H}	Gate ON voltage (SOURCE)	V_{VS} = V_{SX} = 8 V; I_{GHX} = 0; C_{CBX} = 0.1 µF	V_{VS} +6.5 V	-	V_{VS} +14 V	-
		V_{VS} = V_{SX} = 13.5 V; I_{GHX} = 0; C_{CBX} = 0.1 µF	V_{VS}+ 10 V	-	V_{VS} +14 V	-
		V_{VS} = V_{SX} = 20 V; I_{GHX} = 0; C_{CBX} = 0.1 µF	V_{VS} +10 V	-	V_{VS} +14 V	-
R_{GH1} R_{GH2}	Gate discharge resistance	EN = LOW	10	100	-	kΩ
R_{S1} R_{S2}	Sink resistance	-	10	100	-	kΩ
Drivers for external low side PowerMOS						
R_{GL1L} R_{GL2L}	ON-resistance of SINK stage	I_{GLX} = 50 mA; T_J = 25 °C	-	-	10	Ω
		I_{GLX} = 50 mA; T_J = 125 °C	-	-	20	Ω
$R_{GL1H,}$ R_{GL2H}	ON-resistance of SOURCE stage	I_{GLX} = -50 mA; T_J = 25 °C	-	-	10	Ω
		I_{GLX} = -50 mA; T_J = 125 °C	-	-	20	Ω
$V_{GL1H,}$ V_{GL2H}	Gate ON voltage (SOURCE)	V_{VS} = 8 V; I_{GLX} = 0 V_{VS} = 13.5 V; I_{GLX} = 0 V_{VS} = 20 V; I_{GLX} = 0	7 V 10 V 10 V	-	V_{VS} V_{VS} 14 V	-
R_{GL1} R_{GL2}	Gate discharge resistance	EN = LOW	10	100	-	kΩ
Timing of the drivers						
t_{GH1LH} t_{GH2LH}	Propagation delay time	See *Figure 4 on page 13* V_{VS} = 13.5V V_{S1} = V_{S2} =0 C_{CBX} = 0.1µF R_{PR}= 10 kΩ	-	-	500	ns
t_{GH1LH} t_{GH2LH}	Propagation delay time including cross conduction protection time t_{CCP}	See *Figure 4 on page 13* V_{VS} = 13.5 V V_{S1} = V_{S2} = 0 C_{CBX} = 0.1 µF C_{PR} = 150 pF; R_{PR}= 10 kΩ(4)	0.7	1	1.3	µs
t_{GH1HL} t_{GH2HL}	Propagation delay time		-	-	500	ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{GL1LH} t_{GL2LH}	Propagation delay time	See *Figure 4 on page 13* V_{VS} = 13.5 V V_{S1} = V_{S2} =0 C_{CBX} = 0.1 µF R_{PR}= 10 kΩ	-	-	500	ns
t_{GL1LH} t_{GL2LH}	Propagation delay time including cross conduction protection time t_{CCP}	See *Figure 4 on page 13* V_{VS} = 13.5 V V_{S1} = V_{S2} = 0 C_{CBX} = 0.1 µF C_{PR} = 150 pF; R_{PR} = 10 kΩ; (4)	0.7	1	1.3	µs
t_{GL1HL} t_{GL2HL}	Propagation delay time		-	-	500	ns
t_{GH1r} t_{GH2r}	Rise time	See *Figure 4 on page 13* V_{VS} = 13.5 V V_{S1} = V_{S2} = 0 C_{CBX} = 0.1 µF C_{GHX} = 4.7 nF C_{GLX} = 4.7 nF R_{PR} = 10 kΩ;	-	-	1	µs
t_{GH1f} t_{GH2f}	Fall time		-	-	1	µs
t_{GL1r} t_{GL2r}	Rise time		-	-	1	µs
t_{GL1f} t_{GL2f}	Fall time		-	-	1	µs
Short Circuit Detection						
V_{S1TH} V_{S2TH}	Threshold voltage	-	-	4	-	V
t_{SCd}	Detection time	-	5	10	15	µs
Step up converter (ST) (5.2 V ≤ V_{VS} < 10 V)						
V_{STH}	ST disable HIGH threshold	-	-	-	10	V
V_{STh}	ST disable threshold hysteresis voltage (1)	-	1	-	2	V
R_{DSON}	Open drain ON resistance	V_{VS} = 5.2 V; I_{ST} = 50 mA	-	-	20	W
f_{ST}	Clock frequency	-	50	100	149	kHz

1. Not tested in production: guaranteed by design and verified in characterization.
2. Internal V_{VCC} is 4.5 V to 5.5 V.
3. See *Section 4.13 on page 19* for calculation of programmable cross conduction protection time
4. Tested with differed values in production but guaranteed by design and verified in characterization

Figure 3. Timing of the ISO-interface

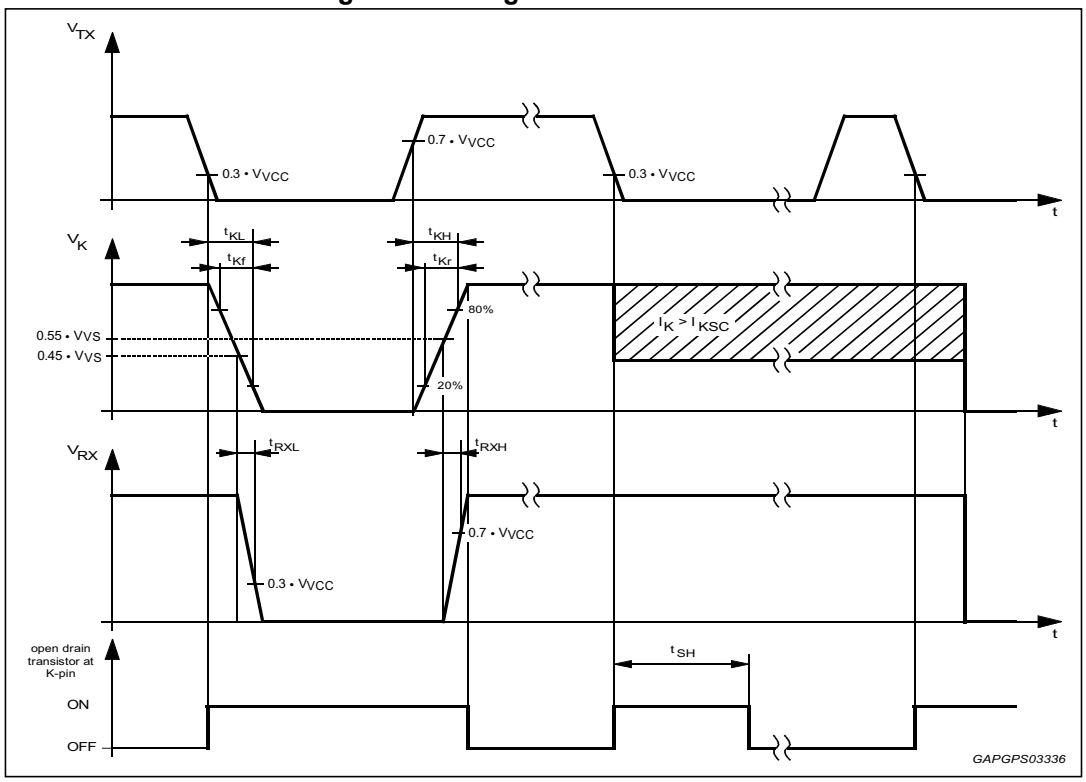


Figure 4. Timing of the drivers for the external MOS regarding the inputs DIR and PWM

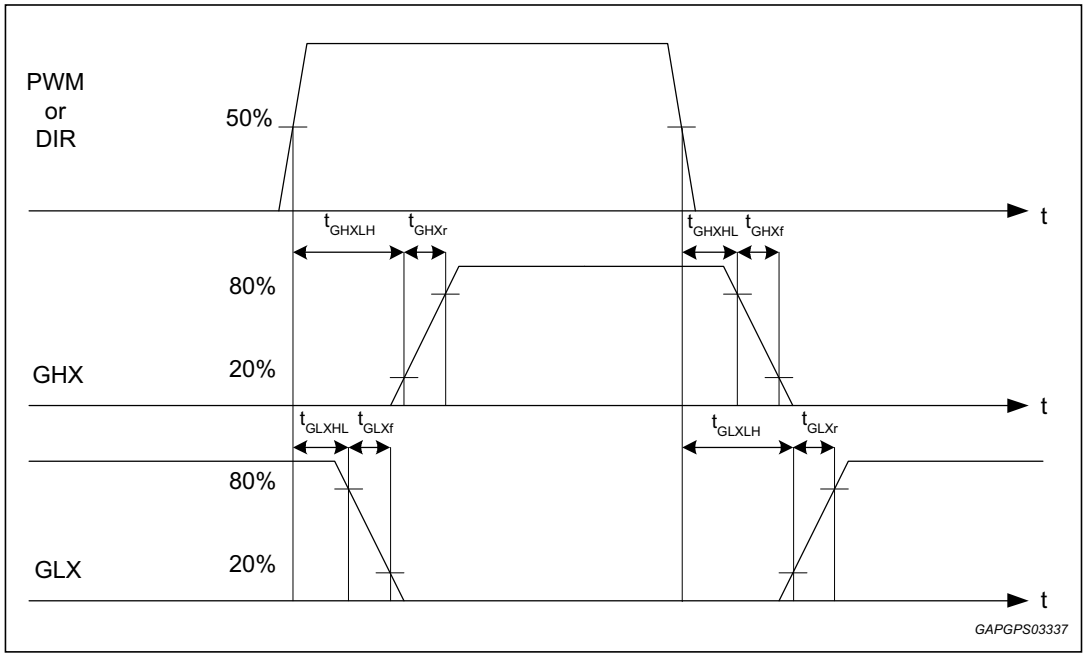


Figure 5. I(V) characteristics of the K-Line for TX = HIGH and V_{VS} = 13.5 V

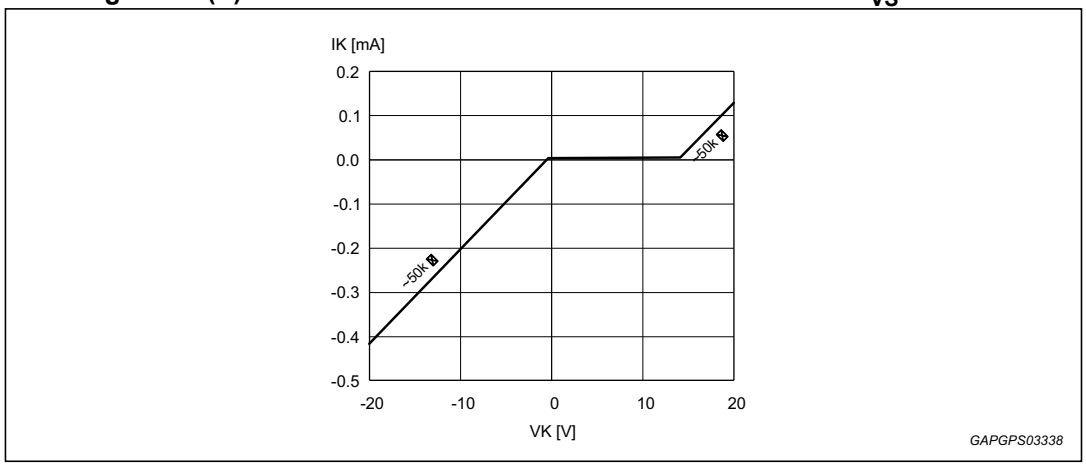
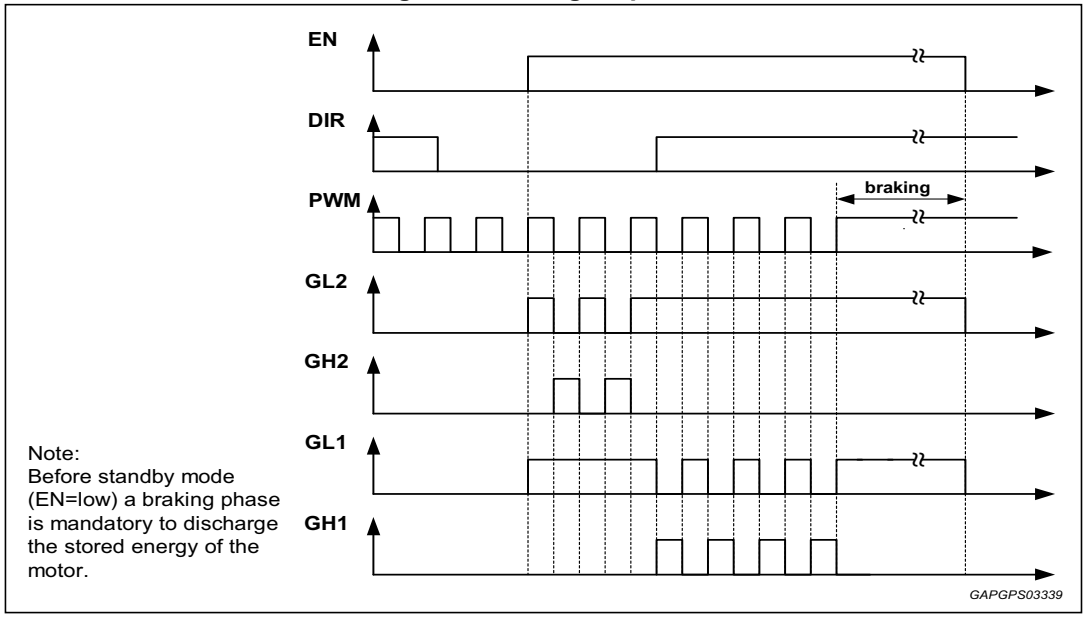


Figure 6. Driving sequence



Note:
Before standby mode (EN=low) a braking phase is mandatory to discharge the stored energy of the motor.

Figure 7. Charging time of an external capacitor of 10 nF connected to CP pin at V_{VS} = 8 V and V_{VS} = 13.5 V

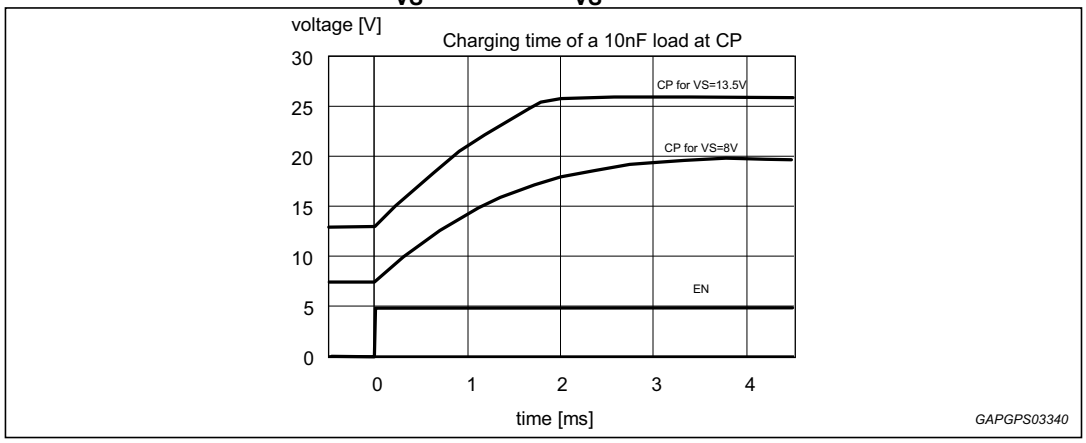
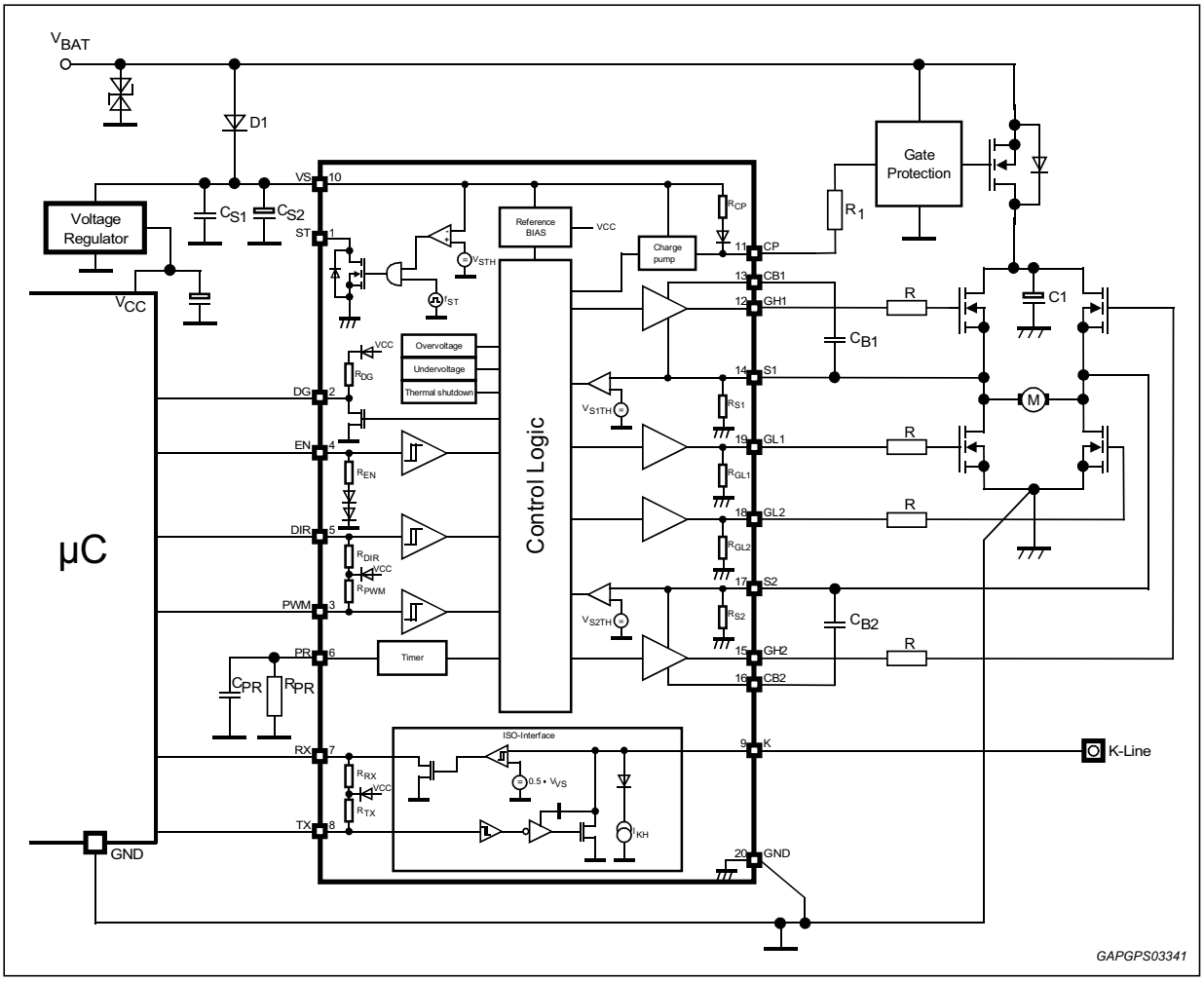


Figure 8. Application circuit diagram



4 Functional description

4.1 General

The RL9904 integrated circuit (IC) is designed to control four external N-channel MOS transistors in H-Bridge configuration for DC-motor driving. It includes an ISO9141 compatible interface. A typical application is shown in *Figure 8*.

4.2 Voltage supply

The IC is supplied via an external reverse battery protection diode to the V_{VS} pin. The typical operating voltage range is down to 8 V.

The supply current consumption of the IC composes of static and a dynamic part. The static current is typically 5.8 mA. The dynamical current I_{dyn} is depending of the PWM frequency f_{PWM} and the required gate charge Q_{Gate} of the external power mos transistor. The current can be estimated by the expression:

$$I_{dyn} = 2 \cdot f_{PWM} \cdot Q_{Gate}$$

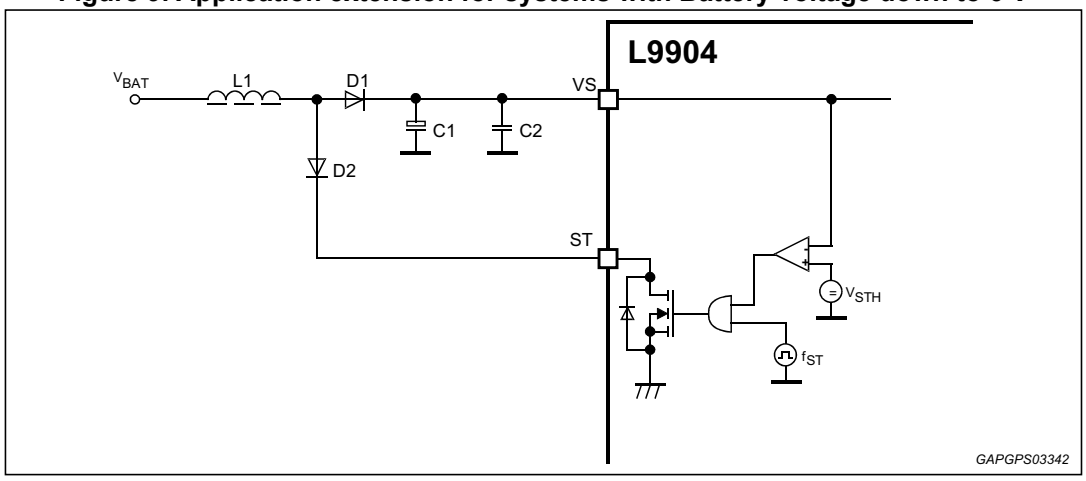
An external power transistor with a gate charge of Q_{Gate} = 160 nC and a PWM frequency of f_{PWM} = 20 kHz requires a dynamical supply current of I_{dyn} = 6.4 mA.

The total supply current consumption is I_{VS} = 5.8 mA + 6.4 mA = 12.2 mA.

4.3 Extended supply voltage range (ST)

The operating battery voltage range can be extended down to 6 V using the additional components shown in *Figure 9*. A small inductor of L~150 µH (I_{peak}~500 mA) in series to the battery supply built up a step up converter with the switching open drain output ST. The switching frequency is typical 100 kHz with a fixed duty cycle of 50 %. The step up converter starts below V_{VS} < 8 V, increases the supply voltage at the V_S pin and switches off at V_{VS} > 10 V to avoid EME at nominal battery voltage. The diode D2 in series with the ST pin is necessary only for systems with negative battery voltage. No additional load can be driven by the step up converter.

Figure 9. Application extension for systems with Battery voltage down to 6 V



4.4 Control inputs (EN, DIR, PWM)

The CMOS level inputs drive the device as shown in *Figure 6* and described in the truth table.

The device is activated with enable input HIGH signal. For enable input floating (not connected) or VEN = 0 V the device is in standby mode. When activating the device a wake-up time of 50 µs is recommended to stabilize the internal supplies.

The DIR and PWM inputs control the driver of the external H-Bridge transistors. The motor direction can be chosen with the DIR input, the duty cycle and frequency with the PWM input. Unconnected inputs are defined by internal pull up resistors. During wake-up and braking and before dis-activating the IC via enable both inputs should be driven HIGH.

Table 6. Truth table

Status	Control inputs			Device status				Driver stage for external PowerMOS				Diagnostic	Comment
	EN	DIR	PWM	TS	OV	UV	SC	GH1	GL1	GH2	GL2	DG	
1	0	x	x	x	x	x	x	R(1)	R	R(1)	R	T	standby mode
2	1	x	x	1	0	0	0	L	L	L	L	L	thermal shutdown
3	1	x	x	0	1	0	0	L	L	L	L	L	overvoltage
4	1	x	x	0	0	1	0	L	L	L	L	L	undervoltage
5	1	x	x	0	0	0	1	X(2)	X(2)	X(2)	X(2)	L	short circuit (2)
6	1	0	0	0	0	0	0	L	H	H	L	H	-
7	1	x	1	0	0	0	0	L	H	L	H	H	braking mode
8	1	1	0	0	0	0	0	H	L	L	H	H	-

1. See Application Note AN2229.
2. Only those external MOS transistors of the H-Bridge which are in short circuit condition are switched off. All others remain driven by DIR and PWM.

Symbols:

x Don't care
0: Logic LOW or not active
1: Logic HIGH or active

R: Resistive output
L: Output in sink condition
H: Output in source condition
T: Tristate

TS:Thermal shutdown
OV:Overvoltage
UV:Undervoltage
SC:Short Circuit

4.5 Thermal shutdown

When the junction temperature exceeds T_{JSD} all driver are switched in sink condition (L), the K- output is off and the diagnostic DG is LOW until the junction temperature drops below T_{JSD} - T_{JHYST}.

4.6 Overvoltage shutdown

When the supply voltage V_{VS} exceeds the overvoltage threshold V_{VSOVH} all driver are switched in sink condition (L), the K- output is off and the diagnostic DG is LOW.

4.7 Undervoltage shutdown

For supply voltages below the undervoltage disable threshold the gate driver remains in sink condition (L) and the diagnostic DG is low.

4.8 Short circuit detection

The output voltage at the S1 and S2 pin of the H-Bridge is monitored by comparators to detect shorts to ground or battery. The activated external high-side MOS transistor will be switched off if the voltage drop remains below the comparator threshold voltage V_{S1TH} and V_{S2TH} for longer than the short current detection time t_{SCd}. The transistor remains in off condition, the diagnostic output goes LOW until the DIR or PWM input status will be changed. The status doesn't change for the other MOS transistors. The external low-side MOS transistor will be switched off if the voltage drop passes over the comparator threshold voltage V_{S1TH} and V_{S2TH} for longer than the short current detection time t_{SCd}. The transistor remains in off condition, the diagnostic output goes LOW until the DIR or PWM input status will be changed. The status doesn't change for the other MOS transistors.

4.9 Diagnostic output (DG)

The diagnostic output provides a real time error detection, if monitors the following error stacks: Thermal shutdown, overvoltage shutdown, undervoltage shutdown and short circuit shutdown. The open drain output with internal pull up resistor is LOW if an error is occurring.

4.10 Bootstrap capacitor (CB1, CB2)

To ensure, that the external PowerMOS transistors reach the required R_{DSON}, a minimum gate source voltage of 5 V for logic level and 10V for standard PowerMOS transistors has to be guaranteed. The high-side transistors require a gate voltage higher than the supply voltage. This is achieved with the internal charge pump circuit in combination with the bootstrap capacitor. The bootstrap capacitor is charged, when the high-side MOS transistor is OFF and the low-side is ON. When the low-side is switched OFF, the charged bootstrap capacitor is able to supply the gate driver of the high-side PowerMOS transistor. For effective charging the values of the bootstrap capacitors should be larger than the gate-source capacitance of the PowerMOS and respect the required PWM ratio.

4.11 Charge pump circuit (CP)

The reverse battery protection can be obtained with an external N-channel MOS transistor as shown in *Figure 8*. In this case its drain-bulk diode provides the protection. The output CP is intended to drive the gate of this transistor above the battery voltage to switch on the MOS and to bypass the drain-bulk diode with the R_{DSON}. The CP has a connection to VS through an internal diode and a 20 kΩ resistor.

4.12 Gate drivers for the external N-channel PowerMOS transistors (GH1, GH2, GL1, GL2)

High level at EN activates the driver of the external MOS under control of the DIR and PWM inputs (see *Table 6: Truth table* and driving sequence *Figure 6*). The external PowerMOS gates are connected via series resistors to the device to reduce electro magnetic emission (EME) of the system. The resistors influence the switching behaviour. They have to be chosen carefully. Too large resistors enlarge the charging and discharging time of the PowerMOS gate and can generate cross current in the half-bridges. The driver assures a longer switching delay time from source to sink stage in order to prevent the cross conduction.

The gate source voltage is limited to 14 V. The charge/discharge current is limited by the R_{DSON} of the driver. The drivers are not protected against shorts.

4.13 Programmable cross conduction protection

The external PowerMOS transistors in H-Bridge (two half bridges) configuration are switched on with an additional delay time t_{CCP} to prevent cross conduction in the half-bridge. The cross conduction protection time t_{CCP} is determined by the external capacitor C_{PR} and resistor R_{PR} at the PR pin. The capacitor C_{PR} is charged up to the voltage limit V_{PRH}. A level change on the control inputs DIR and PWM switches off the concerned external MOS transistor and the charging source at the PR pin. The resistor R_{PR} discharges the capacitor C_{PR}. The concerned external PowerMOS transistor will be switched on again when the voltage at PR reaches the value of V_{PRL}. After that the CPR will be charged again. The capacitor C_{PR} should be chosen between 100 pF and 1 nF. The resistor R_{PR} should be higher than 7 kΩ. The delay time can be expressed as follows:

$$t_{CCP} = R_{PR} \cdot C_{PR} \cdot \ln N_{PR} \quad \text{with} \quad N_{PR} = V_{PRH} / V_{PRL} = 2$$

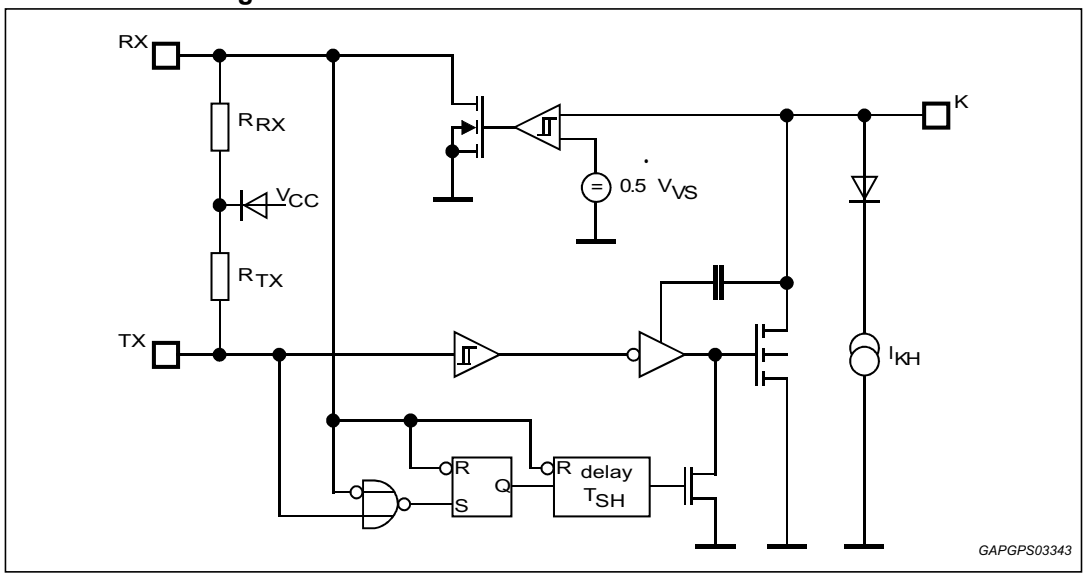
$$t_{CCP} = 0.69 \cdot R_{PR} \cdot C_{PR}$$

4.14 ISO-Interface

The ISO-Interface provides the communication between the micro controller and a serial bus with a baud rate up to 60kbit/s via a single wire which is V_{BAT} and GND compatible. The logic level transmission input TX drives the open drain K-output. The K output can be connected to a serial bus with a pull up resistor to V_{BAT}. The K-pin is protected against overvoltage, short to GND and VS and can be driven beyond V_{VS} and GND. During lack of V_{VS} or GND the output shows high impedance characteristic. The open drain output RX with an internal pull up resistor monitors the status at the K-pin to read the received data and control the transmitted data. Short circuit condition at K-pin is recognized if the internal open drain transistor isn't able to pull the voltage potential at K-pin below the threshold of

0.45·V_{VS}. Then the RX stays in high condition. A timer starts and switches the open drain transistor after typ. 20 µs off. A next low at the TX input resets the timer and the open drain transistor switches on again.

Figure 10. Functional schematic of the ISO-interface



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

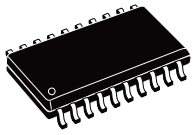
ECOPACK® is an ST trademark.

Figure 11. SO-20 mechanical data and package dimensions

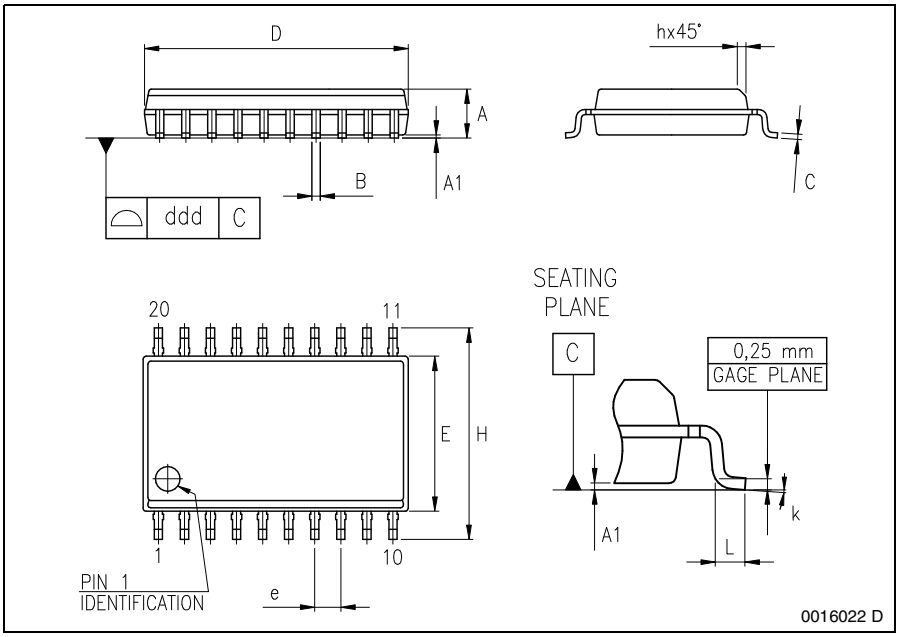
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



GAPGPS00528

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
25-Sep-2014	1	Initial release.