MK1725

Quad Output Spread Spectrum Clock Generator

Description

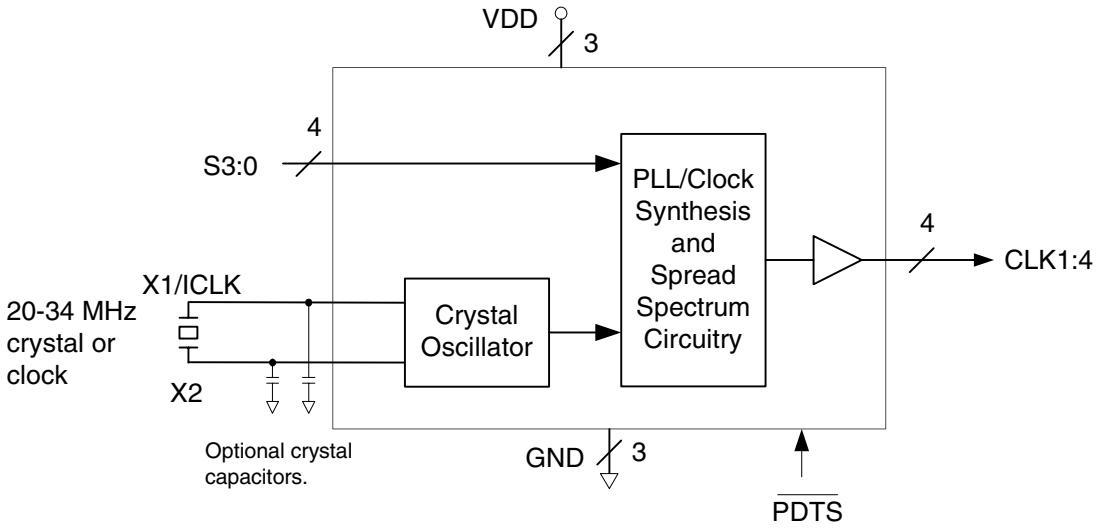
The MK1725 generates 4 high-quality, high-frequency spread spectrum clock outputs. It is designed to replace spread spectrum clock generators and a buffer in many digital consumer applications. Using ICS' patented Phase Locked Loop (PLL) techniques, the device runs from a lower frequency clock or crystal input.

The MK1725 has a 16 location ROM table which provides maximum flexibility for system designers. The chip also has a power down pin which can be used to reduce power.

Features

- Packaged in 16-pin TSSOP
- Available in Pb (lead) free package
- Replaces a spread spectrum clock generator and a buffer
- Input clock or crystal frequency of 20-34 MHz
- Output frequency of 20-136 MHz
- Four spread spectrum clock outputs
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



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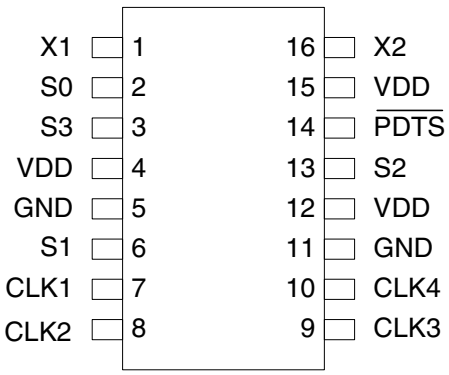
Pin Assignment



16 pin (173 mil) TSSOP

CLK Output Selection Table

S3	S2	S1	S0	CLK1:4	
				Multiplier	Spread %
0	0	0	0	1	-1%
0	0	1	0	1	-0.5%
0	0	0	1	1	+/- 0.5%
0	0	1	1	1	+/- 0.25%
0	1	1	0	2	-1%
0	1	0	1	2	-0.5%
0	1	0	0	2	+/- 0.5%
0	1	1	1	2	+/- 0.25%
1	0	0	0	4	-1%
1	0	1	0	4	-0.5%
1	0	0	1	4	+/- 0.5%
1	0	1	1	4	+/- 0.25%
1	1	1	0	1	OFF
1	1	0	1	2	OFF
1	1	0	0	4	OFF
1	1	1	1	TEST	TEST

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Connect to a 20 - 34 MHz crystal or clock input.
2	S0	Input	Select pin 0. Determines frequency and spread amount on output clocks as per table above. Internal pull-down.
3	S3	Input	Select pin 3. Determines frequency and spread amount on output clocks as per table above. Internal pull-down.
4	VDD	Power	Connect to +3.3V.
5	GND	Power	Connect to ground.
6	S1	Input	Select pin 1. Determines frequency and spread amount on output clocks as per table above. Internal pull-down.
7	CLK1	Output	Clock 1 output. Frequency and spread amount are determined by table above. Weak internal pull-down when tri-state.
8	CLK2	Output	Clock 2 output. Frequency and spread amount are determined by table above. Weak internal pull-down when tri-state.
9	CLK3	Output	Clock 3 output. Frequency and spread amount are determined by table above. Weak internal pull-down when tri-state.

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Pin Number	Pin Name	Pin Type	Pin Description
10	CLK4	Output	Clock 4 output. Frequency and spread amount are determined by table above. Weak internal pull-down when tri-state.
11	GND	Power	Connect to ground.
12	VDD	Power	Connect to +3.3V.
13	S2	Input	Select pin 2. Determines frequency and spread amount on output clocks as per table above. Internal pull-down.
14	$\overline{\text{PDTS}}$	Input	Power Down Tri-state. Powers down entire chip and tri-states outputs when low. Internal pull-up resistor.
15	VDD	Power	Connect to +3.3V.
16	X2	Input	20MHz-34MHz crystal input. Float for clock input.

External Components

Decoupling Capacitor

As with any high performance mixed-signal IC, the MK1725 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 6)*2$. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with an 18 pF load capacitance, each crystal capacitor would be 24 pF [(18-6) x 2] = 24.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor (if needed) should be placed close to the clock outputs.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1725. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1725. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Supply Current	IDD	20M in S3:0=[0100]		22		mA
Input High Voltage	V_{IH}	Input selects	2			V
Input Low Voltage	V_{IL}	Input selects			0.8	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	Clock outputs		±70		mA
Input Capacitance	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PU}	$\overline{PDTS}$ pin		360		kΩ
Internal Pull-down Resistor	R_{PD}	Clock outputs; S3:0		510		kΩ

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AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.0 V ±5%**, Ambient Temperature 0 to +70°C

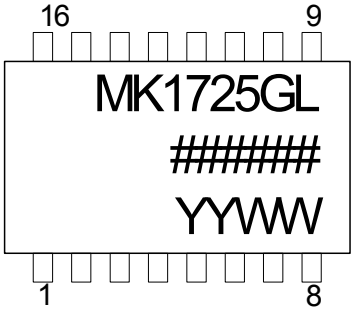
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}	Crystal or clock input	20		34	MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		1.2		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1.0		ns
Output Clock Duty Cycle		At VDD/2, Note 1 1X, 2X modes	45	50	55	%
		at VDD/2, Note 1 4X mode	40	50	60	%
Absolute Clock Period Jitter	t_J	Cycle to cycle, Note 1		150		ps
Modulation Frequency	f_{mod}		25		50	kHz
Output to Output Skew		Non-spread modes			250	ps
Output Enable Time	t_{OE}	$\overline{PDTS}$ high to output spread profile stable		2.6		ms
Output Disable Time	t_{OD}	$\overline{PDTS}$ low to tri-state		10		ns

Note 1: Measured with a 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram



Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. “L” denotes Pb (lead) free package.
4. Bottom marking: (origin). Origin = country of origin of not USA.

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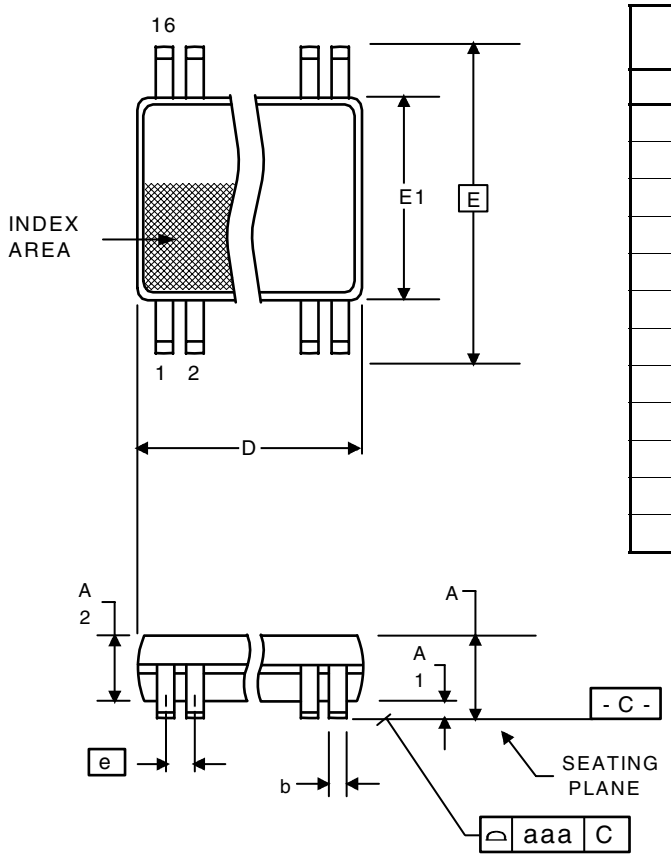
Package Outline and Package Dimensions (16 pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1725GLF	see page 5	Tubes	16-pin TSSOP	0 to +70 °C
MK1725GLFT		Tape and Reel	16-pin TSSOP	0 to +70 °C

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