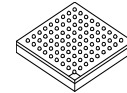


MIMX8MM6DVTLZAA MIMX8MM5DVTLZAA
MIMX8MM5DVTLZCA MIMX8MM5DVTLZDA
MIMX8MM4DVTLZAA MIMX8MM3DVTLZAA
MIMX8MM2DVTLZAA MIMX8MM1DVTLZAA

i.MX 8M Mini Applications Processor Datasheet for Consumer Products



Package Information
Plastic Package
FCBGA 14 x 14 mm, 0.5 mm pitch

| |
|---------------------------------------|
| Ordering Information |
| See Table 2 on page 6 |

1 i.MX 8M Mini introduction

The i.MX 8M Mini applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption.

The i.MX 8M Mini family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M4 400 MHz core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. A wide range of audio interfaces are available, including I2S, AC97, TDM, and S/PDIF. There are a number of other interfaces for connecting peripherals, such as USB, PCIe, and Ethernet.

| | |
|--|----|
| 1. i.MX 8M Mini introduction | 1 |
| 1.1. Block diagram | 5 |
| 1.2. Ordering information | 6 |
| 2. Modules list | 8 |
| 2.1. Recommended connections for unused input/output | 12 |
| 3. Electrical characteristics | 14 |
| 3.1. Chip-level conditions | 14 |
| 3.2. Power supplies requirements and restrictions | 23 |
| 3.3. PLL electrical characteristics | 26 |
| 3.4. On-chip oscillators | 27 |
| 3.6. I/O AC parameters | 29 |
| 3.5. General purpose I/O (GPIO) DC parameters | 28 |
| 3.7. Output buffer impedance parameters | 30 |
| 3.8. System modules timing | 32 |
| 3.9. External peripheral interface parameters | 33 |
| 4. Boot mode configuration | 68 |
| 4.1. Boot mode configuration pins | 68 |
| 4.2. Boot device interface allocation | 69 |
| 5. Package information and contact assignments | 70 |
| 5.1. 14 x 14 mm package information | 70 |
| 5.2. DDR pin function list | 87 |
| 6. Revision history | 91 |



Table 1. Features

| Subsystem | Features |
|--------------------------------|---|
| Arm Cortex-A53 MPCore platform | Quad symmetric Cortex-A53 processors <ul style="list-style-type: none"> • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture: • Floating Point Unit (FPU) with support of the VFPv4-D16 architecture |
| | Support of 64-bit Armv8-A architecture |
| | 512 KB unified L2 cache |
| Arm Cortex-M4 core platform | Low power microcontroller available for customer application: <ul style="list-style-type: none"> • low power standby mode • IoT features including Weave • Manage IR or Wireless Remote |
| | Cortex M4 CPU: <ul style="list-style-type: none"> • 16 KB L1 Instruction Cache • 16 KB L1 Data Cache • 256 KB tightly coupled memory (TCM) |
| Connectivity | One PCI Express (PCIe) <ul style="list-style-type: none"> • Single lane supporting PCIe Gen2 • Dual mode operation to function as root complex or endpoint • Integrated PHY interface • Support L1 low power sub-state |
| | Two USB 2.0 OTG controllers with integrated PHY interfaces: <ul style="list-style-type: none"> • Spread spectrum clock support |
| | Three Ultra Secure Digital Host Controller (uSDHC) interfaces: <ul style="list-style-type: none"> • MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec • SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec • Support for SDXC (extended capacity) |
| | One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588 |
| | Four Universal Asynchronous Receiver/Transmitter (UART) modules |
| | Four I ² C modules |
| | Three ECSPi modules |
| On-chip memory | Boot ROM (256 KB) |
| | On-chip RAM (256 KB + 32 KB) |
| GPIO and pin multiplexing | General-purpose input/output (GPIO) modules with interrupt capability |
| | Input/output multiplexing controller (IOMUXC) to provide centralized pad control |
| Power management | Temperature sensor with programmable trip points |
| | Flexible power domain partitioning with internal power switches to support efficient power management |

Table 1. Features (continued)

| Subsystem | Features |
|---------------------------|--|
| External memory interface | 32/16-bit DRAM interfaces: <ul style="list-style-type: none"> • LPDDR4 (up to 1.5 GHz) • DDR4-2400 • DDR3L-1600 |
| | 8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec) |
| | eMMC 5.1 Flash (2 interfaces, uSDHC1 and uSDHC3) |
| | SPI NOR Flash (3 interfaces) |
| | FlexSPI with support for XIP (for ME in low-power mode) and parallel read mode of two identical FLASH devices |
| Multimedia | Video Processing Unit: <ul style="list-style-type: none"> • 1080p60 VP9 Profile 0, 2 (10-bit) • 1080p60 HEVC/H.265 Decoder • 1080p60 AVC/H.264 Baseline, Main, High decoder • 1080p60 VP8 • 1080p60 AVC/H.264 Encoder • 1080p60 VP8 • TrustZone support |
| | Graphic Processing Unit: <ul style="list-style-type: none"> • GCNanoUltra for 3D acceleration • GC320 for 2D acceleration |
| | LCDIF Display Controller: <ul style="list-style-type: none"> • Support up to 2 layers of overlay • Support up to 1080p60 display through MIPI DSI |
| | MIPI Interface: <ul style="list-style-type: none"> • 4-lane MIPI CSI interface • 4-lane MIPI DSI interface |
| | Audio: <ul style="list-style-type: none"> • S/PDIF input and output, including a new Raw Capture input mode • Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, including one SAI with 8 Tx and 8 Rx lanes, one SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and one SAI with 1 Tx and 1Rx lane. Support over 20 channels of audio subject to I/O limitations. • 8-Channel Pulse Density Modulation (PDM) input |
| System debug | Arm CoreSight debug and trace architecture |
| | Trace Port Interface Unit (TPIU) to support off-chip real-time trace |
| | Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering |
| | Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs |
| | Cross Triggering Interface (CTI) |
| | Support for 5-pin (JTAG) debug interface |

Table 1. Features (continued)

| Subsystem | Features |
|-----------|---|
| Security | Resource Domain Controller (RDC) supports four domains and up to eight regions of DDR |
| | Arm TrustZone (TZ) architecture: <ul style="list-style-type: none"> • Support Arm Cortex-A53 MPCore TrustZone |
| | On-chip RAM (OCRAM) secure region protection using OCRAM controller |
| | High Assurance Boot (HAB) |
| | Cryptographic acceleration and assurance (CAAM) module and Assurance Module: <ul style="list-style-type: none"> • Support Widevine and PlayReady content protection • Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms • Real-time integrity checker (RTIC) • DRM support for RSA, AES, 3DES, DES • Side channel attack resistance • True random number generation (RNG) • Manufacturing protection support |
| | Secure non-volatile storage (SNVS): <ul style="list-style-type: none"> • Secure real-time clock (RTC) |
| | Secure JTAG controller (SJC) |

NOTE

The actual feature set depends on the part numbers as described in [Table 2](#). Functions such as display and camera interfaces, and connectivity interfaces, may not be enabled for specific part numbers.

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Mini applications processor system.

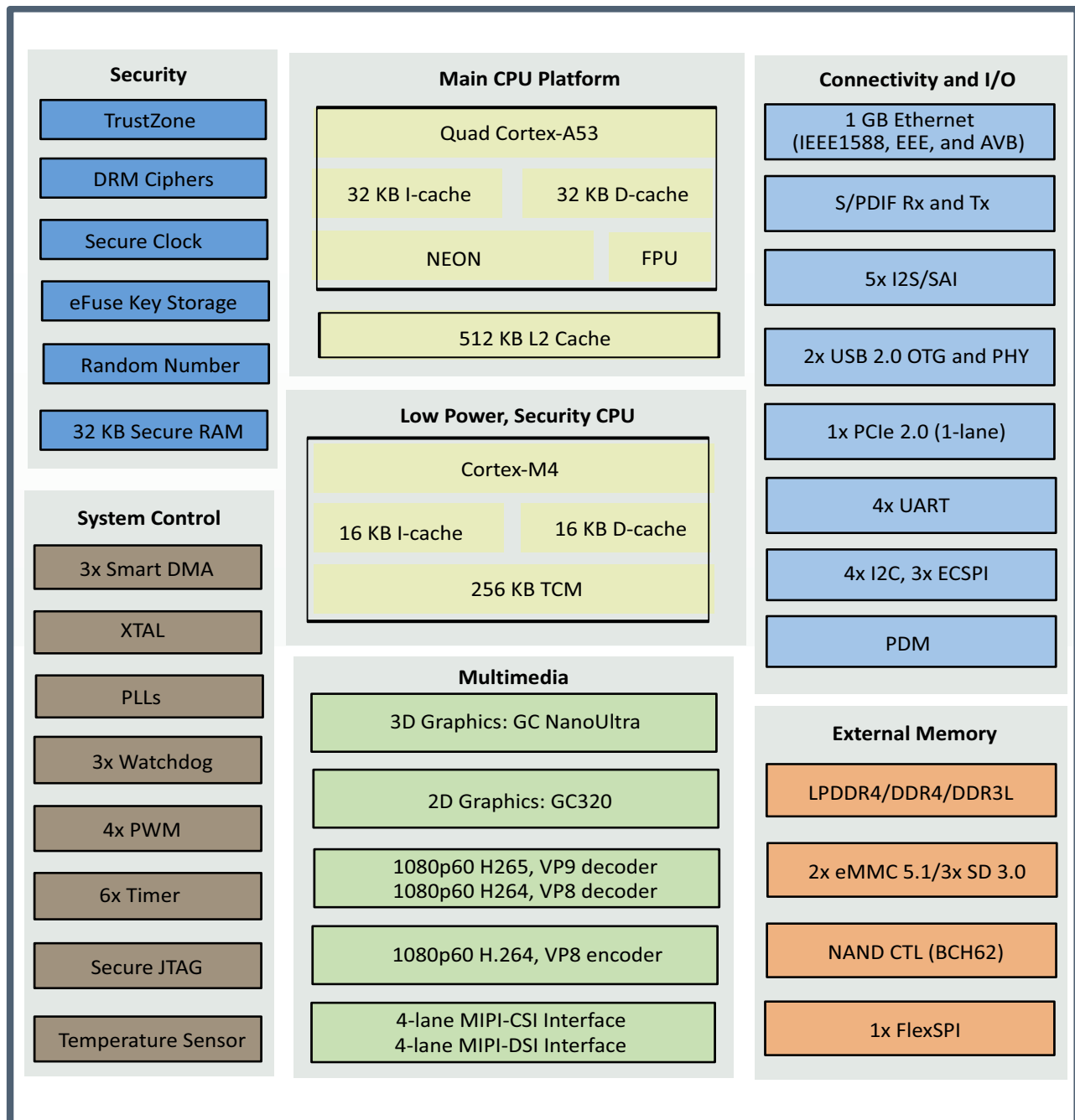


Figure 1. i.MX 8M Mini system block diagram

1.2 Ordering information

Table 2 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

Table 2. Orderable part numbers

| Family | Part number | Part differentiator | Cortex-A53 CPU speed grade | Qualification tier | Temperature T _j (°C) | Package |
|-----------------------|-----------------|---|----------------------------|--------------------|---------------------------------|--------------------------|
| i.MX 8M Mini Quad | MIMX8MM6DVTLZAA | 4x A53, M4, GPU, VPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini QuadLite | MIMX8MM5DVTLZAA | 4x A53, M4, GPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini QuadLite | MIMX8MM5DVTLZCA | 4x A53, M4, GPU, Immersiv3D with Dolby ATMOS support ¹ | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini QuadLite | MIMX8MM5DVTLZDA | 4x A53, M4, GPU, Immersiv3D with Dolby ATMOS and DTS support ¹ | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini Dual | MIMX8MM4DVTLZAA | 2x A53, M4, GPU, VPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini DualLite | MIMX8MM3DVTLZAA | 2x A53, M4, GPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini Solo | MIMX8MM2DVTLZAA | 1x A53, M4, GPU, VPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |
| i.MX 8M Mini SoloLite | MIMX8MM1DVTLZAA | 1x A53, M4, GPU | 1.8 GHz | Consumer | 0 to +95 | 14 x 14 mm, 0.5 mm pitch |

¹ Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.

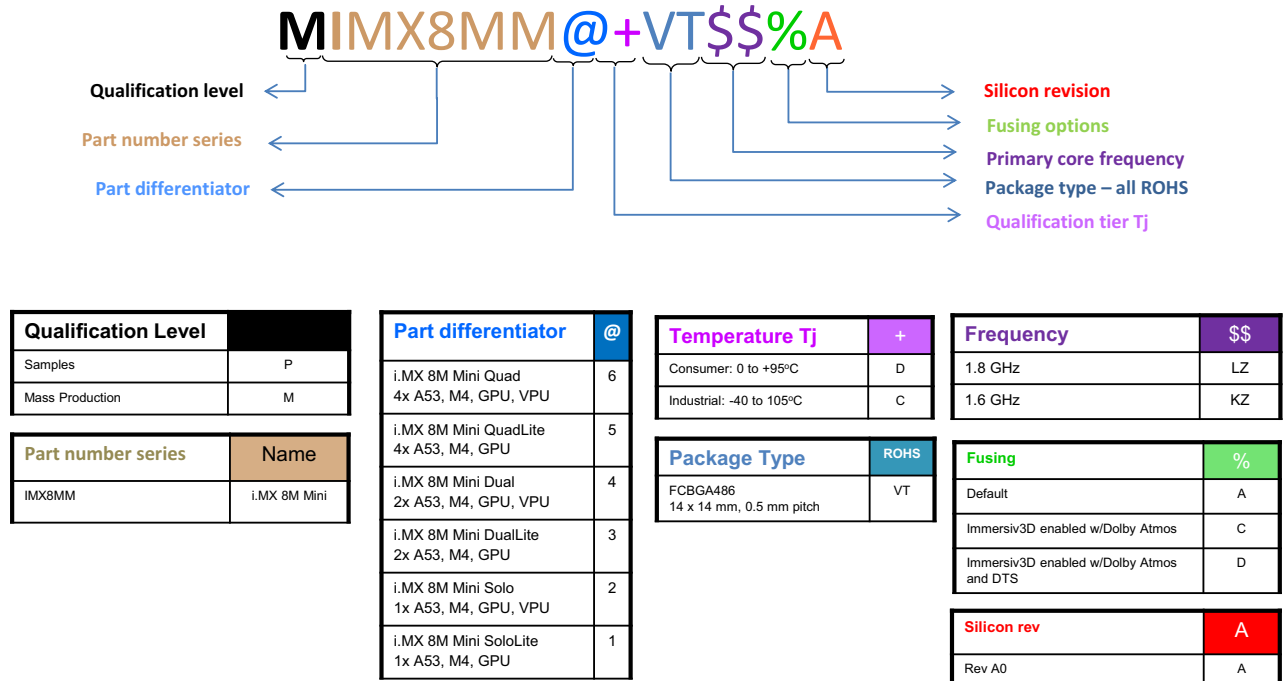


Figure 2. Part number nomenclature—i.MX 8M Mini family of processors

2 Modules list

The i.MX 8M Mini family of processors contains a variety of digital and analog modules. [Table 3](#) describes these modules in alphabetical order.

Table 3. i.MX 8M Mini modules list

| Block mnemonic | Block name | Brief description |
|---|---|--|
| 32k Oscillator | Clock system | 32 KHz oscillator is used as the clock source for RTC and internal low speed clock. It can be supplied by external 32.768 KHz oscillator. |
| APBH-DMA | NAND Flash and BCH ECC DMA Controller | DMA controller used for GPMI2 operation. |
| Arm | Arm Platform | The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M4 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M4 core is used as a customer microcontroller. |
| BCH | Binary-BCH ECC Processor | The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI) |
| CAAM | Cryptographic accelerator and assurance module | CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Mini processors, the secure memory provided is 32 KB. |
| CCM GPC SRC | Clock Control Module, General Power Controller, System Reset Controller | These modules are responsible for clock and reset distribution in the system, and also for the system power management. |
| CSU | Central Security Unit | The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Mini platform. |
| CTI-0 CTI-1 CTI-2 CTI-3 CTI-4 | Cross Trigger Interface | Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform. |
| DAP | Debug Access Port | The DAP provides real-time access for the debugger without halting the core to access: <ul style="list-style-type: none"> • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. |
| DDRC | Double Data Rate Controller | The DDR Controller has the following features: <ul style="list-style-type: none"> • Supports 32/16-bit LPDDR4 (up to 1.5 GHz), DDR4-2400, and DDR3L-1600 • Supports up to 8 Gbyte DDR memory space |
| eCSPI1 eCSPI2 eCSPI3 | Configurable SPI | Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, only one chip select is supported. |

Table 3. i.MX 8M Mini modules list (continued)

| Block mnemonic | Block name | Brief description |
|--|----------------------------------|---|
| ENET1 | Ethernet Controller | The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the <i>i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM)</i> for details. |
| FlexSPI | FlexSPI | The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features: <ul style="list-style-type: none"> • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master |
| GIC | Generic Interrupt Controller | The GIC handles all interrupts from the various subsystems and is ready for virtualization. |
| GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 | General Purpose I/O Modules | Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O. |
| GPMI | General Purpose Memory Interface | The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device. |
| GPT1 GPT2 GPT3 GPT4 GPT5 GPT6 | General Purpose Timer | Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |
| GPU3D | Graphics Processing Unit-3D | The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays. |
| I2C1 I2C2 I2C3 I2C4 | I ² C Interface | I ² C provides serial interface for external devices. Data rates of up to 320 kbps are supported. |
| IOMUXC | IOMUX Control | This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable. |

Table 3. i.MX 8M Mini modules list (continued)

| Block mnemonic | Block name | Brief description |
|--------------------------------------|-------------------------------|---|
| MIPI CSI2 (four-lane) | MIPI Camera Serial Interface | This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps. |
| MIPI DSI (four-lane) | MIPI Display Serial Interface | This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps. |
| OCOTP_CTRL | OTP Controller | The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility. |
| OCRAM | On-Chip Memory controller | The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. In i.MX 8M Mini processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus. |
| PCIe1 | PCI Express 2.0 | The PCIe IP provides PCI Express Gen 2.0 functionality. |
| PDM | Pulse Density Modulation | The PDM supports up to 8-channels (4 lanes). |
| PMU | Power Management Unit | Integrated power management unit. Used to provide power to various SoC domains. |
| PWM1 PWM2 PWM3 PWM4 | Pulse Width Modulation | The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound. |
| SAI1 SAI2 SAI3 SAI5 SAI6 | Synchronous Audio Interface | The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. |

Table 3. i.MX 8M Mini modules list (continued)

| Block mnemonic | Block name | Brief description |
|----------------|--|---|
| SDMA | Smart Direct Memory Access | <p>The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features:</p> <ul style="list-style-type: none"> • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available |
| SJC | Secure JTAG Controller | <p>The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Mini family of processors uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149. 1.</p> <p>The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 8M Mini SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p> |
| SNVS | Secure Non-Volatile Storage | Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting. |
| SPDIF1 | Sony Philips Digital Interconnect Format | A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality. |
| TEMPSENSOR | Temperature Sensor | Temperature sensor |
| TZASC | Trust-Zone Address Space Controller | The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller. |

Table 3. i.MX 8M Mini modules list (continued)

| Block mnemonic | Block name | Brief description |
|----------------------------------|--|---|
| UART1 UART2 UART3 UART4 | UART Interface | Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud |
| uSDHC1 uSDHC2 uSDHC3 | SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller | i.MX 8M Mini SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: <ul style="list-style-type: none"> • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.1. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode. Two uSDHC controllers (uSDHC1 and uSDHC3) can support up to an 8-bit interface, the other controller (uSDHC2) can only support up to a 4-bit interface. |
| USB1 USB2 | 2x USB 2.0 controllers and PHYs | Two USB controllers and PHYs that support USB 2.0. Each USB instance contains: <ul style="list-style-type: none"> • USB 2.0 core, which can operate in 2.0 mode |
| VPU | Video Processing Unit | A high performing video processing unit (VPU), which covers many SD-level and HD-level video decoders. See the <i>i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM)</i> for a complete list of the VPU's decoding and encoding capabilities. |
| WDOG1 WDOG2 WDOG3 | Watchdog | The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line. |
| XTALOSC | Crystal Oscillator interface | The XTALOSC module enables connectivity to an external crystal oscillator device. In a typical application use case, it is used for a 24 MHz oscillator. |

2.1 Recommended connections for unused input/output

If a function of the i.MX 8M Mini is not in use, the I/Os and power rails of that function can be terminated to reduce overall board power.

Table 4 shows the recommended connections for unused power supply rails.

Table 4. Recommended connections for unused power supply rails

| Function | Ball Name | Recommendations if Unused |
|----------------------|--|---------------------------|
| MIP-CSI and MIPI-DSI | VDD_MIPI_0P9, VDD_MIPI_1P2, VDD_MIPI_1P8 | Leave unconnected |
| PCIe | VDD_PCI_0P8, VDD_PCI_1P8 | Leave unconnected |

Table 4. Recommended connections for unused power supply rails (continued)

| Function | Ball Name | Recommendations if Unused |
|----------------------|--|--|
| USB1 and USB2 | VDD_USB_0P8, VDD_USB_1P8, VDD_USB_3P3 | Leave unconnected |
| VPU | VDD_VPU | Leave unconnected |
| GPU | VDD_GPU | Leave unconnected |
| Digital I/O supplies | NVCC_CLK, NVCC_ECSPi, NVCC_ENET, NVCC_GPIO1, NVCC_I2C, NVCC_JTAG, NVCC_NAND, NVCC_SAI1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_SD1, NVCC_SD2, NVCC_UART, NVCC_SNVS_1P8, PVCC0_1P8, PVCC1_1P8, PVCC2_1P8 | All digital I/O supplies listed in this table must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to enable pull in pad control register to limit any floating gate current. |

Table 5 shows recommended connections for unused signal contacts/interfaces.

Table 5. Recommended connections for unused signal contacts/interfaces

| Function | Ball Name | Recommendations if Unused |
|----------|---|---------------------------|
| MIPI-CSI | MIPI_CSI_CLK_P, MIPI_CSI_CLK_N, MIPI_CSI_Dx_P, MIPI_CSI_Dx_N | Tie all signals to ground |
| MIPI-DSI | MIPI_VREG_CAP, MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N | Leave unconnected |
| PCIe | PCIE_CLK_P, PCIe_CLK_N, PCIe_TXN_P, PCIe_TXN_N, PCIe_RXN_P, PCIe_RXN_N, PCIe_RESREF | Leave unconnected |
| USB1 | USB1_VBUS, USB1_DN, USB1_DP, USB1_ID, USB1_TXRTUNE | Leave unconnected |
| USB2 | USB2_VBUS, USB2_DN, USB2_DP, USB2_ID, USB2_TXRTUNE | Leave unconnected |

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Mini family of processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See [Table 6](#) for a quick reference to the individual tables and sections.

Table 6. i.MX 8M Mini chip-level conditions

| For these characteristics, ... | Topic appears ... |
|--|----------------------------|
| Absolute maximum ratings | on page 14 |
| FCBGA package thermal resistance | on page 16 |
| Operating ranges | on page 17 |
| External clock sources | on page 19 |
| Maximum supply currents | on page 20 |

3.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under [Table 7](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 7. Absolute maximum ratings

| Parameter description | Symbol | Min | Max | Unit | Notes |
|-------------------------|--------------------|------|-------|------|-------|
| Core supply voltages | VDD_ARM VDD_SOC | -0.3 | 1.15 | V | — |
| Power supply for GPU | VDD_GPU | -0.3 | 1.15 | V | — |
| Power supply for VPU | VDD_VPU | -0.3 | 1.15 | V | — |
| DDR PHY supply voltage | VDD_DRAM | -0.3 | 1.15 | V | — |
| DDR I/O supply voltage | NVCC_DRAM | -0.3 | 1.575 | V | — |
| DRAM PLL supply voltage | VDD_DRAM_PLL_0P8 | -0.3 | 1.15 | V | — |
| | VDD_DRAM_PLL_1P8 | -0.3 | 2.15 | V | — |
| SNVS IO supply voltage | NVCC_SNVS_1V8 | -0.3 | 2.15 | V | — |
| VDD_SNVS supply voltage | VDD_SNVS_0V8 | -0.3 | 0.95 | V | — |

Table 7. Absolute maximum ratings (continued)

| Parameter description | Symbol | Min | Max | Unit | Notes |
|--------------------------------|---|------|------|------|-------|
| GPIO supply voltage | NVCC_JTAG, NVCCGPIO1, NVCC_ENET, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SA1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPi, NVCC_I2C, NVCC_UART, NVCC_CLK | -0.3 | 3.8 | V | — |
| GPIO pre-driver supply voltage | PVCC0_1P8, PVCC1_1P8, PVCC2_1P8 | -0.3 | 2.15 | V | — |
| Isolated core supply voltage | VDD_ANA_0P8 | -0.3 | 1.15 | V | — |
| Analog core supply voltage | VDD_ANA0_1P8 | -0.3 | 2.15 | V | — |
| | VDD_ANA1_1P8 | -0.3 | 2.15 | V | — |
| Arm PLL supply voltage | VDD_ARM_PLL_0P8 | -0.3 | 0.95 | V | — |
| | VDD_ARM_PLL_1P8 | -0.3 | 2.15 | V | — |
| MIPI PHY supply voltage | VDD_MIPI_0P9 | -0.3 | 1.05 | V | — |
| | VDD_MIPI_1P2 | -0.3 | 1.45 | V | — |
| | VDD_MIPI_1P8 | -0.3 | 2.15 | V | — |
| PCIe PHY supply voltage | VDD_PCIE_0P8 | -0.3 | 0.95 | V | — |
| | VDD_PCIE_1P8 | -0.3 | 2.15 | V | — |
| USB PHY supply voltage | VDD_USB_0P8 | -0.3 | 0.95 | V | — |
| | VDD_USB_1P8 | -0.3 | 2.15 | V | — |
| | VDD_USB_3P3 | -0.3 | 3.95 | V | — |
| USB_VBUS input detected | USB1_VBUS, USB2_VBUS | -0.3 | 3.95 | V | — |
| XTAL supply voltage | VDD_24M_XTAL_1P8 | -0.3 | 2.15 | V | — |
| Storage temperature range | T _{STORAGE} | -40 | 150 | °C | — |

Table 8. Electrostatic discharge and latch up ratings

| Parameter description | | Rating | Reference | Comment |
|-------------------------------|---|---------|-------------|---------|
| Electrostatic Discharge (ESD) | Human Body Model (HBM) | ±1000 V | JS-001-2017 | — |
| | Charged Device Model (CDM) | ±250 V | JS-002-2018 | — |
| Latch UP (LU) | Immunity level: <ul style="list-style-type: none"> Class I @ 25 °C ambient temperature Class II @ 105 °C ambient temperature | A A | JESD78E | — |

3.1.2 Thermal resistance

3.1.2.1 FCBGA package thermal resistance

Table 9 displays the FCBGA package thermal resistance data.

Table 9. Thermal resistance data

| Rating | Test conditions | Symbol | Value | Unit | Notes |
|---|-------------------------|------------------|-------|------|---------|
| Junction to Ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 30 | °C/W | 1, 2 |
| Junction to Ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JA}$ | 22.9 | °C/W | 1, 2, 3 |
| Junction to Ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 24 | °C/W | 1, 3 |
| Junction to Ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 18.5 | °C/W | 1, 3 |
| Junction to Board | — | $R_{\theta JB}$ | 7.8 | °C/W | 4 |
| Junction to Case | — | $R_{\theta JC}$ | 4 | °C/W | 5 |
| Junction to Package Top | Natural Convection | Ψ_{JT} | 0.2 | °C/W | 6 |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.1.3 Operating ranges

Table 10 provides the operating ranges of the i.MX 8M Mini applications processor. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM)*.

Table 10. Operating ranges¹

| Symbol | Min | Typ | Max ^{2,3} | Unit | Comment |
|--|-------|-------|--------------------|------|--|
| VDD_ARM | 0.805 | 0.850 | 0.950 | V | Power supply for Quad-A53, 1.2 GHz |
| | 0.900 | 0.950 | 1.000 | V | Power supply for Quad-A53, 1.6 GHz |
| | 0.950 | 1.000 | 1.050 | V | Power supply for Quad-A53, 1.8 GHz ⁴ |
| VDD_SOC without PCIE | 0.780 | 0.820 | 0.900 | V | Power supply for SoC logic ⁵ |
| VDD_SOC with PCIE | 0.805 | 0.850 | 0.900 | V | Power supply for SoC logic ⁵ |
| VDD_GPU | 0.805 | 0.850 | 0.900 | V | Power supply for 3D GPU, nominal mode, 800 MHz |
| | 0.855 | 0.900 | 1.000 | V | Power supply for 3D GPU, overdrive mode, 1000 MHz |
| VDD_VPU | — | — | — | — | Block G2/G1/H1 |
| | 0.805 | 0.850 | 0.900 | V | Power supply for VPU, 450/450/450 MHz |
| | 0.855 | 0.900 | 0.950 | V | Power supply for VPU, 600/650/650 MHz |
| | 0.900 | 0.950 | 1.000 | V | Power supply for VPU, 700/750/750 MHz |
| VDD_DRAM | 0.805 | 0.850 | 0.900 | V | Power supply for DDRC, 0.85 V supports up to 1.0 GHz (DDR clock) |
| | 0.855 | 0.900 | 0.950 | V | Power supply for DDRC, 0.9 V supports up to 1.2 GHz (DDR clock) |
| | 0.900 | 0.950 | 1.000 | V | Power supply for DDRC, 0.95 V supports up to 1.5 GHz (DDR clock) |
| VDD_SNVS_0P8 | 0.760 | 0.800 | 0.900 | V | Power supply for SNVS core logic |
| NVCC_SNVS_1P8 | 1.620 | 1.800 | 1.980 | V | Power supply for GPIO pre-driver in SNVS bank |
| NVCC_JTAG, NVCC_GPIO1, NVCC_ENET, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SAI1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPi, NVCC_I2C, NVCC_UART, NVCC_CLK | 1.650 | 1.800 | 1.950 | V | Power supply for GPIO when it is in 1.8 V mode |
| | 3.000 | 3.300 | 3.600 | V | Power supply for GPIO when it is in 3.3 V mode |
| NVCC_ENET | 2.250 | 2.500 | 2.750 | V | Power supply for GPIO when it is in 2.5 V mode |

Table 10. Operating ranges¹ (continued)

| Symbol | Min | Typ | Max ^{2,3} | Unit | Comment |
|---|---------------------|--------------------|---------------------|------|---|
| PVCC0_1P8, PVCC1_1P8, PVCC2_1P8 | 1.650 | 1.800 | 1.950 | V | Power supply for GPIO pre-driver |
| VSS | — | — | — | V | Ground for all core logic and I/O |
| NVCC_DRAM | 1.283 | 1.35 | 1.425 | V | DDR3L |
| | 1.14 | 1.2 | 1.26 | V | DDR4 |
| | 1.06 | 1.1 | 1.17 | V | LPDDR4 |
| DRAM_VREF | 0.49 x NVCC_DRAM | 0.5 x NVCC_DRAM | 0.51 x NVCC_DRAM | V | Internal output, no connection is needed. |
| VDD_DRAM_PLL_0P8 | 0.805 | 0.850 | 1.000 | V | 0.8 V logic power supply for DSM. It should be connected to the separate logic power. |
| VDD_ANA0_1P8 VDD_ANA1_1P8 | 1.71 | 1.8 | 1.89 | V | Analog 1.8 V core power |
| VDD_ANA_0P8 | 0.780 | 0.820 | 0.900 | V | Isolated 0.8 V core power |
| VDD_ARM_PLL_0P8 | 0.780 | 0.820 | 0.900 | V | Arm PLL 0.8 V power |
| VDD_ARM_PLL_1P8 | 1.71 | 1.8 | 1.89 | V | Arm PLL 1.8 V power |
| VDD_24M_XTAL_1P8 | 1.71 | 1.8 | 1.89 | V | XTAL 1.8 V power |
| VDD_DRAM_PLL_1P8 | 1.71 | 1.8 | 1.89 | V | Analog 1.8 V core power |
| VDD_MIPI_0P9 | 0.855 | 0.9 | 1.000 | V | 0.9 V power for PLL and internal logic |
| VDD_MIPI_1P2 | 1.14 | 1.2 | 1.26 | V | 1.2 V power for analog |
| VDD_MIPI_1P8 | 1.71 | 1.8 | 1.89 | V | 1.8 V power for PLL and analog |
| VDD_PCI_0P8 ^{6,7} | 0.805 | 0.850 | 0.900 | V | Digital supply for PCIe PHY |
| VDD_PCI_1P8 ⁶ | 1.71 | 1.800 | 1.890 | V | 1.8 V supply for PCIe PHY |
| VDD_USB_0P8 | 0.780 | 0.820 | 0.900 | V | Digital power supply from PHY's I/O power pads |
| VDD_USB_1P8 | 1.71 | 1.80 | 1.89 | V | 1.8 V analog power supply |
| VDD_USB_3P3 | 3.069 | 3.30 | 3.6 | V | 3.3 V analog power supply |
| USB1_VBUS USB2_VBUS | 0.800 | 1.40 | 3.60 | V | USB_VBUS input detect signal |
| Temperature Sensor Accuracy ⁸ | — | ±3 | ±5 | °C | Sensing temperature range 10°C to 105°C |
| T _J | 0 | — | +95 | °C | See Table 2 for complete list of junction temperature capabilities. |

¹ The BD71847MWV PMIC does not support 0.950 V for VDD_GPU, VDD_VPU, and VDD_DRAM. For this PMIC, 0.975 V typical is acceptable and supported.

² Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio.

- ³ Overdrive maximum voltage includes all the nominal frequencies.
- ⁴ 50% duty cycle for 5 years
- ⁵ Booting VDD_SOC at 0.800 V \pm 5% is acceptable ($V_{min} = 0.760$ V). Software is expected to program the VDD_SOC voltage to the typical value in this table prior to first DRAM memory access.
- ⁶ Ensure the VDD_PCI_1P8 does not have more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). Simultaneously, the VDD_PCI_0P8 should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core (0.9 V nominal DC value for the overdrive).
- ⁷ It can be min 0.78 V when supplied but not operating PCIe.
- ⁸ "EN" of TMU Enable Register (TMU_TER) is required to be always enabled for the part to operate correctly.

3.1.4 External clock sources

Each i.MX 8M Mini processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can only be connected to an external oscillator. RTC_XTALO should be directly connected to VDD_SNVS_0P8.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External input clock frequency

| Parameter Description | Symbol | Min | Typ | Max | Unit |
|-----------------------------------|------------|-----|---------------------|-----|------|
| RTC_XTALI Oscillator ¹ | f_{ckil} | — | 32.768 ² | — | kHz |
| XTALI Oscillator ^{1,3} | f_{xtal} | | 24 | | MHz |

¹ The required frequency stability of this clock source is application dependent.

² Recommended nominal frequency 32.768 kHz.

³ External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

The typical values shown in Table 11 are required for use with NXP software to ensure precise time keeping and USB operation. For RTC_XTALI operation, an external oscillator is necessary. RTC_XTALO should be directly connected to VDD_SNVS_0P8 when using an external 32.768 kHz oscillator.

NOTE

There is no internal RC oscillator.

Table 12 shows the external input clock for OSC32K.

Table 12. External input clock for OSC32K

| | Symbol | Min | Typ | Max | Unit |
|-----------|--------|-----|--------|-----|------|
| Frequency | f | — | 32.768 | — | kHz |

Table 12. External input clock for OSC32K

| | Symbol | Min | Typ | Max | Unit |
|-----------|--------|---------------------|-----|---------------------|------|
| RTC_XTALI | VIH | 0.7 x NVCC_SNV5_1P8 | — | NVCC_SNV5_1P8 | V |
| | VIL | 0 | — | 0.3 x NVCC_SNV5_1P8 | V |

3.1.5 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

To help illustrate the effect of the application on power consumption, data was collected while running consumer standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Table 13. Maximum supply currents

| Power rail | Max current | Unit |
|-------------------------------------|--|------|
| VDD_ARM | 2200 | mA |
| VDD_SOC | 1000 | mA |
| VDD_GPU | 500 | mA |
| VDD_VPU | 1000 | mA |
| VDD_DRAM | 1000 | mA |
| VDD_ANA_0P8 | 50 | mA |
| VDD_ANA0_1P8 VDD_ANA1_1P8 | 250 | mA |
| NVCC_SNV5_1P8 | 3 | mA |
| VDD_ARM_PLL_1P8 VDD_24M_XTAL_1P8 | 100 | mA |
| PVCCx_1P8 | 3 | mA |
| NVCC_<XXX> NVCC_DRAM | $I_{max} = N \times C \times V \times (0.5 \times F)$ Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz. | |
| DRAM_VFEF | 10 | mA |

3.1.6 Power modes

The i.MX 8M Mini processors support the following power modes:

- **RUN Mode:** All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- **IDLE Mode:** When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M4 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.
- **SUSPEND Mode:** The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.
- **SNVS Mode:** This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- **OFF Mode:** All power rails are off.

Table 14. Chip power in different LP mode

| Mode | Supply | Typ. ¹ | Unit |
|---------|----------------------------|-------------------|------|
| SNVS | VDD_SNVS_0P8 (0.8 V) | 0.02 | mW |
| | NVCC_SNVS_1P8 (1.8 V) | 0.09 | |
| | Total ² | 0.11 | |
| SUSPEND | NVCC (1.8 V) | 1.20 | mW |
| | NVCC_DRAM (1.1 V) | 0.50 | |
| | NVCC_ENET (1.8 V) | 0.10 | |
| | NVCC_SNVS_1P8 (1.8 V) | 0.10 | |
| | PVCC (1.8 V) | 0.60 | |
| | VDD_MIPI_0P9 (0.9 V) | 2.20 | |
| | VDD_SNVS_0P8 (0.8 V) | 0.10 | |
| | VDD_SOC (0.82 V) | 4.00 | |
| | VDD_ARM_0P8 (0.82 V) | 0.10 | |
| | VDDA_PCIE_USB_0P8 (0.82 V) | 3.00 | |
| | Total ² | 11.90 | |

¹ All the power numbers defined in the table are for information only. These numbers are based on typical silicon at 25°C, under non-OS environment and use case dependent. For power numbers with OS and real use cases, see *Power consumption measurement application note* for more details.

² Sum of the listed supply rails.

Electrical characteristics

Table 15 summarizes the external power supply states in all the power modes.

Table 15. The power supply states

| Power rail | OFF | SNVS | SUSPEND | IDLE | RUN |
|-----------------------|-----|------|---------|------|--------|
| VDD_ARM | OFF | OFF | OFF | ON | ON |
| VDD_SOC | OFF | OFF | ON | ON | ON |
| VDD_GPU | OFF | OFF | OFF | OFF | ON/OFF |
| VDD_VPU | OFF | OFF | OFF | OFF | ON/OFF |
| VDD_DRAM | OFF | OFF | OFF | ON | ON |
| Misc_1P8 ¹ | OFF | OFF | ON | ON | ON |
| Misc_0P8 ¹ | OFF | OFF | ON | ON | ON |
| VDD_MIPI_1P2 | OFF | OFF | OFF | ON | ON |
| VDD_MIPI_0P9 | OFF | OFF | OFF | ON | ON |
| VDD_DRAM_PLL_0P8 | OFF | OFF | ON | ON | ON |
| VDD_SNVS_0P8 | OFF | ON | ON | ON | ON |
| NVCC_SNVS_1P8 | OFF | ON | ON | ON | ON |
| NVCC_<XXX> | OFF | OFF | ON | ON | ON |
| PVCCx_1P8 | OFF | OFF | ON | ON | ON |
| NVCC_DRAM | OFF | OFF | ON | ON | ON |

¹ See Table 16

Table 16. Group name

| | |
|----------|---|
| Misc_1P8 | VDD_24M_XTAL_1P8 VDD_ANA0_1P8 VDD_ANA1_1P8 VDD_ARM_PLL_1P8 VDD_DRAM_PLL_1P8 VDD_MIPI_1P8 VDD_PCI_1P8 VDD_USB_1P8 |
| Misc_0P8 | VDD_ANA_0P8 VDD_ARM_PLL_0P8 VDD_PCI_0P8 VDD_USB_0P8 |

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

3.2.1 Power-up sequence

Figure 5 illustrates the power-up sequence of i.MX 8M Mini processor.

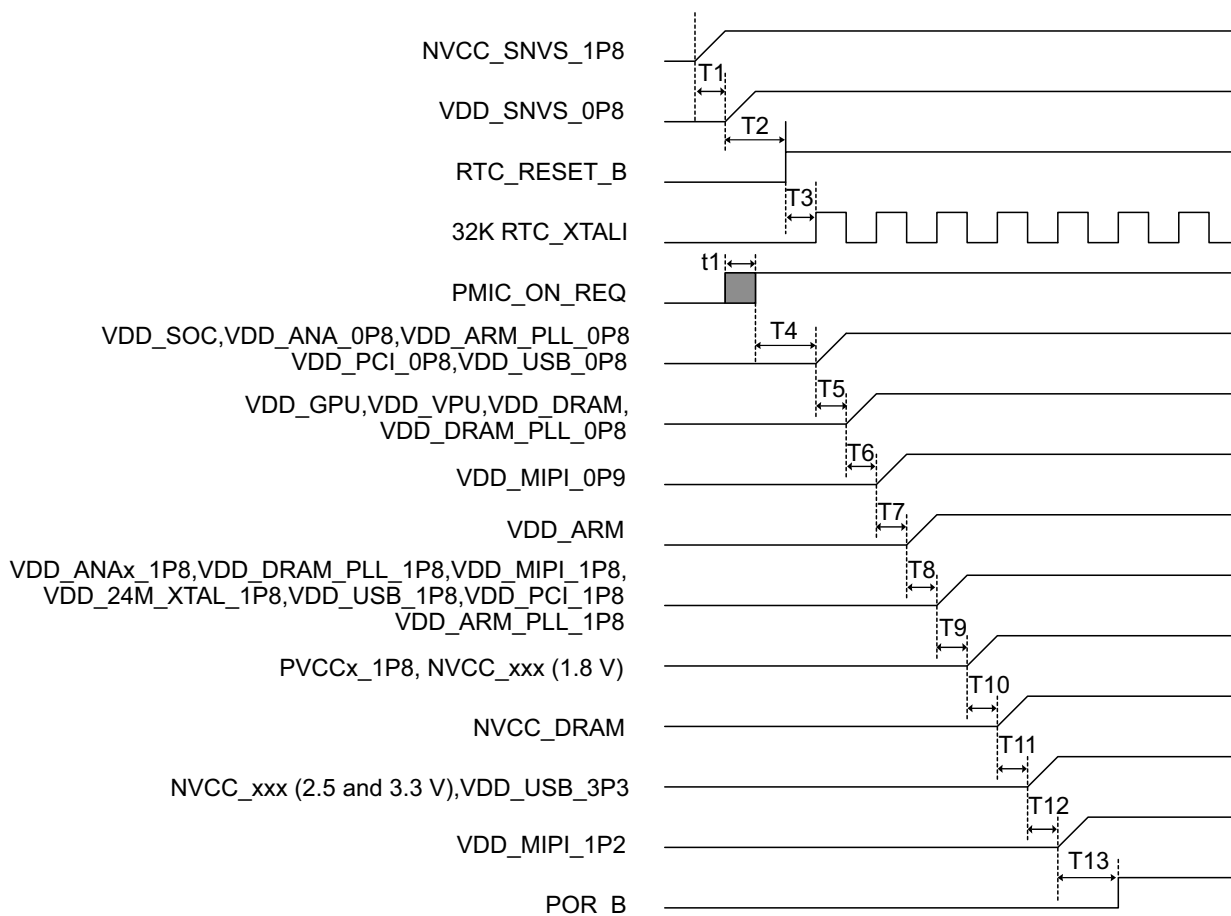


Figure 3. The power-up sequence

Electrical characteristics

Table 17 represents the timing parameters of the power-up sequence.

Table 17. Power-up sequence

| | Description | Min | Typ | Max | Unit |
|------------------|---|-----|-----|-----|------|
| T1 | Delay from NVCC_SNVS_1P8 to VDD_SNVS_0P8 | 0 | 2 | — | ms |
| T2 | Delay from VDD_SNVS_0P8 high or RTC_SET_B de-assert | 0 | 10 | — | ms |
| T3 | Delay from RTC_RESET_B de-assert to stable 32 k existed | — | 40 | 100 | μs |
| T4 | Delay from PMIC_ON_REQ assert to analog 0.8 V on | 0 | 0.2 | — | ms |
| T5 | Delay from analog 0.8 V on to analog 0.8/0/9 V on | 0 | 2 | — | ms |
| T6 | Delay from analog 0.8/0.9 V on to PHY 0.9 V on | 0 | 15 | — | μs |
| T7 | Delay from PHY 0.9 V on to VDD_ARM on | 0 | 2 | — | ms |
| T8 | Delay from VDD_ARM on to analog 1.8 V on | 0 | 15 | — | μs |
| T9 | Delay from analog 1.8 V on to digital 1.8 V on | 0 | 2 | — | ms |
| T10 | Delay from digital 1.8 V on to NVCC_DRAM on | 0 | 2 | — | ms |
| T11 | Delay from NVCC_DRAM on to digital 2.5 V and 3.3 V on | 0 | 2 | — | ms |
| T12 | Delay from digital 2.5 V and 3.3 V on to PHY 1.2 V on | 0 | 2 | — | ms |
| T13 ¹ | Delay from PHY 1.2 V on to POR_B de-assert | 0 | 20 | — | ms |
| t1 | Uncertain period before PMIC_ON_REQ assert during VDD_SNVS_0P8 ramp up. | | | | |
| | For ramp up requirement, only VDD_ANA0_1P8 has 5 μs minimum requirement, others do not have such requirement. During power-up, make sure NVCC_xxx - PVCCx_1P8 < 2 V. | | | | |

¹ The values of T13 depend on T2. RTC_RESET_B must be de-assert before POR_B de-asserts.

3.2.2 Power-down sequence

Figure 5 illustrates the power-down sequence of i.MX 8M Mini processor.

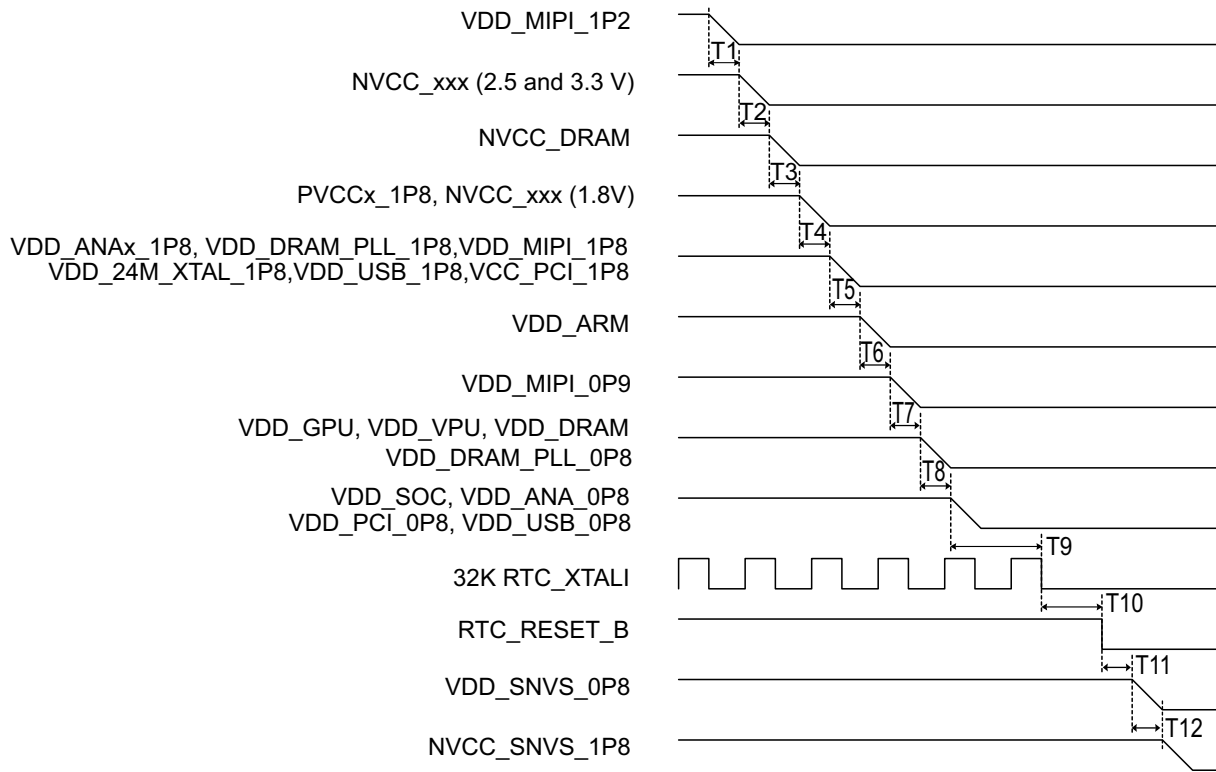


Figure 4. The power-down sequence

Electrical characteristics

Table 18 represents the timing parameters of the power-down sequence.

Table 18. Power-down sequence

| | Description | Min | Typ | Max | Unit |
|-----|--|-----|-----|-----|------|
| T1 | Delay from PHY 1.2 V off to digital 2.5 V and 3.3 V off | 0 | 10 | — | ms |
| T2 | Delay from digital 2.5 V and 3.3 V off to NVCC_DRAM off | 0 | 10 | — | ms |
| T3 | Delay from NVCC_DRAM off to digital 1.8 V off | 0 | 10 | — | ms |
| T4 | Delay from digital 1.8 V off to analog 1.8 V off | 0 | 10 | — | ms |
| T5 | Delay from analog 1.8 V off to VDD_ARM off | 0 | 10 | — | ms |
| T6 | Delay from VDD_ARM off to PHY 0.9 V off | 0 | 10 | — | ms |
| T7 | Delay from PHY 0.9 V off to analog 0.8/0.9 V off | 0 | 10 | — | ms |
| T8 | Delay from analog 0.8/0.9 V off to analog 0.8 V off | 0 | 10 | — | ms |
| T9 | Delay from analog 0.8 V off to 32k off | 0 | 10 | — | ms |
| T10 | Delay from 32k off to RTC_RESET_B assert | 0 | 10 | — | ms |
| T11 | Delay from RTC_RESET_B assert to VDD_SNVS_0P8 off | 0 | 10 | — | ms |
| T12 | Delay from VDD_SNVS_0P8 off to NVCC_SNVS_1P8 off | 0 | 10 | — | ms |
| | During power-down, make sure NVCC_xxx - PVCCx_1P8 < 2 V. | | | | |

3.3 PLL electrical characteristics

Table 19 shows PLL electrical characteristics.

Table 19. PLL electrical parameters

| PLL type | Parameter | Value |
|------------|--------------------|-----------------|
| AUDIO_PLL1 | Clock output range | Maximum 650 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 375 μ s |
| AUDIO_PLL2 | Clock output range | Maximum 650 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 375 μ s |
| VIDEO_PLL1 | Clock output range | Maximum 650 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 375 μ s |
| SYS_PLL1 | Clock output range | 800 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |

Table 19. PLL electrical parameters (continued)

| PLL type | Parameter | Value |
|----------|--------------------|-------------------|
| SYS_PLL2 | Clock output range | 1 GHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |
| SYS_PLL3 | Clock output range | 600 MHz ~ 1 GHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |
| ARM_PLL | Clock output range | 800 MHz ~ 1.6 GHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |
| DRAM_PLL | Clock output range | Maximum 750 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 375 μ s |
| GPU_PLL | Clock output range | Maximum 1 GHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |
| VPU_PLL | Clock output range | 400 MHz ~ 800 MHz |
| | Reference clock | 24 MHz |
| | Lock time | 25 μ s |

3.4 On-chip oscillators

3.4.1 OSC24M

A 24 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for the CPU, BUS, and high-speed interfaces. For fractional PLLs, the 24 MHz clock from the oscillator can be used as the PLL reference clock directly.

Table 20. Crystal specifications¹

| Parameter Description | Min | Typ | Max | Unit |
|-----------------------|-----|-----|-----|----------|
| Frequency | — | 24 | — | MHz |
| Load | — | 12 | — | pF |
| Drive level | 100 | — | — | μ W |
| ESR | — | — | 80 | Ω |

Electrical characteristics

¹ Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

3.4.2 OSC32K

An external 32.768 kHz oscillator is necessary.

3.5 General purpose I/O (GPIO) DC parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 21. GPIO DC parameters

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-----------------|---|---------------------|-----|---------------------|---------------|
| High-level output voltage | $V_{OH(1.8V)}$ | $I_{OH} = 1.6/3.2/6.4/9.6 \text{ mA (1.8 V)}$ $I_{OH} = 2/4/8/12 \text{ mA (3.3 V)}$ | $0.8 \times V_{DD}$ | — | V_{DD} | V |
| | $V_{OH(3.3V)}$ | | $0.8 \times V_{DD}$ | — | V_{DD} | V |
| Low-level output voltage | $V_{OL(1.8V)}$ | $I_{OL} = 1.6/3.2/6.4/9.6 \text{ mA (1.8 V)}$ $I_{OL} = 2/4/8/12 \text{ mA (3.3 V)}$ | 0 | — | $0.2 \times V_{DD}$ | V |
| | $V_{OL(3.3V)}$ | | 0 | — | $0.2 \times V_{DD}$ | V |
| High-level input voltage | V_{IH} | — | $0.7 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V |
| Low-level input voltage | V_{IL} | — | -0.3 | — | $0.3 \times V_{DD}$ | V |
| Pull-up resistor | — | $V_{DD} = 1.65 - 1.95V$ Temp = 0 - 95 °C | 12 | 22 | 49 | K Ω |
| Pull-down resistor | — | | 13 | 23 | 48 | K Ω |
| Pull-up resistor | — | $V_{DD} = 2.25 - 2.75V$ Temp = 0 - 95 °C | 13 | 24 | 69 | K Ω |
| Pull-down resistor | — | | 9.1 | 33 | 69 | K Ω |
| Pull-up resistor ¹ | — | $V_{DD} = 3.0 - 3.6V$ Temp = 0 - 95 °C | — | — | — | K Ω |
| Pull-down resistor ¹ | — | | — | — | — | K Ω |
| High level input current | I _{IH} | — | -4 | — | 4 | μA |
| Low level input current | I _{IL} | — | -0.7 | — | 0.7 | μA |

¹ Does not support internal pull-up or pull-down for 3.3 V IOs.

Table 22. Additional leakage parameters

| Parameter | Symbol | Pins | Min | Max | Unit |
|--------------------------|-----------------|-------------------|-----|-----|---------------|
| High level input current | I _{IH} | PCIE_RXN, USBx_Dx | -30 | 30 | μA |
| | | PCIE_CLK | -8 | 8 | |
| | | MIPI_CSI | -4 | 4 | |

Table 22. Additional leakage parameters (continued)

| Parameter | Symbol | Pins | Min | Max | Unit |
|-------------------------|--------|------------------------|------|-----|---------------|
| Low level input current | IIL | JTAG_TRST_B, USBx_ID | -200 | 200 | μA |
| | | PCIE_CLK, USBx_Dx | -6 | 6 | |
| | | PCIE_RXN | -2.5 | 2.5 | |
| | | MIPI_CSI, ONOFF, POR_B | -0.7 | 0.7 | |

3.5.1 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR 4, DDR4, and DDR3L operational modes. The DDR Memory Controller (DDRMC) is designed to be compatible with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8M Mini applications processor.

3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)

The GPIO load circuit and output transition time waveforms are shown in [Figure 5](#) and [Figure 6](#).

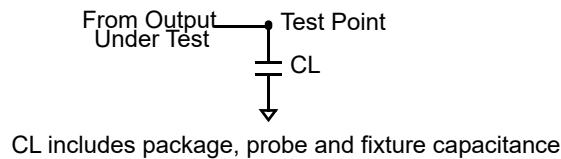


Figure 5. Load circuit for output

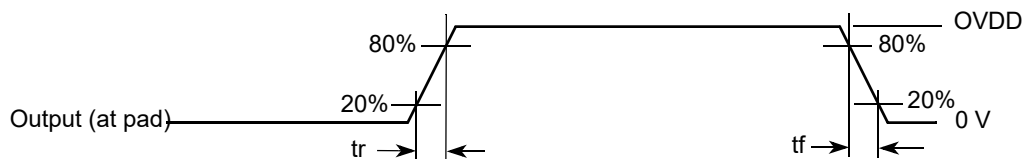


Figure 6. Output transition time waveform

3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes.

Table 23. Maximum frequency of operation for input

| Maximum frequency (MHz) | |
|-------------------------|-------------------------|
| VDD = 1.8 V, CL = 50 pF | VDD = 3.3 V, CL = 50 pF |
| 450 | 440 |

Table 24. Maximum frequency of operation for output

| Parameter | | | Maximum Frequency (MHz) | | | |
|-----------|----------|--------------|-------------------------|------------|-------------|------------|
| | | | VDD = 1.8 V | | VDD = 3.3 V | |
| dse[2:0] | sre[1:0] | Driver type | CL = 10 pF | CL = 20 pF | CL = 10 pF | CL = 20 pF |
| 00X | 0X | 1x Slow Slew | 150 | 80 | 120 | 65 |
| 00X | 1X | 1x Fast Slew | 150 | 80 | 120 | 65 |
| 10X | 0X | 2x Slow Slew | 160 | 90 | 150 | 80 |
| 10X | 1X | 2x Fast Slew | 160 | 90 | 150 | 80 |
| 01X | 0X | 4x Slow Slew | 200 | 100 | 180 | 90 |
| 01X | 1X | 4x Fast Slew | 200 | 100 | 180 | 90 |
| 11X | 0X | 6x Slow Slew | 250 | 130 | 200 | 100 |
| 11X | 1X | 6x Fast Slew | 250 | 130 | 200 | 100 |

3.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Mini family of processors for the following I/O types:

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see [Figure 7](#)).

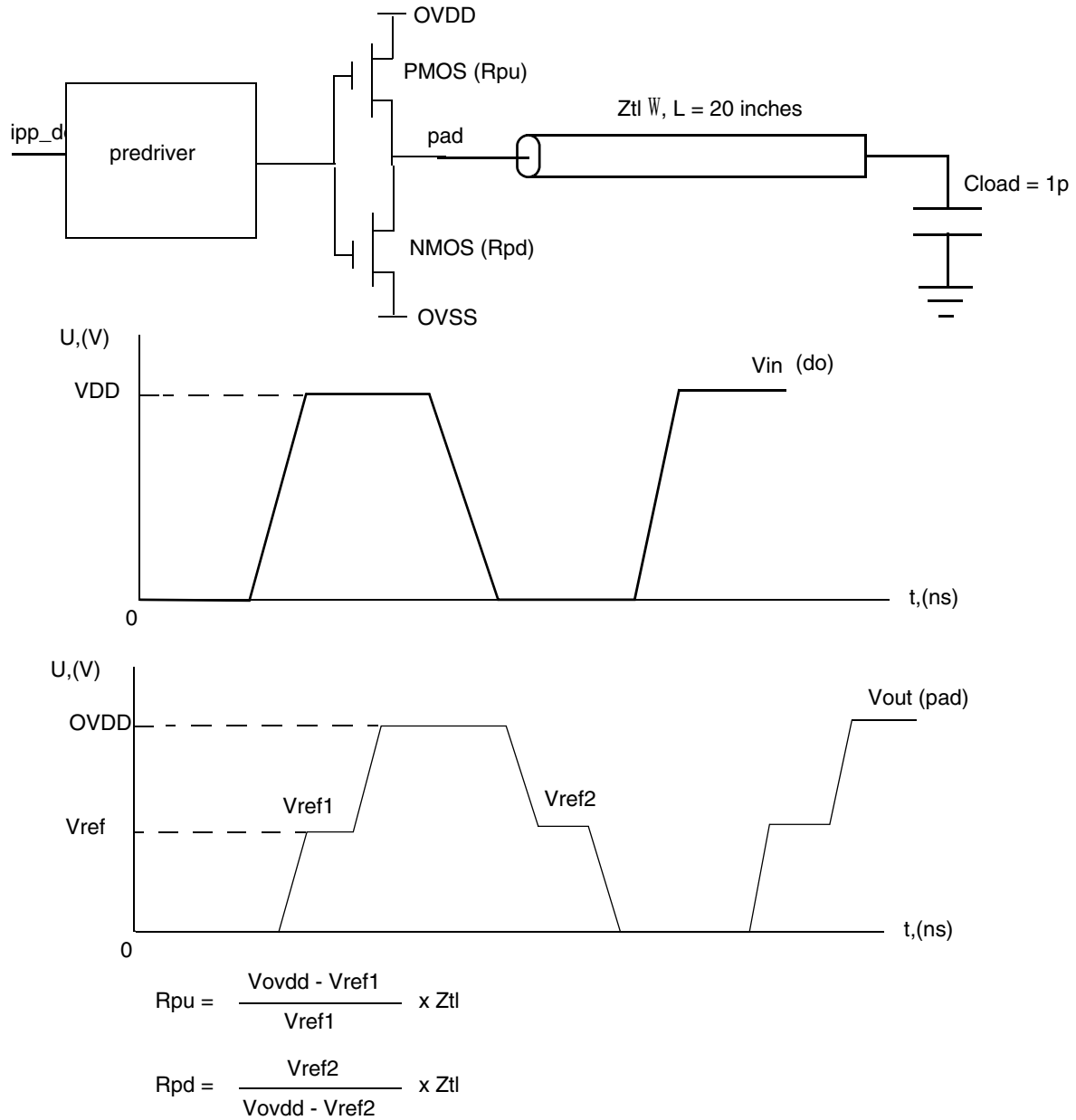


Figure 7. Impedance matching load for measurement

3.7.1 DDR I/O output buffer impedance

Table 25 shows DDR I/O output buffer impedance of i.MX 8M Mini family of processors.

Table 25. DDR I/O output buffer impedance

| Parameter | Symbol | Test Conditions DSE (Drive Strength) | Typical | | | Unit |
|-------------------------|--------|---|----------------------------|--------------------------|----------------------------|------|
| | | | NVCC_DRAM = 1.35 V (DDR3L) | NVCC_DRAM = 1.2 V (DDR4) | NVCC_DRAM = 1.1 V (LPDDR4) | |
| Output Driver Impedance | Rdrv | 000000 | Hi-Z | Hi-Z | Hi-Z | Ω |
| | | 000010 | 240 | 240 | 240 | |
| | | 001000 | 120 | 120 | 120 | |
| | | 001010 | 80 | 80 | 80 | |
| | | 011000 | 60 | 60 | 60 | |
| | | 011010 | 48 | 48 | 48 | |
| | | 111000 | 40 | 40 | 40 | |
| | | 111010 | 34 | 34 | 34 | |

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 8M Mini processor.

3.8.1 Reset timings parameters

Figure 8 shows the reset timing and Table 26 lists the timing parameters.

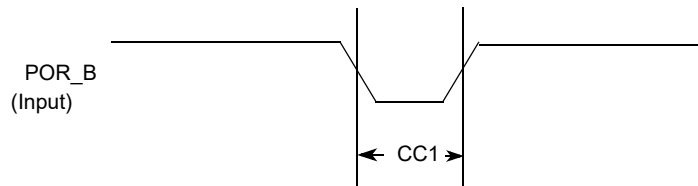


Figure 8. Reset timing diagram

Table 26. Reset timing parameters

| ID | Parameter | Min | Max | Unit |
|-----|---|-----|-----|-----------------|
| CC1 | Duration of POR_B to be qualified as valid. | 1 | — | RTC_XTALI cycle |

3.8.2 WDOG Reset timing parameters

Figure 9 shows the WDOG reset timing and Table 27 lists the timing parameters.

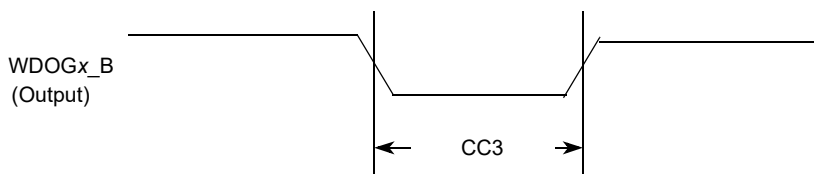


Figure 9. WDOGx_B timing diagram

Table 27. WDOGx_B timing parameters

| ID | Parameter | Min | Max | Unit |
|-----|-------------------------------|-----|-----|-----------------|
| CC3 | Duration of WDOGx_B Assertion | 1 | — | RTC_XTALI cycle |

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μ s.

NOTE

WDOGx_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 8M Mini Applications Processor Reference Manual* (IMX8MMRM) for detailed information.

3.9 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

3.9.1 ECSPi timing parameters

This section describes the timing parameters of the ECSPi blocks. The ECSPi have separate timing parameters for master and slave modes.

3.9.1.1 ECSPi Master mode timing

Figure 10 depicts the timing of ECSPi in master mode. Table 28 lists the ECSPi master mode timing characteristics.

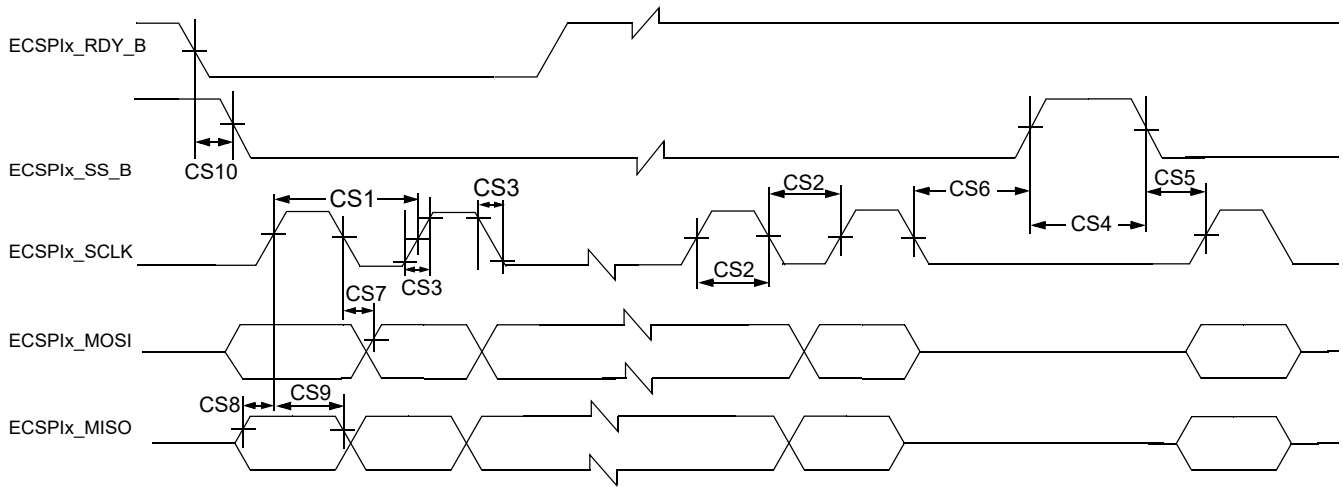


Figure 10. ECSPi Master mode timing diagram

Table 28. ECSPi Master mode timing parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|---|-----------------|----------------------------|-----|------|
| CS1 | ECSPi_SCLK Cycle Time–Read ECSPi_SCLK Cycle Time–Write | t_{clk} | 43 15 | — | ns |
| CS2 | ECSPi_SCLK High or Low Time–Read ECSPi_SCLK High or Low Time–Write | t_{sw} | 21.5 7 | — | ns |
| CS3 | ECSPi_SCLK Rise or Fall ¹ | $t_{RISE/FALL}$ | — | — | ns |
| CS4 | ECSPi_SS_B pulse width | t_{CSLH} | Half ECSPi_SCLK period | — | ns |
| CS5 | ECSPi_SS_B Lead Time (CS setup time) | t_{SCS} | Half ECSPi_SCLK period - 4 | — | ns |
| CS6 | ECSPi_SS_B Lag Time (CS hold time) | t_{HCS} | Half ECSPi_SCLK period - 2 | — | ns |
| CS7 | ECSPi_MOSI Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmosi} | -1 | 1 | ns |
| CS8 | ECSPi_MISO Setup Time | t_{Smiso} | 18 | — | ns |
| CS9 | ECSPi_MISO Hold Time | t_{Hmiso} | 0 | — | ns |
| CS10 | RDY to ECSPi_SS_B Time ² | t_{SDRY} | 5 | — | ns |

¹ See specific I/O AC parameters Section 3.6, I/O ac parameters.”

² SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

3.9.1.2 ECSPi Slave mode timing

Figure 11 depicts the timing of ECSPi in Slave mode. Table 29 lists the ECSPi Slave mode timing characteristics.

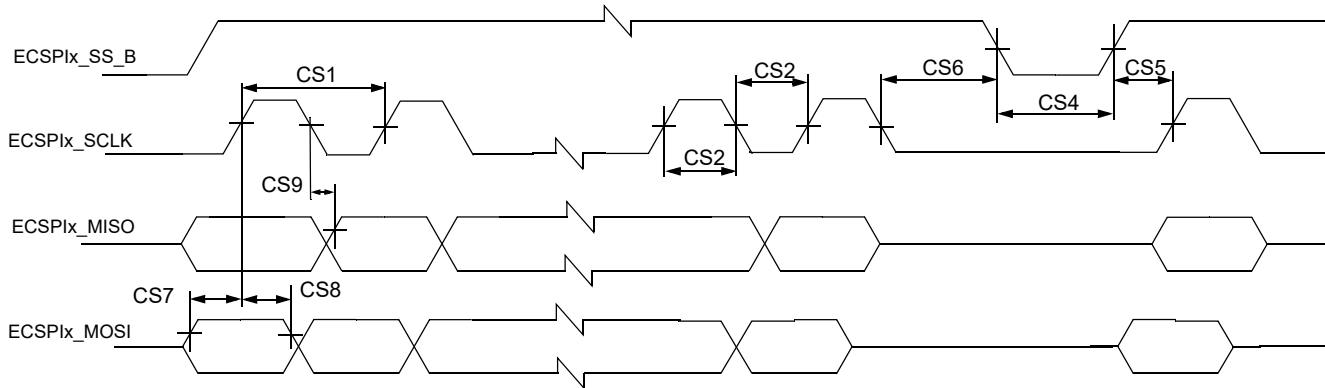


Figure 11. ECSPi Slave mode timing diagram

Table 29. ECSPi Slave mode timing parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|--------------|------------------------|-----|------|
| CS1 | ECSPi_SCLK Cycle Time–Read ECSPi_SCLK Cycle Time–Write | t_{clk} | 15 43 | — | ns |
| CS2 | ECSPi_SCLK High or Low Time–Read ECSPi_SCLK High or Low Time–Write | t_{sw} | 7 21.5 | — | ns |
| CS4 | ECSPi_SS_B pulse width | t_{CSLH} | Half ECSPi_SCLK period | — | ns |
| CS5 | ECSPi_SS_B Lead Time (CS setup time) | t_{SCS} | 5 | — | ns |
| CS6 | ECSPi_SS_B Lag Time (CS hold time) | t_{HCS} | 5 | — | ns |
| CS7 | ECSPi_MOSI Setup Time | t_{Smosi} | 4 | — | ns |
| CS8 | ECSPi_MOSI Hold Time | t_{Hmosi} | 4 | — | ns |
| CS9 | ECSPi_MISO Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmiso} | 4 | 19 | ns |

3.9.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC 5.1 (single data rate) timing, eMMC 5.1/SD3.0 (dual data rate) AC timing, and SDR50/SDR104 AC timing.

3.9.2.1 SD3.0/eMMC 5.1 (single data rate) AC timing

Figure 12 depicts the timing of SD3.0/eMMC5.1 (SDR), and Table 30 lists the SD3.0/eMMC5.1 (SDR) timing characteristics.

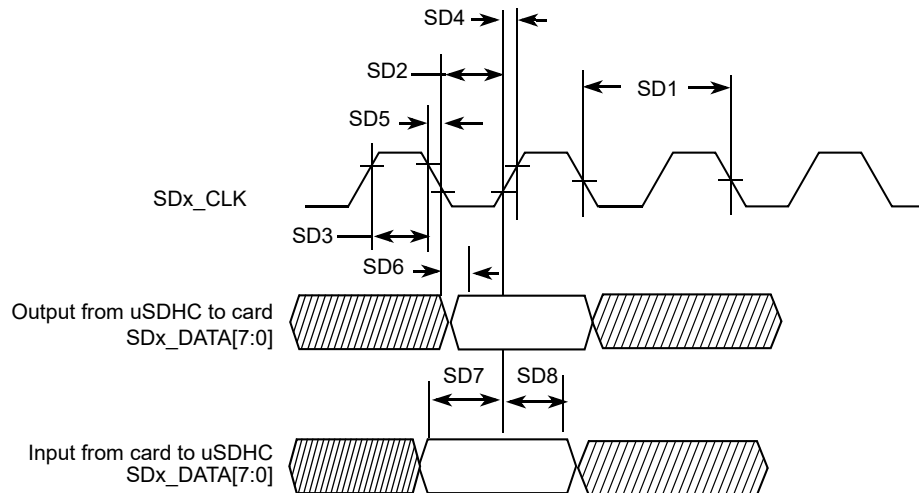


Figure 12. SD3.0/eMMC5.1 (SDR) timing

Table 30. SD3.0/eMMC5.1 (SDR) interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|---|------------|-----|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Low Time | t_{WL} | 7 | — | ns |
| SD3 | Clock High Time | t_{WH} | 7 | — | ns |
| SD4 | Clock Rise Time | t_{TLH} | — | 3 | ns |
| SD5 | Clock Fall Time | t_{THL} | — | 3 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD6 | uSDHC Output Delay | t_{OD} | 6.6 | 3.6 | ns |

Table 30. SD3.0/eMMC5.1 (SDR) interface timing specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|--|------------------------------------|-----------|-----|-----|------|
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD7 | uSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD8 | uSDHC Input Hold Time ⁴ | t_{IH} | 1.5 | — | ns |

¹ In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In High-speed mode, clock frequency can be any value between 0–50 MHz.

³ In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In High-speed mode, clock frequency can be any value between 0–52 MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.9.2.2 eMMC 5.1/SD3.0 (dual data rate) AC timing

Figure 13 depicts the timing of eMMC 5.1/SD3.0 (DDR). Table 31 lists the eMMC 5.1/SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

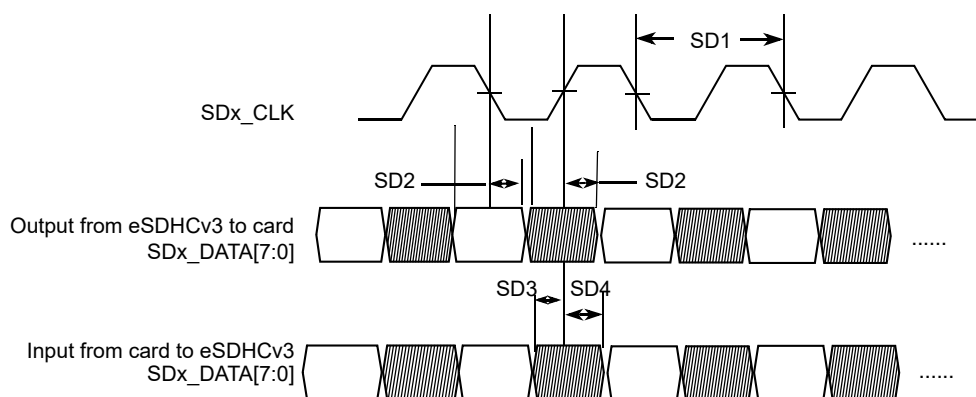


Figure 13. eMMC5.1/SD3.0 (DDR) timing

Table 31. eMMC5.1/SD3.0 (DDR) interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|-------------------------------|----------|-----|-----|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (eMMC5.1 DDR) | f_{PP} | 0 | 52 | MHz |
| SD1 | Clock Frequency (SD3.0 DDR) | f_{PP} | 0 | 50 | MHz |
| uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |
| SD2 | uSDHC Output Delay | t_{OD} | 2.7 | 6.9 | ns |
| uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) | | | | | |

Table 31. eMMC5.1/SD3.0 (DDR) interface timing specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|-----|------------------------|-----------|-----|-----|------|
| SD3 | uSDHC Input Setup Time | t_{ISU} | 2.4 | — | ns |
| SD4 | uSDHC Input Hold Time | t_{IH} | 1.3 | — | ns |

3.9.2.3 HS400 DDR AC timing

Figure 14 depicts the timing of HS400 mode, and Table 32 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 34 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

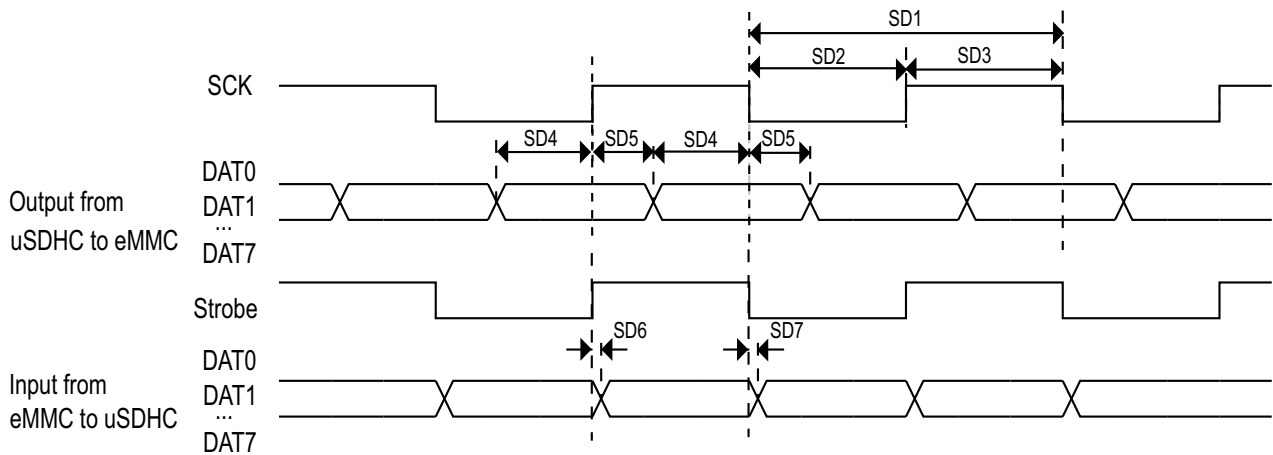


Figure 14. HS400 timing

Table 32. HS400 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|--------------------------------------|--------------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock frequency | f_{PP} | 0 | 200 | MHz |
| SD2 | Clock low time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock high time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs DAT (Reference to SCK) | | | | | |
| SD4 | Output skew from data of edge of SCK | t_{OSkew1} | 0.45 | — | ns |
| SD5 | Output skew from edge of SCK to data | t_{OSkew2} | 0.45 | — | ns |
| uSDHC Input/Card Outputs DAT (Reference to Strobe) | | | | | |

Table 32. HS400 interface timing specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|-----|------------------|-----------|-----|------|------|
| SD6 | uSDHC input skew | t_{RQ} | — | 0.45 | ns |
| SD7 | uSDHC hold skew | t_{RQH} | — | 0.45 | ns |

3.9.2.4 HS200 Mode AC timing

Figure 15 depicts the timing of HS200 mode, and Table 33 lists the HS200 timing characteristics.

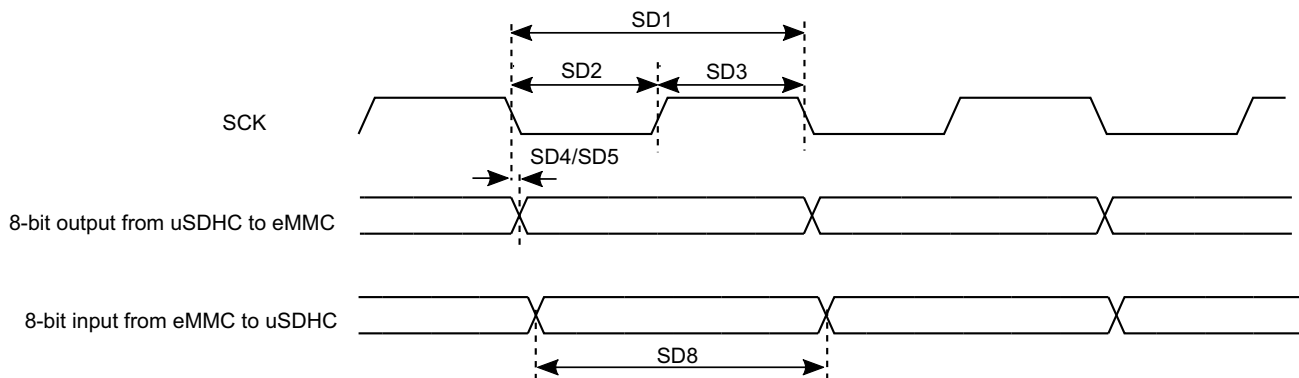


Figure 15. HS200 timing

Table 33. HS200 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|--------------------------|-----------|----------------------|----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 5.0 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.3 \times t_{CLK}$ | $0.7 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.3 \times t_{CLK}$ | $0.7 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 1 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)¹ | | | | | |
| SD8 | uSDHC Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹ HS200 is for 8 bits while SDR104 is for 4 bits.

3.9.2.5 SDR50/SDR104 AC timing

Figure 16 depicts the timing of SDR50/SDR104, and Table 34 lists the SDR50/SDR104 timing characteristics.

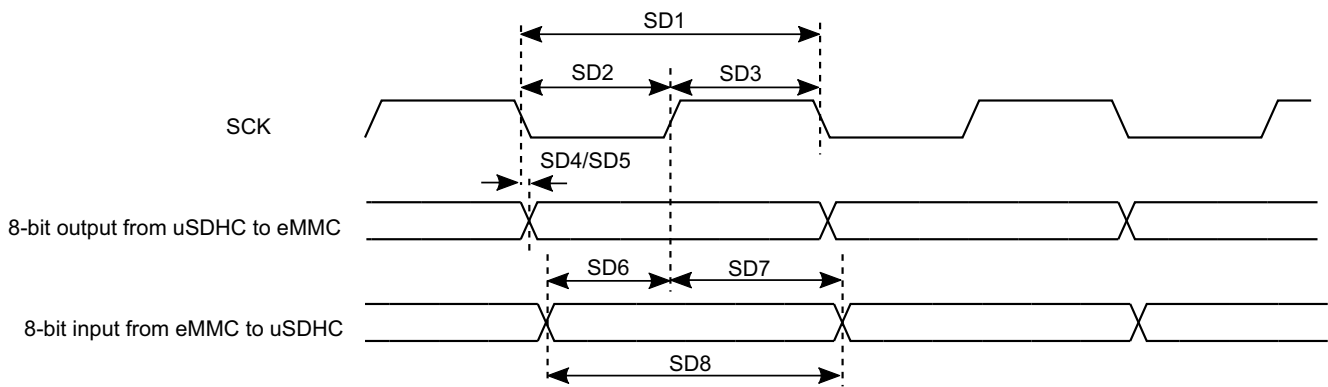


Figure 16. SDR50/SDR104 timing

Table 34. SDR50/SDR104 interface timing specification

| ID | Parameter | Symbols | Min | Max | Unit |
|--|--------------------------|-----------|-----------------------|-----------------------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency Period | t_{CLK} | 5 | — | ns |
| SD2 | Clock Low Time | t_{CL} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| SD3 | Clock High Time | t_{CH} | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD4 | uSDHC Output Delay | t_{OD} | -3 | 1 | ns |
| uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK) | | | | | |
| SD5 | uSDHC Output Delay | t_{OD} | -1.6 | 1 | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK) | | | | | |
| SD6 | uSDHC Input Setup Time | t_{ISU} | 2.4 | — | ns |
| SD7 | uSDHC Input Hold Time | t_{IH} | 1.4 | — | ns |
| uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)¹ | | | | | |
| SD8 | uSDHC Output Data Window | t_{ODW} | $0.5 \times t_{CLK}$ | — | ns |

¹ Data window in SDR100 mode is variable.

3.9.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 21, "GPIO DC parameters," on page 28.

3.9.3 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 35. ENET signal mapping

| Pad name | Description | Mode | Alt mode | Direction | Comments |
|-------------|---|------------|-----------|-----------|--|
| ENET_MDC | enet1.MDC | RMII/RGMII | ALT0 | O | — |
| ENET_MDIO | enet1.MDIO | RMII/RGMII | ALT0 | I/O | — |
| ENET_TD3 | RGMII.TD3 | RGMII | ALT0 | O | Only used for RGMII |
| ENET_TD2 | RMII.CLK; RGMII.TD2 | RMII/RGMII | ALT0 | I/O | Used as RMII clock and RGMII data, there are two RGMII clock schemes. <ul style="list-style-type: none"> • MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock. • MAC use external 50M clock. |
| ENET_TD1 | RMII and RGMII.TD1 | RMII/RGMII | ALT0 | O | — |
| ENET_TD0 | RMII and RGMII.TD0 | RMII/RGMII | ALT0 | O | — |
| ENET_TX_CTL | RMII.TX_EN; RGMII.TX_CTL | RMII/RGMII | ALT0 | O | — |
| ENET_TXC | RMII.TX_ERR; RGMII.TX_CLK | RGMII | ALT0/ALT1 | O | For RMII—ENET_TXC works as RMII.TX_ERR need to work in the ALT1 mode. For RGMII—ENET_TXC works as RGMII.TX_CLK need to work in the ALT0 mode. |
| ENET_RX_CTL | RMII.RX_EN (CRS_DV); RGMII.RC_CTL | RMII/RGMII | ALT0 | I | — |
| ENET_RXC | RMII.RX_ERR; RGMII.RX_CLK | RGMII | ALT0/ALT1 | I | For RMII—ENET_RXC works as RMII.RX_ERR need to work in the ALT1 mode. For RGMII—ENET_RXC works as RGMII.RX_CLK need to work in the ALT0 mode. |
| ENET_RD0 | RMII and RGMII.RD0 | RMII/RGMII | ALT0 | I | — |
| ENET_RD1 | RMII and RGMII.RD1 | RMII/RGMII | ALT0 | I | — |
| ENET_RD2 | RGMII.RD2 | RGMII | ALT0 | I | — |
| ENET_RD3 | RGMII.RD3 | RGMII | ALT0 | I | — |
| GPIO1_IO06 | enet1.MDC | RMII/RGMII | ALT1 | O | — |
| GPIO1_IO07 | enet1.MDIO | RMII/RGMII | ALT1 | I/O | — |
| I2C1_SCL | enet1.MDC | RMII/RGMII | ALT1 | O | — |

Table 35. ENET signal mapping (continued)

| Pad name | Description | Mode | Alt mode | Direction | Comments |
|------------|---------------------------|------------|----------|-----------|---|
| I2C1_SDA | enet1.MDIO | RMII/RGMII | ALT1 | I/O | — |
| I2C2_SCL | enet1.1588_EV ENT1_IN | RMII/RGMII | ALT1 | O | — |
| I2C2_SDA | enet1.1588_EV ENT1_OUT | RMII/RGMII | ALT1 | I/O | — |
| GPIO1_IO00 | ENET_PHY_RE F_CLK_ROOT | RGMII | ALT1 | O | Reference clock for PHY. |
| GPIO1_IO08 | enet1.1588_EV ENT0_IN | RMII/RGMII | ALT1 | I | Capture/compare block input/output event bus signal. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_EVENT is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TCSRn[TDRE] is set. |
| GPIO1_IO09 | enet1.1588_EV ENT0_OUT | RMII/RGMII | ALT1 | O | — |

3.9.3.1 RMII mode timing

Figure 17 shows RMII mode timings. Table 36 describes the timing parameters (M16–M21) shown in the figure.

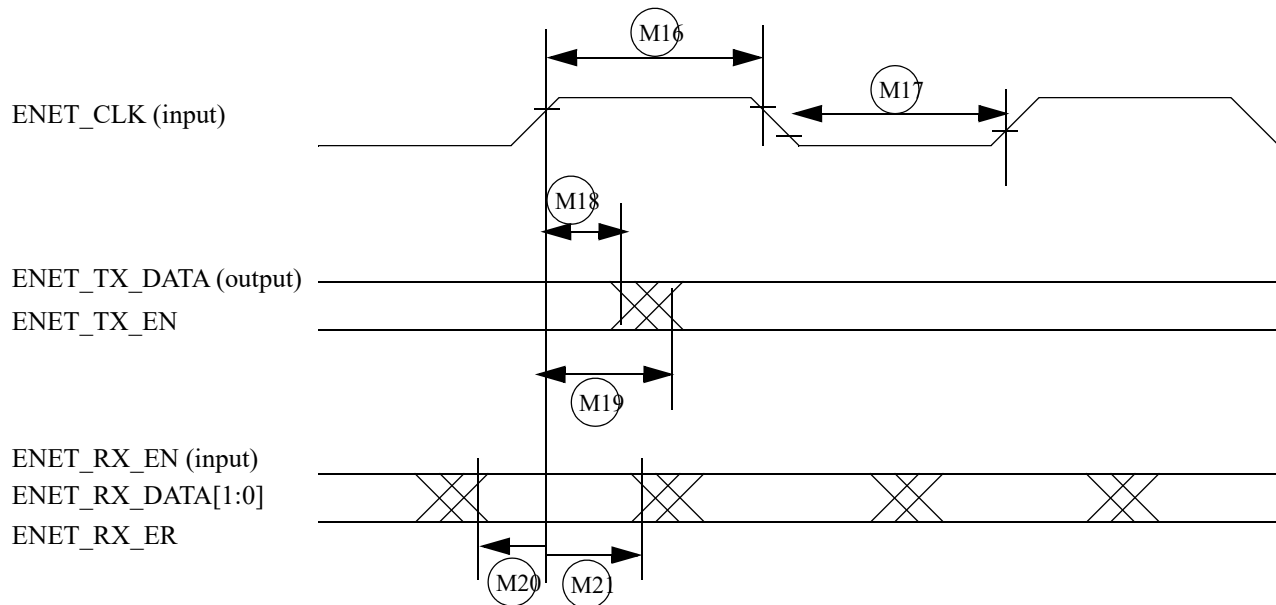


Figure 17. RMI mode signal timing diagram

Table 36. RMI signal timing

| ID | Characteristic | Min. | Max. | Unit |
|-----|---|------|------|-----------------|
| M16 | ENET_CLK pulse width high | 35% | 65% | ENET_CLK period |
| M17 | ENET_CLK pulse width low | 35% | 65% | ENET_CLK period |
| M18 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid | 4 | — | ns |
| M19 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid | — | 15 | ns |
| M20 | ENET_RX_DATA[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup | 4 | — | ns |
| M21 | ENET_CLK to ENET_RX_DATA[1:0], ENET_RX_EN, ENET_RX_ER hold | 2 | — | ns |

3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 37. RGMII signal switching specifications¹

| Symbol | Description | Min. | Max. | Unit |
|---------------------|--|------|------|------|
| T_{cyc}^2 | Clock cycle duration | 7.2 | 8.8 | ns |
| T_{skewT}^3 | Data to clock output skew at transmitter | -500 | 500 | ps |
| T_{skewR}^3 | Data to clock input skew at receiver | 1 | 2.6 | ns |
| Duty_G ⁴ | Duty cycle for Gigabit | 45 | 55 | % |
| Duty_T ⁴ | Duty cycle for 10/100T | 40 | 60 | % |
| Tr/Tf | Rise/fall time (20–80%) | — | 0.75 | ns |

Electrical characteristics

- 1 The timings assume the following configuration:
 DDR_SEL = (11)b
 DSE (drive-strength) = (111)b
- 2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns \pm 40 ns and 40 ns \pm 4 ns respectively.
- 3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.
- 4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

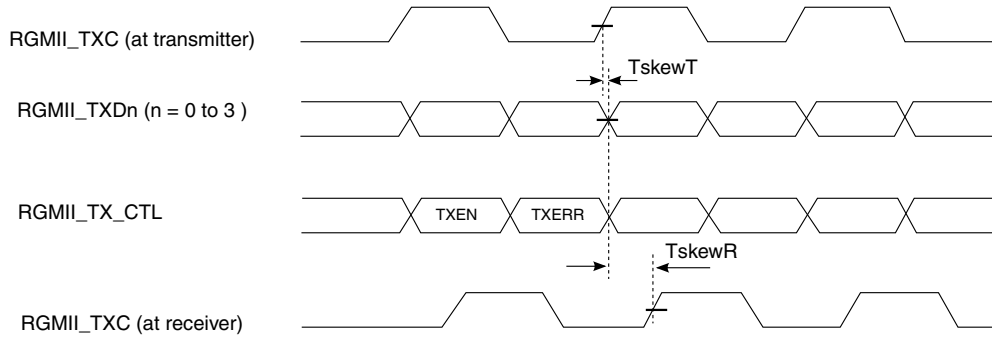


Figure 18. RGMII transmit signal timing diagram original

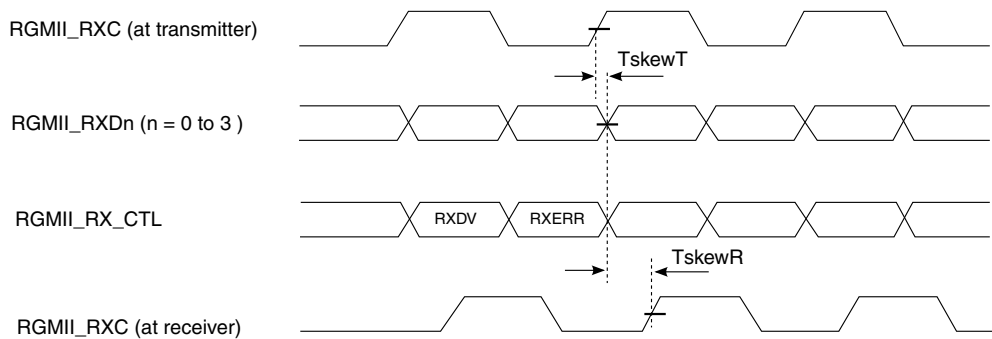


Figure 19. RGMII receive signal timing diagram original

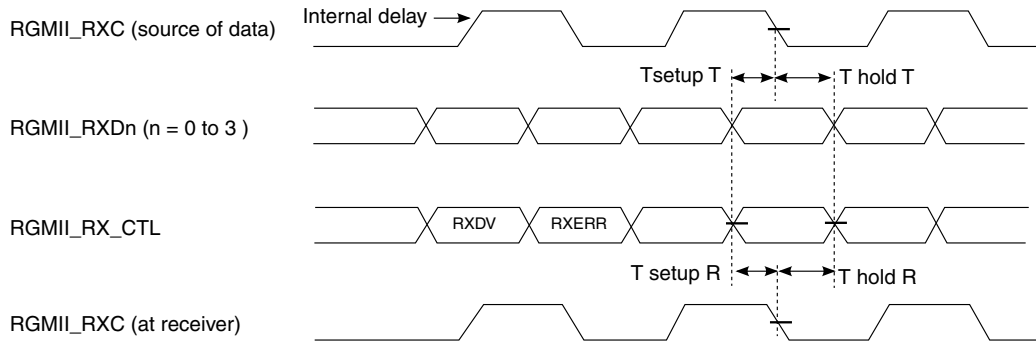


Figure 20. RGMII receive signal timing diagram with internal delay

3.9.4 General-purpose media interface (GPMI) timing

The i.MX 8M Mini GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 21 through Figure 24 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 38 describes the timing parameters (NF1–NF17) that are shown in the figures.

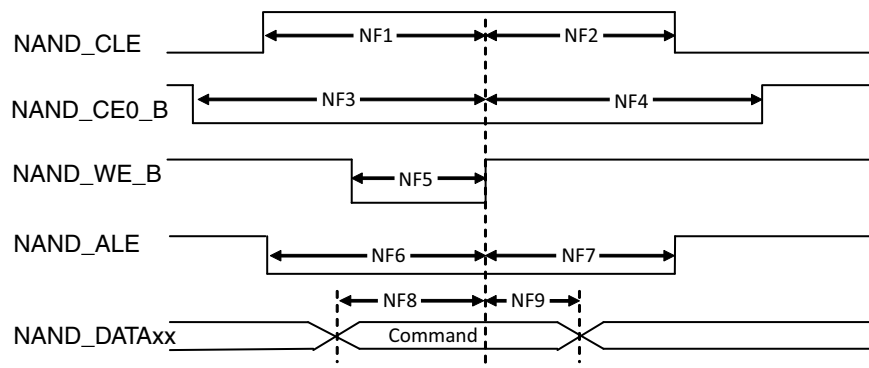


Figure 21. Command Latch cycle timing diagram

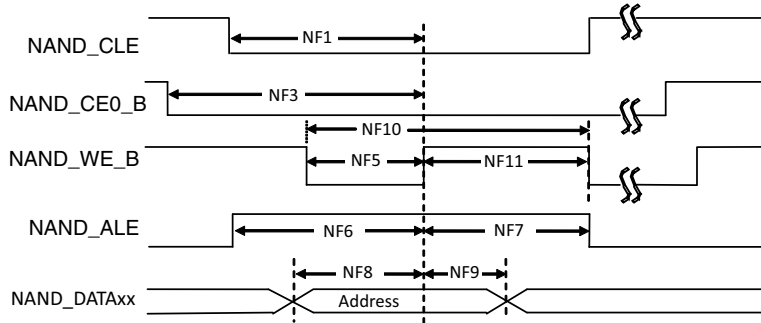


Figure 22. Address Latch cycle timing diagram

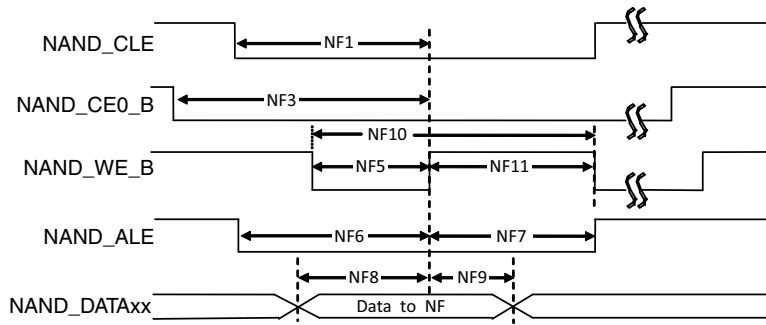


Figure 23. Write Data Latch cycle timing diagram

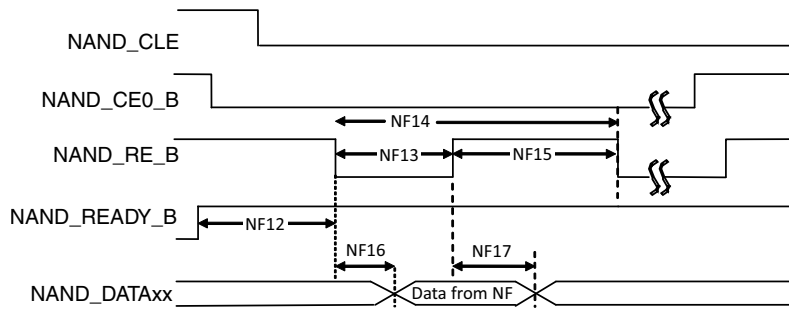


Figure 24. Read Data Latch cycle timing diagram (Non-EDO Mode)

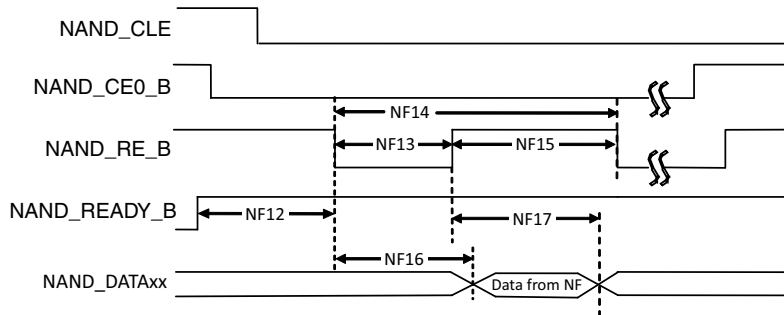


Figure 25. Read Data Latch cycle timing diagram (EDO mode)

Table 38. Asynchronous mode timing parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|--------------------------|------------------|---|--|------|
| | | | Min. | Max. | |
| NF1 | NAND_CLE setup time | tCLS | $(AS + DS) \times T - 0.12$ [see notes ^{2,3}] | | ns |
| NF2 | NAND_CLE hold time | tCLH | $DH \times T - 0.72$ [see note ²] | | ns |
| NF3 | NAND_CE0_B setup time | tCS | $(AS + DS + 1) \times T$ [see notes ^{3,2}] | | ns |
| NF4 | NAND_CE0_B hold time | tCH | $(DH+1) \times T - 1$ [see note ²] | | ns |
| NF5 | NAND_WE_B pulse width | tWP | $DS \times T$ [see note ²] | | ns |
| NF6 | NAND_ALE setup time | tALS | $(AS + DS) \times T - 0.49$ [see notes ^{3,2}] | | ns |
| NF7 | NAND_ALE hold time | tALH | $DH \times T - 0.42$ [see note ²] | | ns |
| NF8 | Data setup time | tDS | $DS \times T - 0.26$ [see note ²] | | ns |
| NF9 | Data hold time | tDH | $DH \times T - 1.37$ [see note ²] | | ns |
| NF10 | Write cycle time | tWC | $(DS + DH) \times T$ [see note ²] | | ns |
| NF11 | NAND_WE_B hold time | tWH | $DH \times T$ [see note ²] | | ns |
| NF12 | Ready to NAND_RE_B low | tRR ⁴ | $(AS + 2) \times T$ [see ^{3,2}] | — | ns |
| NF13 | NAND_RE_B pulse width | tRP | $DS \times T$ [see note ²] | | ns |
| NF14 | READ cycle time | tRC | $(DS + DH) \times T$ [see note ²] | | ns |
| NF15 | NAND_RE_B high hold time | tREH | $DH \times T$ [see note ²] | | ns |
| NF16 | Data setup on read | tDSR | — | $(DS \times T - 0.67)/18.38$ [see notes ^{5,6}] | ns |
| NF17 | Data hold on read | tDHR | 0.82/11.83 [see notes ^{5,6}] | — | ns |

¹ GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

² AS minimum value can be 0, while DS/DH minimum value is 1.

³ T = GPMI clock period -0.075 ns (half of maximum p-p jitter).

⁴ NF12 is guaranteed by the design.

⁵ Non-EDO mode.

⁶ EDO mode, GPMI clock \approx 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 are different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND_DATAxx at the rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 8M Mini Applications Processor Reference Manual* [IMX8MMRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous mode.

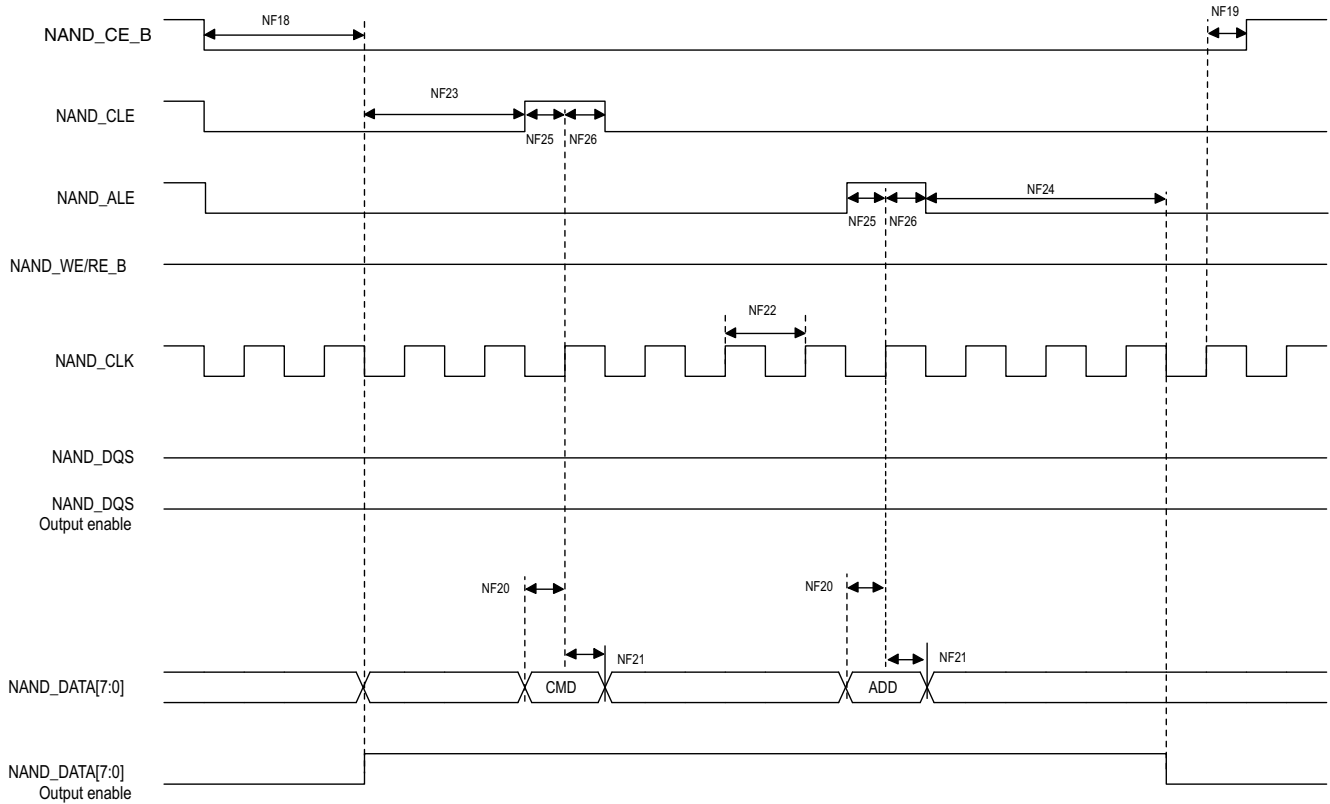


Figure 26. Source Synchronous mode command and address timing diagram

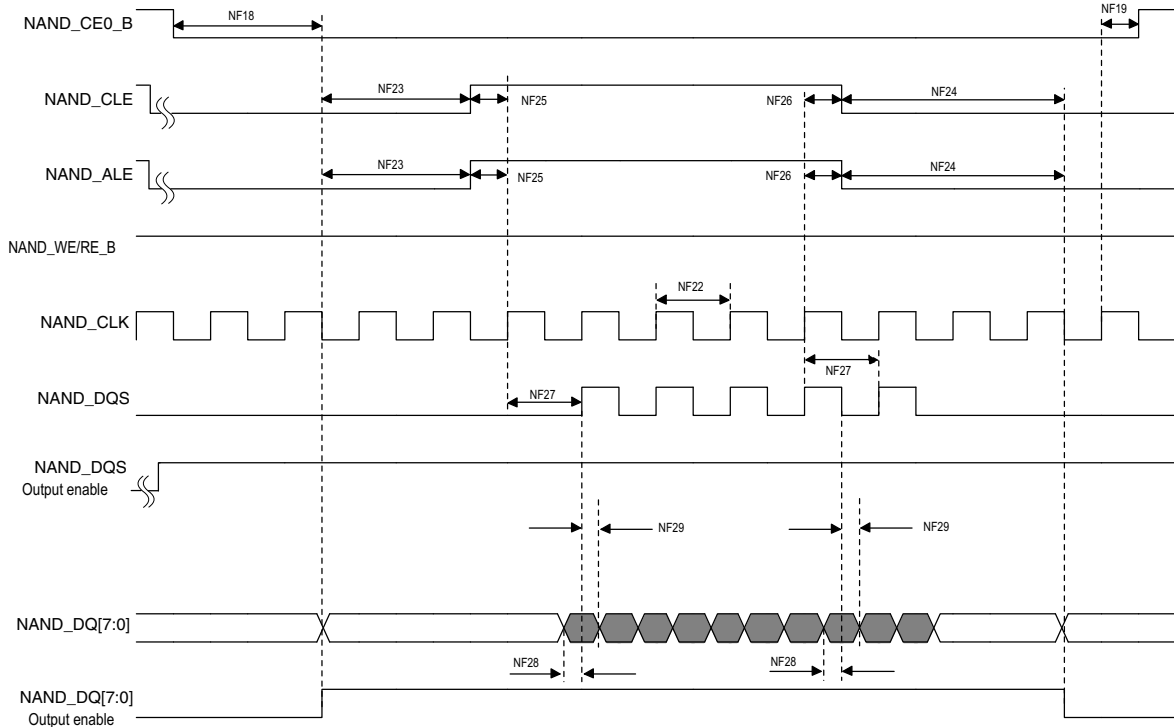


Figure 27. Source Synchronous mode data write timing diagram

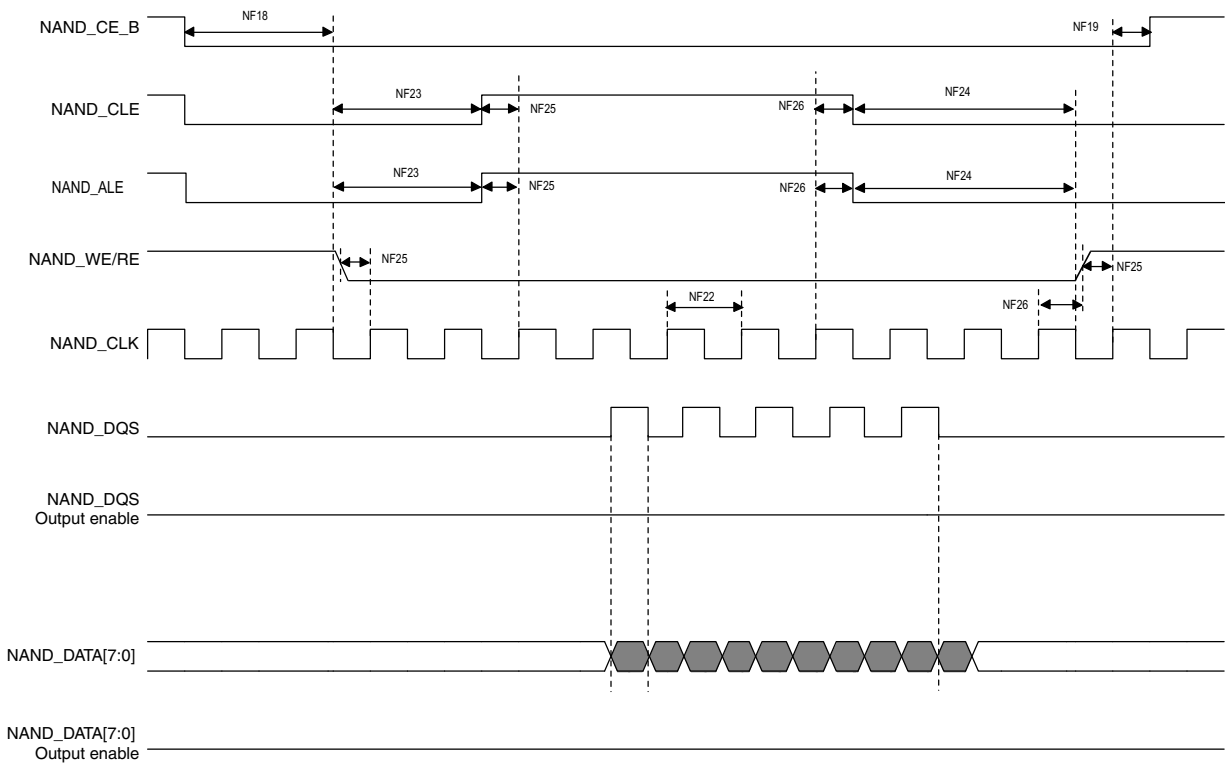


Figure 28. Source Synchronous mode data read timing diagram

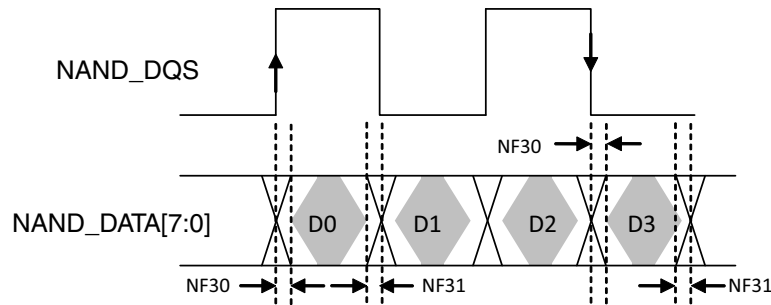


Figure 29. NAND_DQS/NAND_DQ read valid window

Table 39. Source Synchronous mode timing parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|--|--------|--|------|------|
| | | | Min. | Max. | |
| NF18 | NAND_CEO_B access time | tCE | CE_DELAY × T - 0.79 [see note ²] | | ns |
| NF19 | NAND_CEO_B hold time | tCH | 0.5 × tCK - 0.63 [see note ²] | | ns |
| NF20 | Command/address NAND_DATAxx setup time | tCAS | 0.5 × tCK - 0.05 | | ns |
| NF21 | Command/address NAND_DATAxx hold time | tCAH | 0.5 × tCK - 1.23 | | ns |
| NF22 | clock period | tCK | — | | ns |
| NF23 | preamble delay | tPRE | PRE_DELAY × T - 0.29 [see note ²] | | ns |
| NF24 | postamble delay | tPOST | POST_DELAY × T - 0.78 [see note ²] | | ns |
| NF25 | NAND_CLE and NAND_ALE setup time | tCALS | 0.5 × tCK - 0.86 | | ns |
| NF26 | NAND_CLE and NAND_ALE hold time | tCALH | 0.5 × tCK - 0.37 | | ns |
| NF27 | NAND_CLK to first NAND_DQS latching transition | tDQSS | T - 0.41 [see note ²] | | ns |
| NF28 | Data write setup | — | 0.25 × tCK - 0.35 | | |
| NF29 | Data write hold | — | 0.25 × tCK - 0.85 | | |
| NF30 | NAND_DQS/NAND_DQ read setup skew | — | — | 2.06 | |
| NF31 | NAND_DQS/NAND_DQ read hold skew | — | — | 1.95 | |

¹ GPMI's Source Synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING2_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

² T = tCK(GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

For DDR Source Synchronous mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Mini Applications Processor Reference Manual [IMX8MMRM]*). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

3.9.4.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See [Section 3.9.4.1, Asynchronous mode AC timing \(ONFI 1.0 compatible\)](#),” for details.

3.9.4.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See [Section 3.9.4.4, Toggle mode AC Timing](#),” for details.

3.9.4.4 Toggle mode AC Timing

3.9.4.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See [Section 3.9.4.1, Asynchronous mode AC timing \(ONFI 1.0 compatible\)](#),” for details.

3.9.4.4.2 Read and write timing

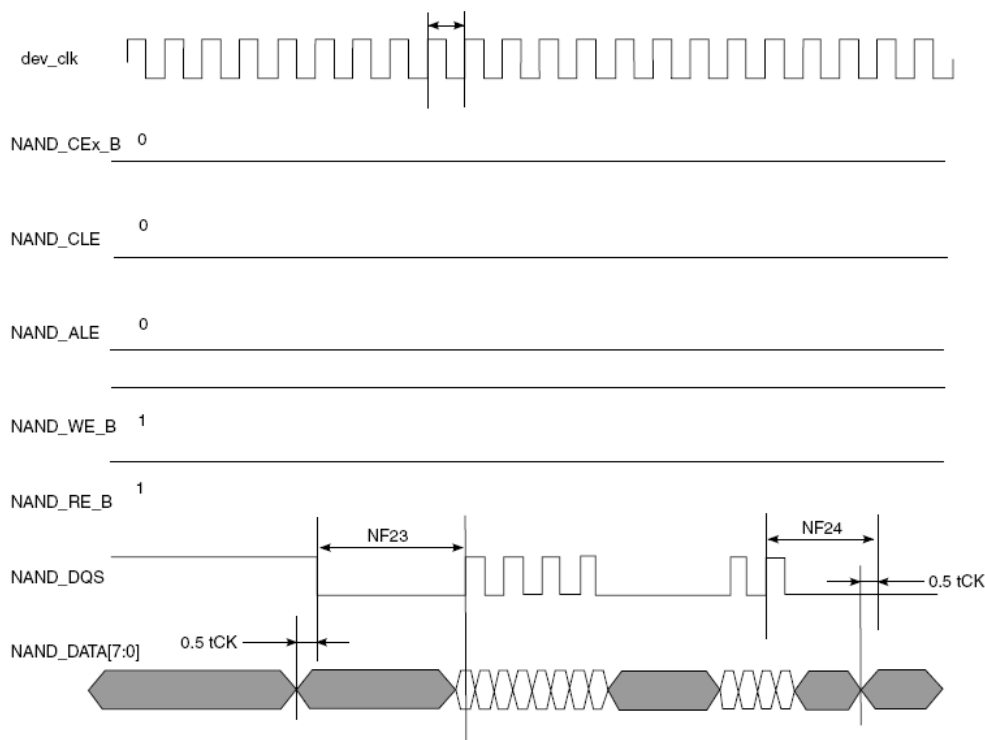


Figure 30. Toggle mode data write timing

Electrical characteristics

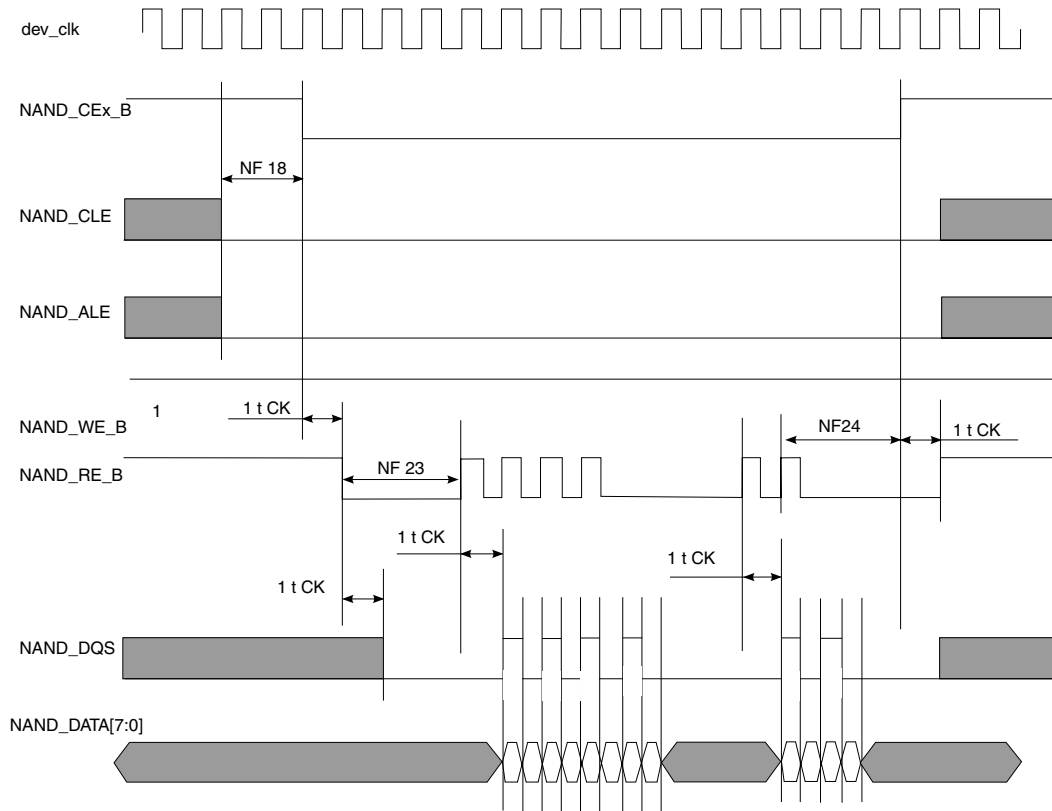


Figure 31. Toggle mode data read timing

Table 40. Toggle mode timing parameters

| ID | Parameter | Symbol | Timing T = GPML Clock Cycle | | Unit |
|------|--|--------|--|------|------|
| | | | Min. | Max. | |
| NF1 | NAND_CLE setup time | tCLS | $(AS + DS) \times T - 0.12$ [see note ^{1,2}] | | |
| NF2 | NAND_CLE hold time | tCLH | $DH \times T - 0.72$ [see note ²] | | |
| NF3 | NAND_CE0_B setup time | tCS | $(AS + DS) \times T - 0.58$ [see notes ²] | | |
| NF4 | NAND_CE0_B hold time | tCH | $DH \times T - 1$ [see note ²] | | |
| NF5 | NAND_WE_B pulse width | tWP | $DS \times T$ [see note ²] | | |
| NF6 | NAND_ALE setup time | tALS | $(AS + DS) \times T - 0.49$ [see notes ²] | | |
| NF7 | NAND_ALE hold time | tALH | $DH \times T - 0.42$ [see note ²] | | |
| NF8 | Command/address NAND_DATAxx setup time | tCAS | $DS \times T - 0.26$ [see note ²] | | |
| NF9 | Command/address NAND_DATAxx hold time | tCAH | $DH \times T - 1.37$ [see note ²] | | |
| NF18 | NAND_CEx_B access time | tCE | $CE_DELAY \times T$ [see notes ^{3,2}] | — | ns |
| NF22 | clock period | tCK | — | — | ns |
| NF23 | preamble delay | tPRE | $PRE_DELAY \times T$ [see notes ^{4,2}] | — | ns |

Table 40. Toggle mode timing parameters (continued)

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Unit |
|------|----------------------------------|--------------------|--|------|------|
| | | | Min. | Max. | |
| NF24 | postamble delay | tPOST | POST_DELAY × T + 0.43 [see note ²] | — | ns |
| NF28 | Data write setup | tDS ⁵ | 0.25 × tCK - 0.32 | — | ns |
| NF29 | Data write hold | tDH ⁵ | 0.25 × tCK - 0.79 | — | ns |
| NF30 | NAND_DQS/NAND_DQ read setup skew | tDQSQ ⁶ | — | 3.18 | ns |
| NF31 | NAND_DQS/NAND_DQ read hold skew | tQHS ⁶ | — | 3.27 | ns |

¹ AS minimum value can be 0, while DS/DH minimum value is 1.

² T = tCK (GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

³ CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

⁴ PRE_DELAY+1 ≥ (AS+DS)

⁵ Shown in Figure 30.

⁶ Shown in Figure 31.

For DDR Toggle mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI samples NAND_DATA[7:0] at both the rising and falling edges of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by the GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Mini Applications Processor Reference Manual* [IMX8MMRM]). Generally, the typical delay value is equal to 0x7, which means a 1/4 clock cycle delay is expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.5 I²C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

3.9.6 MIPI D-PHY timing parameters

MIPI D-PHY electrical specifications are compliance.

Table 41. MIPI PHY worst power dissipation¹

| MODE | | Power consume on VDD_MIPI_0P9 (mW) | Power consume on VDD_MIPI_1P2 (mW) | Power consume on VDD_MIPI_1P8 (mW) | Total power consume (mW) |
|----------|-----------------|------------------------------------|------------------------------------|------------------------------------|--------------------------|
| 2.1 Gbps | M4 on S4 on | 226.1 | 4.1 | 35.6 | 265.8 |
| | M4 on S4 off | 164.7 | 4.03 | 28.6 | 197.33 |
| | M4 off S4 on | 63.02 | 0 | 15.8 | 78.82 |
| ULPS | | 4.26 | 0.0367 | 0.0584 | 4.36 |

¹ M4 indicates MIPI DSI have 4 data lane enable (at least 1 clock lane enable). S4 indicates MIPI CSI have 4 data lane enable (at least 1 clock lane enable).

3.9.7 PCIe PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

Table 42. PCIe DC electrical characteristics

| Parameter | Description | Min | Typ | Max | Unit | |
|-----------|-------------------|----------------|-----|-------|------|----|
| PD | Power Consumption | Normal Gen2 | — | 129.5 | — | mW |
| | | Partial Mode | — | 98.2 | — | mW |
| | | Slumber Mode | — | 4.9 | — | mW |
| | | Full Powerdown | — | 0.1 | — | mW |

3.9.7.1 PCIE_RESREF reference resistor connection

The impedance calibration process requires connection of reference resistor 8.2 k Ω . 1% precision resistor on PCIE_RESREF pads to ground. It is used for termination impedance calibration.

3.9.8 PDM timing parameters

Figure 32 illustrates the input timing of the PDM.

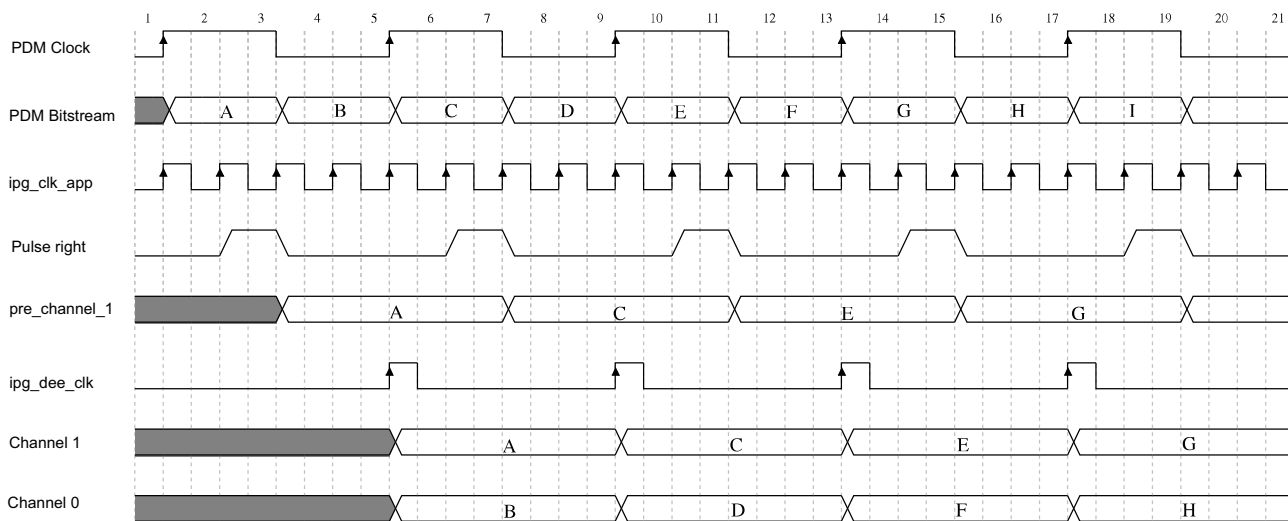


Figure 32. PDM input timing

PDM clock operative range is from 500 kHz to 6 MHz. Within range, only need to configure `ipg_clk_app` rate and `CLKDIV` without I/O timing concerns.

3.9.9 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 33 depicts the timing of the PWM, and Table 43 lists the PWM timing parameters.

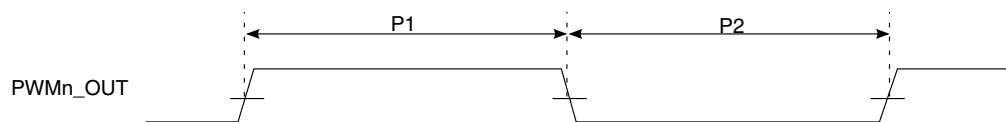


Figure 33. PWM timing

Table 43. PWM output timing parameters

| ID | Parameter | Min | Max | Unit |
|----|-----------------------------|-----|-----------------------------|------|
| | PWM Module Clock Frequency | 0 | 66 (<code>ipg_clk</code>) | MHz |
| P1 | PWM output pulse width high | 12 | — | ns |
| P2 | PWM output pulse width low | 12 | — | ns |

3.9.10 FlexSPI timing parameters

Measurements are with a load of 15 pF and an input slew rate of 1 V/ns.

3.9.10.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI_n_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI_n_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI_n_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these four internal sample clock sources.

3.9.10.1.1 SDR mode with FlexSPI_n_MCR0[RXCLKSRC] = 0x0, 0x1

Table 44. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x0

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| — | [D:] Frequency of operation | — | 66 | MHz | — |
| F1 | [D:] Setup time for incoming data | 8.67 | — | ns | 1 |
| F2 | [D:] Hold time for incoming data | 0 | — | ns | — |

¹ The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 45. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x1

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| — | [D:] Frequency of operation | — | 133 | MHz | — |
| F1 | [D:] Setup time for incoming data | 1.5 | — | ns | 1 |
| F2 | [D:] Hold time for incoming data | 1 | — | ns | — |

¹ The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

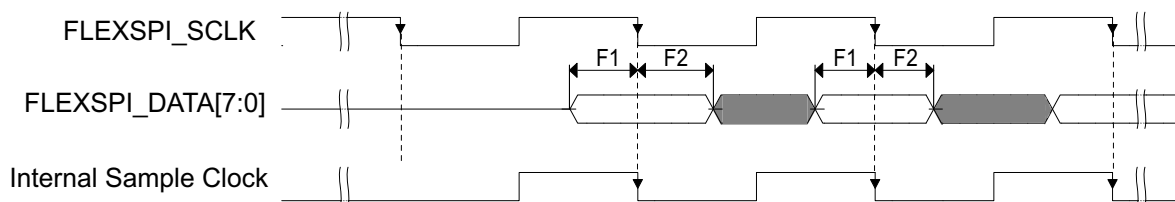


Figure 34. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x0, 0x1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

3.9.10.1.2 SDR mode with FlexSPI_n_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 46. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (Case A1)

| Symbol | Parameter | Min. | Max. | Unit |
|--------|---|------|------|------|
| — | [D:] Frequency of operation | — | 166 | MHz |
| F3 | [D:] Time from SCK to data valid | — | — | ns |
| F4 | [D:] Time from SCK to DQS | — | — | ns |
| — | [D:] Time delta between TSCKD and TSCKDQS | -2 | 2 | ns |

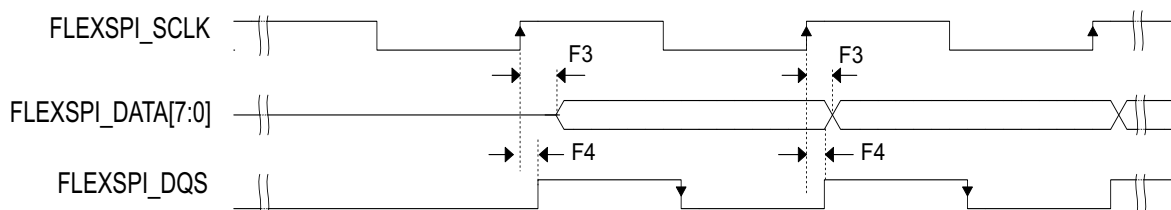


Figure 35. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (Case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 47. FlexSPI input timing in SDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (Case A2)

| Symbol | Parameter | Min. | Max. | Unit |
|--------|---|------|------|------|
| — | [D:] Frequency of operation | — | 166 | MHz |
| F5 | [D:] Time from SCK to data valid | — | — | ns |
| F6 | [D:] Time from SCK to DQS | — | — | ns |
| — | [D:] Time delta between TSCKD and TSCKDQS | -2 | 2 | ns |

Electrical characteristics

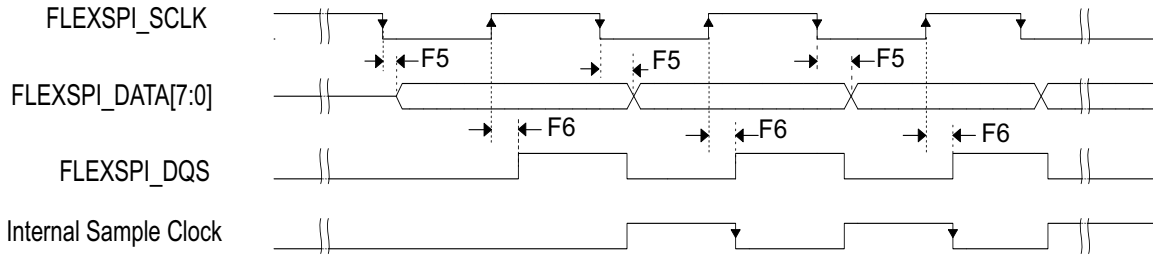


Figure 36. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (Case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half-cycle delayed DQS falling edge.

3.9.10.1.3 DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1

Table 48. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| — | [D:] Frequency of operation | — | 33 | MHz | — |
| F1 | [D:] Setup time for incoming data | 8.67 | — | ns | 1 |
| F2 | [D:] Hold time for incoming data | 0 | — | ns | — |

¹ The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 49. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x1

| Symbol | Parameter | Min. | Max. | Unit | Notes |
|--------|-----------------------------------|------|------|------|-------|
| — | [D:] Frequency of operation | — | 66 | MHz | — |
| F1 | [D:] Setup time for incoming data | 1.5 | — | ns | 1 |
| F2 | [D:] Hold time for incoming data | 1 | — | ns | — |

¹ The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

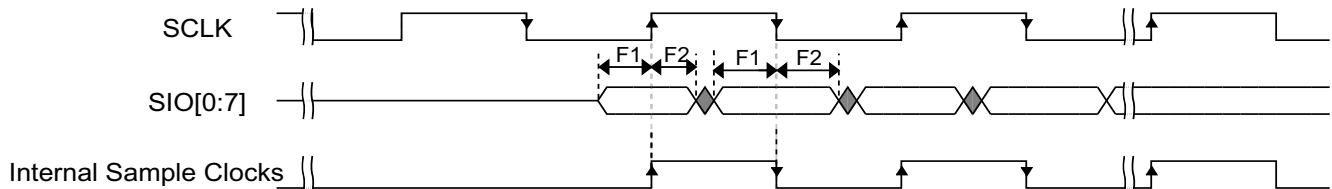


Figure 37. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1

3.9.10.1.4 DDR mode with FlexSPI_n_MCR0[RXCLKSRC] = 0x3

Table 50. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3 (Case 1)

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|------|------|------|
| — | [D:] Frequency of operation | — | 166 | MHz |
| T _{SCKD} | [D:] Time from SCK to data valid | — | — | ns |
| T _{SCKDQS} | [D:] Time from SCK to DQS | — | — | ns |
| T _{SCKD} - T _{SCKDQS} | [D:] Time delta between T _{SCKD} and T _{SCKDQS} | -0.6 | 0.6 | ns |

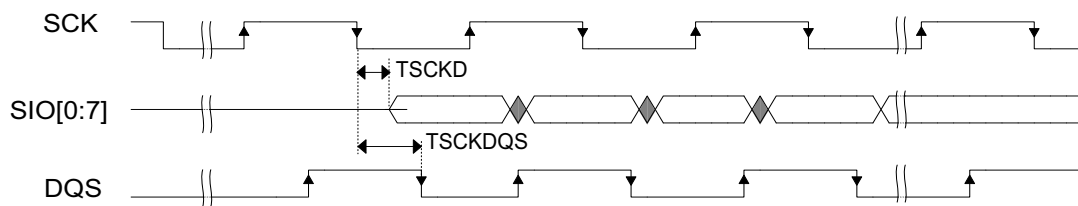


Figure 38. FlexSPI input timing in DDR mode where FlexSPI_n_MCR0[RXCLKSRC] = 0x3

3.9.10.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

3.9.10.2.1 SDR mode

Table 51. FlexSPI output timing in SDR mode

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------------------|--|-------------------------|------|------|
| — | [D:] Frequency of operation ¹ | — | 166 | MHz |
| T _{CK} | [D:] SCK clock period | 6.02 | — | ns |
| T _{D_{SO}} | [D:] Output data setup time | 2 | — | ns |
| T _{D_{HO}} | [D:] Output data hold time | 2 | — | ns |
| T _{C_{SS}} | [D:] Chip select output setup time | 3 x T _{CK} - 1 | — | ns |
| T _{C_{SH}} | [D:] Chip select output hold time | 3 x T _{CK} - 1 | — | ns |

Electrical characteristics

¹ The actual maximum frequency supported is limited by the FlexSPI_n_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI_n_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM)* for more details.

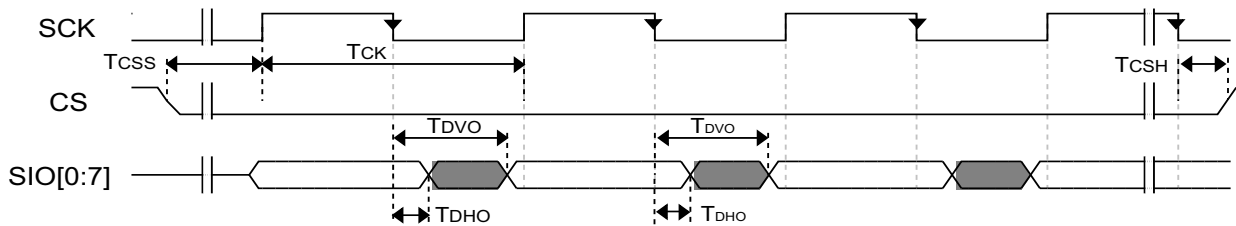


Figure 39. FlexSPI output timing in SDR mode

3.9.10.2.2 DDR mode

Table 52. FlexSPI output timing in DDR mode

| Symbol | Parameter | Min. | Max. | Unit |
|-----------|--|---------------------------|------|------|
| — | [D:] Frequency of operation ¹ | — | 166 | MHz |
| T_{CK} | [D:] SCK clock period | 6.02 | — | ns |
| T_{DSO} | [D:] Output data setup time | — | 0.6 | ns |
| T_{DHO} | [D:] Output data hold time | 0.6 | — | ns |
| T_{CSS} | [D:] Chip select output setup time | $3 \times T_{CK} - 1.075$ | — | ns |
| T_{CSH} | [D:] Chip select output hold time | $3 \times T_{CK} - 1.075$ | — | ns |

¹ The actual maximum frequency supported is limited by the FlexSPI_n_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI_n_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM)* for more details.

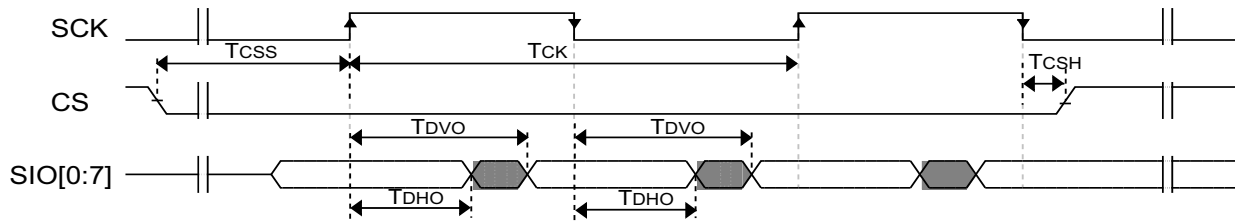


Figure 40. FlexSPI output timing in DDR mode

3.9.11 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 53. Master mode SAI timing (50 MHz)¹

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|-------------|
| S1 | SAI_MCLK cycle time | 20 | — | ns |
| S2 | SAI_MCLK pulse width high/low | 40% | 60% | MCLK period |
| S3 | SAI_BCLK cycle time | 20 | — | ns |
| S4 | SAI_BCLK pulse width high/low | 40% | 60% | BCLK period |
| S5 | SAI_BCLK to SAI_FS output valid | — | 2 | ns |
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | — | ns |
| S7 | SAI_BCLK to SAI_TXD valid | — | 2 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | — | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 2 | — | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | — | ns |

¹ To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.

Table 54. Master mode SAI timing (25 MHz)

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------|-----|-----|-------------|
| S1 | SAI_MCLK cycle time | 40 | — | ns |
| S2 | SAI_MCLK pulse width high/low | 40% | 60% | MCLK period |
| S3 | SAI_BCLK cycle time | 40 | — | ns |
| S4 | SAI_BCLK pulse width high/low | 40% | 60% | BCLK period |
| S5 | SAI_BCLK to SAI_FS output valid | — | 2 | ns |

Electrical characteristics

Table 54. Master mode SAI timing (25 MHz) (continued)

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|------|
| S6 | SAI_BCLK to SAI_FS output invalid | 0 | — | ns |
| S7 | SAI_BCLK to SAI_TXD valid | — | 2 | ns |
| S8 | SAI_BCLK to SAI_TXD invalid | 0 | — | ns |
| S9 | SAI_RXD/SAI_FS input setup before SAI_BCLK | 12 | — | ns |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK | 0 | — | ns |

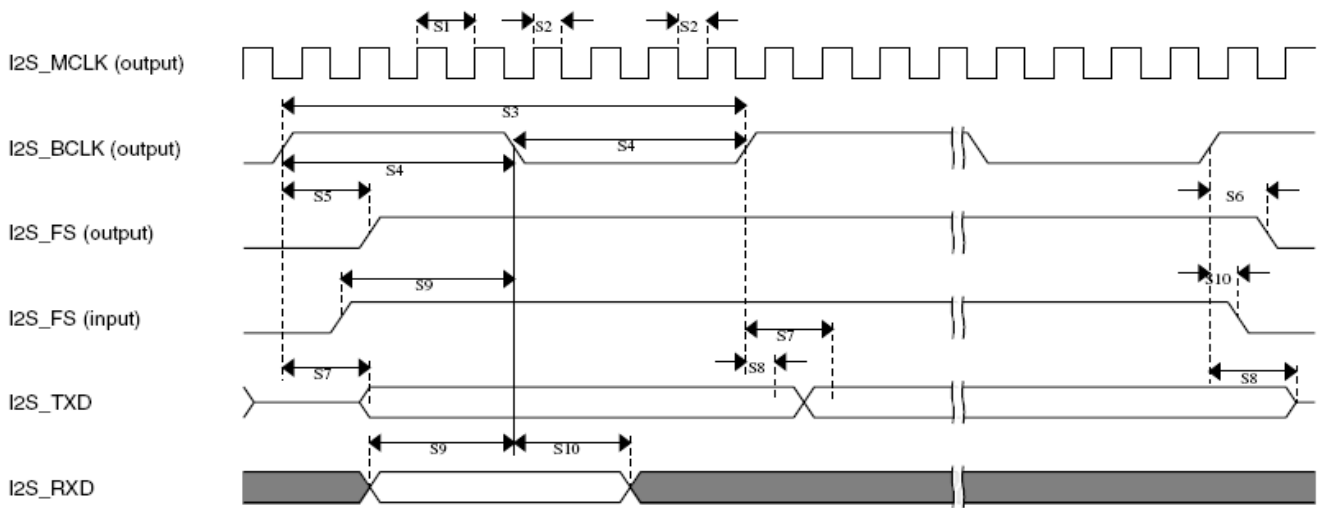


Figure 41. SAI timing—Master modes

Table 55. Slave mode SAI timing (50 MHz)¹

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------------|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input) | 20 | — | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 40% | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK | 2 | — | ns |
| S14 | SAI_FA input hold after SAI_BCLK | 2 | — | ns |
| S17 | SAI_RXD setup before SAI_BCLK | 2 | — | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | — | ns |

¹ TX does not support 50 MHz operation in Slave mode.

Table 56. Slave mode SAI timing (25 MHz)

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------------|-----|-----|-------------|
| S11 | SAI_BCLK cycle time (input) | 40 | — | ns |
| S12 | SAI_BCLK pulse width high/low (input) | 40% | 60% | BCLK period |

Table 56. Slave mode SAI timing (25 MHz) (continued)

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|------|
| S13 | SAI_FS input setup before SAI_BCLK | 12 | — | ns |
| S14 | SAI_FA input hold after SAI_BCLK | 2 | — | ns |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid | — | 7 | ns |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0 | — | ns |
| S17 | SAI_RXD setup before SAI_BCLK | 12 | — | ns |
| S18 | SAI_RXD hold after SAI_BCLK | 2 | — | ns |

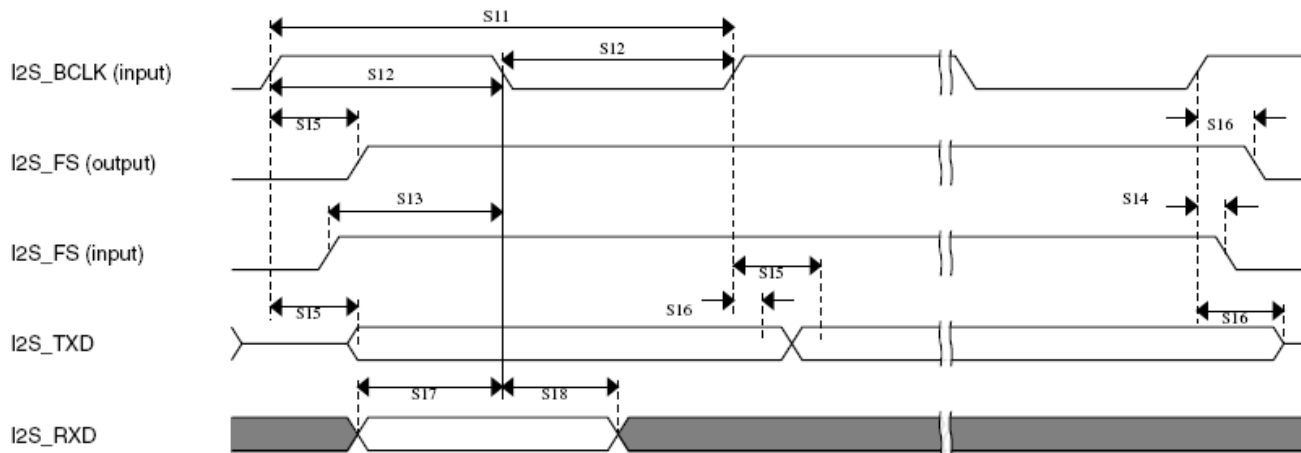


Figure 42. SAI Timing — Slave Modes

3.9.12 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 57 and Figure 43 and Figure 44 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 57. SPDIF timing parameters

| Parameter | Symbol | Timing Parameter Range | | Unit |
|--|--------|------------------------|------|------|
| | | Min | Max | |
| SPDIF_IN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIF_OUT output (Load = 50 pf) | | | | |
| • Skew | — | — | 1.5 | ns |
| • Transition rising | — | — | 24.2 | |
| • Transition falling | — | — | 31.3 | |

Table 57. SPDIF timing parameters (continued)

| Parameter | Symbol | Timing Parameter Range | | Unit |
|--|--------|------------------------|---------------------|------|
| | | Min | Max | |
| SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling | — | — | 1.5 13.6 18.0 | ns |
| Modulating Rx clock (SPDIF_SR_CLK) period | srckp | 40.0 | — | ns |
| SPDIF_SR_CLK high period | srckph | 16.0 | — | ns |
| SPDIF_SR_CLK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (SPDIF_ST_CLK) period | stckp | 40.0 | — | ns |
| SPDIF_ST_CLK high period | stckph | 16.0 | — | ns |
| SPDIF_ST_CLK low period | stckpl | 16.0 | — | ns |

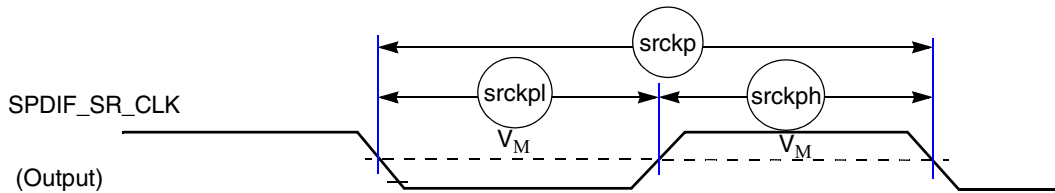


Figure 43. SPDIF_SR_CLK timing diagram

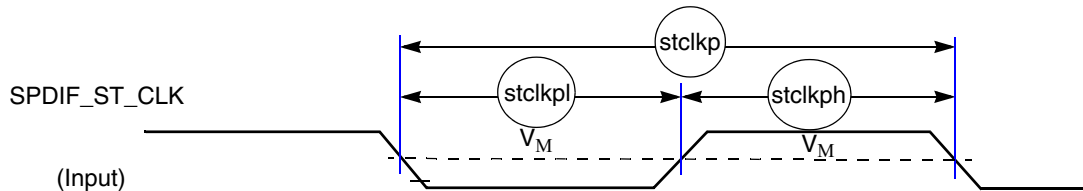


Figure 44. SPDIF_ST_CLK timing diagram

3.9.13 UART I/O configuration and timing parameters

3.9.13.1 UART RS-232 I/O configuration in different modes

The i.MX 8M Mini UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 58 shows the UART I/O configuration based on the enabled mode.

Table 58. UART I/O configuration vs. mode

| Port | DTE Mode | | DCE Mode | |
|---------------|-----------|-----------------------------|-----------|-----------------------------|
| | Direction | Description | Direction | Description |
| UARTx_RTS_B | Output | UARTx_RTS_B from DTE to DCE | Input | UARTx_RTS_B from DTE to DCE |
| UARTx_CTS_B | Input | UARTx_CTS_B from DCE to DTE | Output | UARTx_CTS_B from DCE to DTE |
| UARTx_TX_DATA | Input | Serial data from DCE to DTE | Output | Serial data from DCE to DTE |
| UARTx_RX_DATA | Output | Serial data from DTE to DCE | Input | Serial data from DTE to DCE |

3.9.13.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

3.9.13.2.1 UART transmitter

Figure 45 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 59 lists the UART RS-232 Serial mode transmit timing characteristics.

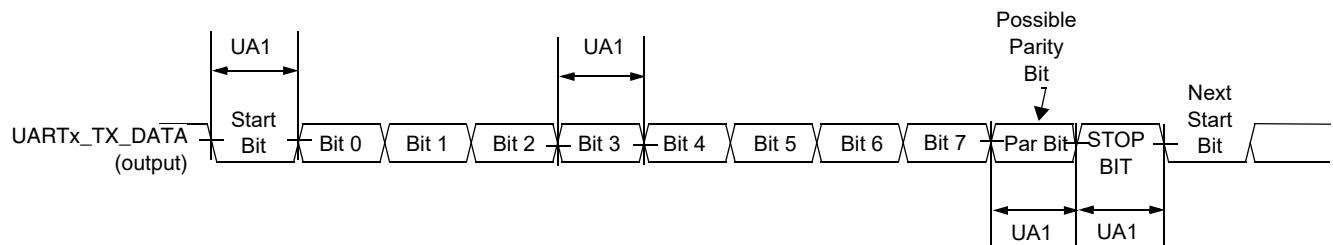


Figure 45. UART RS-232 Serial mode transmit timing diagram

Table 59. RS-232 Serial mode transmit timing parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------|------------|---------------------------------------|-----------------------------------|------|
| UA1 | Transmit Bit Time | t_{Tbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

3.9.13.2.2 UART receiver

Figure 46 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 60 lists Serial mode receive timing characteristics.

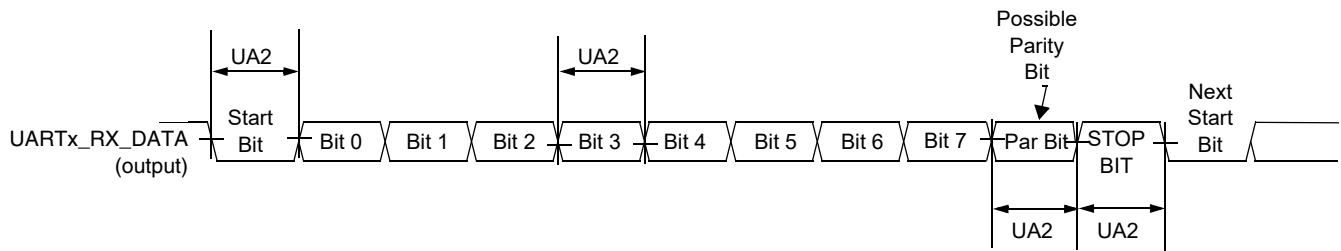


Figure 46. UART RS-232 Serial mode receive timing diagram

Table 60. RS-232 Serial mode receive timing parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------------------|------------|---|---|------|
| UA2 | Receive Bit Time ¹ | t_{Rbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

3.9.14 USB PHY parameters

This section describes the USB-OTG PHY parameters.

3.9.14.1 Pad/Package/Board connections

The USBx_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

Each USBx_VBUS pin must be isolated by an external 30 K Ω 1% precision resistor.

The USB 2.0 PHY uses USBx_TXRTUNE and an external resistor to calibrate the USBx_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on each of USBx_TXRTUNE pad to ground.

3.9.14.2 USB PHY worst power consumption

Table 61 shows the USB 2.0 PHY worst power dissipation.

Table 61. USB 2.0 PHY worst power dissipation

| Mode | VDD_USB_0P8 | VDD_USB_3P3 | VDD_USB_1P8 | Total Power |
|---------|-------------|-------------|-------------|-------------|
| HS TX | 8.286 | 4.63 | 23.409 | 70.448 |
| FS TX | 6.767 | 12.52 | 5.968 | 63.22 |
| LS TX | 7.001 | 13.58 | 6.224 | 67.779 |
| Suspend | 0.752 | 0.164 | 0.106 | 1.465 |
| Sleep | 0.761 | 0.163 | 0.106 | 1.472 |

4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

Table 62 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the “System Boot, Fusemap, and eFuse” chapter in the *i.MX 8M Mini Applications Processor Reference Manual* (IMX8MMRM).

Table 62. Fuses and associated pins used for boot

| Pin | Direction at Reset | eFuse name | State during reset (POR_B asserted) | State after reset (POR_B deasserted) | Details |
|------------|--------------------|--------------|-------------------------------------|--------------------------------------|--|
| BOOT_MODE0 | Input | N/A | Input with pull down | Input with pull down | Boot mode selection |
| BOOT_MODE1 | Input | N/A | Input with pull down | Input with pull down | |
| SAI1_RXD0 | Input | BOOT_CFG[0] | Input with pull down | Input with pull down | Boot options pin value overrides fuse settings for BT_FUSE_SEL = "0". Signal configuration as fuse override input at power up. These are special I/O lines that control the boot configuration during product development. In production, the boot configuration can be controlled by fuses. |
| SAI1_RXD1 | Input | BOOT_CFG[1] | Input with pull down | Input with pull down | |
| SAI1_RXD2 | Input | BOOT_CFG[2] | Input with pull down | Input with pull down | |
| SAI1_RXD3 | Input | BOOT_CFG[3] | Input with pull down | Input with pull down | |
| SAI1_RXD4 | Input | BOOT_CFG[4] | Input with pull down | Input with pull down | |
| SAI1_RXD5 | Input | BOOT_CFG[5] | Input with pull down | Input with pull down | |
| SAI1_RXD6 | Input | BOOT_CFG[6] | Input with pull down | Input with pull down | |
| SAI1_RXD7 | Input | BOOT_CFG[7] | Input with pull down | Input with pull down | |
| SAI1_TXD0 | Input | BOOT_CFG[8] | Input with pull down | Input with pull down | |
| SAI1_TXD1 | Input | BOOT_CFG[9] | Input with pull down | Input with pull down | |
| SAI1_TXD2 | Input | BOOT_CFG[10] | Input with pull down | Input with pull down | |
| SAI1_TXD3 | Input | BOOT_CFG[11] | Input with pull down | Input with pull down | |
| SAI1_TXD4 | Input | BOOT_CFG[12] | Input with pull down | Input with pull down | |
| SAI1_TXD5 | Input | BOOT_CFG[13] | Input with pull down | Input with pull down | |
| SAI1_TXD6 | Input | BOOT_CFG[14] | Input with pull down | Input with pull down | |

4.2 Boot device interface allocation

Table 63 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 63. Interface allocation during boot

| Interface | IP Instance | Allocated Pads During Boot | Comment |
|------------|-------------|---|--|
| SPI | ECSPI-1 | ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0 | The chip-select pin used depends on the fuse "CS select (SPI only)". |
| SPI | ECSPI-2 | ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0 | The chip-select pin used depends on the fuse "CS select (SPI only)". |
| SPI | ECSPI-3 | UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD | The chip-select pin used depends on the fuse "CS select (SPI only)". |
| NAND Flash | GPMI | NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B | 8-bit, only CS0 is supported. |
| SD/MMC | USDHC-1 | GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7 | 1, 4, or 8-bit |
| SD/MMC | USDHC-2 | GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3 | 1 or 4-bit |
| SD/MMC | USDHC-3 | NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B | 1, 4, or 8-bit |
| FlexSPI | FlexSPI | NAND_ALE, NAND_CE0_B, NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B | For FlexSPI flash |
| USB | USB_OTG PHY | Dedicated USB pins | — |

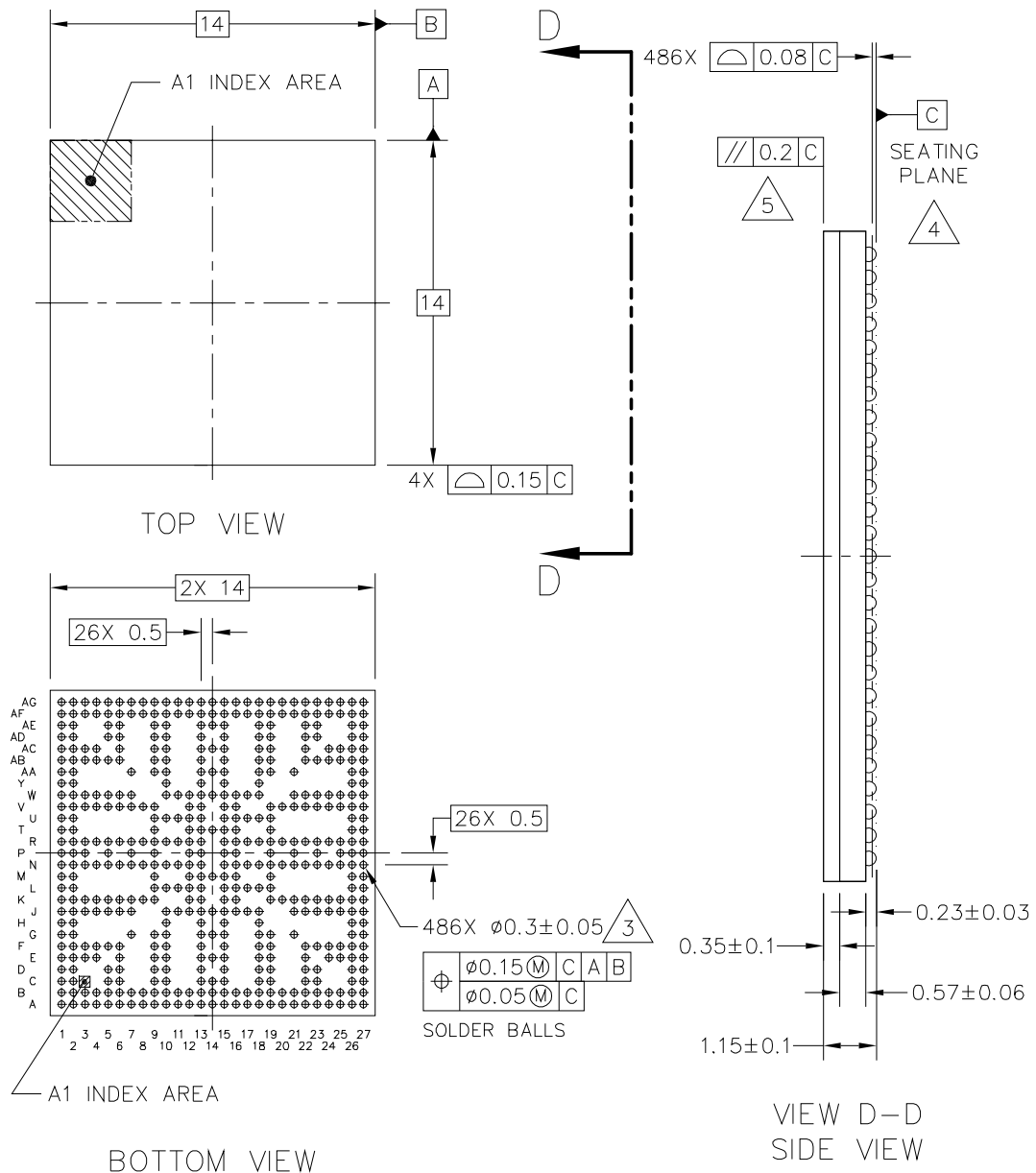
5 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 14 x 14 mm package information

5.1.1 14 x 14 mm, 0.5 mm pitch, ball matrix

[Figure 47](#) shows the top, bottom, and side views of the 14 × 14 mm FCBGA package.



| | | |
|--|---------------------------|----------------------------|
| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: FCPBGA, MOLDED ARRAY, 14 X 14 X 1.15 PKG, 0.5 MM PITCH, 486 I/O | DOCUMENT NO: 98ASA01200D | REV: B |
| | STANDARD: NON-JEDEC | |
| | SOT1967-1 | 02 AUG 2018 |

Figure 47. 14 X 14 MM BGA, case x package top, bottom, and side views

5.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 64 shows supplies contact assignments for the 14 x 14 mm package.

Table 64. i.MX 8M Mini 14 x 14 mm supplies contact assignments

| Supply Rail Name | Ball(s) Position(s) | Remark |
|------------------|--|----------------------------|
| NC | J18 | — |
| NVCC_CLK | M19 | Supply for CLK interface |
| NVCC_DRAM | P7, K8, N8, R8, V8, K9, L9, M9, N9, R9, T9, U9, V9 | Supply for DRAM interface |
| NVCC_ECSPi | H10 | Supply for ECSPi interface |
| NVCC_ENET | W22 | Supply for ENET interface |
| NVCC_GPIO1 | W12 | Supply for GPIO1 interface |
| NVCC_I2C | J11 | Supply for I2C interface |
| NVCC_JTAG | L19 | Supply for JTAG interface |
| NVCC_NAND | U19 | Supply for NAND interface |
| NVCC_SAI1 | W18 | Supply for SAI interface |
| NVCC_SAI2 | V19 | Supply for SAI interface |
| NVCC_SAI3 | Y10 | Supply for SAI interface |
| NVCC_SAI5 | W17 | Supply for SAI interface |
| NVCC_SD1 | V20 | Supply for SD interface |
| NVCC_SD2 | V22 | Supply for SD interface |
| NVCC_SNVS_1P8 | J22 | Supply for SNVS interface |
| NVCC_UART | J12 | Supply for UART interface |
| PVCC0_1P8 | AB13 | Digital IO pre-drive |
| PVCC1_1P8 | T19 | Digital IO pre-drive |
| PVCC2_1P8 | J13 | Digital IO pre-drive |
| VDD_24M_XTAL_1P8 | N19 | Supply for XTAL |
| VDD_ANA_0P8 | L17, N17 | Supply for Analog logic |
| VDD_ANA0_1P8 | AA14, Y15 | Supply for Analog logic |
| VDD_ANA1_1P8 | P19, N20 | Supply for Analog logic |
| VDD_ARM | R13, T13, U13, V13, W13, T14, W14, R15, T15, U15, V15, W15, V16, W16 | Supply for ARM |
| VDD_ARM_PLL_0P8 | P16 | Supply for ARM PLL |
| VDD_ARM_PLL_1P8 | R19 | Supply for ARM PLL |
| VDD_DRAM | J10, L10, N10, R10, U10, W10 | Supply for DRAM module |

Table 64. i.MX 8M Mini 14 x 14 mm supplies contact assignments (continued)

| | | |
|------------------|---|-----------------------|
| VDD_DRAM_PLL_0P8 | P9 | Supply for DRAM PLL |
| VDD_DRAM_PLL_1P8 | P5 | Supply for DRAM PLL |
| VDD_GPU | R11, U11, W11, P12, V12 | Supply for GPU |
| VDD_MIPI_0P9 | J14 | Supply for MIPI PHY |
| VDD_MIPI_1P2 | J15 | Supply for MIPI PHY |
| VDD_MIPI_1P8 | H13 | Supply for MIPI PHY |
| VDD_PCI_0P8 | J16 | Supply for PCIe PHY |
| VDD_PCI_1P8 | G14 | Supply for PCIe PHY |
| VDD_SNVS_0P8 | K22 | Supply for SNVS logic |
| VDD_SOC | N13, K15, L15, M15, N15, K16, R17, U17, L18, N18, R18, U18 | Supply for SOC logic |
| VDD_USB_0P8 | J17 | Supply for USB PHY |
| VDD_USB_1P8 | H15 | Supply for USB PHY |
| VDD_USB_3P3 | K19 | Supply for USB PHY |
| VDD_VPU | L11, N11, K12, K13, L13, M13, M14 | Supply for VPU |
| VSS | A1, AG1, C2, H2, Y2, AE2, B3, E3, F3, J3, K3, N3, P3, R3, V3, W3, AB3, AC3, AF3, C5, AE5, C6, AE6, G7, J7, K7, N7, R7, V7, W7, AA7, C9, G9, AA9, AE9, C10, G10, AA10, AE10, L12, M12, N12, R12, T12, U12, C13, G13, P13, Y13, AA13, AE13, C14, AE14, C15, G15, P15, AA15, AE15, L16, M16, N16, R16, T16, U16, C18, G18, H18, Y18, AA18, AE18, C19, G19, AA19, AE19, K20, R20, G21, J21, K21, N21, P21, R21, V21, W21, AA21, C22, AE22, C23, AE23, E25, F25, J25, K25, N25, P25, R25, V25, W25, AB25, AC25, B26, A27, AG27 | — |

Table 65 shows an alpha-sorted list of functional contact assignments for the 14 x 14 mm package.

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|------------|------|------------------|-----------|-----------------|---------------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| 24M_XTALI | B27 | VDD_24M_XTAL_1P8 | ANALOG | — | — | Input |
| 24M_XTALO | C26 | VDD_24M_XTAL_1P8 | ANALOG | — | — | Output |
| BOOT_MODE0 | G26 | NVCC_JTAG | GPIO | ALT0 | ccmsrcgpcmix.BOOT_MODE[0] | Input with PD |
| BOOT_MODE1 | G27 | NVCC_JTAG | GPIO | ALT0 | ccmsrcgpcmix.BOOT_MODE[1] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|-----------|------|-------------|-----------|-----------------|------------------|--------------------------|
| | | | | Default mode | Default function | Input/Output status |
| CLKIN1 | H27 | NVCC_CLK | GPIO | — | — | Input without PU/PD |
| CLKIN2 | J27 | NVCC_CLK | GPIO | — | — | Input without PU/PD |
| CLKOUT1 | H26 | NVCC_CLK | GPIO | — | — | Output low without PU/PD |
| CLKOUT2 | J26 | NVCC_CLK | GPIO | — | — | Output low without PU/PD |
| DRAM_AC00 | F4 | NVCC_DRAM | DDR | — | — | Output low |
| DRAM_AC01 | F5 | NVCC_DRAM | DDR | — | — | Output low |
| DRAM_AC02 | K4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC03 | J4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC04 | L2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC05 | L1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC06 | F6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC07 | J5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC08 | J6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC09 | K6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC10 | E4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC11 | D5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC12 | N4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC13 | N5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC14 | K5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC15 | N6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC16 | M1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC17 | M2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC19 | N2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC20 | AB4 | NVCC_DRAM | DDR | — | — | Output low |
| DRAM_AC21 | AB5 | NVCC_DRAM | DDR | — | — | Output low |
| DRAM_AC22 | W4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC23 | V4 | NVCC_DRAM | DDR | — | — | Input |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|--------------|------|-------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| DRAM_AC24 | U2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC25 | U1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC26 | N1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC27 | R6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC28 | W6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC29 | V6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC30 | AC4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC31 | AD5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC32 | R4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC33 | R5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC34 | T1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC35 | T2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC36 | V5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC37 | W5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_AC38 | AB6 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_ALERT_N | R2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DM0 | A4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DM1 | F1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DM2 | AB1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DM3 | AG4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ00 | A5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ01 | B5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ02 | D2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ03 | D1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ04 | C1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ05 | B1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ06 | A3 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ07 | B4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ08 | F2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ09 | G2 | NVCC_DRAM | DDR | — | — | Input |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|-------------|------|-------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| DRAM_DQ10 | J1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ11 | J2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ12 | K2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ13 | K1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ14 | E1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ15 | E2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ16 | AB2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ17 | AA2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ18 | W1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ19 | W2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ20 | V2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ21 | V1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ22 | AC1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ23 | AC2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ24 | AG5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ25 | AF5 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ26 | AD2 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ27 | AD1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ28 | AE1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ29 | AF1 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ30 | AG3 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQ31 | AF4 | NVCC_DRAM | DDR | — | — | Input |
| DRAM_DQS0_N | B2 | NVCC_DRAM | — | — | — | Input |
| DRAM_DQS0_P | A2 | NVCC_DRAM | DDRCLK | — | — | Input |
| DRAM_DQS1_N | H1 | NVCC_DRAM | — | — | — | Input |
| DRAM_DQS1_P | G1 | NVCC_DRAM | DDRCLK | — | — | Input |
| DRAM_DQS2_N | Y1 | NVCC_DRAM | — | — | — | Input |
| DRAM_DQS2_P | AA1 | NVCC_DRAM | DDRCLK | — | — | Input |
| DRAM_DQS3_N | AF2 | NVCC_DRAM | — | — | — | Input |
| DRAM_DQS3_P | AG2 | NVCC_DRAM | DDRCLK | — | — | Input |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|-------------------------|------|-------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| DRAM_RESET_N | R1 | NVCC_DRAM | DDR | — | — | Output low |
| DRAM_VREF | P1 | NVCC_DRAM | DDR | — | — | — |
| DRAM_ZN | P2 | NVCC_DRAM | DDR | — | — | — |
| ECSPI1_MISO | A7 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[8] | Input with PD |
| ECSPI1_MOSI | B7 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[7] | Input with PD |
| ECSPI1_SCLK | D6 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[6] | Input with PD |
| ECSPI1_SS0 | B6 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[9] | Input with PD |
| ECSPI2_MISO | A8 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[12] | Input with PD |
| ECSPI2_MOSI | B8 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[11] | Input with PD |
| ECSPI2_SCLK | E6 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[10] | Input with PD |
| ECSPI2_SS0 | A6 | NVCC_ECSPi | GPIO | ALT5 | GPIO5.IO[13] | Input with PD |
| ENET_MDC | AC27 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[16] | Input with PD |
| ENET_MDIO | AB27 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[17] | Input with PD |
| ENET_RD0 | AE27 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[26] | Input with PD |
| ENET_RD1 | AD27 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[27] | Input with PD |
| ENET_RD2 | AD26 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[28] | Input with PD |
| ENET_RD3 | AC26 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[29] | Input with PD |
| ENET_RXC | AE26 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[25] | Input with PD |
| ENET_RX_CTL | AF27 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[24] | Input with PD |
| ENET_TD0 | AG26 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[21] | Input with PD |
| ENET_TD1 | AF26 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[20] | Input with PD |
| ENET_TD2 | AG25 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[19] | Input with PD |
| ENET_TD3 | AF25 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[18] | Input with PD |
| ENET_TXC | AG24 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[23] | Input with PD |
| ENET_TX_CTL | AF24 | NVCC_ENET | GPIO | ALT5 | GPIO1.IO[22] | Input with PD |
| GPIO1_IO00 | AG14 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[0] | Input with PD |
| GPIO1_IO01 ¹ | AF14 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[1] | Output low |
| GPIO1_IO02 | AG13 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[2] | Input with PU |
| GPIO1_IO03 | AF13 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[3] | Input with PD |
| GPIO1_IO04 | AG12 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[4] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|-------------------------|------|--------------|-----------|-----------------|----------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| GPIO1_IO05 ² | AF12 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[5] | Output high |
| GPIO1_IO06 | AG11 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[6] | Input with PD |
| GPIO1_IO07 | AF11 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[7] | Input with PU |
| GPIO1_IO08 | AG10 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[8] | Input with PD |
| GPIO1_IO09 | AF10 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[9] | Input with PD |
| GPIO1_IO10 | AD10 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[10] | Input with PD |
| GPIO1_IO11 | AC10 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[11] | Input with PD |
| GPIO1_IO12 | AB10 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[12] | Input with PD |
| GPIO1_IO13 | AD9 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[13] | Input with PD |
| GPIO1_IO14 | AC9 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[14] | Input with PD |
| GPIO1_IO15 | AB9 | NVCC_GPIO1 | GPIO | ALT0 | GPIO1.IO[15] | Input with PD |
| I2C1_SCL | E9 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[14] | Input with PD |
| I2C1_SDA | F9 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[15] | Input with PD |
| I2C2_SCL | D10 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[16] | Input with PD |
| I2C2_SDA | D9 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[17] | Input with PD |
| I2C3_SCL | E10 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[18] | Input with PD |
| I2C3_SDA | F10 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[19] | Input with PD |
| I2C4_SCL | D13 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[20] | Input with PD |
| I2C4_SDA | E13 | NVCC_I2C | GPIO | ALT5 | GPIO5.IO[21] | Input with PD |
| JTAG_MOD | D27 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.MOD | Input with PD |
| JTAG_TCK | F26 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.TCK | Input with PU |
| JTAG_TDI | E27 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.TDI | Input with PU |
| JTAG_TDO | E26 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.TDO | Input with PU |
| JTAG_TMS | F27 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.TMS | Input with PU |
| JTAG_TRST_B | C27 | NVCC_JTAG | GPIO | ALT0 | cjtag_wrapper.TRST_B | Input with PU |
| MIPI_CSI_CLK_N | A16 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_CLK_P | B16 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D0_N | A14 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D0_P | B14 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D1_N | A15 | VDD_MIPI_1P8 | PHY | — | — | Input |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|----------------|------|---------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| MIPI_CSI_D1_P | B15 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D2_N | A17 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D2_P | B17 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D3_N | A18 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_CSI_D3_P | B18 | VDD_MIPI_1P8 | PHY | — | — | Input |
| MIPI_DSI_CLK_N | A11 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_CLK_P | B11 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D0_N | A9 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D0_P | B9 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D1_N | A10 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D1_P | B10 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D2_N | A12 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D2_P | B12 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D3_N | A13 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_DSI_D3_P | B13 | VDD_MIPI_1P8 | PHY | — | — | Output low |
| MIPI_VREG_CAP | D15 | 0.35 - 0.45 V | PHY | — | — | Output |
| NAND_ALE | N22 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[0] | Input with PD |
| NAND_CE0_B | N24 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[1] | Input with PU |
| NAND_CE1_B | P27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[2] | Input with PD |
| NAND_CE2_B | M27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[3] | Input with PD |
| NAND_CE3_B | L27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[4] | Input with PD |
| NAND_CLE | K27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[5] | Input with PD |
| NAND_DATA00 | P23 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[6] | Input with PD |
| NAND_DATA01 | K24 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[7] | Input with PD |
| NAND_DATA02 | K23 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[8] | Input with PD |
| NAND_DATA03 | N23 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[9] | Input with PD |
| NAND_DATA04 | M26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[10] | Input with PD |
| NAND_DATA05 | L26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[11] | Input with PD |
| NAND_DATA06 | K26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[12] | Input with PD |
| NAND_DATA07 | N26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[13] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|---------------|------|---------------|-----------|-----------------|----------------------------|--------------------------------|
| | | | | Default mode | Default function | Input/Output status |
| NAND_DQS | R22 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[14] | Input with PD |
| NAND_RE_B | N27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[15] | Input with PU |
| NAND_READY_B | P26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[16] | Input with PD |
| NAND_WE_B | R26 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[17] | Input with PD |
| NAND_WP_B | R27 | NVCC_NAND | GPIO | ALT5 | GPIO3.IO[18] | Input with PD |
| ONOFF | A25 | NVCC_SNVS_1P8 | GPIO | ALT0 | snvsmix.ONOFF | Input without PU/PD |
| PCIE_CLK_N | A21 | VDD_PCI_1P8 | PHY | — | — | High-Z |
| PCIE_CLK_P | B21 | VDD_PCI_1P8 | PHY | — | — | High-Z |
| PCIE_RESREF | D19 | VDD_PCI_1P8 | PHY | — | — | High-Z |
| PCIE_RXN_N | A19 | VDD_PCI_1P8 | PHY | — | — | Input, High-Z |
| PCIE_RXN_P | B19 | VDD_PCI_1P8 | PHY | — | — | Input, High-Z |
| PCIE_TXN_N | A20 | VDD_PCI_1P8 | PHY | — | — | Output, High-Z |
| PCIE_TXN_P | B20 | VDD_PCI_1P8 | PHY | — | — | Output, High-Z |
| PMIC_ON_REQ | A24 | NVCC_SNVS_1P8 | GPIO | ALT0 | snvsmix.PMIC_ON_REQ | Open-drain output high with PU |
| PMIC_STBY_REQ | E24 | NVCC_SNVS_1P8 | GPIO | ALT0 | ccmsrcgpcmix.PMIC_STBY_REQ | Output low with PD |
| POR_B | B24 | NVCC_SNVS_1P8 | GPIO | ALT0 | snvsmix.POR_B | Input without PU/PD |
| RTC_XTALI | A26 | NVCC_SNVS_1P8 | ANALOG | — | — | Input |
| RTC_XTALO | B25 | NVCC_SNVS_1P8 | ANALOG | — | — | Output, inverted of RTC_XTALI |
| RTC_RESET_B | F24 | NVCC_SNVS_1P8 | GPIO | ALT0 | snvsmix.RTC_POR_B | Input without PU/PD |
| SAI1_MCLK | AB18 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[20] | Input with PD |
| SAI1_RXC | AF16 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[1] | Input with PD |
| SAI1_RXD0 | AG15 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[2] | Input with PD |
| SAI1_RXD1 | AF15 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[3] | Input with PD |
| SAI1_RXD2 | AG17 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[4] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|-----------|------|-------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| SAI1_RXD3 | AF17 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[5] | Input with PD |
| SAI1_RXD4 | AG18 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[6] | Input with PD |
| SAI1_RXD5 | AF18 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[7] | Input with PD |
| SAI1_RXD6 | AG19 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[8] | Input with PD |
| SAI1_RXD7 | AF19 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[9] | Input with PD |
| SAI1_RXFS | AG16 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[0] | Input with PD |
| SAI1_TXC | AC18 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[11] | Input with PD |
| SAI1_TXD0 | AG20 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[12] | Input with PD |
| SAI1_TXD1 | AF20 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[13] | Input with PD |
| SAI1_TXD2 | AG21 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[14] | Input with PD |
| SAI1_TXD3 | AF21 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[15] | Input with PD |
| SAI1_TXD4 | AG22 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[16] | Input with PD |
| SAI1_TXD5 | AF22 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[17] | Input with PD |
| SAI1_TXD6 | AG23 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[18] | Input with PD |
| SAI1_TXD7 | AF23 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[19] | Input with PD |
| SAI1_TXFS | AB19 | NVCC_SAI1 | GPIO | ALT5 | GPIO4.IO[10] | Input with PD |
| SAI2_MCLK | AD19 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[27] | Input with PD |
| SAI2_RXC | AB22 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[22] | Input with PD |
| SAI2_RXD0 | AC24 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[23] | Input with PD |
| SAI2_RXFS | AC19 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[21] | Input with PD |
| SAI2_TXC | AD22 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[25] | Input with PD |
| SAI2_TXD0 | AC22 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[26] | Input with PD |
| SAI2_TXFS | AD23 | NVCC_SAI2 | GPIO | ALT5 | GPIO4.IO[24] | Input with PD |
| SAI3_MCLK | AD6 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[2] | Input with PD |
| SAI3_RXC | AG7 | NVCC_SAI3 | GPIO | ALT5 | GPIO4.IO[29] | Input with PD |
| SAI3_RXD | AF7 | NVCC_SAI3 | GPIO | ALT5 | GPIO4.IO[30] | Input with PD |
| SAI3_RXFS | AG8 | NVCC_SAI3 | GPIO | ALT5 | GPIO4.IO[28] | Input with PD |
| SAI3_TXC | AG6 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[0] | Input with PD |
| SAI3_TXD | AF6 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[1] | Input with PD |
| SAI3_TXFS | AC6 | NVCC_SAI3 | GPIO | ALT5 | GPIO4.IO[31] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|------------------------|------|-------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| SAI5_MCLK ³ | AD15 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[25] | Input without PU/PD |
| SAI5_RXC | AC15 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[20] | Input with PD |
| SAI5_RXD0 | AD18 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[21] | Input with PD |
| SAI5_RXD1 | AC14 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[22] | Input with PD |
| SAI5_RXD2 | AD13 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[23] | Input with PD |
| SAI5_RXD3 | AC13 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[24] | Input with PD |
| SAI5_RXFS | AB15 | NVCC_SAI5 | GPIO | ALT5 | GPIO3.IO[19] | Input with PD |
| SD1_CLK | V26 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[0] | Input with PD |
| SD1_CMD | V27 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[1] | Input with PD |
| SD1_DATA0 | Y27 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[2] | Input with PD |
| SD1_DATA1 | Y26 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[3] | Input with PD |
| SD1_DATA2 | T27 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[4] | Input with PD |
| SD1_DATA3 | T26 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[5] | Input with PD |
| SD1_DATA4 | U27 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[6] | Input with PD |
| SD1_DATA5 | U26 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[7] | Input with PD |
| SD1_DATA6 | W27 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[8] | Input with PD |
| SD1_DATA7 | W26 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[9] | Input with PD |
| SD1_RESET_B | R23 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[10] | Input with PD |
| SD1_STROBE | R24 | NVCC_SD1 | GPIO | ALT5 | GPIO2.IO[11] | Input with PD |
| SD2_CD_B | AA26 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[12] | Input with PD |
| SD2_CLK | W23 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[13] | Input with PD |
| SD2_CMD | W24 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[14] | Input with PD |
| SD2_DATA0 | AB23 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[15] | Input with PD |
| SD2_DATA1 | AB24 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[16] | Input with PD |
| SD2_DATA2 | V24 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[17] | Input with PD |
| SD2_DATA3 | V23 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[18] | Input with PD |
| SD2_RESET_B | AB26 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[19] | Input with PD |
| SD2_WP | AA27 | NVCC_SD2 | GPIO | ALT5 | GPIO2.IO[20] | Input with PD |
| SPDIF_EXT_CLK | AF8 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[5] | Input with PD |
| SPDIF_RX | AG9 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[4] | Input with PD |

Table 65. i.MX 8M Mini 14 x 14 mm functional contact assignments (continued)

| Ball name | Ball | Power group | Ball type | Reset condition | | |
|------------------|------|--------------|-----------|-----------------|------------------|---------------------|
| | | | | Default mode | Default function | Input/Output status |
| SPDIF_TX | AF9 | NVCC_SAI3 | GPIO | ALT5 | GPIO5.IO[3] | Input with PD |
| TEST_MODE | D26 | NVCC_JTAG | GPIO | ALT0 | tcu.TEST_MODE | Input with PD |
| TSENSOR_TEST_OUT | J23 | VDD_ANA1_1P8 | ANALOG | — | — | Output low |
| TSENSOR_REST_EXT | J24 | VDD_ANA1_1P8 | ANALOG | — | — | — |
| UART1_RXD | E14 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[22] | Input with PD |
| UART1_TXD | F13 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[23] | Input with PD |
| UART2_RXD | F15 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[24] | Input with PD |
| UART2_TXD | E15 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[25] | Input with PD |
| UART3_RXD | E18 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[26] | Input with PD |
| UART3_TXD | D18 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[27] | Input with PD |
| UART4_RXD | F19 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[28] | Input with PD |
| UART4_TXD | F18 | NVCC_UART | GPIO | ALT5 | GPIO5.IO[29] | Input with PD |
| USB1_DN | A22 | VDD_USB_3P3 | PHY | — | — | Input |
| USB1_DP | B22 | VDD_USB_3P3 | PHY | — | — | Input |
| USB1_ID | D22 | VDD_USB_1P8 | PHY | — | — | Input |
| USB1_TXRTUNE | E19 | VDD_USB_1P8 | PHY | — | — | — |
| USB1_VBUS | F22 | VDD_USB_3P3 | PHY | — | — | — |
| USB2_DN | A23 | VDD_USB_3P3 | PHY | — | — | Input |
| USB2_DP | B23 | VDD_USB_3P3 | PHY | — | — | Input |
| USB2_ID | D23 | VDD_USB_1P8 | PHY | — | — | Input |
| USB2_TXRTUNE | E22 | VDD_USB_1P8 | PHY | — | — | — |
| USB2_VBUS | F23 | VDD_USB_3P3 | PHY | — | — | — |

¹ Works as JTAG Active output when the internal reset is asserted, default is output low. After the internal reset is deasserted, it becomes input with PD.

² Works as INT_BOOT output when the internal reset is asserted, default is output high. After the internal reset is deasserted, it becomes input with PU.

³ Works as TESTER_ACK input when the internal reset is asserted, default is input without PU/PD. After the internal reset is deasserted, it becomes input with PD.

5.1.3 i.MX 8M Mini 14 x 14 mm 0.5 mm pitch ball map

Table 66 shows the i.MX 8M Mini 14 x 14 mm 0.5 mm pitch ball map.

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

| P | N | M | L | K | J | H |
|------------------|------------------|-------------|-------------|--------------|------------------|--------------|
| DRAM_VREF | DRAM_AC26 | DRAM_AC16 | DRAM_AC05 | DRAM_DQ13 | DRAM_DQ10 | DRAM_DQS1_N |
| DRAM_ZN | DRAM_AC19 | DRAM_AC17 | DRAM_AC04 | DRAM_DQ12 | DRAM_DQ11 | VSS |
| VSS | VSS | | | VSS | VSS | |
| VDD_DRAM_PLL_1P8 | DRAM_AC12 | | | DRAM_AC02 | DRAM_AC03 | |
| | DRAM_AC13 | | | DRAM_AC14 | DRAM_AC07 | |
| | DRAM_AC15 | | | DRAM_AC09 | DRAM_AC08 | |
| NVCC_DRAM | VSS | | | VSS | VSS | |
| | NVCC_DRAM | | | NVCC_DRAM | | |
| VDD_DRAM_PLL_0P8 | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | NVCC_DRAM | | |
| | VDD_DRAM | | VDD_DRAM | | VDD_DRAM | NVCC_ECSP1 |
| | VDD_VPU | | VDD_VPU | | NVCC_I2C | |
| VDD_GPU | VSS | VSS | VSS | VDD_VPU | NVCC_UART | |
| VSS | VDD_SOC | VDD_VPU | VDD_VPU | VDD_VPU | PVCC2_1P8 | VDD_MIPI_1P8 |
| | VDD_SOC | VDD_VPU | VDD_SOC | VDD_SOC | VDD_MIPI_0P9 | |
| VSS | VDD_SOC | VDD_SOC | VDD_SOC | VDD_SOC | VDD_MIPI_1P2 | VDD_USB_1P8 |
| VDD_ARM_PLL_0P8 | VSS | VSS | VSS | VDD_SOC | VDD_PCI_0P8 | |
| | VDD_ANA_0P8 | | VDD_ANA_0P8 | | VDD_USB_0P8 | |
| | VDD_SOC | | VDD_SOC | | NC_J18 | VSS |
| VDD_ANA1_1P8 | VDD_24M_XTAL_1P8 | NVCC_CLK | NVCC_JTAG | VDD_USB_3P3 | | |
| | VDD_ANA1_1P8 | | | VSS | | |
| VSS | VSS | | | VSS | VSS | |
| | NAND_ALE | | | VDD_SNV5_0P8 | NVCC_SNV5_1P8 | |
| NAND_DATA00 | NAND_DATA03 | | | NAND_DATA02 | TSENSOR_TEST_OUT | |
| | NAND_CE0_B | | | NAND_DATA01 | TESENSOR_RES_EXT | |
| VSS | VSS | | | VSS | VSS | |
| NAND_READY_B | NAND_DATA07 | NAND_DATA04 | NAND_DATA05 | NAND_DATA06 | CLKOUT2 | CLKOUT1 |
| NAND_CE1_B | NAND_RE_B | NAND_CE2_B | NAND_CE3_B | NAND_CLE | CLKIN2 | CLKIN1 |

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | | | |
|----|--------------|--------------|-----|-----------|-----------|-----------|-----|-----------|------------|------------|---------|------------|-----------|--------------|--------------|---------|-----------|-----------|-----------------|----------|-----|-----------|-----------|-----------|----------|-------------|------------|-----|-----------|-----------|
| AB | DRAM_DM2 | DRAM_DQ16 | VSS | DRAM_AC20 | DRAM_AC21 | DRAM_AC38 | | | GPIO1_IO15 | GPIO1_IO12 | | | PVCC0_1P8 | | SAI5_RXFS | | | SAI1_MCLK | SAI1_TXFS | | | SAI2_RXC | SD2_DATA0 | SD2_DATA1 | VSS | SD2_RESET_B | ENET_MDIO | | | |
| AA | DRAM_DQS2_P | DRAM_DQ17 | | | | VSS | | | VSS | VSS | VSS | VSS | VSS | VDD_ANA0_1P8 | VSS | | | VSS | VSS | VSS | VSS | | | | | SD2_CD_B | SD2_WP | | | |
| Y | DRAM_DQS2_N | VSS | | | | | | | | NVCC_SAI3 | | | | | VDD_ANA0_1P8 | | | | | | | | | | | SD1_DATA1 | SD1_DATA0 | | | |
| W | DRAM_DQ18 | DRAM_DQ19 | VSS | DRAM_AC22 | DRAM_AC37 | DRAM_AC28 | VSS | | | VDD_DRAM | VDD_GPU | NVCC_GPIO1 | VDD_ARM | VDD_ARM | VDD_ARM | VDD_ARM | NVCC_SAI5 | NVCC_SAI1 | | | VSS | NVCC_ENET | SD2_CLK | SD2_CMD | VSS | SD1_DATA7 | SD1_DATA6 | | | |
| V | DRAM_DQ21 | DRAM_DQ20 | VSS | DRAM_AC23 | DRAM_AC36 | DRAM_AC29 | VSS | NVCC_DRAM | NVCC_DRAM | | | VDD_GPU | VDD_ARM | | VDD_ARM | VDD_ARM | | | NVCC_SAI2 | NVCC_SD1 | VSS | NVCC_SD2 | SD2_DATA3 | SD2_DATA2 | VSS | SD1_CLK | SD1_CMD | | | |
| U | DRAM_AC25 | DRAM_AC24 | | | | | | | NVCC_DRAM | VDD_DRAM | VDD_GPU | VSS | VDD_ARM | | VDD_ARM | VSS | VDD_SOC | VDD_SOC | NVCC_NAND | | | | | | | SD1_DATA5 | SD1_DATA4 | | | |
| T | DRAM_AC34 | DRAM_AC35 | | | | | | | NVCC_DRAM | | | VSS | VDD_ARM | VDD_ARM | VDD-ARM | VSS | | | PVCC1_1P8 | | | | | | | SD1_DATA3 | SD1_DATA2 | | | |
| R | DRAM_RESET_N | DRAM_ALERT_N | VSS | DRAM_AC32 | DRAM_AC33 | DRAM_AC27 | VSS | | NVCC_DRAM | VDD_DRAM | VDD_GPU | VSS | VDD_ARM | | VDD_ARM | VSS | VDD_SOC | VDD_SOC | VDD_ARM_PLL_1P8 | | VSS | VSS | | | NAND_DQS | SD1_RESET_B | SD1_STROBE | VSS | NAND_WE_B | NAND_WP_B |

Table 66. 14 x 14 mm, 0.5 mm pitch ball map (continued)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
|-----------|-----------|-------------|-----------|-----------|-----------|-----------|----------|---------------|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|----------|----------|-------------|
| AG | VSS | DRAM_DQS3_P | DRAM_DQ30 | DRAM_DM3 | DRAM_DQ24 | SAI3_TXC | SAI3_RXC | SAI3_RXFS | SPDIF_RX | GPIO1_IO08 | GPIO1_IO06 | GPIO1_IO04 | GPIO1_IO02 | GPIO1_IO00 | SAI1_RXD0 | SAI1_RXFS | SAI1_RXD2 | SAI1_RXD4 | SAI1_RXD6 | SAI1_TXD0 | SAI1_TXD2 | SAI1_TXD4 | SAI1_TXD6 | ENET_TXC | ENET_TD2 | ENET_TD0 | VSS |
| AF | DRAM_DQ29 | DRAM_DQS3_N | VSS | DRAM_DQ31 | DRAM_DQ25 | SAI3_TXD | SAI3_RXD | SPDIF_EXT_CLK | SPDIF_TX | GPIO1_IO09 | GPIO1_IO07 | GPIO1_IO05 | GPIO1_IO03 | GPIO1_IO01 | SAI1_RXD1 | SAI1_RXC | SAI1_RXD3 | SAI1_RXD5 | SAI1_RXD7 | SAI1_TXD1 | SAI1_TXD3 | SAI1_TXD5 | SAI1_TXD7 | ENET_TX_CTL | ENET_TD3 | ENET_TD1 | ENET_RX_CTL |
| AE | DRAM_DQ28 | VSS | | | VSS | VSS | | | VSS | VSS | | | VSS | VSS | VSS | | | VSS | VSS | | | VSS | VSS | | | ENET_RXC | ENET_RD0 |
| AD | DRAM_DQ27 | DRAM_DQ26 | | | DRAM_AC31 | SAI3_MCLK | | | GPIO1_IO13 | GPIO1_IO10 | | | SAI5_RXD2 | SAI5_RXD1 | SAI5_MCLK | | | SAI5_RXD0 | SAI2_MCLK | | | SAI2_TXC | SAI2_TXFS | | | ENET_RD2 | ENET_RD1 |
| AC | DRAM_DQ22 | DRAM_DQ23 | VSS | DRAM_AC30 | | SAI3_TXFS | | | GPIO1_IO14 | GPIO1_IO11 | | | SAI5_RXD3 | SAI5_RXD0 | SAI5_RXC | | | SAI1_TXC | SAI2_RXFS | | | SAI2_TXD0 | | SAI2_RXD0 | VSS | ENET_RD3 | ENET_MDC |

5.2 DDR pin function list

Table 67 shows the DDR pin function list.

Table 67. DDR pin function list

| Ball name | LPDDR4 | DDR4 | DDR3/3L |
|-------------|----------|--------------------|---------|
| DRAM_DQS0_P | DQS0_t_A | DQSL_t_A | DQSL_A |
| DRAM_DQS0_N | DQS0_c_A | DQSL_c_A | DQSL#_A |
| DRAM_DM0 | DMI0_A | DML_n_A / DBIL_n_A | DML_A |
| DRAM_DQ00 | DQ0_A | DQL0_A | DQL0_A |
| DRAM_DQ01 | DQ1_A | DQL1_A | DQL1_A |
| DRAM_DQ02 | DQ2_A | DQL2_A | DQL2_A |
| DRAM_DQ03 | DQ3_A | DQL3_A | DQL3_A |
| DRAM_DQ04 | DQ4_A | DQL4_A | DQL4_A |
| DRAM_DQ05 | DQ5_A | DQL5_A | DQL5_A |

Table 67. DDR pin function list (continued)

| | | | |
|-------------|----------|--------------------|---------|
| DRAM_DQ06 | DQ6_A | DQL6_A | DQL6_A |
| DRAM_DQ07 | DQ7_A | DQL7_A | DQL7_A |
| DRAM_DQS1_P | DQS1_t_A | DQSU_t_A | DQSU_A |
| DRAM_DQS1_N | DQS1_c_A | DQSU_c_A | DQSU#_A |
| DRAM_DM1 | DMI1_A | DMU_n_A / DBIU_n_A | DMU_A |
| DRAM_DQ08 | DQ08_A | DQU0_A | DQU0_A |
| DRAM_DQ09 | DQ09_A | DQU1_A | DQU1_A |
| DRAM_DQ10 | DQ10_A | DQU2_A | DQU2_A |
| DRAM_DQ11 | DQ11_A | DQU3_A | DQU3_A |
| DRAM_DQ12 | DQ12_A | DQU4_A | DQU4_A |
| DRAM_DQ13 | DQ13_A | DQU5_A | DQU5_A |
| DRAM_DQ14 | DQ14_A | DQU6_A | DQU6_A |
| DRAM_DQ15 | DQ15_A | DQU7_A | DQU7_A |
| DRAM_DQS2_P | DQS0_t_B | DQSL_t_B | DQSL_B |
| DRAM_DQS2_N | DQS0_c_B | DQSL_c_B | DQSL#_B |
| DRAM_DM2 | DMI0_B | DML_n_B / DBIL_n_B | DML_B |
| DRAM_DQ16 | DQ0_B | DQL0_B | DQL0_B |
| DRAM_DQ17 | DQ1_B | DQL1_B | DQL1_B |
| DRAM_DQ18 | DQ2_B | DQL2_B | DQL2_B |
| DRAM_DQ19 | DQ3_B | DQL3_B | DQL3_B |
| DRAM_DQ20 | DQ4_B | DQL4_B | DQL4_B |
| DRAM_DQ20 | DQ4_B | DQL4_B | DQL4_B |
| DRAM_DQ21 | DQ5_B | DQL5_B | DQL5_B |
| DRAM_DQ22 | DQ6_B | DQL6_B | DQL6_B |
| DRAM_DQ23 | DQ7_B | DQL7_B | DQL7_B |
| DRAM_DQS3_P | DQS1_t_B | DQSU_t_B | DQSU_B |
| DRAM_DQS3_N | DQS1_c_B | DQSU_c_B | DQSU#_B |
| DRAM_DM3 | DMI1_B | DMU_n_B / DBIU_n_B | DMU_B |
| DRAM_DQ24 | DQ08_B | DQU0_B | DQU0_B |
| DRAM_DQ25 | DQ09_B | DQU1_B | DQU1_B |
| DRAM_DQ26 | DQ10_B | DQU2_B | DQU2_B |
| DRAM_DQ27 | DQ11_B | DQU3_B | DQU3_B |
| DRAM_DQ28 | DQ12_B | DQU4_B | DQU4_B |
| DRAM_DQ29 | DQ13_B | DQU5_B | DQU5_B |

Table 67. DDR pin function list (continued)

| | | | |
|--------------|---------|------------------|-----------|
| DRAM_DQ30 | DQ14_B | DQU6_B | DQU6_B |
| DRAM_DQ31 | DQ15_B | DQU7_B | DQU7_B |
| DRAM_RESET_N | RESET_N | RESET_n | RESET# |
| DRAM_ALERT_N | MTEST1 | ALERT_n / MTEST1 | MTEST1 |
| DRAM_AC00 | CKE0_A | CKE0 | CKE0 |
| DRAM_AC01 | CKE1_A | CKE1 | CKE1 |
| DRAM_AC02 | CS0_A | CS0_n | CS0# |
| DRAM_AC03 | CS1_A | C0 | — |
| DRAM_AC04 | CK_t_A | BG0 | BA2 |
| DRAM_AC05 | CK_c_A | BG1 | A14 |
| DRAM_AC06 | — | ACT_n | A15 |
| DRAM_AC07 | — | A9 | A9 |
| DRAM_AC08 | CA0_A | A12 | A12 / BC# |
| DRAM_AC09 | CA1_A | A11 | A11 |
| DRAM_AC10 | CA2_A | A7 | A7 |
| DRAM_AC11 | CA3_A | A8 | A8 |
| DRAM_AC12 | CA4_A | A6 | A6 |
| DRAM_AC13 | CA5_A | A5 | A5 |
| DRAM_AC14 | — | A4 | A4 |
| DRAM_AC15 | — | A3 | A3 |
| DRAM_AC16 | — | CK_t_A | CK_A |
| DRAM_AC17 | — | CK_c_A | CK#_A |
| DRAM_AC19 | MTEST | MTEST | MTEST |
| DRAM_AC20 | CKE0_B | CK_t_B | CK_B |
| DRAM_AC21 | CKE1_B | CK_c_B | CK#_B |
| DRAM_AC22 | CS1_B | — | — |
| DRAM_AC23 | CS0_B | — | — |
| DRAM_AC24 | CK_t_B | A2 | A2 |
| DRAM_AC25 | CK_c_B | A1 | A1 |
| DRAM_AC26 | — | BA1 | BA1 |
| DRAM_AC27 | — | PARITY | — |
| DRAM_AC28 | CA0_B | A13 | A13 |
| DRAM_AC29 | CA1_B | BA0 | BA0 |
| DRAM_AC30 | CA2_B | A10 / AP | A10 / AP |

Table 67. DDR pin function list (continued)

| | | | |
|-----------|-------|-------------|------|
| DRAM_AC31 | CA3_B | A0 | A0 |
| DRAM_AC32 | CA4_B | C2 | — |
| DRAM_AC33 | CA5_B | CAS_n / A15 | CAS# |
| DRAM_AC34 | — | WE_n / A14 | WE# |
| DRAM_AC35 | — | RAS_n / A16 | RAS# |
| DRAM_AC36 | — | ODT0 | ODT0 |
| DRAM_AC37 | — | ODT1 | ODT1 |
| DRAM_AC38 | — | CS1_n | CS1# |
| DRAM_ZN | ZQ | ZQ | ZQ |
| DRAM_VREF | VREF | VREF | VREF |

6 Revision history

Table 68 provides a revision history for this data sheet.

Table 68. Revision history

| Rev. number | Date | Substantive change(s) |
|-------------|---------|---|
| Rev. 1 | 07/2020 | <ul style="list-style-type: none"> Updated the eMMC descriptions in the Table 1, "Features" Updated numbers of SD 3.0 in the Figure 1, "i.MX 8M Mini system block diagram" Added two part numbers and updated the part differentiator in the Table 2, "Orderable part numbers" Updated the part differentiator and Fusing in the Figure 2, "Part number nomenclature—i.MX 8M Mini family of processors" Updated eCSPI, SJC, and uSDHC descriptions in the Table 3, "i.MX 8M Mini modules list" Updated a typo for NVCC_ENET in the Table 4, "Recommended connections for unused power supply rails" Updated the min values and a typo in the Table 7, "Absolute maximum ratings"; removed ESD parameters from the Table 7, "Absolute maximum ratings" Added the Table 8, "Electrostatic discharge and latch up ratings" Added a footnote in the Table 10, "Operating ranges" Added VDD_24M_XTAL_1P8, VDD_ARM_PLL_1P8, and PVCCx_1P8 in the Table 13, "Maximum supply currents" Updated the Table 14, "Chip power in different LP mode" Updated the suspend mode state of VDD_MIPI_0P9 and VDD_MIPI_1P2 in the Table 15, "The power supply states" Updated the maximum values of T1, T2, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13 and minimum value of T3 in the Table 17, "Power-up sequence" Updated the maximum values in the Table 18, "Power-down sequence" Removed the USBx_ID, ONOFF, and POR_B from the Table 22, "Additional leakage parameters" Added GPIO1_09, I2C2_SCL, and I2C2_SDA in the Table 35, "ENET signal mapping" Removed 0x2 from the Section 3.9.10.1.1, SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1 and Section 3.9.10.1.3, DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1 Updated the parameters of GPIO1_IO00, GPIO1_IO01, GPIO1_IO05, GPIO1_IO09, and SAI5_MCLK in the Table 65, "i.MX 8M Mini 14 x 14 mm functional contact assignments" Fixed typos in the Table 66, "14 x 14 mm, 0.5 mm pitch ball map" |
| Rev. 0.2 | 04/2019 | <ul style="list-style-type: none"> Updated numbers of eMMC and FlexSPI in the Figure 1, "i.MX 8M Mini system block diagram" Updated the descriptions about USB and uSDHC in the Table 3, "i.MX 8M Mini modules list" Updated the comment of VDD_VPU and the LPDDR4 maximum value of NVCC_DRAM in the Table 10, "Operating ranges" |
| Rev. 0.1 | 02/2019 | <ul style="list-style-type: none"> Updated the SNVS states in the Table 15, "The power supply states" |
| Rev. 0 | 02/2019 | <ul style="list-style-type: none"> Initial version |



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