



# GO2953

CWDM DUAL OPTICAL TRANSMITTER MODULE

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## GO2953 CWDM Dual Optical Transmitter

### Features

- Robust error free transmission of signals from 50Mbps to 3Gbps
- Up to 50km reach in a 3Gbps CWDM installation
- Available wavelengths: 1270nm ~ 1610nm, 20nm spacing
- Supports video pathological patterns for SD-SDI, HD-SDI and 3G-SDI
- Hot-pluggable
- Two independent laser disable pins
- Digital diagnostics and control via I<sup>2</sup>C interface including:
  - ♦ Monitoring laser bias current, average output power, supply voltage and temperature
  - ♦ Alarm reporting with self shut down when transmitter is at fault
  - ♦ Module ID polling
- Single +3.3V power supply
- Low power consumption — typically 680mW
- RoHS compliant
- Operating temperature range: 0°C to 70°C
- 56.5mm x 13.4mm x 8.6mm SFP Package
- SMPTE 297-2006 compatible

### Applications

- SMPTE 297-2006 compatible electrical-to-optical interfaces
- High-density video routers

### Description

The GO2953 is a dual channel CWDM optical transmitter module designed to transmit optical serial digital signals as defined in SMPTE 297-2006. The GO2953 is specifically designed for robust performance in the presence of SDI pathological patterns for SMPTE 259M, SMPTE 344M, SMPTE 292M and SMPTE 424M serial rates.

The GO2953 contains two independent DFB laser transmitters, each designed to provide error-free transmission of signals from 50Mbps to 3Gbps. The GO2953 is hot-pluggable with typical power consumption of 680mW using a single power supply of +3.3V.

The GO2953 provides extensive operational status monitoring through an I<sup>2</sup>C interface. For each transmitter channel, output optical power and bias current are monitored. Other operating conditions such as supply voltage and operating temperature are also monitored. If a parameter monitored is outside the pre-defined range, the alarm flag associated with the parameter will be raised.

## Revision History

Version	ECR	Date	Changes and/or Modifications
0	157039	November 2011	New document.
1	157987	April 2012	Updated extinction ratio in <a href="#">Table 3-2</a> .

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# 1. Functional Block Diagram

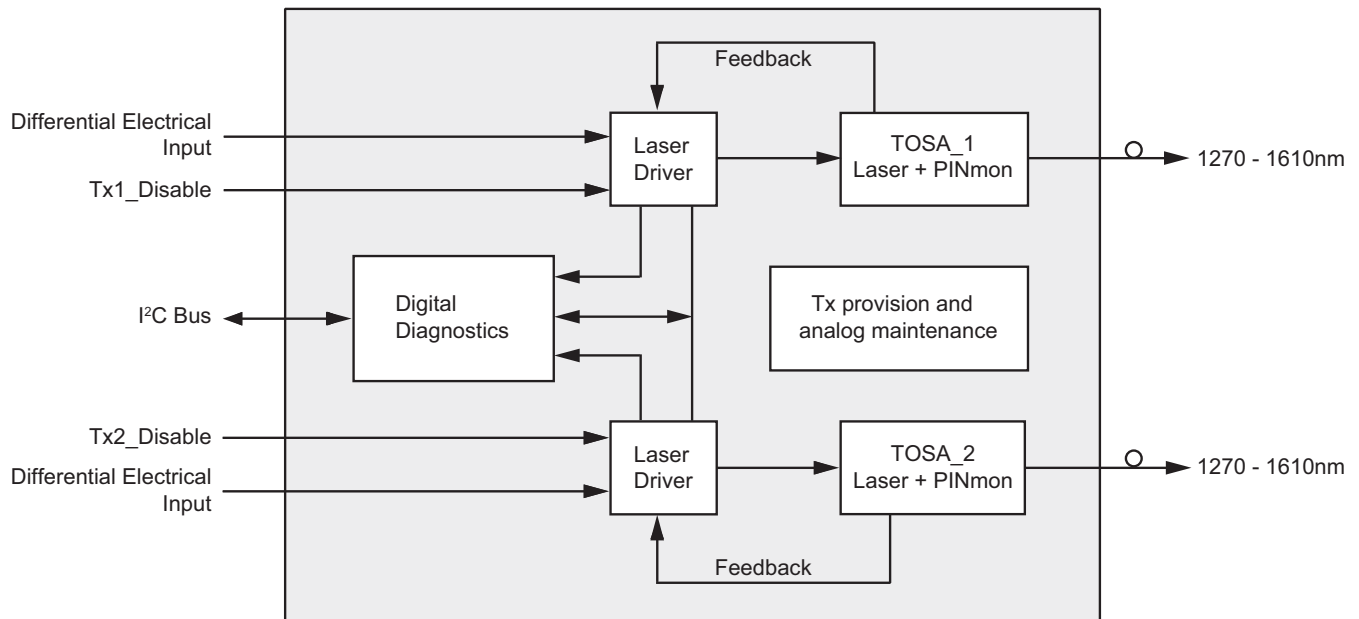


Figure 1-1: GO2953 Functional Block Diagram

## 2. Pin Specifications

### 2.1 Pin Configuration

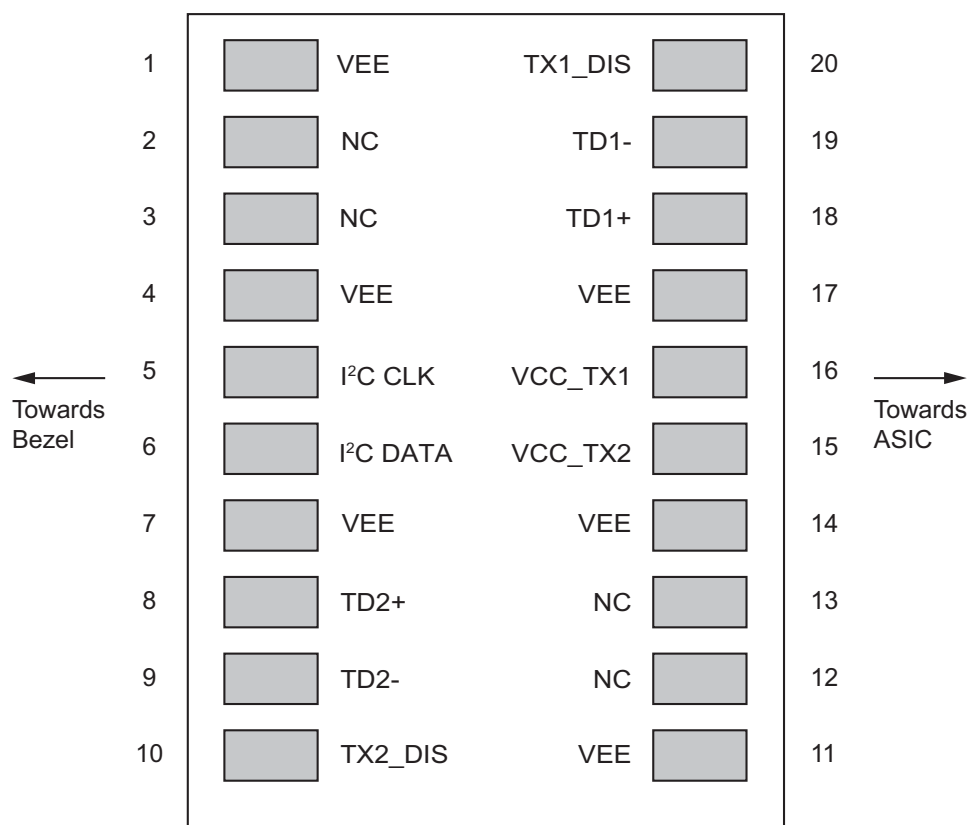


Figure 2-1: Pin Configuration for GO2953

### 2.2 Pin Descriptions

Table 2-1: Pin Descriptions

Number	Name	Type	Description
1	VEE	Ground	Ground connection
2	NC	No Connect	No Connection
3	NC	No Connect	No Connection
4	VEE	Ground	Ground connection
5	I <sup>2</sup> C CLK	Digital (Input)	I <sup>2</sup> C Clock
6	I <sup>2</sup> C DATA	Digital (Bi-Directional)	I <sup>2</sup> C Data

**Table 2-1: Pin Descriptions (Continued)**

Number	Name	Type	Description
7	VEE	Ground	Ground connection
8	TD2+	Input	Positive Differential Input. Internally AC-coupled.
9	TD2-	Input	Negative Differential Input. Internally AC-coupled.
10	TX2_Dis	Digital (Input)	Transmitter Disable. The bias current and modulation current are turned off if TX2_DIS = HIGH. Internal 4.7k $\Omega$ pull-up.
11	VEE	Ground	Ground connection
12	NC	No Connect	No Connection
13	NC	No Connect	No Connection
14	VEE	Ground	Ground connection
15	VCC_TX2	Power	Transmitter Power Supply
16	VCC_TX1	Power	Transmitter Power Supply
17	VEE	Ground	Ground connection
18	TD1+	Input	Positive Differential Input. Internally AC-coupled.
19	TD1-	Input	Negative Differential Input. Internally AC-coupled.
20	TX1_Dis	Digital (Input)	Transmitter Disable. The bias current and modulation current are turned off if TX1_DIS = HIGH. Internal 4.7k $\Omega$ pull-up.

## 2.3 Host Board Power Supply Requirements

The host board is required to provide a regulated and filtered power supply of 3.3V +/- 5% V for the GO2953 via the on board SFP connector. The host board is required to filter the VCC\_TX power supply as recommended by the SFP MSA. [Figure 2-2](#) shows the recommended board supply filtering. When the host board is loaded with a resistive load in place of the SFP module and sourcing the maximum rated current, the peak-to-peak power supply noise measured on the SFP connector should comply to [Table 2-2](#).

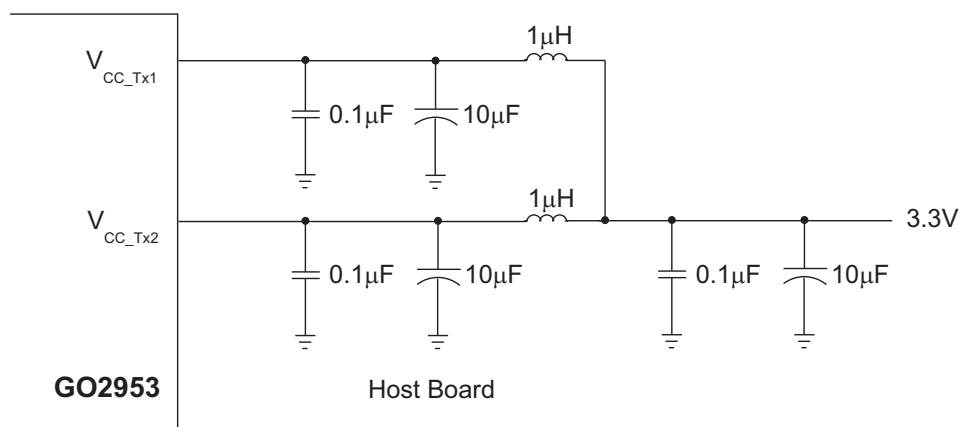


Figure 2-2: Recommended Host Board Supply Filtering

Table 2-2: Host Board Power Supply Noise Requirement at  $V_{CC}R$

Frequency (MHz)	Peak-to-Peak Noise Amplitude (%)
0.02-1	2
1-10	3

## 2.4 Optical Connector Requirements

An LC connector with PC/UPC polish is required for each port.

## 3. Product Specifications

### 3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings for the GO2953. Conditions exceeding the limits listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3-1: Absolute Maximum Ratings**

Parameter	Conditions	Value/Units
Supply Voltage	–	4V
Operating Case Temperature	–	$-20^{\circ}\text{C} \leq T_{\text{CASE}} \leq 80^{\circ}\text{C}$
Storage Temperature	–	$-40^{\circ}\text{C} \leq T_{\text{STG}} \leq 100^{\circ}\text{C}$
ESD tolerance on all pins	–	1 kV HBM
Relative Humidity (non-condensing)	–	5% - 95% RH

### 3.2 Optical Performance Specifications

Table 3-2 lists the optical performance specifications for the GO2953.

**Table 3-2: Optical Performance Specifications**

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>System</b>							
Wavelength	$\lambda$	–	X-6.5	X	X+6.5	nm	2
Spectral Line Width	–	–	–	0.2	1	nm	–
Average Optical Output Power	$P_{\text{OUT}}$	–	0	+2.5	+5	dBm	–
Extinction Ratio	ER	–	8	–	–	dB	–



**Table 3-2: Optical Performance Specifications (Continued)**

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Optical Signal Intrinsic Jitter	–	Measured with PRBS 2 <sup>23</sup> -1 and colour bar test signal at 2.97Gbps, 1.485Gbps, 270Mbps	–	40	60	ps	3
		SMPTE 424M 2.97Gbps Pathological	–	50	90	ps	3
		SMPTE 292M 1.485Gbps Pathological	–	60	120	ps	3
		SMPTE 259M 270Mbps Pathological	–	110	200	ps	3
Optical Signal Rise Time (20% to 80%)	t <sub>r</sub>	SMPTE 424M 2.97Gbps	–	130	180	ps	3
		SMPTE 292M 1.485Gbps	–	175	270	ps	3
		SMPTE 259M 270Mbps	–	300	800	ps	3
Optical Signal Fall Time (20% to 80%)	t <sub>f</sub>	SMPTE 424M 2.97Gbps	–	130	180	ps	3
		SMPTE 292M 1.485Gbps	–	175	270	ps	3
		SMPTE 259M 270Mbps	–	300	800	ps	3

**NOTES:**

1. Outside the specified range, performance is not guaranteed.
2. X = Centre Wavelength: 1271, 1291, 1311, 1331, 1351, 1371, 1391, 1411, 1431, 1451, 1471, 1491, 1511, 1531, 1551, 1571, 1591 & 1611nm
3. Measured following a fourth-order Bessel-Thompson filter with a bandwidth of 0.75 x clock frequency corresponding to the serial data rate.

## 3.3 DC Electrical Specifications

Table 3-3 lists the DC electrical specifications for the GO2953.

Table 3-3: DC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
<b>System</b>							
Operating Temperature Range	T <sub>CASE</sub>	–	0	–	70	°C	1,3
Power Supply Voltage	V <sub>CC</sub>	–	3.13	3.3	3.47	V	1,3
Total Power Consumption	–	–	–	650	1000	mW	3
Input Data Amplitude	–	–	0.2	–	1.2	V <sub>pp</sub>	2,3
<b>Laser</b>							
Laser Bias Current Monitoring Accuracy	–	–	-1	–	+1	dB	3
Laser Power Monitoring Accuracy	–	–	-1	–	+1	dB	3
NOTES:							
1. Outside the specified range, performance is not guaranteed.							
2. AC coupled 50Ω single-ended termination.							
3. Specifications apply at the beginning of life.							

## 3.4 AC Electrical Specifications

Table 3-4 lists the AC electrical specifications for the GO2953.

Table 3-4: AC Electrical Specifications

Parameter	Symbol	Condition	Min	Max	Units
Bit Rate	BR	–	50	3000	Mbps
Tx_Disable Assert Time	t <sub>off</sub>	Time from rising edge of TX_DIS to when the optical output falls below 10% of nominal	–	10	μs
Tx_Disable Negate Time	t <sub>on</sub>	Time from falling edge of TX_DIS to when the modulated optical output rises above 90% of nominal	–	1	ms
Time to Initialize	t <sub>init</sub>	From power on	–	300	ms
Serial ID Clock Rate	f <sub>serial_clock</sub>	–	–	400	kHz

## 3.5 Supporting Circuit Specifications

### 3.5.1 In-Rush Current Control Circuit

Due to the hot-pluggable requirement, the GO2953 has built-in circuits to limit the in-rush current upon hot insertion. The specifications of the in-rush limiting circuits are summarized in [Table 3-5](#).

**Table 3-5: In-rush Current Limiting Circuits Specifications**

Parameter	Value
Max. In-rush current ramp rate	50mA/ms
Max. In-rush current	30mA over steady state

### 3.5.2 Digital Diagnosis

#### 3.5.2.1 I<sup>2</sup>C Bus Interface

The I<sup>2</sup>C bus interface uses the 2-wire serial CMOS E<sup>2</sup>PROM protocol. The serial interface meets the following specifications:

1. Support a maximum clock rate of 400kHz.
2. Input/Output levels comply with LVCMOS/LVTTL or compatible logics.
  - ♦ Low: 0 – 0.8V
  - ♦ High: 2.0 – 3.3V
  - ♦ Undefined: 0.8 – 2.0V

#### 3.5.2.2 Serial Interface Memory Map

Module identification and diagnostic information is accessible through the address map shown in [Table 3-6](#). Block addresses starting with the letter 'A' refer to Channel 1 and block addresses starting with the letter 'B' refer to Channel 2.

**Table 3-6: Serial Interface Memory Map**

Address	Size	Name	Description and Value of the Field
<b>Base ID Fields (Block Address: A0h)</b>			
0	1	Identifier	Type of serial transceiver. 81h
1	1	Ext. Identifier	Extended identifier of type of serial transceiver. 04h
2	1	Connector	Code for connector type. 07h for LC connectors.

**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
3	1	Standards Compliance	41h, for SMPTE259M/344M/292M/424M and SMPTE 297.
4-10	8	Transceiver Code	Code for electronic compatibility or optical compatibility. Not applicable for GO2953.
11	1	Encoding	Code for serial encoding algorithm. Value: 03H for NRZ.
12	1	BR, Nominal	Nominal bit rate, units of 100Mbps, 1Eh for 3Gbps.
13	1	Reserved	Xxh
14	1	Length(9mm) - km	Link length supported for standard SMF, units of km, 32h for 50km.
15	1	Length(9mm)	Link length supported for standard SMF, units of 100 m, 00h
16	1	Length (50mm)	Link length supported for 50/125mm fiber, units of 10m. 00h
17	1	Length (62.5mm)	Link length supported for 62.5/125mm fiber, units of 10m. 00h
18	1	Length (Copper)	Link length supported for copper, units of meters. 00h
19	1	Reserved	Xxh
20-35	16	Vendor name	SFP with OM transceiver vendor name (ASCII). G E N N U M
20	1	G	47h
21	1	E	45h
22	1	N	4Eh
23	1	N	4Eh
24	1	U	55h
25	1	M	4Dh
26-35	10	–	20h for each byte
36	1	Reserved	–
37-39	3	Vendor OUI	SFP with OM transceiver vendor IEEE company ID. 00 0A DF
40-55	16	Vendor PN	Part number provided by SFP with OM transceiver vendor. G O 2 9 5 3.
40	1	G	47h
41	1	O	4Fh
42	1	2	32h
43	1	9	39h

**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
44	1	5	35h
45	1	3	33h
46	1	X	Model dependent.
47	1	X	Model dependent.
48	1	Y	Model dependent.
49	1	Y	Model dependent.
50	1	C	43h
51	1	H	48h
52-55	4	–	20h for each byte.
56-58	3	–	Reserved
59	1	Vendor Rev	Revision level for part number provided by vendor.
60	1	Wavelength1	XX for the middle two digits of the wavelength of Channel #1.
61	1	Wavelength2	YY for the middle two digits of the wavelength of Channel #2.
62	1	Reserved	Xxh
63	1	CC_BASE	Check code for Base ID Fields (The value of the lower 8 bits of the sum of the contents from address 0 to 62).
64-65	2	Options	Indicates which optional SFP with OM signals are implemented.
64	1	–	Xxh
65	1	–	x001100xh
66	1	BR, max	Upper bit rate margin, units of %, 5h.
67	1	BR, min	Lower bit rate margin, units of %, 5Fh.
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-85	2	Year	Manufacturing date code (ASCII).
86-87	2	Month	Manufacturing date code (ASCII).
88-89	2	Day	Manufacturing date code (ASCII).
90-91	2	Blank	–
92	1	Calibration flag	20h for calibrated average output power
93	1	–	E0h, Enhanced alarm/warning flags.
94	1	Reserved	Xxh

**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
95	1	CC_EXT	Check code for the Extended ID Fields (The value of the lower 8 bits of the sum of the contents from address 64 to 94)
96-255	160	Reserved	–
<b>Alarm and Warning Thresholds (Block Address: A2h and B2h)</b>			
0-1	2	Temp High Alarm	MSB at lower address. 70°C ambient
2-3	2	Temp Low Alarm	MSB at lower address. 0°C ambient
4-5	2	Temp High Warning	MSB at lower address. 65°C ambient
6-7	2	Temp Low Warning	MSB at lower address. 5°C ambient
8-9	2	Supply Voltage High Alarm	MSB at lower address. 3.6V
10-11	2	Supply Voltage Low Alarm	MSB at lower address. 3.0V
12-13	2	Supply Voltage High Warning	MSB at lower address. 3.47V
14-15	2	Supply Voltage Low Warning	MSB at lower address. 3.14V
16-17	2	Laser Bias High Alarm	MSB at lower address. 100mA.
18-19	2	Laser Bias Low Alarm	MSB at lower address. 5mA.
20-21	2	Laser Bias High Warning	MSB at lower address. 90mA.
22-23	2	Laser Bias Low Warning	MSB at lower address. 10mA
24-25	2	Tx Power High Alarm	MSB at lower address. 5.5dBm
26-27	2	Tx Power Low Alarm	MSB at lower address. 0dBm
28-29	2	Tx Power High Warning	MSB at lower address. 5dBm
30-31	2	Tx Power Low Warning	MSB at lower address. 0.5dBm
32-95	65	Reserved.	–
96	1	Temperature MSB	Internally measured module temperature
97	1	Temperature LSB	Internally measured module temperature

**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
98	1	Vcc MSB	Internally measured module supply voltage
99	1	Vcc LSB	Internally measured module supply voltage
100	1	Laser Bias MSB	Internally measured laser bias current.
101	1	Laser Bias LSB	Internally measured laser bias current.
102	1	Tx Power MSB	Internally measured Tx Power.
103	1	Tx Power LSB	Internally measured Tx Power.
104-109	11	Reserved	–
110	1	Tx Disable State	Bit 7: State of TX_DIS input pin
		Tx Disable Select	Bit 6: Read/write bit that allows software disable of laser. Writing “1” disables laser
		Reserved	Bit 5
		Reserved	Bit 4
		Reserved	Bit 3
		Tx Fault	Bit 2: State of TX_FAULT
		N/A	Bit 1
		Data_Ready	Bit 0
111	1	Conversion Update	–
		Temp Update	Bit 7 goes to high after a temperature update
		Vcc Update	Bit 6 goes to high after a Vcc update
		Mon1 Update	Bit 5 goes to high after a Tx bias current update
		Mon2 Update	Bit 4 goes to high after a Tx power update
		Mon3 Update	Bit 3 goes to high after a Tx modulation current update.
		Reserved	Bit 0 to Bit 2.

**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
112	1	Temp High Alarm Flag	Bit 7, set when the internal temperature exceeds the high temp alarm threshold.
		Temp Low Alarm Flag	Bit 6, set when the internal temperature goes below the low temp alarm threshold.
		Supply Voltage High Alarm Flag	Bit 5, set when the internal Vcc exceeds the supply voltage high alarm threshold.
		Supply Voltage Low Alarm Flag	Bit 4, set when the internal Vcc goes below the supply voltage low alarm threshold.
		Laser Bias High Alarm Flag	Bit 3, set when the monitored laser bias current exceeds the laser bias high alarm threshold.
		Laser Bias Low Alarm Flag	Bit 2, set when monitored laser bias current goes below the laser bias low alarm threshold.
		Tx Power High Alarm Flag	Bit 1, set when the monitored Tx power exceeds the Tx power high alarm threshold.
		Tx Power Low Alarm Flag	Bit 0, set when monitored Tx power current goes below the Tx power low alarm threshold.
113	1	Mod Current High Alarm Flag	Bit 7, set when the monitored laser modulation current exceeds the laser bias high alarm threshold.
		Mod Current Low Alarm Flat	Bit 6, set when monitored laser bias current goes below the laser modulation low alarm threshold.
		Reserved	Bit 0 - 5.
114-115	2	Reserved	–



**Table 3-6: Serial Interface Memory Map (Continued)**

Address	Size	Name	Description and Value of the Field
116	1	Temp High Warning Flag	Bit 7, set when the internal temperature exceeds the high temp warning threshold.
		Temp Low Warning Flag	Bit 6, set when the internal temperature goes below the low temp warning threshold.
		Supply Voltage High Warning Flag	Bit 5, set when the internal Vcc exceeds the supply voltage high warning threshold.
		Supply Voltage Low Warning Flag	Bit 4, set when the internal Vcc goes below the supply voltage low warning threshold.
		Laser Bias High Warning Flag	Bit 3, set when the monitored laser bias current exceeds the laser bias high warning threshold.
		Laser Bias Low Warning Flag	Bit 2, set when monitored laser bias current goes below the laser bias low warning threshold.
		Tx Power High Warning Flag	Bit 1, set when the monitored Tx power exceeds the Tx power high warning threshold.
		Tx Power Low Warning Flag	Bit 0, set when monitored Tx power current goes below the Tx power low warning threshold.
117	1	Mod Current High Warning Flag	Bit 7, set when the monitored laser modulation current exceeds the laser bias high alarm threshold.
		Mod Current Low Warning Flag	Bit 6, set when monitored laser bias current goes below the laser modulation low alarm threshold.
		Reserved	Bit 0 - 5
118-127	10	Reserved	–
<b>Vendor Specific ID Fields</b>			
128-247	120	User Writeable Area	–
248-255	8	Reserved	–

## 4. Application Reference Design

### 4.1 Typical Application Circuit

Figure 4-1 shows a typical application circuit for the GO2953.

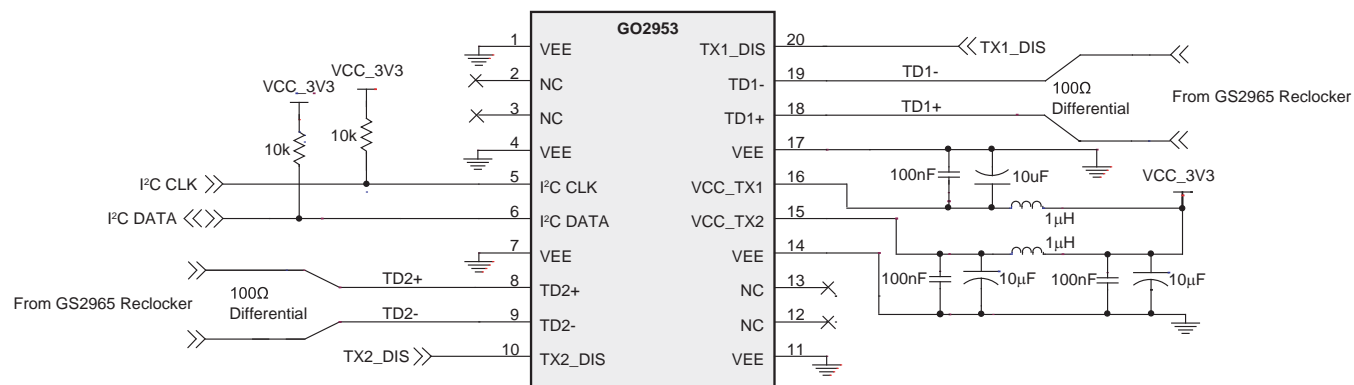


Figure 4-1: Typical Application Circuit

## 5. References and Relevant Standards

**Table 5-1: References and Relevant Standards**

INF-8074i Rev 1.0	SFP (Small Formfactor Pluggable) Transceiver
SMPTE 259M-2008	SDTV Digital Signal/Data – Serial Digital Interface
SMPTE 292M-2008	1.5 Gb/s Signal / Data Serial Interface
SMPTE 297-2006	Serial Digital Fiber Transmission System for SMPTE 259M, SMPTE 344M, SMPTE 292 and SMPTE 424M Signals
SMPTE 344M-2000	540 Mb/s Serial Digital Interface
SMPTE 424M-2006	3 Gb/s Signal/Data Serial Interface
ITU-T G.694.2	Spectral grids for WDM applications: CWDM wavelength grid

## 6. Package Information

### 6.1 Package Dimensions

A common mechanical outline, as shown in Figure 6-1, is used for all SFP modules.

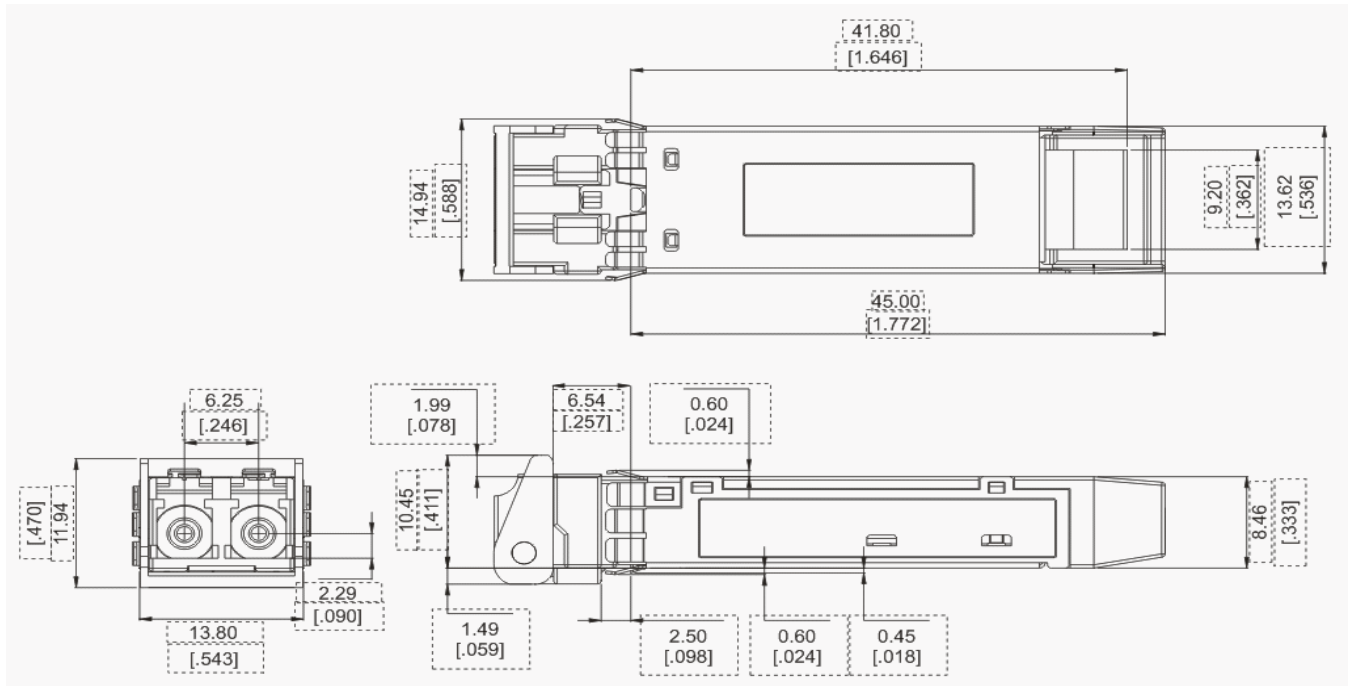


Figure 6-1: Common SFP Package Outline

## 6.2 PCB Layout Recommendations

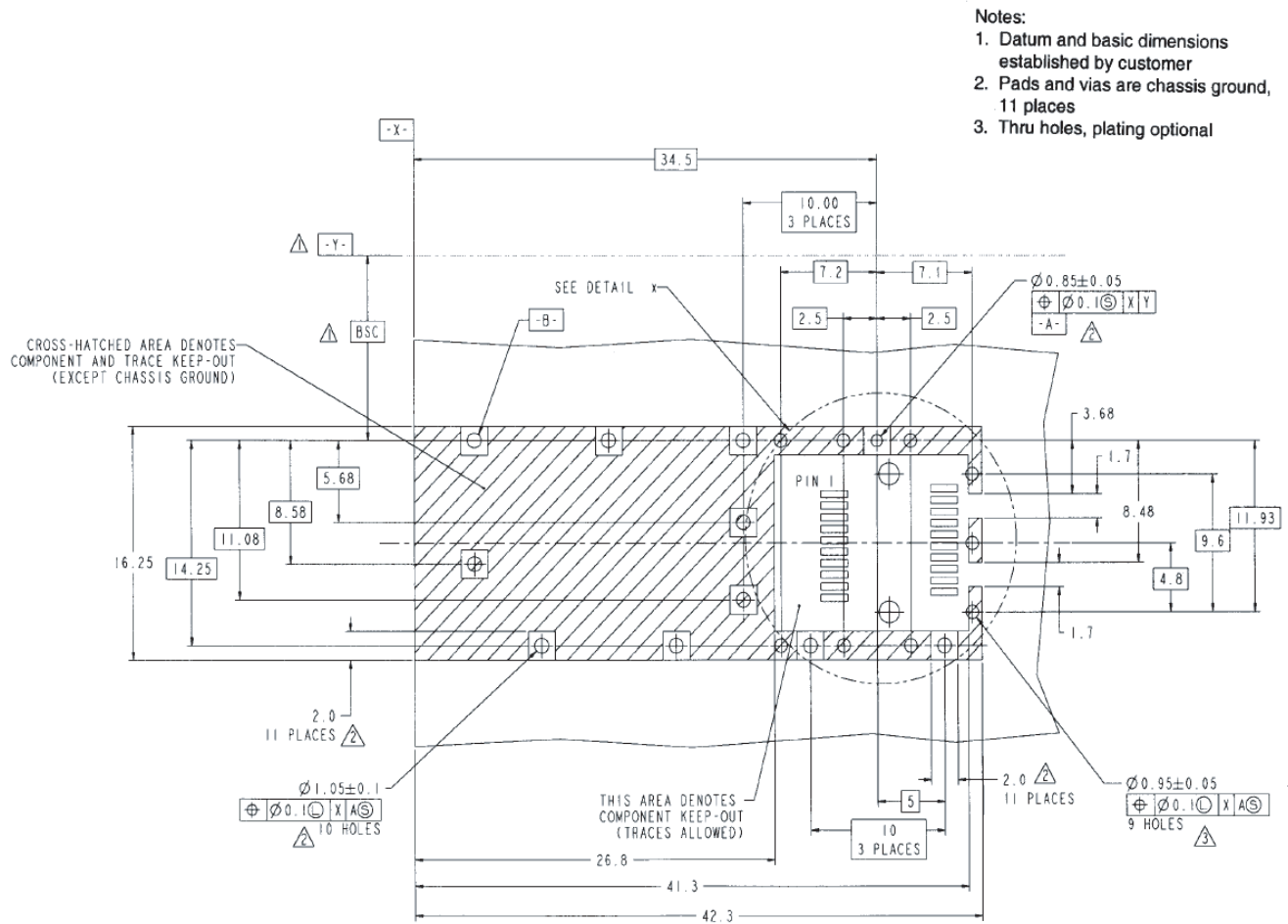


Figure 6-2: Host PCB Layout – Part 1

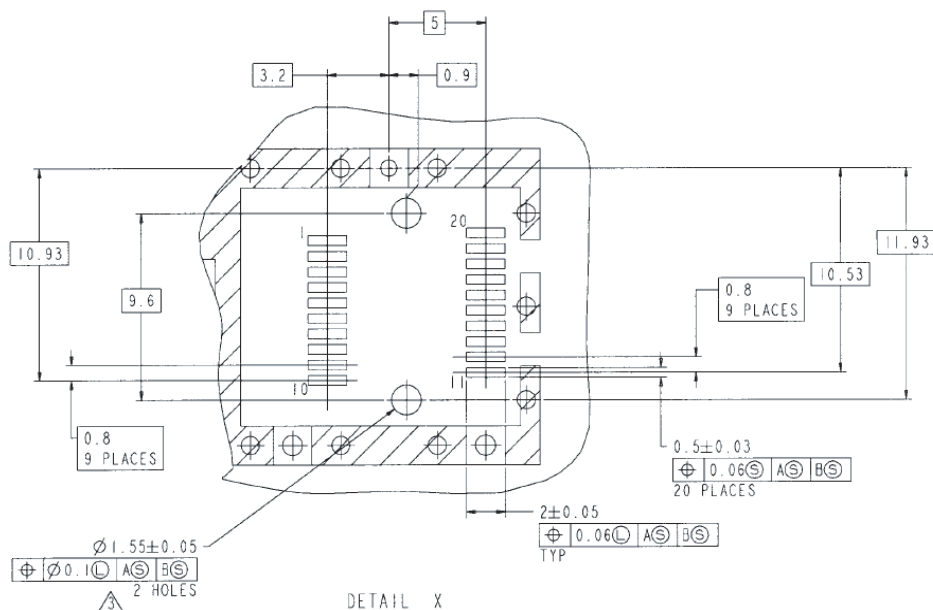


Figure 6-3: Host PCB Layout – Part 2

## 6.3 Marking Information

Table 6-1: Marking Information

Label Code	Description
XXYY	4-digit wavelength code - see <a href="#">Table 6-2: Ordering Information</a> .
ZZZZZZZ	7-digit serial number
UUUU	Channel 1 wavelength in nanometers
VVVV	Channel 2 wavelength in nanometers
YYYY	Year of manufacture
WW	Week of manufacture

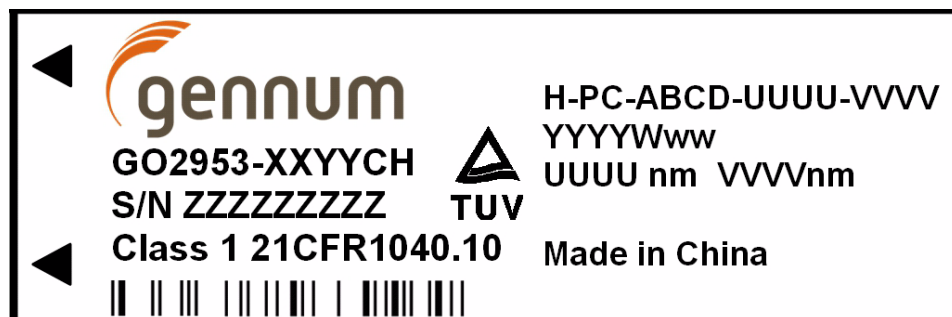


Figure 6-4: GO2953 Marking Information

## 6.4 Ordering Information

Table 6-2: Ordering Information

Part Number	Package	Wavelength	Temperature Range
GO2953-2729CH	SFP	Ch1: 1271nm Ch2: 1291nm	0°C to 70°C
GO2953-3133CH	SFP	Ch1: 1311nm Ch2: 1331nm	0°C to 70°C
GO2953-3537CH	SFP	Ch1: 1351nm Ch2: 1371nm	0°C to 70°C
GO2953-3941CH	SFP	Ch1: 1391nm Ch2: 1411nm	0°C to 70°C
GO2953-4345CH	SFP	Ch1: 1431nm Ch2: 1451nm	0°C to 70°C
GO2953-4749CH	SFP	Ch1: 1471nm Ch2: 1491nm	0°C to 70°C
GO2953-5153CH	SFP	Ch1: 1511nm Ch2: 1531nm	0°C to 70°C
GO2953-5557CH	SFP	Ch1: 1551nm Ch2: 1571nm	0°C to 70°C
GO2953-5961CH	SFP	Ch1: 1591nm Ch2: 1611nm	0°C to 70°C
GO2953-3155CH	SFP	Ch1: 1310nm Ch2: 1550nm	0°C to 70°C

## DOCUMENT IDENTIFICATION

### APPLICATION NOTE

Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Gennum assumes no liability for any errors in this document, or for the application or design described herein. Gennum reserves the right to make changes to the product or this document at any time without notice.

## CAUTION

### ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



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