INCH-POUND
MIL-M-38510/2G
8 February 2005
SUPERSEDING
MIL-M-38510/2E
24 December 1974
MIL-M-0038510/2F (USAF)
24 OCTOBER 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outlines/lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -1.5 V dc at -12 mA to 5.5 V dc
Storage temperature range ..... -65° to +150°C
Maximum power dissipation, (P_D)
flip-flop, 1/..... 110 mW 1/
Lead temperature (soldering, 10 seconds)..... 300°C
Thermal resistance, junction to case (θ_{JC}):..... 0.09°C/mW for flat packs
0.08°C/mW for dual-in-line pack
Junction temperature (T_J)..... 175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc minimum to
5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) ..... 2.0 V dc
Maximum low-level input voltage (V_{IL}) ..... 0.8 V dc
Normalized fanout (each output) 2/..... 10 maximum
Case operating temperature range (T_C)..... -55 °C to +125 °C
Input set up time:
Device type 01, 02, 03 and 04, ... $\geq$ clock pulse width
Device type 05, 06, and 07..... 20 ns
Input hold time
Device types 01, 02, 03 and 04..... 0 ns
Device type 05, 06 and 07 ..... 5 ns

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration
2/ Device will fanout in both high and low levels to the specified number of I_{IL1}/I_{IH1} inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ *or* http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figures 1.

3.3.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. Subgroups 7 and 8 testing requires only a summary of attributes data.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 9/	Device Type	Limits		Units
				Min	Max	
High-level output voltage	V_{OH}	V_{CC}=4.5 V I_{OH} = -400 µA	All	2.4	--	Volts
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL}=16 mA	All		0.4	Volts
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IC} = -12 mA T_C = 25ºC	All		-1.5	Volts
Low-level input current	I_{IL1}	V_{CC} = 5.5 V V_{IN} = 0.4 V 1/	01, 02, 03, 04, 05, 06	-0.7	-1.6	mA
			07	-0.5	-1.6	mA
Low-level input current	I_{IL2}	V_{CC} = 5.5 V V_{IN} = 0.4 V 2/	01, 02, 03, 04, 05	-1.4	-3.2	mA
			07	-1.0	-3.2	mA
Low-level input current	I_{IL3}	V_{CC} = 5.5 V V_{IN} = 0.4 V 6/	01, 02, 03, 04	-0.7	-3.2	mA
High-level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.4 V 5/	All		40	µA
High-level input current	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 5.5 V 5/	All		100	µA
High-level input current	I_{IH3}	V_{CC} = 5.5 V V_{IN} = 2.4 V 3/	All 11/		80	µA
High-level input current	I_{IH4}	V_{CC} = 5.5 V V_{IN} = 5.5 V 3/ 7/	All		200	µA
High-level input current	I_{IH5}	V_{CC} = 5.5 V V_{IN} = 2.4 V 7/ 8/	01, 02, 03, 04, 05, 07	-50	-850 120	µA µA
High-level input current	I_{IH6}	V_{CC} = 5.5 V V_{IN} = 5.5 V 8/	05, 07		300	µA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V V_{IN} = 0 4/	All	-20	-57	mA
Supply current per device	I_{CC}	V_{CC} = 5.5 V V_{IN} = 5 V	01		20	mA
			02, 03, 04		40	
			05, 06, 07		30	
Maximum clock frequency 10/	f_{MAX}	V_{CC} = 5 V CL = 50 pF minimum RL = 390Ω ± 5%	01, 02, 03 04, 05, 07	10		MHz
			06	15		
Propagation delay to high logic level (clear or preset to output)	t_{PLH}		01, 02, 03, 04, 05	5	39	ns
			06	5	62	
			07	5	31	
Propagation delay to low logic level (clear or preset to output)	t_{PHL}		01, 02, 03, 04, 05	5	50	ns
			06	5	62	
			07	5	39	
Propagation delay to high logic level (clock to output)	t_{PLH}		06	5	62	ns
			01, 02, 03, 04, 05	5	39	
			07	5	31	
Propagation delay to low logic level (clock to output)	t_{PHL}		06	5	62	ns
			01, 02, 03, 04, 05	5	50	
			07	5	39	

1/ Input condition – J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.
2/ Input condition – Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.
3/ Input condition – Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.
4/ No more than one output should be shorted at a time.
5/ Input condition – J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.
6/ Input condition – Clear or preset for device types 01, 02, 03 and 04.
7/ Input condition – Clock for device types 01, 02, 03 and 04.

8/ Input condition – Clear for device types 05 and 07.
9/ See table III for complete terminal conditions.
10/ Minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
11/ For device types 02 and 03,limits are 0 to 120 μA.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 8, 9	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7 9
Group B test when using the method 5005 QCI option	1, 2, 3,	N/A
Group C end-point electrical parameters	1, 2, 3,	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

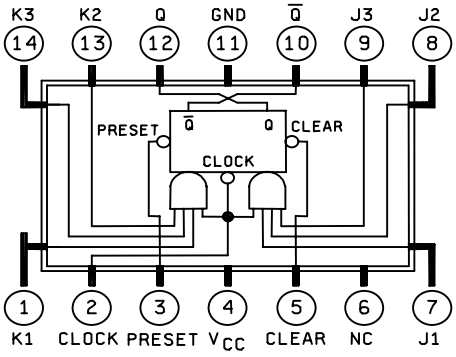
4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

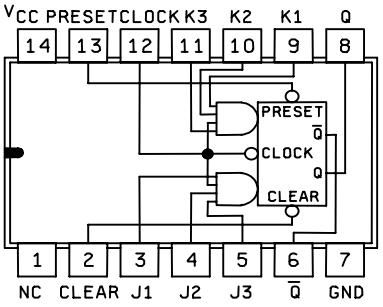
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

DEVICE TYPE 01

CASES A,B AND D

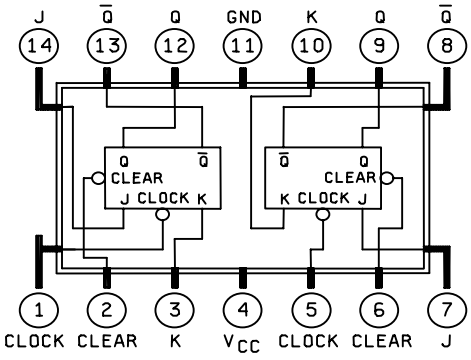


CASE C

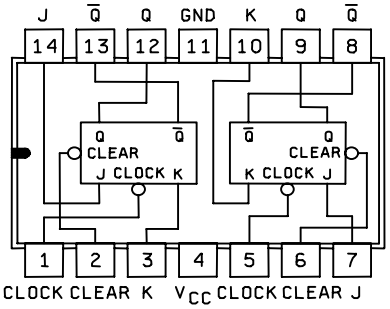


DEVICE TYPE 02

CASES A,B AND D



CASE C



DEVICE TYPE 03

CASE C

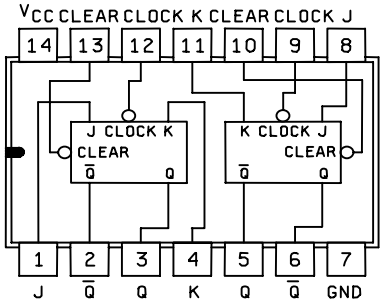
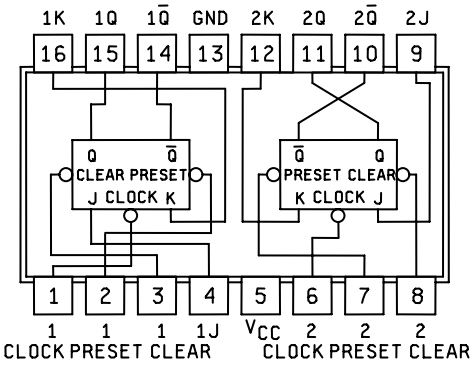


FIGURE 1. Logic diagram and terminal connections.

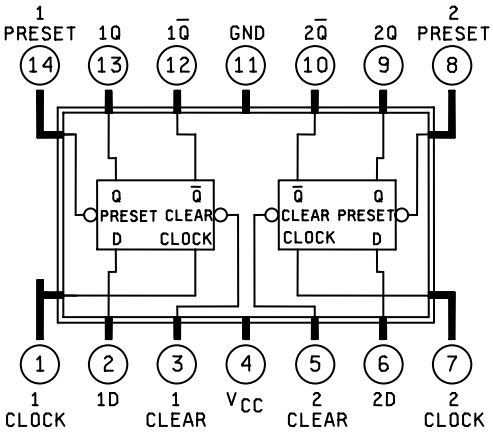
DEVICE TYPE 04

CASES E AND F

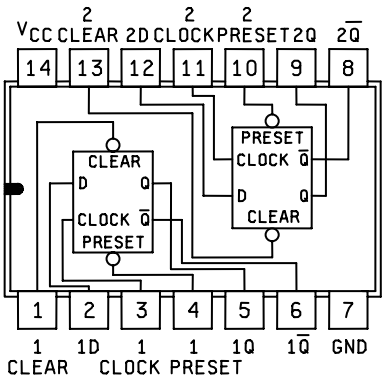


DEVICE TYPES 05 AND 07

CASES A,B AND D

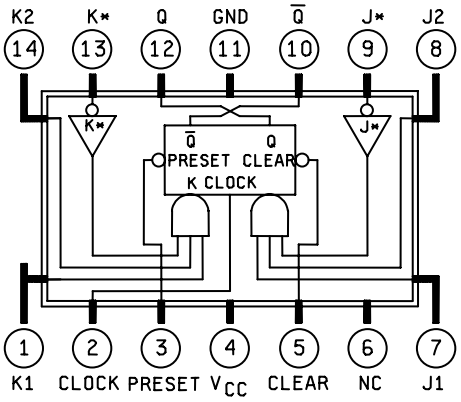


CASE C



DEVICE TYPE 06

CASES A,B AND D



CASE C

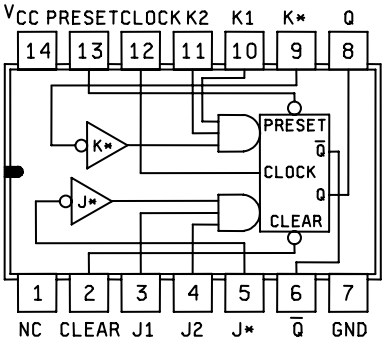


FIGURE 1. Logic diagram and terminal connections – Continued.

Device type 01

Truth table		
t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level
Low input to clear sets Q to low-level
Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. $t_n + 1$ = Bit time after clock pulse.

Device type 02 and 03

Truth table each flip-flop		
t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to clear sets Q to low-level
Clear is independent of clock and dominate regardless of the state of clock or J or K inputs.

NOTES: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time after clock pulse.

FIGURE 2. Truth tables.

Device type 04

Truth table each flip-flop		
t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level
Low input to clear sets Q to low-level
Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time after clock pulse.

Device type 05 and 07

Truth table each flip-flop		
t_n	$t_n + 1$	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

Positive logic: Low input to preset sets Q to high-level
Low input to clear sets Q to low-level
Preset and clear are independent of clock and dominate regardless of the state of clock or D input.

NOTES: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time after clock pulse.

FIGURE 2. Truth tables – Continued.

Device type 06

Truth table		
t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high-level
Low input to clear sets Q to low-level
Preset or clear function can occur only
When clock input is low.

NOTES: 1. $J = J1 \bullet J2 \bullet \overline{J^*}$
2. $K = K1 \bullet K2 \bullet \overline{K^*}$
3. t_n = Bit time before clock pulse.
4. $t_n + 1$ = Bit time after clock pulse.
5. If inputs J* or K* are not used must be grounded.

FIGURE 2. Truth tables – Continued.

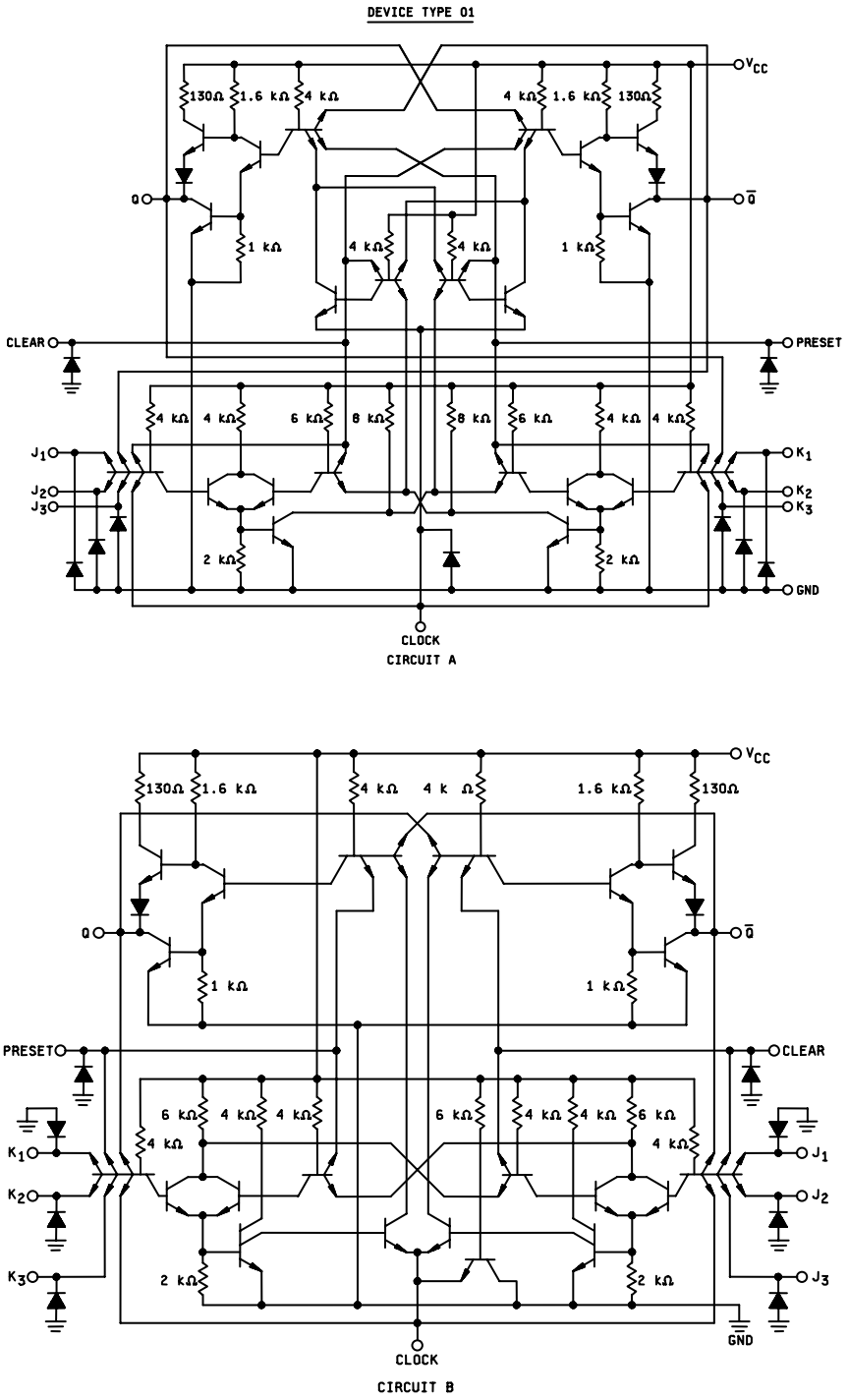


FIGURE 3. Schematic circuits.

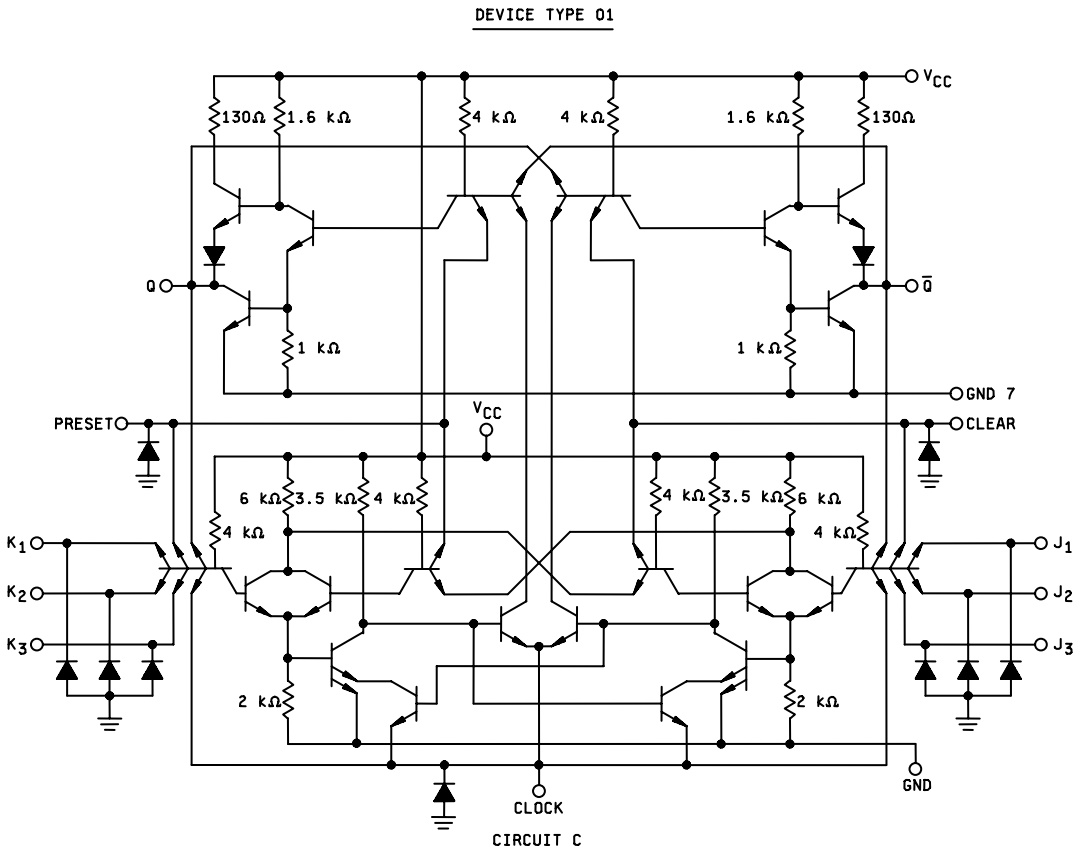


FIGURE 3. Schematic circuits – Continued.

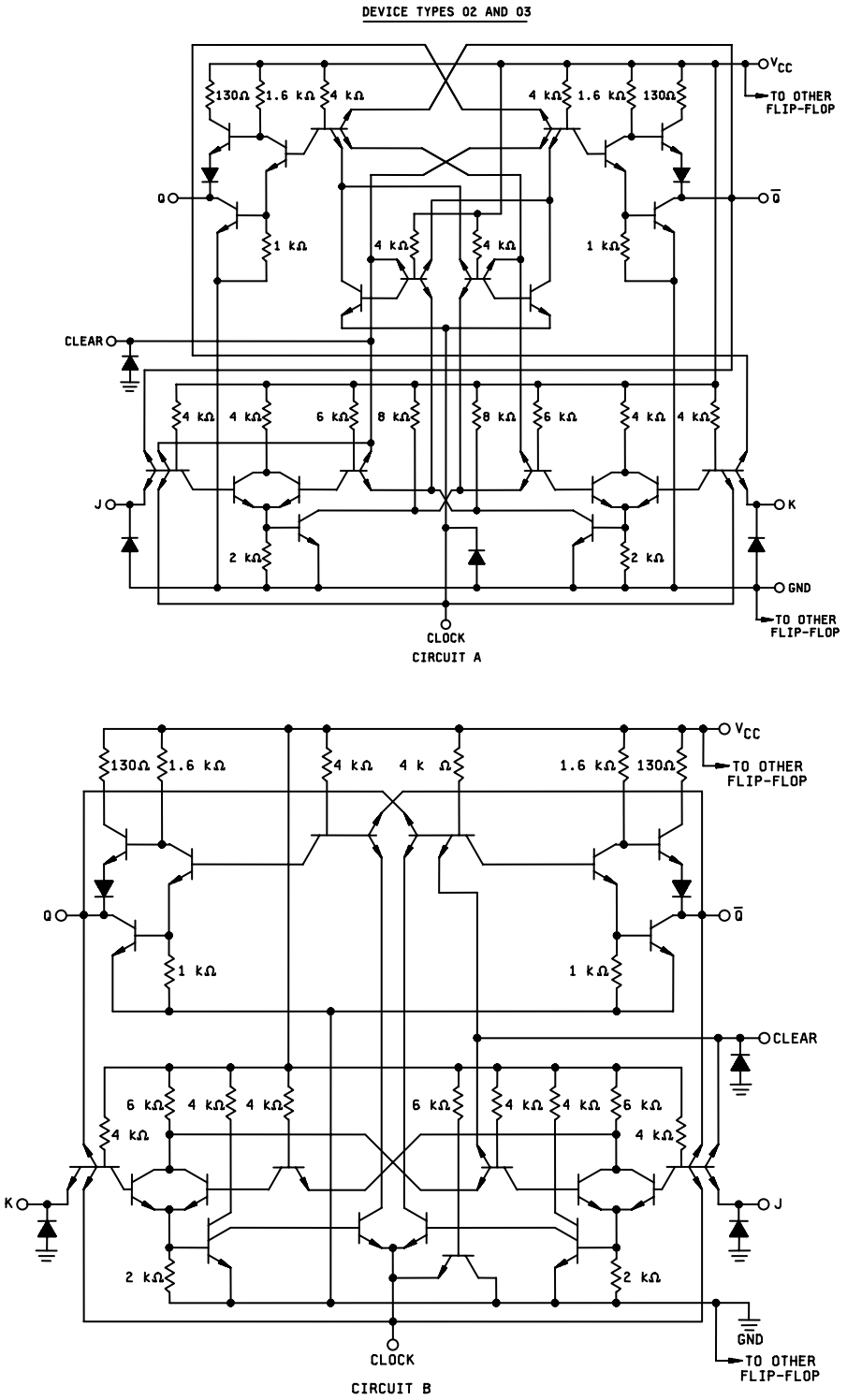
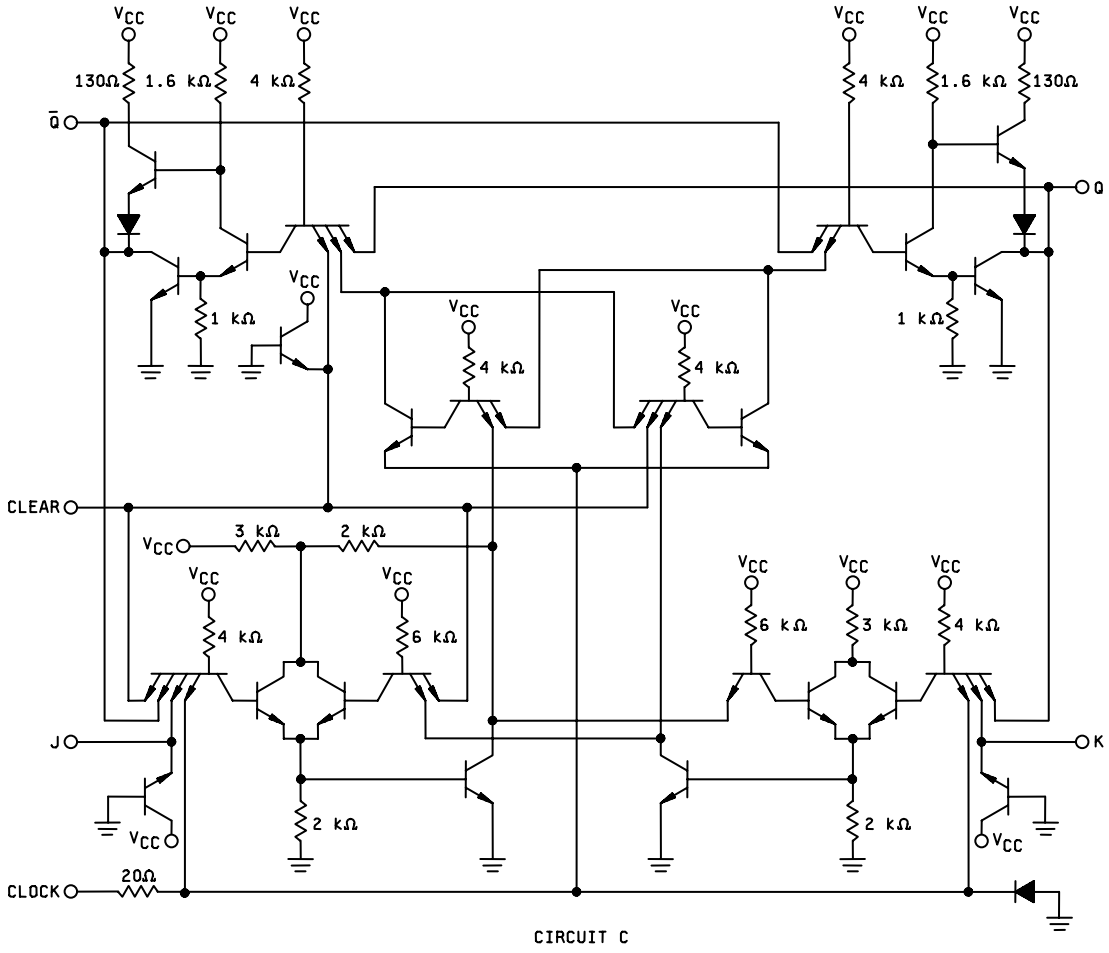


FIGURE 3. Schematic circuits – Continued.

DEVICE TYPES 02 AND 03



CIRCUIT C

NOTES:
1. Circuits A, B, and C are the only acceptable variations for device types 02 and 03.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.

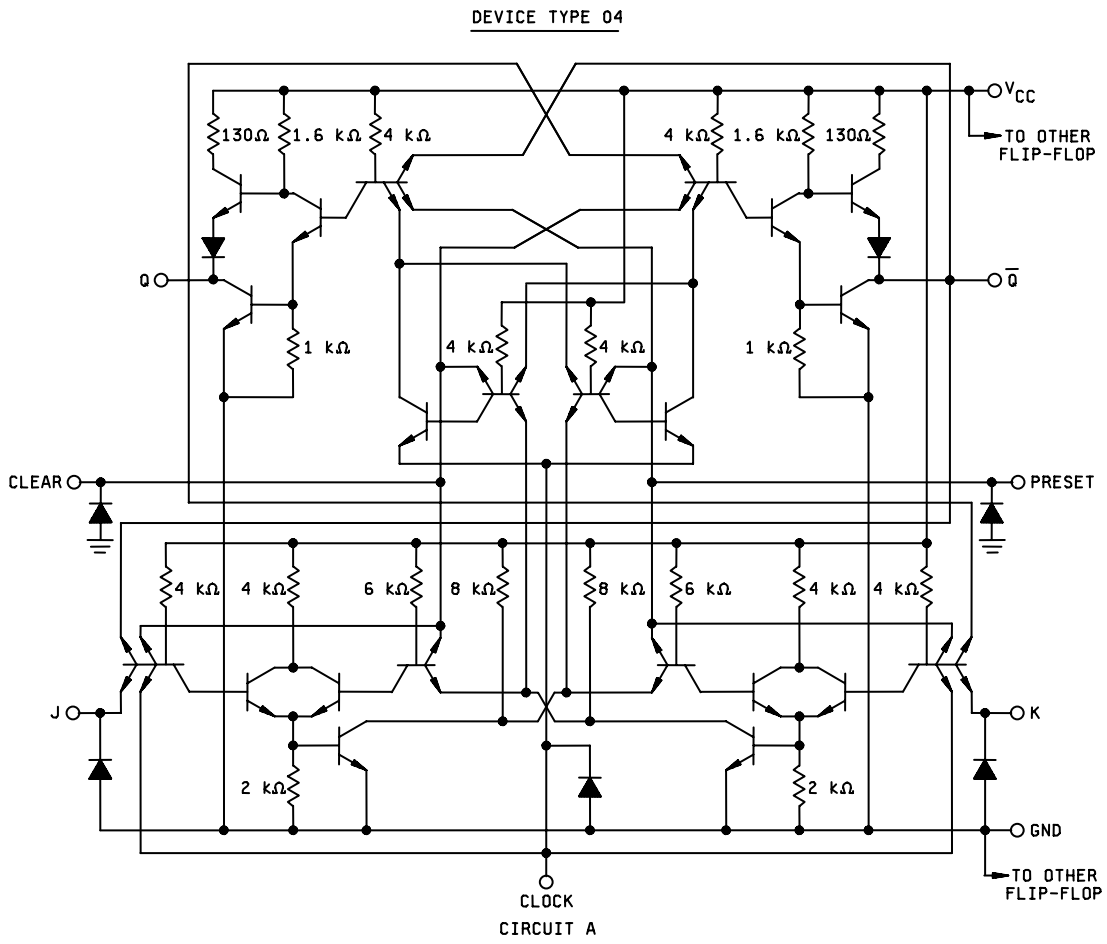


FIGURE 3. Schematic circuits – Continued.

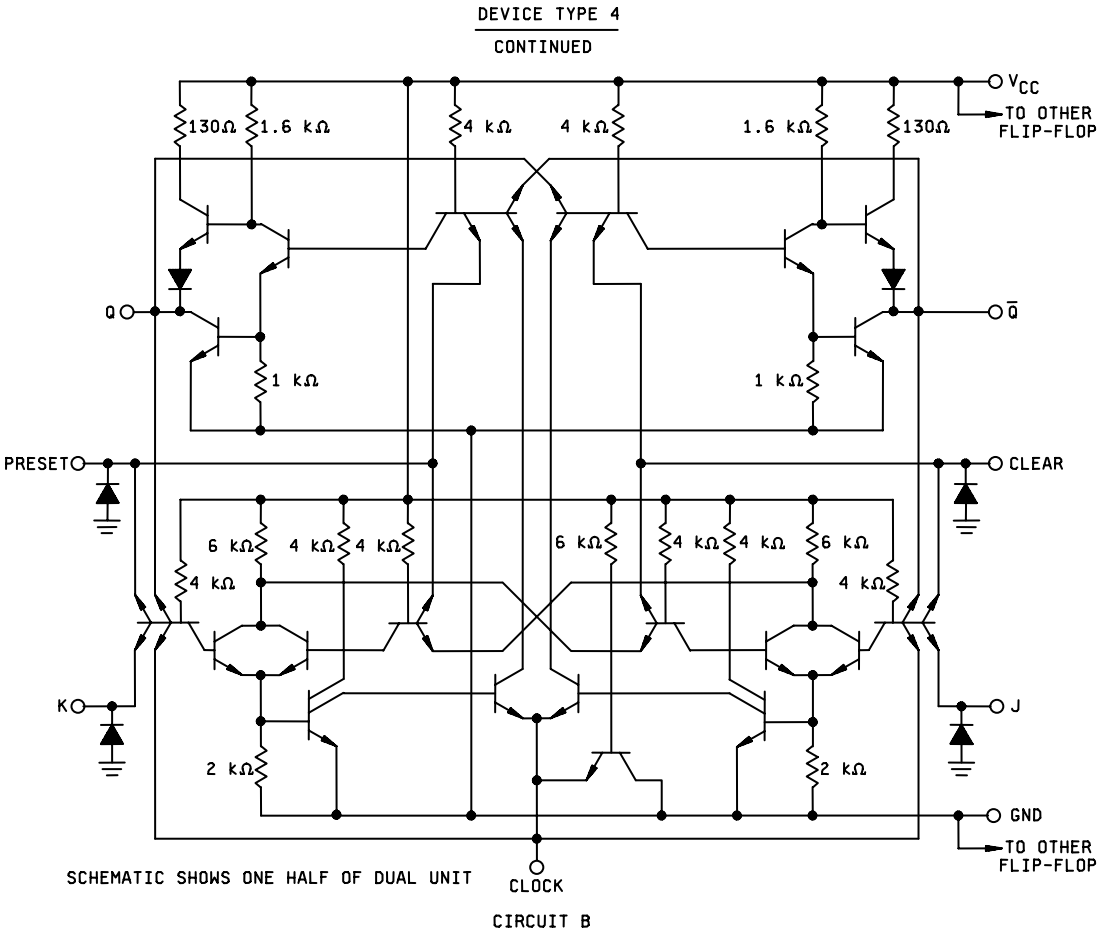
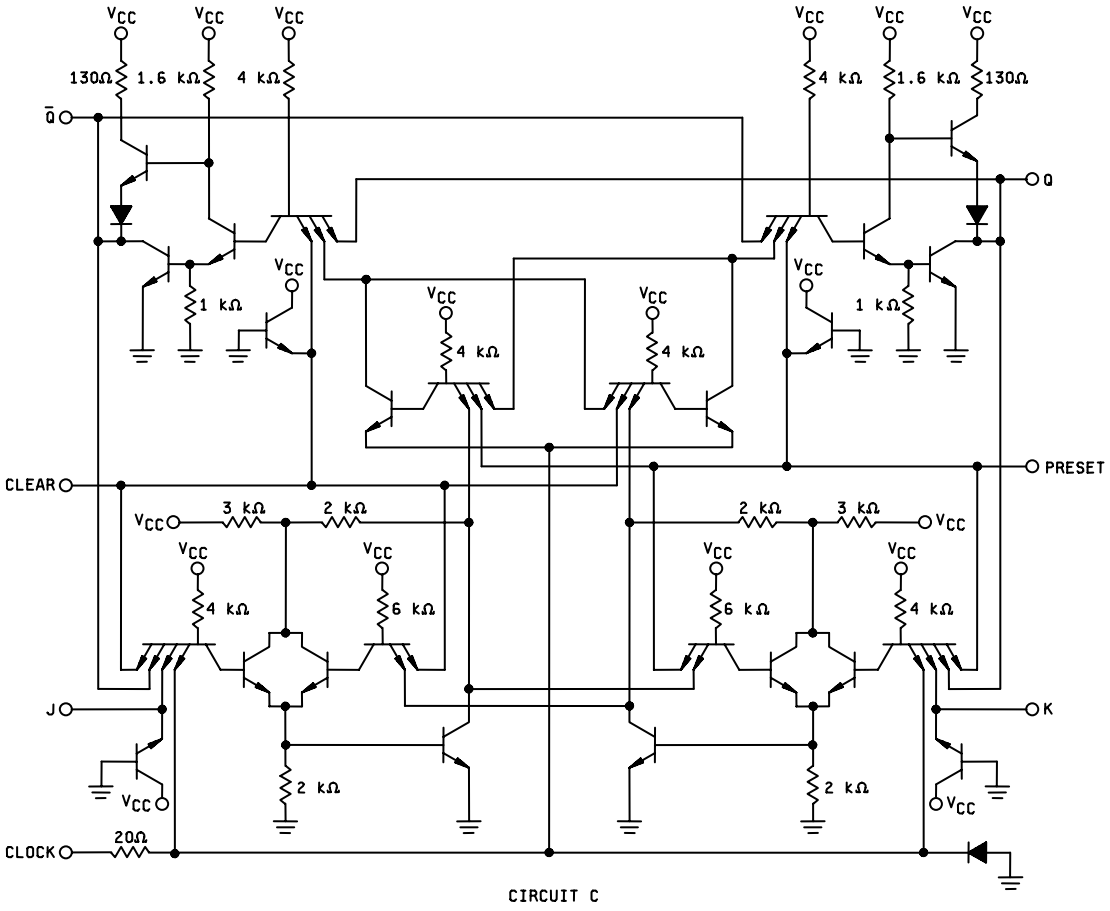


FIGURE 3. Schematic circuits – Continued.

DEVICE TYPE 04
CONTINUED

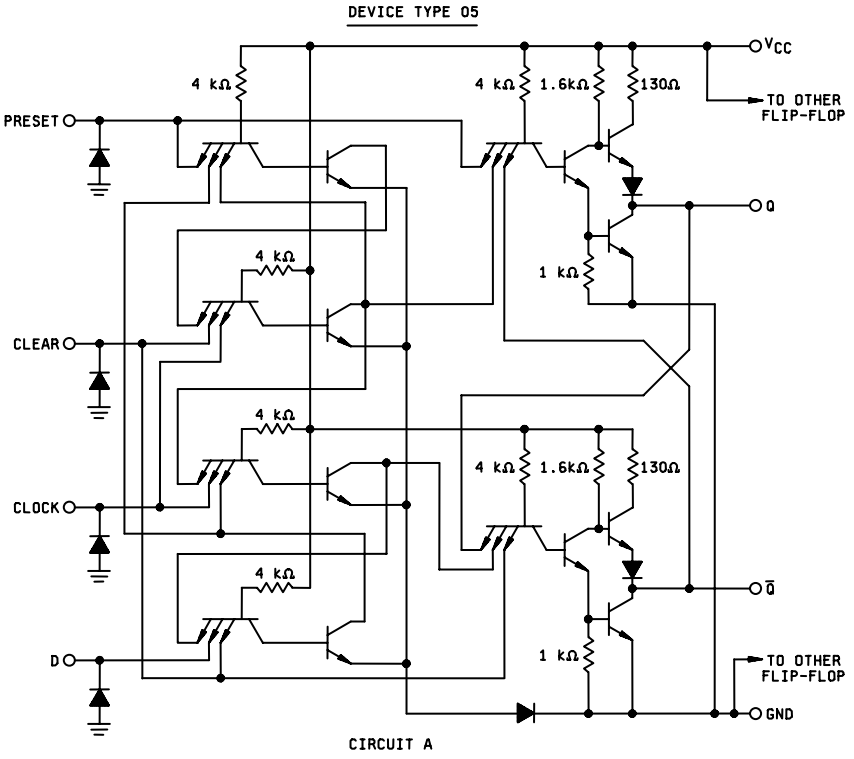


CIRCUIT C

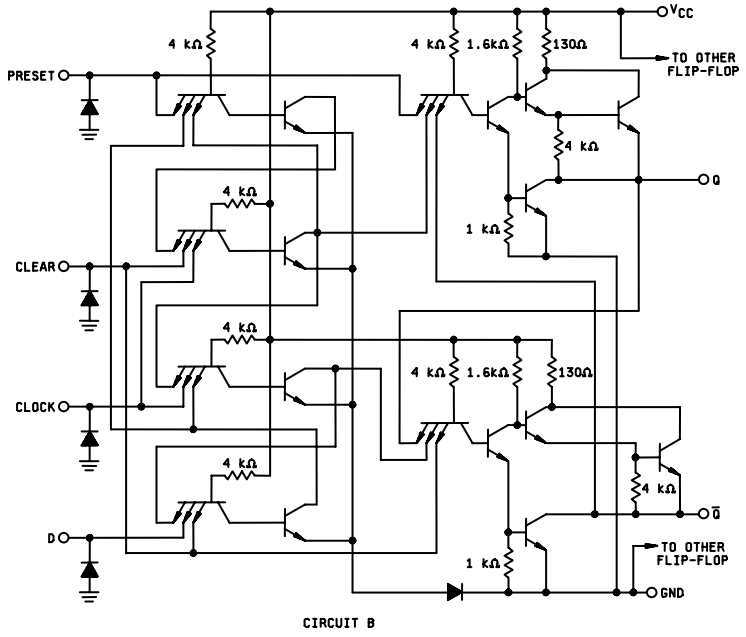
NOTES:
1. Circuits A, B and C are the only acceptable variation for device type 04.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.

DEVICE TYPE 05



CIRCUIT A



CIRCUIT B

NOTES:
1. Circuits A, B, and C are the only acceptable variations for device type 05.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.

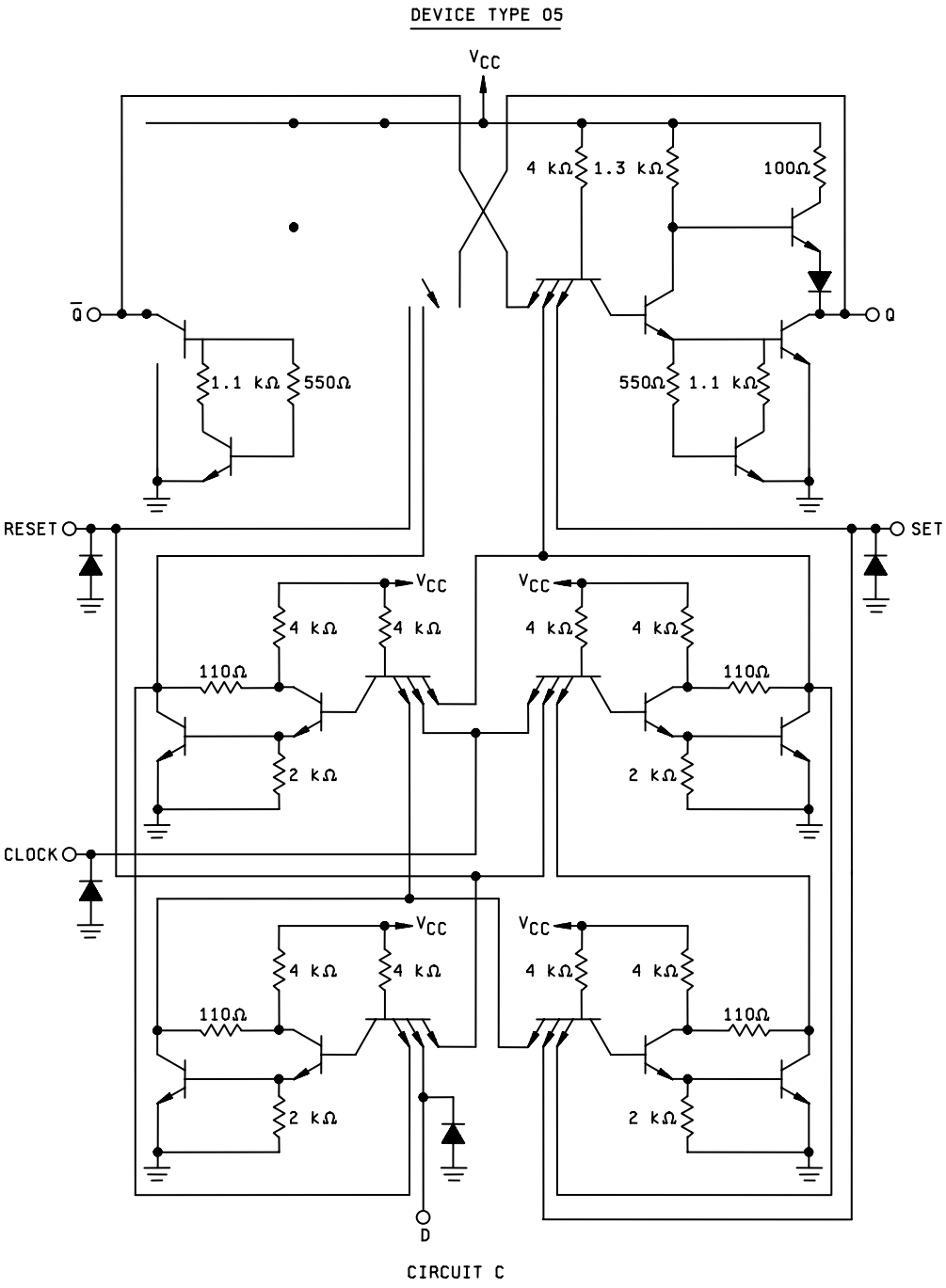
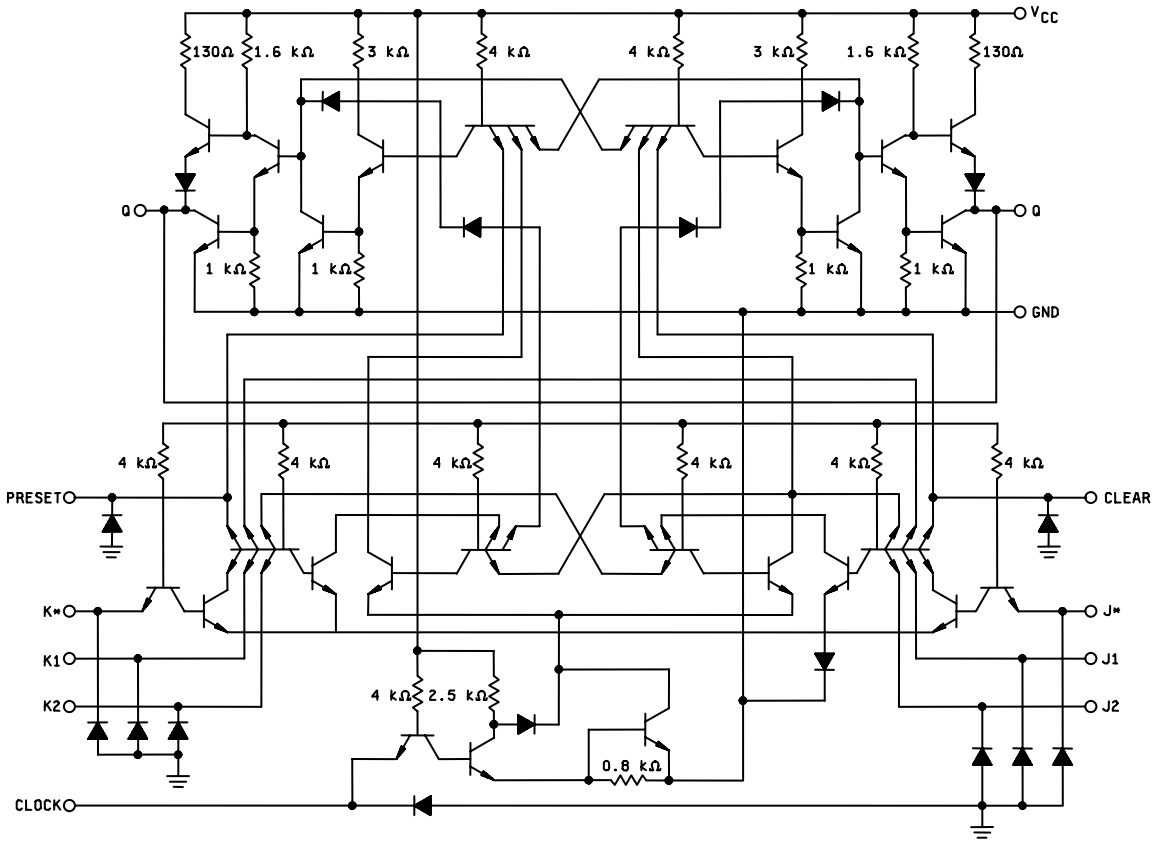


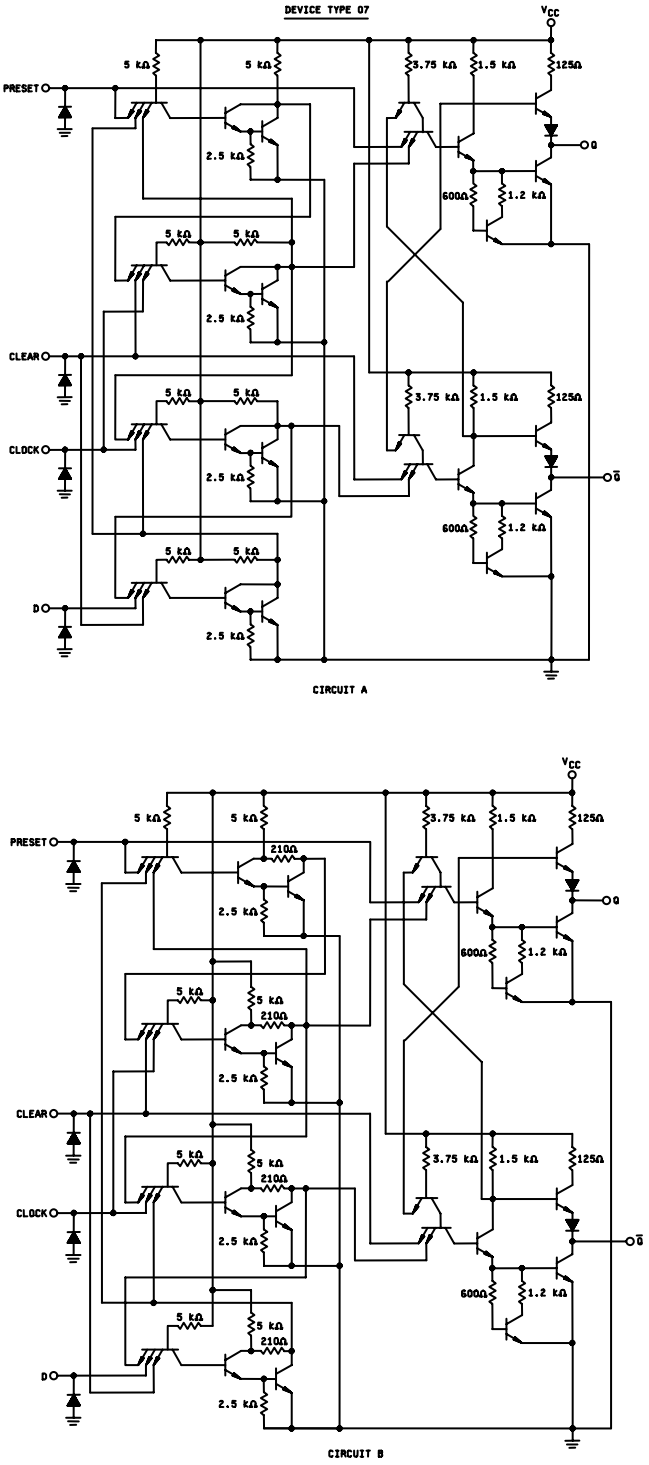
FIGURE 3. Schematic circuits – Continued.

DEVICE TYPE 06



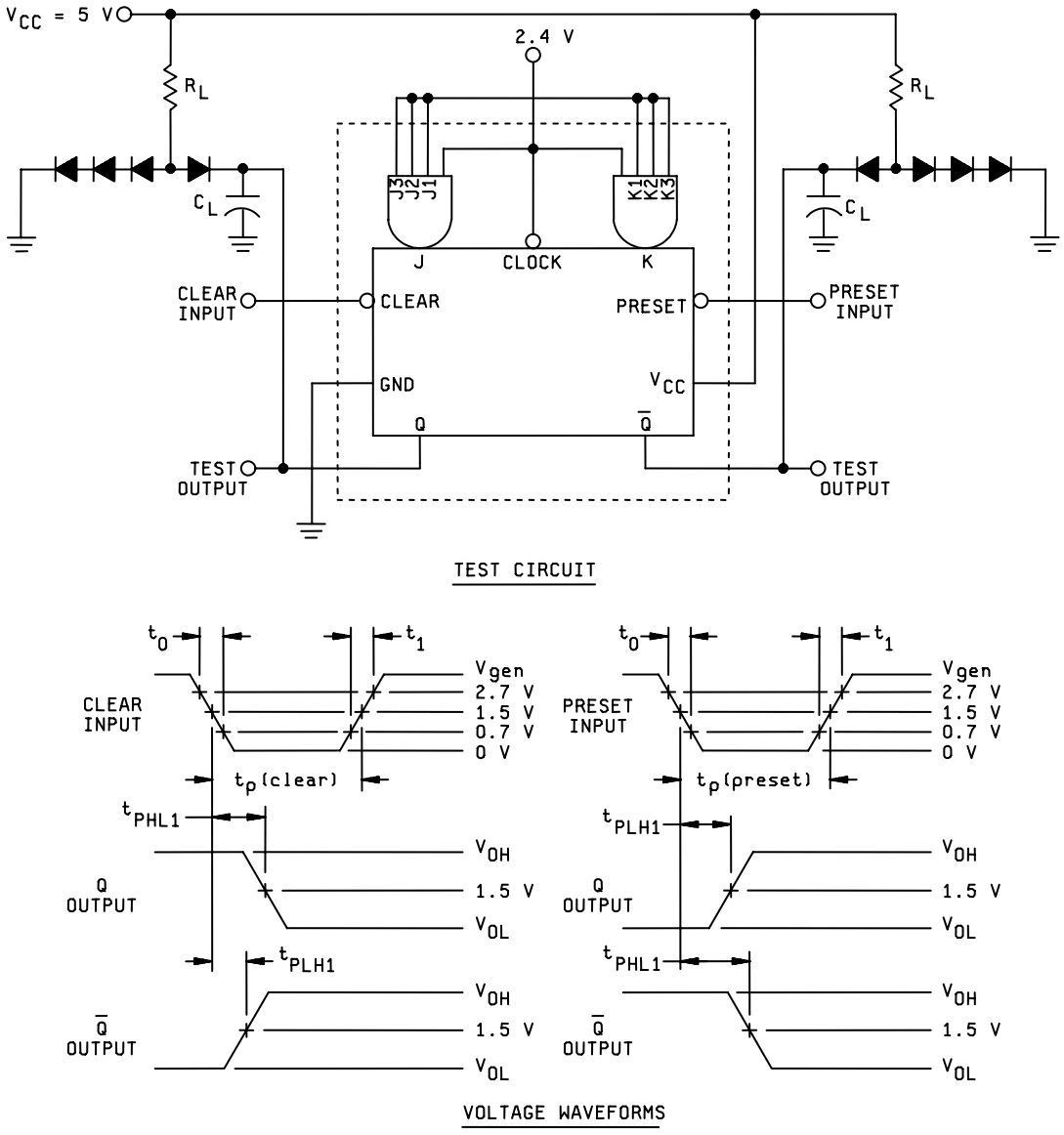
NOTE: All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.



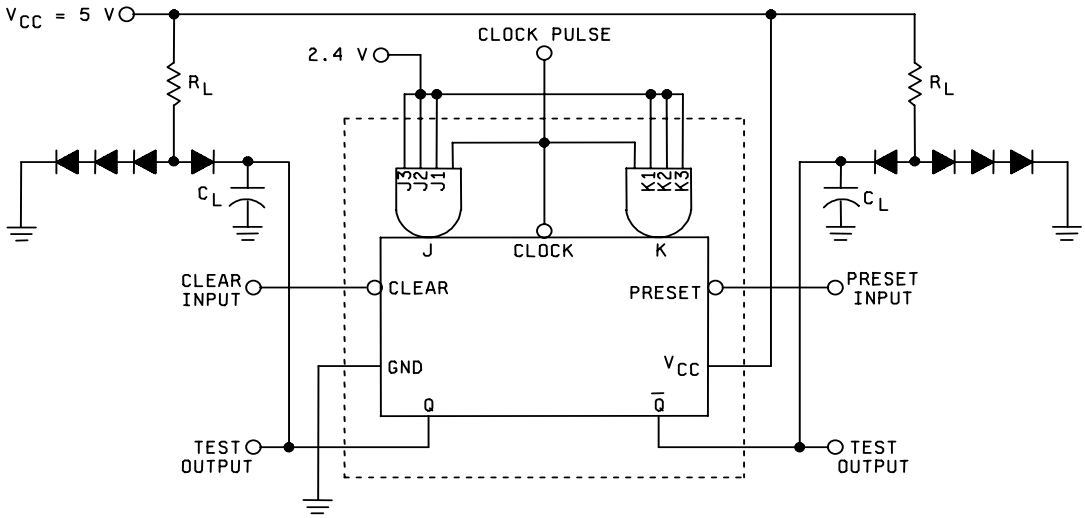
NOTES:
1. Circuits A and B are the only acceptable variations for device type 07.
2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.

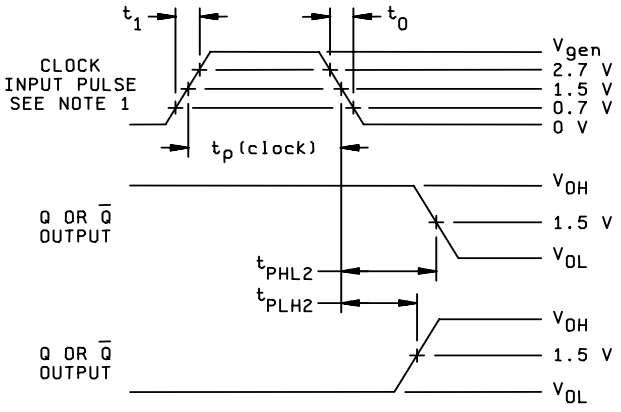


NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3 V, $t_0 = t_1$ = 10 ns, t_p(clear) = t_p(preset) = 30 ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
3. C_L = 50 pF, minimum (C_L includes probe and jig capacitance).
4. $R_L = 390\Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 4. Clear and preset switching test circuit and waveforms for device type 01.



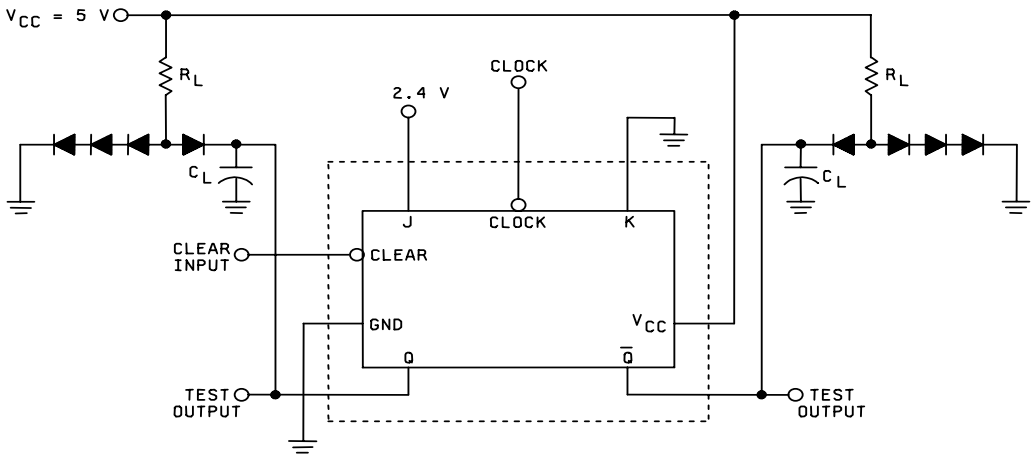
TEST CIRCUIT



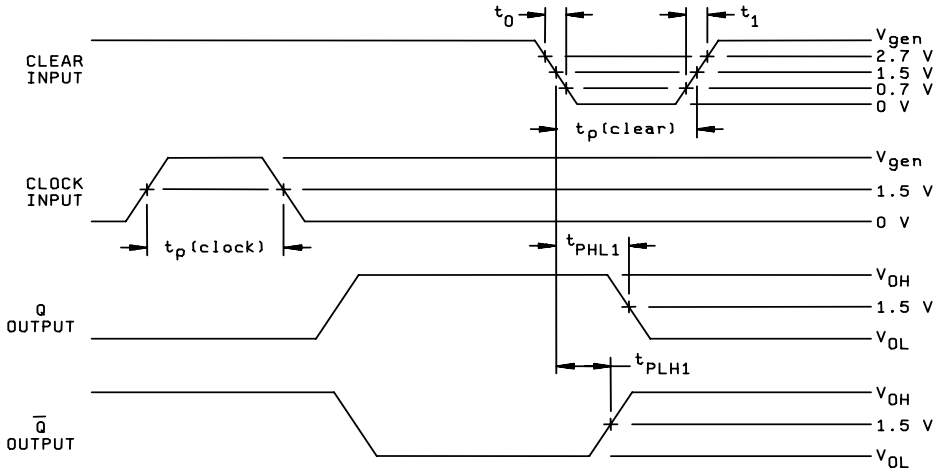
VOLTAGE WAVEFORMS

NOTES:
1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
2. J = J1 • J2 • J3; and K = K1 • K2 • K3
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF minimum (C_L includes probe and jig capacitance).
5. R_L = 390Ω ±5%

FIGURE 5. Synchronous switching test circuit for device type 01.



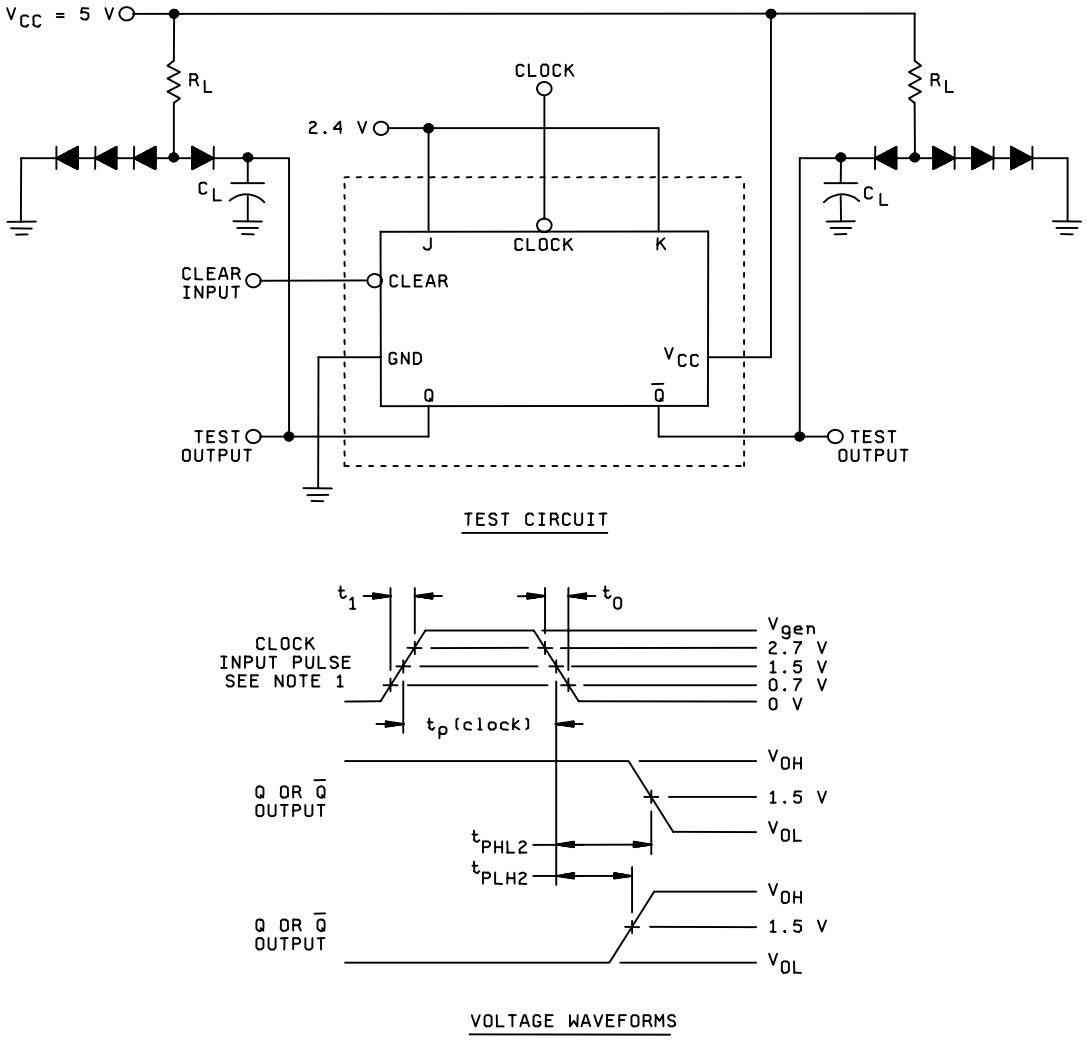
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Clear inputs dominate regardless of the state of clock or J-K inputs.
2. Clear input pulse characteristics: V_{gen} = 3 V, $t_0 = t_1$ = 10 ns, t_p(clear) = 30 ns, PRR = 1 MHz.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF, minimum (C_L includes probe and jig capacitance).
5. R_L = 390Ω ±5%.
6. Clock input pulse characteristics: V_{gen} = 3 V, t_p (clock) ≥ 25 ns, PRR = 1 MHz.

FIGURE 6. Clear switching test circuit and waveforms for device types 02 and 03.

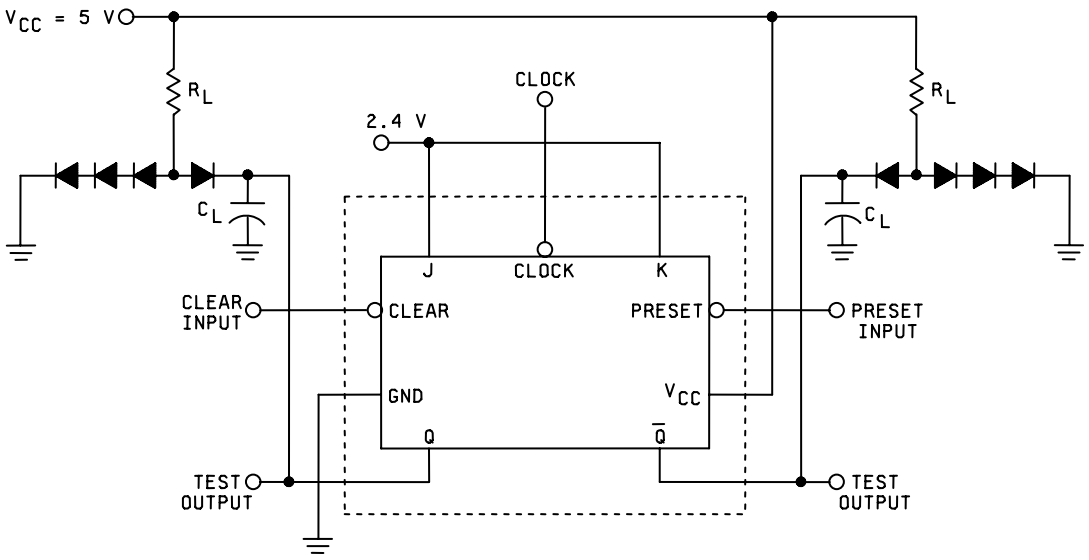


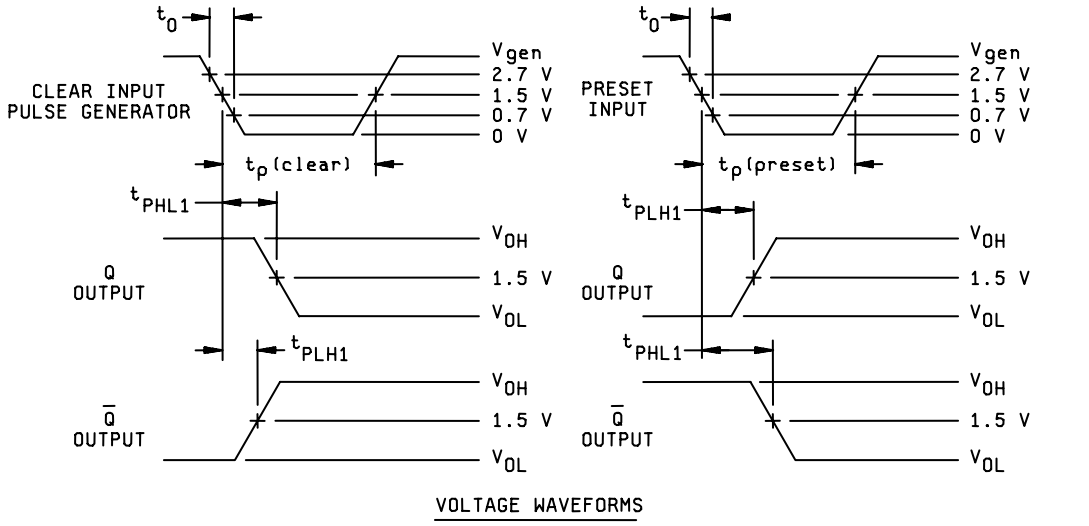
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 20 ns, and PRR = 10 MHz for subgroups 9, 10, and 11.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF minimum (including jig and probe capacitance).
4. R_L = 390Ω ±5%

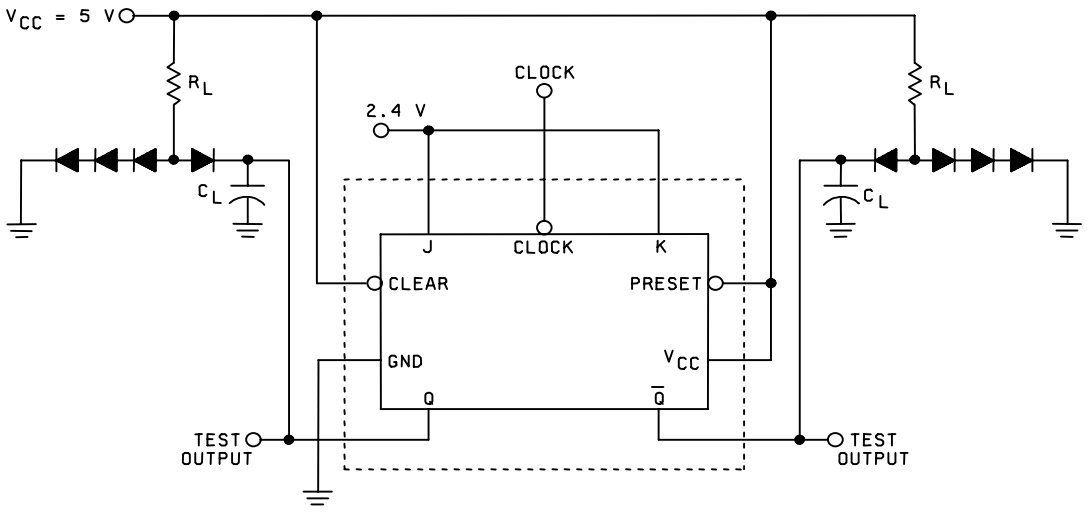
FIGURE 7. Synchronous switching test circuit for device type 02 and 03.



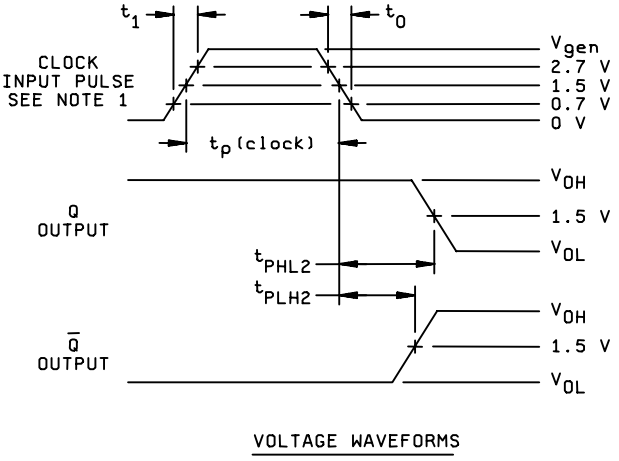


NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3 V, $t_0 = t_1$ = 10 ns, t_p(clear) = t_p(preset) = 30 ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
3. C_L = 50 pF, minimum (including jig and probe capacitance).
4. $R_L = 390\Omega \pm 5\%$.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 8. Clear and preset switching test circuit and waveforms for device type 04.



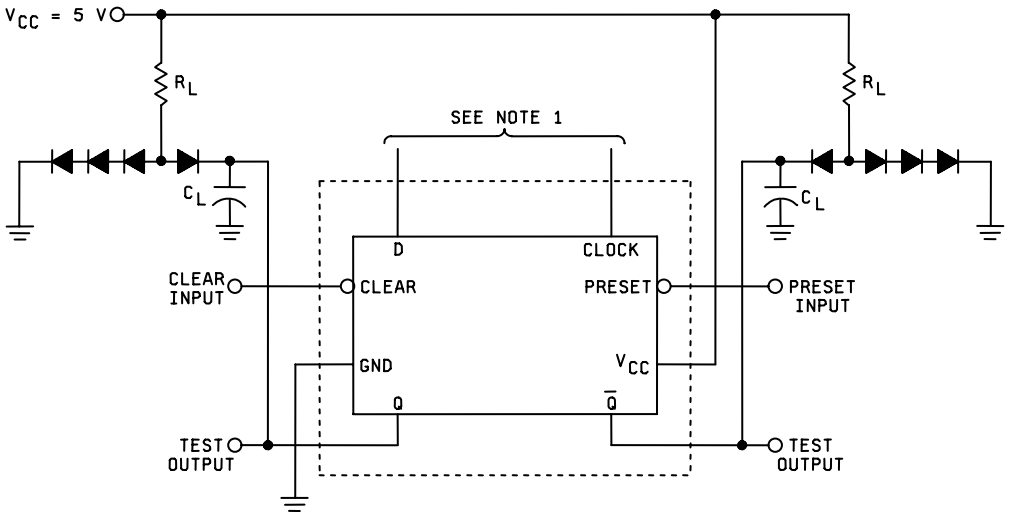
TEST CIRCUIT



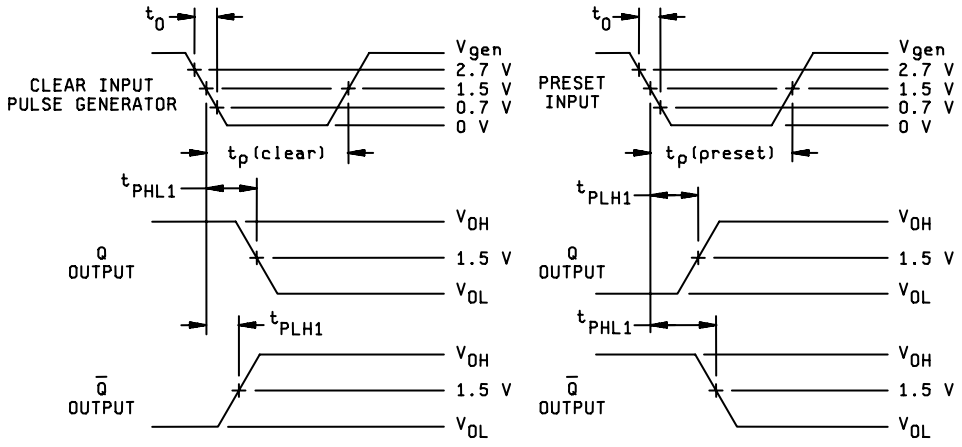
VOLTAGE WAVEFORMS

NOTES:
1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output), V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF minimum (including jig and probe capacitance).
4. R_L = 390Ω ±5%

FIGURE 9. Synchronous switching test circuit for device type 04.



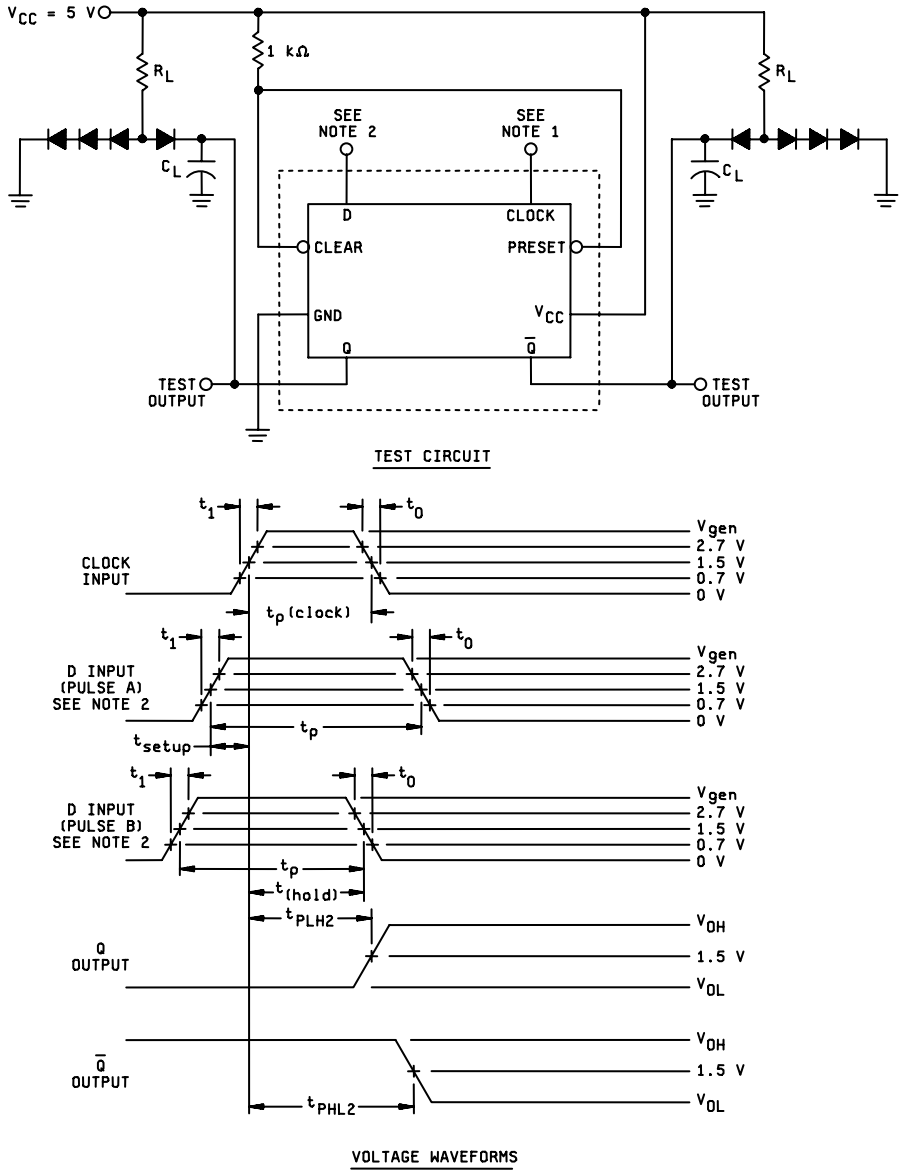
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
2. All diodes are 1N3064, or equivalent.
3. Clear or preset input pulse characteristics: V_{gen} = 3 V, $t_o \leq 7$ ns, t_p (clear) = t_p (preset) = 35 ns, and PRR = 1 MHz.
4. C_L = 50 pF, minimum (including jig and probe capacitance).
5. R_L = 390Ω ±5%.
6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 10. Clear and preset switching test circuit and waveforms for device types 05 and 07.



NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3 V, $t_o = t_1 \leq 10$ ns, t_p (clock) = 30 ns, and PRR = 1 MHz. When testing f_{MAX}, PRR = see table III.
2. D input (pulse A) has the following characteristics: V_{gen} = 3 V, $t_o = t_1 \leq 10$ ns, t_{SETUP} = 25 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3 V, $t_o = t_1 < 7$ ns, t_{hold} = 6 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF minimum (including jig and probe capacitance).
5. R_L = 390Ω ±5%

FIGURE 11. Synchronous switching test circuit (high level data) for device types 05 and 07.

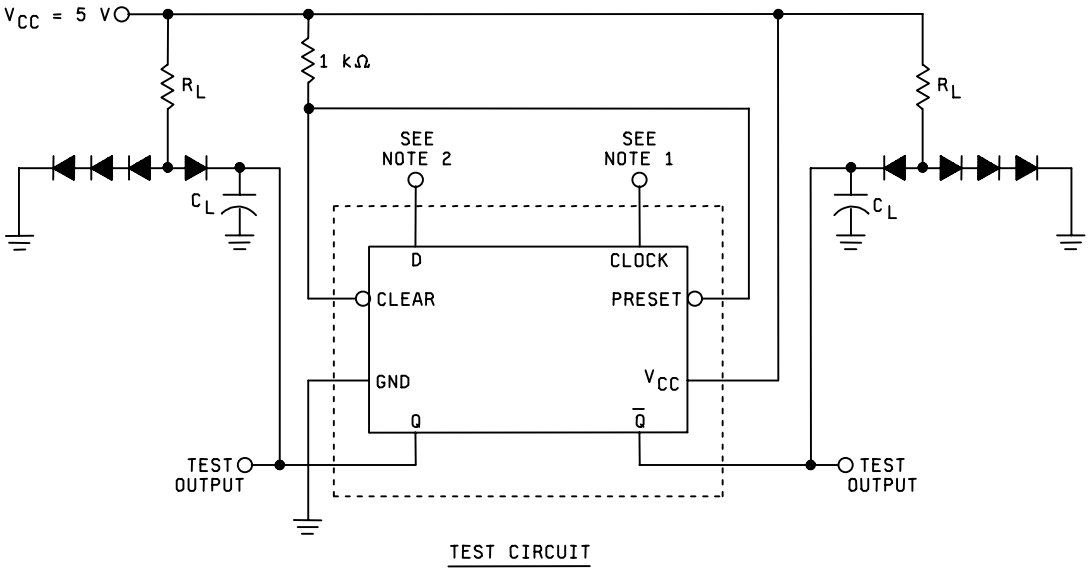
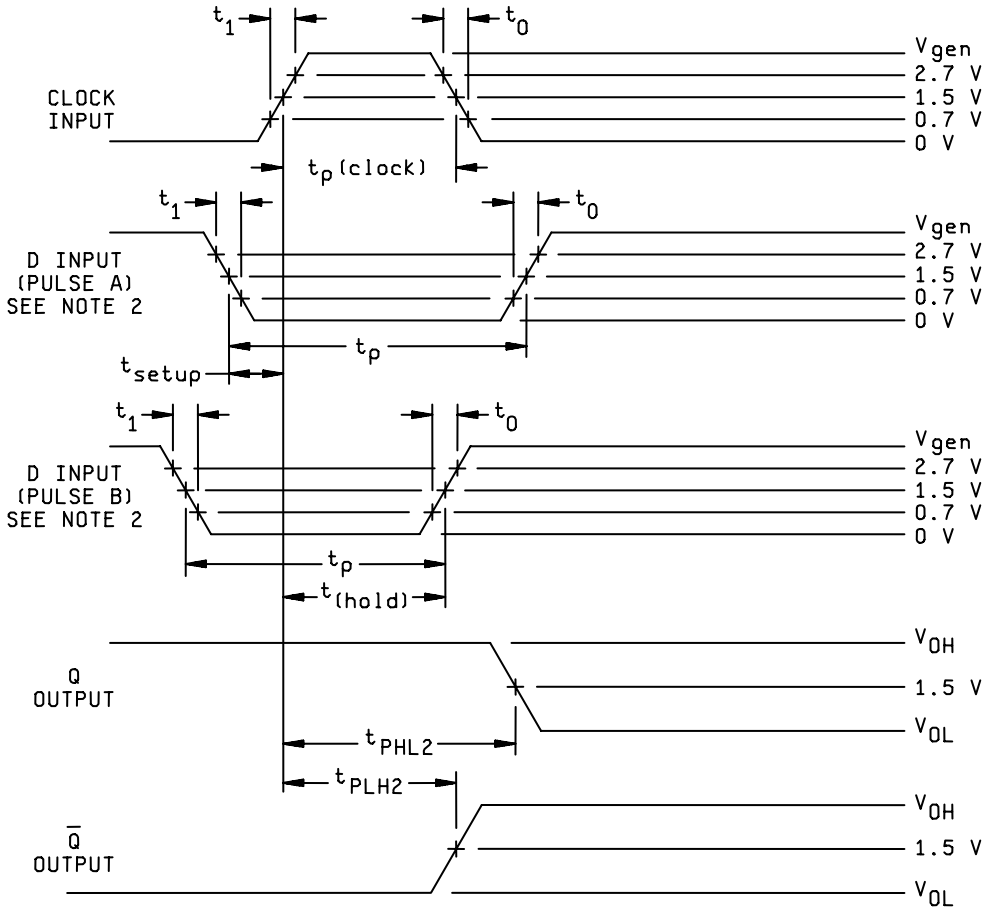


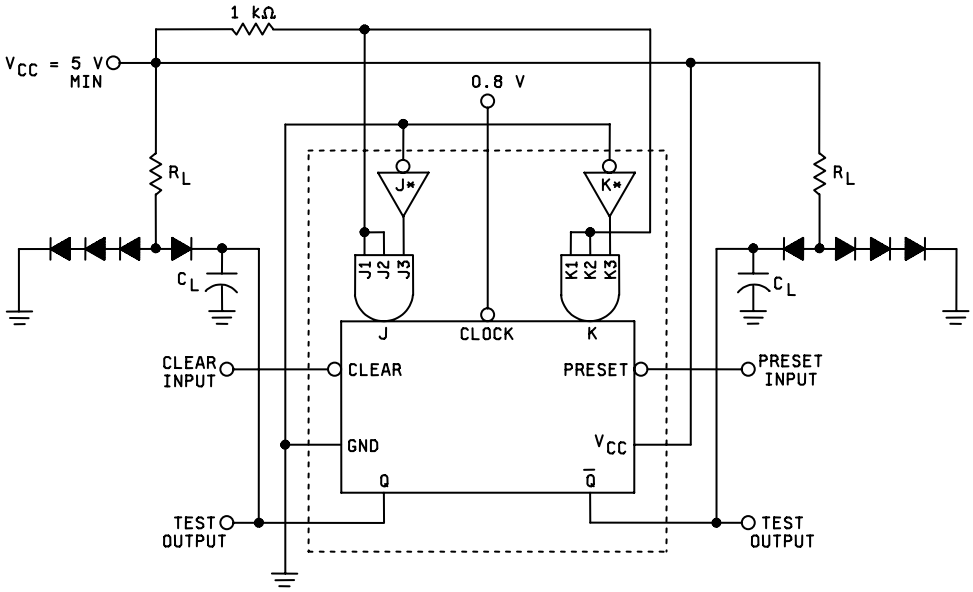
FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07.



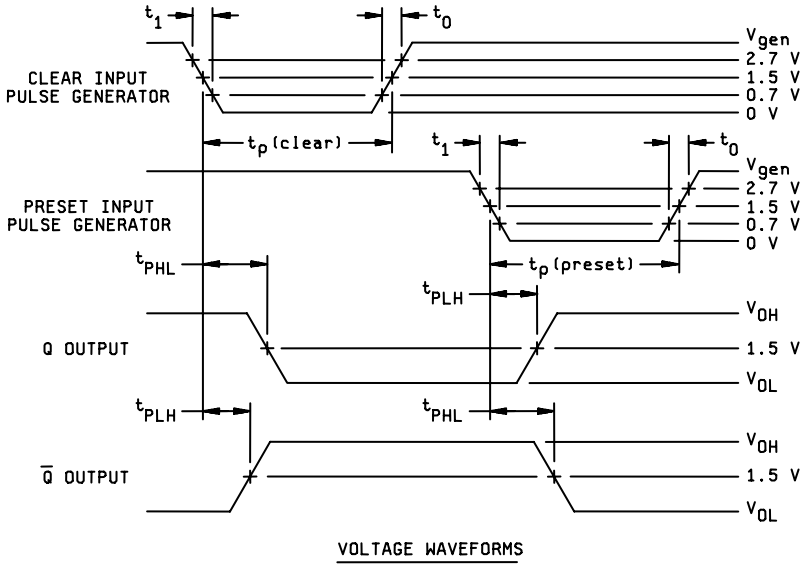
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3 V, $t_o = t_1 < 10$ ns, t_p (clock) = 30 ns, and PRR = 1 MHz.
2. D input (pulse A) has the following characteristics: V_{gen} = 3 V, $t_o = t_1 \leq 10$ ns, t_{SETUP} = 25 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3 V, $t_o = t_1 < 10$ ns, t_{hold} = 6 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF minimum (including jig and probe capacitance).
5. R_L = 390Ω ±5%

FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07 – Continued.



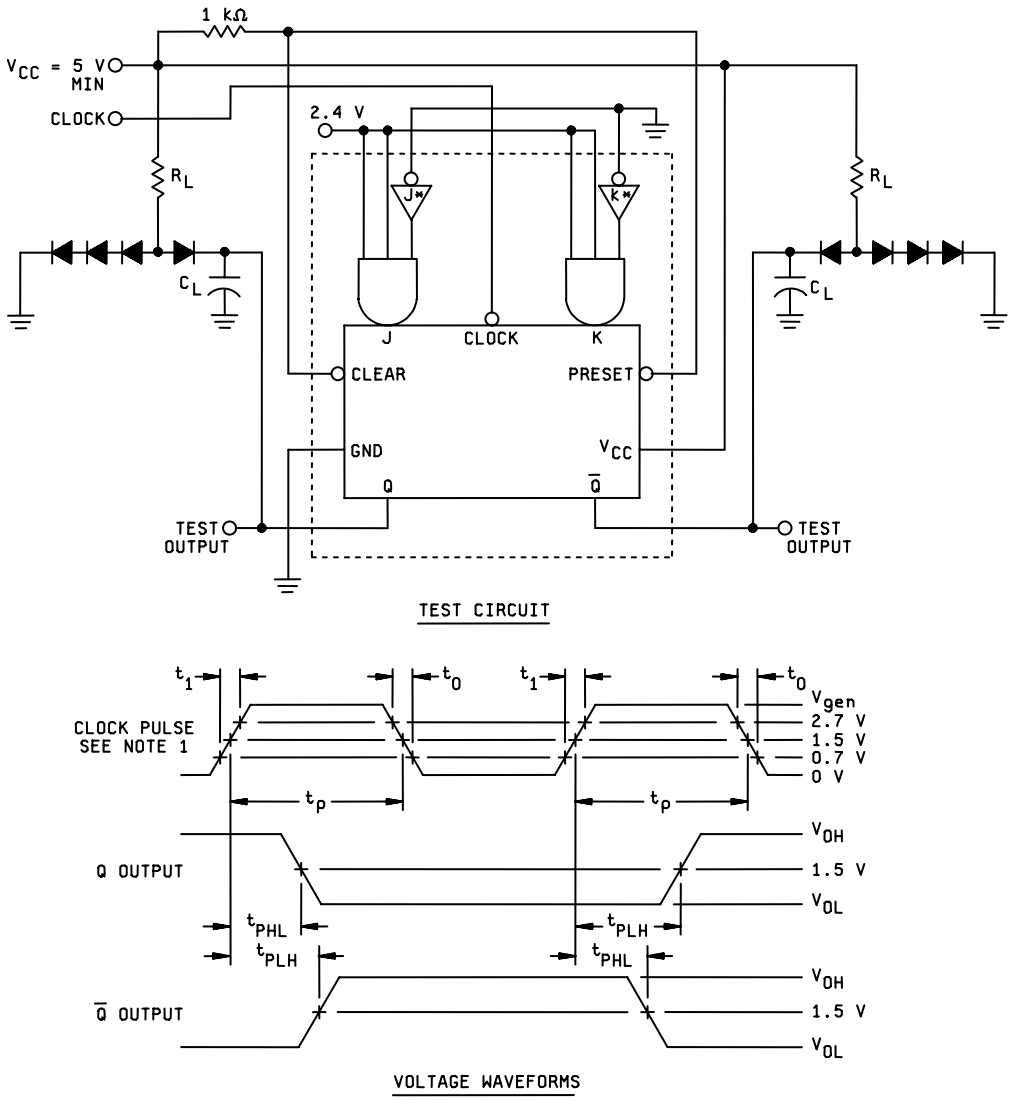
TEST CIRCUIT



VOLTAGE WAVEFORMS

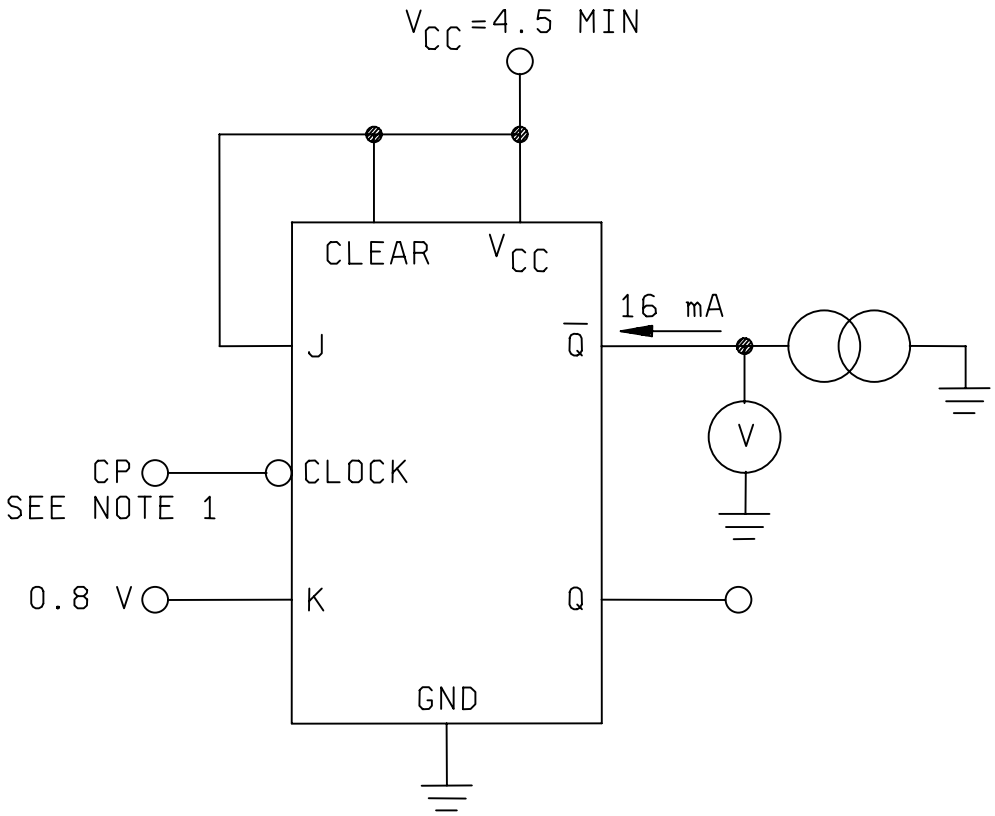
NOTES:
1. Preset or clear function can occur only when clock input is low. Gated inputs are inhibited.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF, minimum, including jig and probe capacitance.
4. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, t_o = 5 ns, $t_1 \leq$ 10 ns, t_p = 25 ns.
5. R_L = 390Ω ±5%.

FIGURE 13. Clear and preset switching test circuit and waveforms for device types 06.



NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{MAX}, PRR = see table III.
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF minimum including jig and probe capacitance.
4. $R_L = 390\Omega \pm 5\%$

FIGURE 14. Synchronous switching test circuit for device type 06.



NOTES:
1. Apply normal clock pulse, then sink -12 mA on the clock input.
2. The output $\overline{Q}$ is measured after -12 mA is applied to the clock to insure it is still in the low state.

FIGURE 15. Input clamp voltage test circuit for device types 01, 02, 03, and 04 (circuit B).

TABLE III. Group A inspection for device type 01. 1/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D Case C Test No.	1 9 K1	2 12 Clock	3 13 Preset	4 14 V_{CC}	5 2 Clear	6 1 NC	7 3 J1	8 4 J2	9 5 J3	10 6 $\overline{Q}$	11 7 GND	12 8 Q	13 10 K2	14 11 K3	Meas. terminal	Test limits Min	 Max	 Unit
1 2/ T_C = 25°C	V_{OH}	3006	1	0.8 V	A		4.5 V			2.0 V	2.0 V	2.0 V		"	-.4 mA	0.8 V	0.8 V	Q	2.4		V
"	"	"	2	2.0 V	A		"			0.8 V	0.8 V	0.8 V	-.4 mA	"		2.0 V	2.0 V	$\overline{Q}$	"		"
"	"	"	3			0.8 V	"	2.0 V						"	-.4 mA			Q	"		"
"	"	"	4			2.0 V	"	0.8 V					-.4 mA	"				$\overline{Q}$	"		"
"	V_{OL}	3007	5	2.0 V	A		"			0.8 V	0.8 V	0.8 V		"	16 mA	2.0 V	2.0 V	Q		0.4	"
"	"	"	6	0.8 V	A		"			2.0 V	2.0 V	2.0 V	16 mA	"		0.8 V	0.8 V	$\overline{Q}$		"	"
"	"	"	7			0.8 V	"	2.0 V					16 mA	"				$\overline{Q}$		"	"
"	"	"	8			2.0 V	"	0.8 V						"	16 mA			Q		"	"
"	V_{IC}	"	9				"			-12 mA				"				J1		-1.5	"
"	"	"	10				"				-12 mA			"				J2		"	"
"	"	"	11				"					-12 mA		"				J3		"	"
"	"	"	12	-12 mA			"							"				K1		"	"
"	"	"	13				"							"		-12 mA		K2		"	"
"	"	"	14				"							"			-12 mA	K3		"	"
"	"	"	15				"	-12 mA						"				Clear		"	"
"	"	"	16			-12 mA	"							"				Preset		"	"
"	"	"	17		-12 mA		"							"				Clock		"	"
"	"	"	17 CKT B	0.8 V	A*		"	4.5 V		4.5 V	4.5 V	4.5 V				0.8 V	0.8 V	Clock		0.5	"
"	I_{IL1}	3009	18	GND	4.5 V		5.5 V	B		0.4 V	4.5 V	4.5 V		"		GND	GND	J1	-0.7	-1.6	mA
"	"	"	19	"	"		"	B		4.5 V	0.4 V	4.5 V		"		GND	GND	J2	"	"	"
"	"	"	20	"	"		"	B		4.5 V	4.5 V	0.4 V		"		GND	GND	J3	"	"	"
"	"	"	21	0.4 V	"	B	"			GND	GND	GND		"		4.5 V	4.5 V	K1	"	"	"
"	"	"	22	4.5 V	"	B	"			GND	GND	GND		"		0.4 V	4.5 V	K2	"	"	"
"	"	"	23	4.5 V	"	B	"			GND	GND	GND		"		4.5 V	0.4 V	K3	"	"	"
"	I_{IL2}	"	24	4.5 V	0.4 V	B	"			4.5 V	4.5 V	4.5 V		"		4.5 V	4.5 V	Clock	-1.4	-3.2	mA
"	I_{IL2}	"	25	"	0.4 V		"	B		"	"	"		"		"	"	Clock	-1.4	-3.2	"
"	I_{IL3}	"	26 CKT A	"	4.5 V	0.4 V	"			"	"	"		"		"	"	Preset	-0.7	-1.6	"
"	"	"	26 CKT B	"	"	0.4 V	"			"	"	"		"		"	"	Preset	-1.4	-3.2	"
"	"	"	27 CKT A	"	"		"	0.4 V		"	"	"		"		"	"	Clear	-0.7	-1.6	"
"	"	"	27 CKT B	"	"		"	0.4 V		"	"	"		"		"	"	Clear	-1.4	-3.2	"
"	I_{IH1}	3010	28		GND		"	GND		2.4 V	GND	GND		"				J1		40	µA
"	"	"	29		"		"	GND		GND	2.4 V	GND		"				J2		"	"
"	"	"	30		"		"	GND		GND	GND	2.4 V		"				J3		"	"
"	"	"	31	2.4 V	"	GND	"							"		GND	GND	K1		"	"
"	"	"	32	GND	"	GND	"							"		2.4 V	GND	K2		"	"
"	"	"	33	GND	"	GND	"							"		GND	2.4 V	K3		"	"
"	I_{IH2}	"	34		"		"	GND		5.5 V	GND	GND		"				J1		100	"
"	"	"	35		"		"	GND		GND	5.5 V	GND		"				J2		"	"
"	"	"	36		"		"	GND		GND	GND	5.5 V		"				J3		"	"
"	"	"	37	5.5 V	"	GND	"							"		GND	GND	K1		"	"
"	"	"	38	GND	"	GND	"							"		5.5 V	GND	K2		"	"
"	"	"	39	GND	"	GND	"							"		GND	5.5 V	K3		"	"
"	I_{IH3}	"	40	4.5 V	A		"	2.4 V		GND	GND	GND		"		4.5 V	4.5 V	Clear		80	"
"	I_{IH3}	"	41	GND	A	2.4 V	"	GND		4.5 V	4.5 V	4.5 V		"		GND	GND	Preset		80	"
"	I_{IH4}	"	42	GND	A	5.5 V	"	GND		4.5 V	4.5 V	4.5 V		"		GND	GND	Preset		200	"
"	"	"	43	4.5 V	A		"	5.5 V		GND	GND	GND		"		4.5 V	4.5 V	Clear		"	"
"	"	"	44	GND	5.5 V		"	GND		GND	GND	GND		"		GND	GND	Clock		"	"
"	"	"	45	GND	5.5 V	GND	"			GND	GND	GND		"		GND	GND	Clock		"	"

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11				
			Test No.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3		Min	Max	Unit
1	I_{IH5}	3010	46 CKT A	GND	2.4 V		5.5 V	GND		GND	GND	GND		GND		GND	GND	Clock	-50	-700	µA
T_C = 25°C	"	"	46 CKT B	"	"		"	GND		"	"	"		"		"	"	"	-200	-850	"
"	"	"	46 CKT C	"	"		"	GND		"	"	"		"		"	"	"	-400	-1000	"
"	"	"	47 CKT A	"	"	GND	"			"	"	"		"		"	"	"	-50	-700	"
"	"	"	47 CKT B	"	"	GND	"			"	"	"		"		"	"	"	-200	-850	"
"	"	"	47 CKT C	"	"	GND	"			"	"	"		"		"	"	"	-400	-1000	"
"	I_{OS}	3011	48	4.5 V	GND	GND	5.5 V			4.5 V	4.5 V	4.5 V		"		4.5 V	4.5 V	Q	-20	-57	mA
"	I_{OS}	3011	49	4.5 V	"		"	GND		4.5 V	4.5 V	4.5 V	GND	"		4.5 V	4.5 V	$\overline{Q}$	-20	-57	"
"	I_{CC}	3005	50	GND	"	GND	"			GND	GND	GND		"		GND	GND	V_{CC}		20	"
"	I_{CC}	3005	51	GND	"		"	GND		GND	GND	GND		"		GND	GND	V_{CC}		20	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				
7 2/ 4			52	B	B	A	4.5 V	B	B	B	B	B	H 3/	GND	L 3/	B	B	All	H or L		
T_C = 25°C			53	B	B	B	"	A	B	B	B	B	L	"	H	B	B	output	as shown 3/		
			54	B	B	A	"	A	B	B	B	B	L	"	H	A	A	"	"		
"			55	B	A	A	"	A	B	B	B	B	L	"	H	A	A	"	"		
"			56	B	B	A	"	A	B	B	B	B	L	"	H	A	A	"	"		
"			57	A	B	A	"	A	B	B	B	B	L	"	H	B	A	"	"		
"			58	A	A	A	"	A	B	B	B	B	L	"	H	B	A	"	"		
"			59	A	B	A	"	A	B	B	B	B	L	"	H	B	A	"	"		
"			60	A	B	A	"	A	B	B	B	B	L	"	H	A	B	"	"		
"			61	A	A	A	"	A	B	B	B	B	L	"	H	A	B	"	"		
"			62	A	B	A	"	A	B	B	B	B	L	"	H	A	B	"	"		
"			63	A	B	A	"	B	B	B	B	B	H	"	L	A	B	"	"		
"			64	B	B	A	"	A	B	B	A	A	H	"	L	B	B	"	"		
"			65	B	A	A	"	A	B	B	A	A	H	"	L	B	B	"	"		
"			66	B	B	A	"	A	B	B	A	A	H	"	L	B	B	"	"		
"			67	B	B	A	"	A	B	A	B	A	H	"	L	B	B	"	"		
"			68	B	A	A	"	A	B	A	B	A	H	"	L	B	B	"	"		
"			69	B	B	A	"	A	B	A	B	A	H	"	L	B	B	"	"		
"			70	B	B	A	"	A	B	A	A	B	H	"	L	B	B	"	"		
"			71	B	A	A	"	A	B	A	A	B	H	"	L	B	B	"	"		
"			72	B	B	A	"	A	B	A	A	B	H	"	L	B	B	"	"		
"			73	A	B	A	"	A	B	A	A	A	H	"	L	A	A	"	"		
"			74	A	A	A	"	A	B	A	A	A	H	"	L	A	A	"	"		
"			75	A	B	A	"	A	B	A	A	A	L	"	H	A	A	"	"		
"			76	A	A	A	"	A	B	A	A	A	L	"	H	A	A	"	"		
"			77	A	B	A	"	A	B	A	A	A	H	"	L	A	A	"	"		
"			78	A	B	A	"	B	B	A	A	A	H	"	L	A	A	"	"		
"			79	A	A	A	"	B	B	A	A	A	H	"	L	A	A	"	"		
"			80	A	B	A	"	B	B	A	A	A	H	"	L	A	A	"	"		
"			81	A	B	B	"	B	B	A	A	A	H	"	H	A	A	"	"		
"			82	A	A	B	"	B	B	A	A	A	H	"	H	A	A	"	"		
"			83	A	B	B	"	B	B	A	A	A	H	"	H	A	A	"	"		
"			84	A	A	B	"	A	B	A	A	A	L	"	H	A	A	"	"		
"			85	A	A	A	"	A	B	A	A	A	L	"	H	A	A	"	"		
"			86	B	A	A	"	A	B	A	A	A	L	"	H	A	A	"	"		
"			87	B	A	A	"	A	B	B	A	A	L	"	H	A	A	"	"		
"			88	B	B	A	"	A	B	B	A	A	H	"	L	A	A	"	"		
"			89	A	A	A	"	A	B	A	A	A	H	"	L	A	A	"	"		
"			90	A	A	A	"	A	B	B	A	A	H	"	L	A	A	"	"		

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11				
			Test No.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3		Min	Max	Unit
7 2/ 4/			91	B	A	A	4.5 V	A	B	B	A	A	H	GND	L	A	A	All output	H or L As shown 3/		
T_C = 25°C			92	B	B	A	4.5 V	A	B	B	A	A	L	GND	H	A	A				
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125 and -55°C.																				
9	F_{MAX} 5/	(Fig. 5)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	10		MHz
T_C = 25°C	F_{MAX} 5/	(Fig. 5)	94	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	$\overline{Q}$	10		MHz
"	t_{PLH1}	3003	95	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to Q	5	25	ns
"	t_{PLH1}	(Fig. 4)	96	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to Q	"	25	"
"	t_{PHL1}	"	97	"	"	J	"	IN		"	"	"		"	OUT	"	"	Clear to Q	"	40	"
"	t_{PHL1}	"	98	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	40	"
"	t_{PLH2}	3003 (Fig 5	99	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	30	ns
"	t_{PLH2}	"	100	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	30	"
"	t_{PHL2}	"	101	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	40	"
"	t_{PHL2}	"	102	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q		40	"
10	F_{MAX} 5/	(Fig 5)	103	"	"	"	"	"		"	"	"		"	OUT	"	"	Q	10		MHz
T_C = 125°C	F_{MAX} 5/	(Fig 5)	104	"	"	"	"	"		"	"	"	OUT	"		"	"	$\overline{Q}$	10		MHz
"	t_{PLH1}	3003 (Fig. 4)	105	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to $\overline{Q}$	5	39	ns
"	t_{PLH1}	"	106	"	"	IN	"	J		"	"	"		"	OUT	"	"	Preset to Q	"	39	"
"	t_{PHL1}	"	107	"	"	J	"	IN		"	"	"			OUT	"	"	Clear to Q	"	50	"
"	t_{PHL1}	"	108	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	50	"
"	t_{PLH2}	(Fig 5)	109	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	39	ns
"	t_{PLH2}	"	110	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	39	"
"	t_{PHL2}	"	111	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	50	"
"	t_{PHL2}	"	112	"	"	"	"	"		"		"		"	OUT	"	"	Clock to Q	"	50	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

NOTES:

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
J = Input pulse t_p = 100 ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V

*After clock pulse apply –12 mA to clock pin to insure $\overline{Q}$ is still in the low state (see figure 15).

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A= 2.0 volts minimum and B = 0.8 volts maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double camparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test No.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}_2$	Q2	K2	GND	Q1	$\overline{Q}_1$	J1		Min	Max	Unit
1	V_{OH}	3006	1	A		0.8 V	4.5 V							GND	-.4 mA		2.0 V	Q	2.4		V
T_C = 25°C	"	"	2	A		2.0 V	"							"		-.4 mA	0.8 V	$\overline{Q}_1$	"		"
"	"	"	3		0.8 V		"							"		-.4 mA		$\overline{Q}_1$	"		"
"	"	"	4				"	A		2.0 V		-.4 mA	0.8 V	"				Q2	"		"
"	"	"	5				"	A		0.8 V	-.4 mA		2.0 V	"				$\overline{Q}_2$	"		"
"	"	"	6				"		0.8 V		-.4 mA			"				$\overline{Q}_2$	"		"
"	V_{OL}	3007	7	A		2.0 V	"							"	16 mA		0.8 V	Q1		0.4	"
"	"	"	8	A		0.8 V	"							"		16 mA	2.0 V	$\overline{Q}_1$		"	"
"	"	"	9		0.8 V		"							"	16 mA			Q1		"	"
"	"	"	10				"	A		0.8 V		16 mA	2.0 V	"				Q2		"	"
"	"	"	11				"	A		2.0 V	16 mA		0.8 V	"				$\overline{Q}_2$		"	"
"	"	"	12				"		0.8 V			16 mA		"				Q2		"	"
"	V_{IC}		13				"							"			-12 mA	J1		-1.5	"
"	"		14				"			-12 mA				"				J2		"	"
"	"		15			-12 mA	"							"				K1		"	"
"	"		16				"						-12 mA	"				K2		"	"
"	"		17		-12 mA		"							"				Clear 1		"	"
			18	-12 mA			"							"				Clock 1		"	
"	"		18 CKT B	A*	4.5 V	0.8 V	"							"			4.5 V	Clock 1		-0.5	"
"	"		19				"		-12 mA					"				Clear 2		-1.5	"
"	"		20				"	-12 mA						"				Clock 2		-1.5	"
"	"		20 CKT B				"	A*	4.5 V	4.5 V			0.8 V	"				Clock 2		-0.5	
"	I_{IL1}	3009	21	5/	4.5 V		5.5 V							"			0.4 V	J1	-0.7	-1.6	mA
"	"	"	22	5/	4.5 V	0.4 V	"							"				K1	"	"	"
"	"	"	23				"	5/	4.5 V	0.4 V				"				J2	"	"	"
"	"	"	24				"	5/	4.5 V				0.4 V	"				K2	"	"	"
"	I_{IL2}	"	25	0.4 V	B	4.5 V	"							"			4.5 V	Clock 1	-1.4	-3.2	"
"	I_{IL2}	"	26				"	0.4 V	B	4.5 V			4.5 V	"				Clock 2	-1.4	-3.2	"
"	I_{IL3}	"	27 CKT A, C	4.5 V	0.4 V		"							"			4.5 V	Clear 1	-0.7	-1.6	"
"	"	"	27 CKT B	4.5 V	0.4 V		"							"			4.5 V	Clear 1	-1.4	-3.2	"
"	"	"	28 CKT A, C				"	4.5 V	0.4 V	4.5 V				"				Clear 2	-0.7	-1.6	"
"	"	"	28 CKT B				"	4.5 V	0.4 V	4.5 V				"				Clear 2	-1.4	-3.2	"
"	I_{IH1}	3010	29	GND	GND		5.5 V							"			2.4 V	J1		40	µA
"	"	"	30	GND	B	2.4 V	"							"				K1		"	"
"	"	"	31				"	GND	GND	2.4 V				"				J2		"	"
"	"	"	32				"	GND	B				2.4 V	"				K2		"	"
"	I_{IH2}	"	33	GND	GND		"							"			5.5 V	J1		100	"
"	"	"	34	GND	B	5.5 V	"							"				K1		"	"
"	"	"	35				"	GND	GND	5.5 V				"				J2		"	"
"	"	"	36				"	GND	B				5.5 V	"				K2		"	"
"	I_{IH3} 7/	"	37	GND	E		"							"			GND	Clear 1		80	"
"	I_{IH3} 7/	"	38				"	GND	E	GND				"				Clear 2		80	"
"	I_{IH4}	"	39	5.5 V	5.5 V	GND	"							"			GND	Clock 1		200	"
"	"	"	40	GND	E		"							"			GND	Clear 1		"	"
"	"	"	41				"	5.5 V	5.5 V	GND			GND	"				Clock 2		"	"
"	"	"	42				"	GND	F	GND				"				Clear 2		"	"
"	I_{IH5}	"	43 CKT A, C	2.4 V	E	GND	"							"			GND	Clock 1	-50	-700	"
"	"	"	43 CKT B	2.4 V	2.4 V	GND	"							"			GND	Clock 1	-200	-850	"
"	"	"	44 CKT A, C				"	2.4 V	E	GND			GND	"				Clock 2	-50	-700	"
"	"	"	44 CKT B				"	2.4 V	2.4 V	GND			GND	"				Clock 2	-200	-850	"

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test No.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}_2$	Q2	K2	GND	Q1	$\overline{Q}_1$	J1		Min	Max	Unit
1 T_C = 25°C	I_{OS}	3011	45	2.4 V	GND	2.4 V	5.5 V							GND		GND	2.4 V	$\overline{Q}_1$	-20	-57	mA
"	"	3011**	46	A	4.5 V	0	"							"	GND		4.5 V	Q1	"	"	"
"	"	3011**	47				"	GND	4.5 V	4.5 V		GND	0 V	"				Q2	"	"	"
"	"	3011	48				"	2.4 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q}_2$	"	"	"
"	I_{CC}	3005	49	D	4.5 V	GND	"	D	4.5 V	4.5 V			GND	"			4.5 V	V_{CC}		40	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				
7 2/ 4/ T_C = 25°C			50	B	B	B	4.5 V	B	B	A	H 3/	L 3/	B	GND	L 3/	H 3/	A	All output	H or L as shown 3/		
			51	A	B	B	"	A	B	A	H	L	B	"	L	H	A				
			52	B	B	B	"	B	B	A	H	L	B	"	L	H	A	"	"		
"			53	B	B	A	"	B	B	A	H	L	A	"	L	H	A	"	"		
"			54	A	B	A	"	A	B	A	H	L	A	"	L	H	A	"	"		
"			55	B	B	A	"	B	B	A	H	L	A	"	L	H	A	"	"		
"			56	B	A	A	"	B	A	A	H	L	A	"	L	H	A	"	"		
"			57	A	A	A	"	A	A	A	H	L	A	"	L	H	A	"	"		
"			58	B	A	A	"	B	A	A	L	H	A	"	H	L	A	"	"		
"			59	A	A	A	"	A	A	A	L	H	A	"	H	L	A	"	"		
"			60	B	A	A	"	B	A	A	H	L	A	"	L	H	A	"	"		
"			61	A	A	A	"	A	A	A	H	L	A	"	L	H	A	"	"		
"			62	B	A	A	"	B	A	A	L	H	A	"	H	L	A	"	"		
"			63	B	A	B	"	B	A	B	L	H	B	"	H	L	B	"	"		
"			64	A	A	B	"	A	A	B	L	H	B	"	H	L	B	"	"		
"			65	B	A	B	"	B	A	B	L	H	B	"	H	L	B	"	"		
"			66	B	B	B	"	B	B	B	H	L	B	"	L	H	B	"	"		
"			67	B	A	B	"	B	A	B	H	L	B	"	L	H	B	"	"		
"			68	A	A	B	"	A	A	B	H	L	B	"	L	H	B	"	"		
"			69	B	A	B	"	B	A	B	H	L	B	"	L	H	B	"	"		
"			70	B	A	B	"	B	A	A	H	L	B	"	L	H	A	"	"		
"			71	A	A	B	"	A	A	A	H	L	B	"	L	H	A	"	"		
"			72	B	A	B	"	B	A	A	L	H	B	"	H	L	A	"	"		
"			73	B	A	A	"	B	A	B	L	H	A	"	H	L	B	"	"		
"			74	A	A	A	"	A	A	B	L	H	A	"	H	L	B	"	"		
"			75	B	A	A	"	B	A	B	H	L	A	"	L	H	B	"	"		
"			76	A	B	A	"	A	B	A	H	L	A	"	L	H	A	"	"		
"			77	A	A	A	"	A	A	A	H	L	A	"	L	H	A	"	"		
"			78	A	A	A	"	A	A	B	H	L	A	"	L	H	B	"	"		
"			79	A	A	B	"	A	A	B	H	L	B	"	L	H	B	"	"		
"			80	B	A	B	"	B	A	B	L	H	B	"	H	L	B	"	"		
"			81	A	A	A	"	A	A	A	L	H	A	"	H	L	A	"	"		
"			82	A	A	B	"	A	A	A	L	H	B	"	H	L	A	"	"		
"			83	A	A	B	"	A	A	B	L	H	B	"	H	L	B	"	"		
"			84	B	A	B	"	B	A	B	H	L	B	"	L	H	B	"	"		
"			85	A	A	B	"	A	A	A	H	L	B	"	L	H	A	"	"		
"			86	B	A	B	"	B	A	A	L	H	B	"	H	L	A	"	"		
"			87	A	A	B	"	A	A	A	L	H	B	"	H	L	A	"	"		
"			88	A	B	B	"	A	B	A	H	L	B	"	L	H	A	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55°C.																				

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test No.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}_2$	Q2	K2	GND	Q1	$\overline{Q}_1$	J1		Min	Max	Unit
9	F_{MAX} 6/	(Fig 7)	89	IN		2.4 V	5.0 V							GND	OUT		2.4 V	Q_1	10		MHz
T_C = 25°C	"	"	90	IN		2.4 V	"							"		OUT	2.4 V	$\overline{Q}_1$	"		"
"	"	"	91				"	IN		2.4 V		OUT	2.4 V	"				Q_2	"		"
"	"	"	92				"	IN		2.4 V	OUT		2.4 V	"				$\overline{Q}_2$	"		"
"	t_{PLH1}	3003 (Fig 6)	93	IN	IN	GND	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}_1$	5	25	"
"	t_{PLH1}	"	94				"	IN	IN	2.4 V	OUT		GND	"				Clear 2 to $\overline{Q}_2$	"	25	"
"	t_{PHL1}	"	95	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	"	40	"
"	t_{PHL1}	"	96				"	IN	IN	2.4 V		OUT	GND	"				Clear 2 to Q2	"	40	"
"	t_{PLH2}	3003 (Fig 7)	97	IN	5.0 V	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	30	"
"	"	"	98	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}_1$	"	"	"
"	"	"	99				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	100				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}_2$	"	"	"
"	t_{PHL2}	"	101	IN	5.0 V	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	40	"
"	"	"	102	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}_1$	"	"	"
"	"	"	103				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	104				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}_2$	"	"	"
10	F_{MAX} 6/	(Fig 7)	105	IN		2.4 V	"							"	OUT		2.4 V	Q1	10		MHz
T_C = 125°C	"	"	106	IN		2.4 V	"							"		OUT	2.4 V	$\overline{Q}_1$	"		"
"	"	"	107				"	IN		2.4 V		OUT	2.4 V	"				Q2	"		"
"	"	"	108				"	IN		2.4 V	OUT		2.4 V	"				$\overline{Q}_2$	"		"
"	t_{PLH1}	3003 (Fig 6)	109	IN	IN	GND	"							"		OUT	2.4 V	Clear 1 to $\overline{Q}_1$	5	39	ns
"	t_{PLH1}	"	110				"	IN	IN	2.4 V	OUT		GND	"				Clear 2 to $\overline{Q}_2$	"	39	"
"	t_{PHL1}	"	111	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	"	50	"
"	t_{PHL1}	"	112				"	IN	IN	2.4 V		OUT	GND	"				Clear 2 to Q2	"	50	"
"	t_{PLH2}	3003 (Fig 7)	113	IN	5.0 V	2.4 V	"							"	OUT		2.4 V	Clock 1 to Q1	"	39	"
"	"	"	114	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}_1$	"	"	"
"	"	"	115				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	116				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}_2$	"	"	"

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
			Test No.	Clock 1	Clear 1	K1	V_{CC}	Clock 2	Clear 2	J2	$\overline{Q}_2$	Q2	K2	GND	Q1	$\overline{Q}_1$	J1		Min	Max	Unit
10 T_C = 125°C	t_{PHL2}	3003	117	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Clock 1 to Q1	5	50	ns
"	"	"	118	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1 to $\overline{Q}_1$	"	"	"
"	"	"	119				"	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	120				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}_2$	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This note has been deleted.
D = Momentary 4.5 V, then GND.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.
J = This note has been deleted.

* After clock pulse apply –12 mA to clock pin to insure $\overline{Q}$ is still in the low state (see figure 15).

** Test time limit ≤ 100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open.)
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Input shall be one normal clock pulse, then 4.5 V
6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall ge one-half of the input frequency.
7/ For CKT A, I_{IH3} limits are 0 to 120 μA.

TABLE III. Group A inspection for device type 03. 1/

Subgroup	Symbol	MIL-STD-883 method	Case C Test No.	1 J1	2 $\overline{Q}_1$	3 Q1	4 K1	5 Q2	6 $\overline{Q}_2$	7 GND	8 J2	9 Clock 2	10 Clear 2	11 K2	12 Clock 1	13 Clear 1	14 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_C = 25°C	V_{OH}	3006	1	2.0 V		-.4 mA	0.8 V			GND					A		4.5 V	Q1	2.4		V
"	"	"	2	0.8 V	-.4 mA		2.0 V			"					A		"	$\overline{Q}_1$	"		"
"	"	"	3		-.4 mA					"						0.8 V	"	$\overline{Q}_1$	"		"
"	"	"	4					-.4 mA		"	2.0 V	A		0.8 V				Q2	"		"
"	"	"	5						-.4 mA	"	0.8 V	A		2.0 V			"	$\overline{Q}_2$	"		"
"	"	"	6						-.4 mA	"			0.8 V					$\overline{Q}_2$	"		"
"	V_{OL}	3007	7	0.8 V		16 mA	2.0 V			"					A		"	Q1		0.4	"
"	"	"	8	2.0 V	16 mA		0.8 V			"					A			$\overline{Q}_1$		"	"
"	"	"	9			16 mA				"						0.8 V	"	Q1		"	"
"	"	"	10					16 mA		"	0.8 V	A		2.0 V				Q2		"	"
"	"	"	11						16 mA	"	2.0 V	A		0.8 V			"	$\overline{Q}_2$		"	"
"	"	"	12					16 mA		"			0.8 V					Q2		"	"
"	V_{IC}		13	-12 mA						"							"	J1		-1.5	"
"	"		14				-12 mA			"								K1		"	"
"	"		15							"	-12 mA						"	J2		"	"
"	"		16							"				-12 mA				K2		"	"
"	"		17							"						-12 mA	"	Clear 1		"	"
"			18							"					-12 mA			Clock 1		"	"
"	"		18 CKT B	4.5 V			0.8 V			"					A*	4.5 V	"	Clock 1		-0.5	"
"	"		19							"			-12 mA					Clear 2		-1.5	"
"	"		20							"		-12 mA					"	Clock 2		-1.5	"
"	"		20 CKT B							"	4.5 V	A*	4.5 V	0.8 V			"	Clock 2		-0.5	"
"	I_{IL1}	3009	21	0.4 V						"					5/	4.5 V	5.5 V	J1	-0.7	-1.6	mA
"	"	"	22				0.4 V			"					5/	4.5 V	"	K1	"	"	"
"	"	"	23							"	0.4 V	5/	4.5 V				"	J2	"	"	"
"	"	"	24							"		5/	4.5 V	0.4 V			"	K2	"	"	"
"	I_{IL2}	"	25	4.5 V			4.5 V			"					0.4 V	B	"	Clock 1	-1.25	-3.2	"
"	I_{IL2}	"	26							"	4.5 V	0.4 V	B	4.5 V			"	Clock 2	-1.25	-3.2	"
"	I_{IL3}	"	27 CKT A, C	4.5 V						"					4.5 V	0.4 V	"	Clear 1	-0.7	-1.6	"
"	"	"	27 CKT B	4.5 V						"					4.5 V	0.4 V	"	Clear 1	-1.4	-3.2	"
"	"	"	28 CKT A, C							"	4.5 V	4.5 V	0.4 V				"	Clear 2	-0.7	-1.6	"
"	"	"	28 CKT B							"	4.5 V	4.5 V	0.4 V				"	Clear 2	-1.4	-3.2	"
"	I_{IH1}	3010	29	2.4 V						"					GND	GND	"	J1		40	µA
"	"	"	30				2.4 V			"					GND	B	"	K1		"	"
"	"	"	31							"	2.4 V	GND	GND				"	J2		"	"
"	"	"	32							"		GND	B	2.4 V			"	K2		"	"
"	I_{IH2}	"	33	5.5 V						"					GND	GND	"	J1		100	"
"	"	"	34				5.5 V			"					GND	B	"	K1		"	"
"	"	"	35							"	5.5 V	GND	GND				"	J2		"	"
"	"	"	36							"		GND	B	5.5 V			"	K2		"	"
"	I_{IH3} 7/	"	37	GND						"					GND	E	"	Clear 1		80	"
"	I_{IH3} 7/	"	38							"	GND	GND	E				"	Clear 2		80	"
"	I_{IH4}	"	39	GND			GND			"					5.5 V	GND	"	Clock 1		200	"
"	"	"	40	GND						"					GND	F	"	Clear 1		"	"
"	"	"	41							"	GND	5.5 V	GND	GND			"	Clock 2		"	"
"	"	"	42							"	GND	GND	F				"	Clear 2		"	"
"	I_{IH5}	"	43 CKT A, C	GND			GND			"					2.4 V	GND	"	Clock 1	-50	-700	"
"	"	"	43 CKT B	GND			GND			"					2.4 V	GND	"	Clock 1	-200	-850	"
"	"	"	44 CKT A, C							"	GND	2.4 V	GND	GND			"	Clock 2	-50	-700	"
"	"	"	44 CKT B							"	GND	2.4 V	GND	GND			"	Clock 2	-80	-850	"

See notes at end of device type 03.

TABLE III. Group A inspection for device type 03. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case C Test No.	1 J1	2 $\overline{Q}_1$	3 Q1	4 K1	5 Q2	6 $\overline{Q}_2$	7 GND	8 J2	9 Clock 2	10 Clear 2	11 K2	12 Clock 1	13 Clear 1	14 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1	I_{OS}	3011	45	2.4 V	GND		2.4 V			"					2.4 V	GND	5.5 V	$\overline{Q}$ 1	-20	-57	mA
T_C = 25°C	"	3011 *	46	4.5 V	GND	GND	0 V			"					A	4.5 V	"	Q1	"		"
"	"	3011 *	47					GND	GND	"	4.5 V	A	4.5 V	2.4 V			"	Q2	"		"
"	"	3011	48						GND	"	2.4 V	2.4 V	GND	0 V				$\overline{Q}$ 2	"		"
"	I_{CC}	3005	49	4.5 V			GND			"	4.5 V	D	4.5 V	GND	D	4.5 V	"	V_{CC}		40	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				
7 2/ 4			50	A	H 3/	L 3/	B	L 3/	H 3/	GND	A	B	B	B	B	B	4.5 V	All	H or L		
T_C = 25°C			51	A	H	L	B	L	H	"	A	A	B	B	A	B	"	output	as shown 3/		
"			52	A	H	L	B	L	H	"	A	B	B	B	B	B	"	"	"		
"			53	A	H	L	A	L	H	"	A	B	B	A	B	B	"	"	"		
"			54	A	H	L	A	L	H	"	A	A	B	A	A	B	"	"	"		
"			55	A	H	L	A	L	H	"	A	B	B	A	B	B	"	"	"		
"			56	A	H	L	A	L	H	"	A	B	A	A	B	A	"	"	"		
"			57	A	H	L	A	L	H	"	A	A	A	A	A	A	"	"	"		
"			58	A	L	H	A	H	L	"	A	B	A	A	B	A	"	"	"		
"			59	A	L	H	A	H	L	"	A	A	A	A	A	A	"	"	"		
"			60	A	H	L	A	L	H	"	A	B	A	A	B	A	"	"	"		
"			61	A	H	L	A	L	H	"	A	A	A	A	A	A	"	"	"		
"			62	A	L	H	A	H	L	"	A	B	A	A	B	A	"	"	"		
"			63	B	L	H	B	H	L	"	B	B	A	B	B	A	"	"	"		
"			64	B	L	H	B	H	L	"	B	A	A	B	A	A	"	"	"		
"			65	B	L	H	B	H	L	"	B	B	A	B	B	A	"	"	"		
"			66	B	H	L	B	L	H	"	B	B	B	B	B	B	"	"	"		
"			67	B	H	L	B	L	H	"	B	B	A	B	B	A	"	"	"		
"			68	B	H	L	B	L	H	"	B	A	A	B	A	A	"	"	"		
"			69	B	H	L	B	L	H	"	B	B	A	B	B	A	"	"	"		
"			70	A	H	L	B	L	H	"	A	B	A	B	B	A	"	"	"		
"			71	A	H	L	B	L	H	"	A	A	A	B	A	A	"	"	"		
"			72	A	L	H	B	H	L	"	A	B	A	B	B	A	"	"	"		
"			73	B	L	H	A	H	L	"	B	B	A	A	B	A	"	"	"		
"			74	B	L	H	A	H	L	"	B	A	A	A	A	A	"	"	"		
"			75	B	H	L	A	L	H	"	B	B	A	A	B	A	"	"	"		
"			76	A	H	L	A	L	H	"	A	A	B	A	A	B	"	"	"		
"			77	A	H	L	A	L	H	"	A	A	A	A	A	A	"	"	"		
"			78	B	H	L	A	L	H	"	B	A	A	A	A	A	"	"	"		
"			79	B	H	L	B	L	H	"	B	A	A	B	A	A	"	"	"		
"			80	B	L	H	B	H	L	"	B	B	A	B	B	A	"	"	"		
"			81	A	L	H	A	H	L	"	A	A	A	A	A	A	"	"	"		
"			82	A	L	H	B	H	L	"	A	A	A	B	A	A	"	"	"		
"			83	B	L	H	B	H	L	"	B	A	A	B	A	A	"	"	"		
"			84	B	H	L	B	L	H	"	B	B	A	B	B	A	"	"	"		
"			85	A	H	L	B	L	H	"	A	A	A	B	A	A	"	"	"		
"			86	A	L	H	B	H	L	"	A	B	A	B	B	A	"	"	"		
"			87	A	L	H	B	H	L	"	A	A	A	B	A	A	"	"	"		
"			88	A	H	L	B	L	H	"	A	A	B	B	A	B	"	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55°C.																				

See notes at end of device type 03.

TABLE III. Group A inspection for device type 03. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case C Test No.	1 J1	2 $\overline{Q}_1$	3 Q1	4 K1	5 Q2	6 $\overline{Q}_2$	7 GND	8 J2	9 Clock 2	10 Clear 2	11 K2	12 Clock 1	13 Clear 1	14 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
9 T_C = 25°C	F_{MAX}	(Fig. 7) 6/	89	2.4 V		OUT	2.4 V			GND					IN	5.0 V	5.0 V	Q1	10		MHz
"	"	"	90	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	$\overline{Q}_1$	"		"
"	"	"	91					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Q2	"		"
"	"	"	92						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	$\overline{Q}_2$	"		"
"	t_{PLH}	3003 (Fig. 6)	93	2.4 V	OUT		GND			"					A	IN	"	Clr 1 to $\overline{Q}_1$	5	25	ns
"	t_{PLH}	"	94						OUT	"	2.4 V	A	IN	GND			"	Clr 2 to $\overline{Q}_2$	"	25	"
"	t_{PHL}	"	95	2.4 V		OUT	GND			"					A	IN	"	Clr 1 to Q1	"	40	"
"	t_{PHL}	"	96					OUT		"	2.4 V	A	IN	GND			"	Clr 2 to Q2	"	40	"
"	t_{PLH}	3003 (Fig. 7)	97	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	5	30	ns
"	"		98	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to $\overline{Q}_1$	"	"	"
"	"	"	99					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
"	"	"	100						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to $\overline{Q}_2$	"	"	"
"	t_{PHL}	"	101	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	"	40	"
"	"	"	102	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to $\overline{Q}_1$	"	"	"
"	"	"	103					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
"	"	"	104						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to $\overline{Q}_2$	"	"	"
10 T_C = 125°C	F_{MAX}	(Fig. 7) 6/	105	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Q1	10		MHz
"	"	"	106	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	$\overline{Q}_1$	"		"
"	"	"	107					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Q2	"		"
"	"	"	108						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	$\overline{Q}_2$	"		"
"	t_{PLH}	3003 (Fig 6)	109	2.4 V	OUT		GND			"					A	IN	"	Clr 1 to $\overline{Q}_1$	5	39	ns
"	t_{PLH}	"	110						OUT	"	2.4 V	A	IN	GND			"	Clr 2 to $\overline{Q}_2$	"	39	"
"	t_{PHL}	"	111	2.4 V		OUT	GND			"					A	IN	"	Clr 1 to Q1	"	50	"
"	t_{PHL}	"	112					OUT		"	2.4 V	A	IN	GND			"	Clr 2 to Q2	"	50	"
"	t_{PLH}	3003 (Fig 7)	113	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	5	39	ns
"	"		114	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to $\overline{Q}_1$	"	"	"
"	"	"	115					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
"	"	"	116						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to $\overline{Q}_2$	"	"	"
"	t_{PHL}	"	117	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	"	50	"
"	"	"	118	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to $\overline{Q}_1$	"	"	"
"	"	"	119					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
"	"	"	120						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to $\overline{Q}_2$	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

See notes at end of device type 03.

NOTES:

A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This note has been deleted.
D = Momentary 4.5 V, then GND.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.

* After clock pulse apply –12 mA to clock pin to insure $\overline{Q}$ is still in the low state (see figure 15).

** Test time limit ≤100 ms.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ One normal clock pulse, then 4.5 V.
6 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
7/ For CKT A, I_{IH3} limits are 0 to 120 μA.

TABLE III. Group A inspection for device type 04. 1/

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clock 1	2 Preset 1	3 Clear 1	4 J1	5 V_{CC}	6 Clock 2	7 Preset 2	8 Clear 2	9 J2	10 $\overline{Q}$ 2	11 Q2	12 K2	13 GND	14 $\overline{Q}$ 1	15 Q1	16 K1	Meas. terminal	Test limits Min	Max	Unit
1	V_{OH}	3006	1	A			2.0 V	4.5 V								GND		-.4 mA	0.8 V	Q1	2.4		V
T_C = 25°C	"	"	2	A			0.8 V	"								"	-.4 mA		2.0 V	$\overline{Q}$ 1	"		"
"	"	"	3		2.0 V	0.8 V		"								"	-.4 mA			$\overline{Q}$ 1	"		"
"	"	"	4		0.8 V	2.0 V		"								"		-.4 mA		Q1	"		"
"	"	"	5					"	A			2.0 V		-.4 mA	0.8 V	"				Q2	"		"
"	"	"	6					"	A			0.8 V	-.4 mA		2.0 V	"				$\overline{Q}$ 2	"		"
"	"	"	7					"		2.0 V	0.8 V		-.4 mA			"				$\overline{Q}$ 2	"		"
"	"	"	8					"		0.8 V	2.0 V			-.4 mA		"				Q2	"		"
"	V_{OL}	3007	9	A			0.8 V	"								"		16 mA	2.0 V	Q1		0.4	"
"	"	"	10	A			2.0 V	"								"	16 mA		0.8 V	$\overline{Q}$ 1		"	"
"	"	"	11		0.8 V	2.0 V		"								"	16 mA			$\overline{Q}$ 1		"	"
"	"	"	12		2.0 V	0.8 V		"								"		16 mA		Q1		"	"
"	"	"	13					"	A			0.8 V		16 mA	2.0 V	"				Q2		"	"
"	"	"	14					"	A			2.0 V	16 mA		0.8 V	"				$\overline{Q}$ 2		"	"
"	"	"	15					"		0.8 V	2.0 V		16 mA			"				$\overline{Q}$ 2		"	"
"	"	"	16					"		2.0 V	0.8 V			16 mA		"				Q2		"	"
"	V_{IC}		17				-12 mA	"								"				J1		-1.5	"
"	"		18					"								"			-12 mA	K1		"	"
"	"		19					"				-12 mA				"				J2		"	"
"	"		20					"							-12 mA	"				K2		"	"
"	"		21	-12 mA				"								"				Clock 1		"	"
"	"		22		-12 mA			"								"				Preset 1		"	"
"	"		23			-12 mA		"								"				Clear 1		"	"
"	"		24					"	-12 mA							"				Clock 2		"	"
"	"		25					"		-12 mA						"				Preset 2		"	"
"	"		26					"			-12 mA					"				Clear 2		"	"
"	I_{IL1}	3009	27	4.5 V		B	0.4 V	5.5 V								"				J1	-0.7	-1.6	mA
"	"	"	28	4.5 V	B	4.5 V		"								"			0.4 V	K1	"	"	"
"	"	"	29					"	4.5 V		B	0.4 V				"				J2	"	"	"
"	"	"	30					"	4.5 V	B	4.5 V				0.4 V	"				K2	"	"	"
"	I_{IL2}	"	31	0.4 V	B		4.5 V	"								"			4.5 V	Clock 1	-1.25	-3.2	"
"	"	"	32	0.4 V		B	4.5 V	"								"			4.5 V	Clock 1	"	"	"
"	"	"	33					"	0.4 V	B		4.5 V			4.5 V	"				Clock 2	"	"	"
"	"	"	34					"	0.4 V		B	4.5 V			4.5 V	"				Clock 2	"	"	"
"	I_{IL3}	"	35 A, C	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-0.7	-1.6	"
"	"	"	35 B	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-1.4	-3.2	"
"	"	"	36 A, C	4.5 V	0.4 V		4.5 V	"								"			4.5 V	Preset 1	-0.7	-1.6	"
"	"	"	36 B	4.5 V	0.4 V		4.5 V	"								"			4.5 V	Preset 1	-1.4	-3.2	"
"	"	"	37 A, C					"	4.5 V		0.4 V	4.5 V			4.5 V	"				Clear 2	-0.7	-1.6	"
"	"	"	37 B					"	4.5 V		0.4 V	4.5 V			4.5 V	"				Clear 2	-1.4	-3.2	"
"	"	"	38 A, C					"	4.5 V	0.4 V		4.5 V			4.5 V	"				Preset 2	-0.7	-1.6	"
"	"	"	38 B					"	4.5 V	0.4 V		4.5 V			4.5 V	"				Preset 2	-1.4	-3.2	"
"	I_{IH1}	3010	39	GND		GND	2.4 V	"								"				J1		40	µA
"	"	"	40	GND	GND			"								"			2.4 V	K1		"	"
"	"	"	41					"	GND		GND	2.4 V				"				J2		"	"
"	"	"	42					"	GND	GND					2.4 V	"				K2		"	"
"	I_{IH2}	"	43	GND		GND	5.5 V	"								"				J1		100	"
"	"	"	44	GND	GND			"								"			5.5 V	K1		"	"
"	"	"	45					"	GND		GND	5.5 V				"				J2		"	"
"	"	"	46					"	GND	GND					5.5 V	"				K2		"	"

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clock 1	2 Preset 1	3 Clear 1	4 J1	5 V_{CC}	6 Clock 2	7 Preset 2	8 Clear 2	9 J2	10 $\overline{Q}$ 2	11 Q2	12 K2	13 GND	14 $\overline{Q}$ 1	15 Q1	16 K1	Meas. terminal	Test limits Min	Max	Unit
1	I_{IH3}	3010	47	GND		E	GND	5.5 V								GND			4.5 V	Clear 1		160	µA
T_C = 25°C	"	"	48	GND	E		4.5 V	"								"			GND	Preset 1		"	"
"	"	"	49					"	GND		E	GND			4.5 V	"				Clear 2		"	"
"	"	"	50					"	GND	E		4.5 V			GND	"				Preset 2		"	"
"	I_{IH4}	"	51	GND		F	GND	"								"			4.5 V	Clear 1		200	"
"	"	"	52	GND	F		4.5 V	"								"			GND	Preset 1		"	"
"	"	"	53					"	GND		F	GND			4.5 V	"				Clear 2		"	"
"	"	"	54					"	GND	F		4.5 V			GND	"				Preset 2		"	"
"	"	"	55	5.5 V		GND	GND	"								"			GND	Clock 1		"	"
"	"	"	56					"	5.5 V		GND	GND			GND	"				Clock 2		"	"
"	I_{IH5}	"	57 CKT A, C	2.4 V		GND	GND	"								"			GND	Clock 1	-50	-700	"
"	"	"	57 CKT B	2.4 V		GND	GND	"								"			GND	Clock 1	-200	-850	"
"	"	"	58 CKT A, C					"	2.4 V		GND	GND			GND	"				Clock 2	-50	-700	"
"	"	"	58 CKT B					"	2.4 V		GND	GND			GND	"				Clock 2	-200	-850	"
"	I_{OS}	3011	59 **	2.4 V	GND	4.5 V	2.4 V	"								"		GND	2.4 V	Q1	-20	-57	mA
"	"	"	60	2.4 V	4.5 V	GND	2.4 V	"								"	GND		2.4 V	$\overline{Q}$ 1	"	"	"
"	"	"	61**					"	2.4 V	GND	4.5 V	2.4 V		GND	2.4 V	"				Q2	"	"	"
"	"	"	62					"	2.4 V	4.5 V	GND	2.4 V	GND		2.4 V	"				$\overline{Q}$ 2	"	"	"
"	I_{CC}	3005	63	GND	4.5 V	GND	GND	"	GND	4.5 V	GND	GND			GND	"			GND	V_{CC}		40	"
"	I_{CC}	3005	64	GND	GND	4.5 V	GND	"	GND	GND	4.5 V	GND			GND	"			GND	V_{CC}		40	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																						
7 2/ 4/			65	B	A	B	A	4.5 V	B	A	B	A	H 3/	L 3/	B	GND	H 3/	L 3/	B	All	H or L		
T_C = 25°C			66	A	A	B	A	"	A	A	B	A	H	L	B	"	H	L	B	output	as shown 3/		
"			67	B	A	B	A	"	B	A	B	A	H	L	B	"	H	L	B	"	"		
"			68	B	A	B	A	"	B	A	B	A	H	L	A	"	H	L	A	"	"		
"			69	A	A	B	A	"	A	A	B	A	H	L	A	"	H	L	A	"	"		
"			70	B	A	B	A	"	B	A	B	A	H	L	A	"	H	L	A	"	"		
"			71	B	B	A	A	"	B	B	A	A	L	H	A	"	L	H	A	"	"		
"			72	A	B	A	A	"	A	B	A	A	L	H	A	"	L	H	A	"	"		
"			73	B	B	A	A	"	B	B	A	A	L	H	A	"	L	H	A	"	"		
"			74	B	B	A	B	"	B	B	A	B	L	H	A	"	L	H	A	"	"		
"			75	A	B	A	B	"	A	B	A	B	L	H	A	"	L	H	A	"	"		
"			76	B	B	A	B	"	B	B	A	B	L	H	A	"	L	H	A	"	"		
"			77	B	A	A	B	"	B	A	A	B	L	H	B	"	L	H	B	"	"		
"			78	A	A	A	B	"	A	A	A	B	L	H	B	"	L	H	B	"	"		
"			79	B	A	A	B	"	B	A	A	B	L	H	B	"	L	H	B	"	"		
"			80	B	A	B	B	"	B	A	B	B	H	L	B	"	H	L	B	"	"		
"			81	B	A	A	B	"	B	A	A	B	H	L	B	"	H	L	B	"	"		
"			82	A	A	A	B	"	A	A	A	B	H	L	B	"	H	L	B	"	"		
"			83	B	A	A	B	"	B	A	A	B	H	L	B	"	H	L	B	"	"		
"			84	B	A	A	A	"	B	A	A	A	H	L	B	"	H	L	B	"	"		
"			85	A	A	A	A	"	A	A	A	A	H	L	B	"	H	L	B	"	"		
"			86	B	A	A	A	"	B	A	A	A	L	H	B	"	L	H	B	"	"		

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clock 1	2 Preset 1	3 Clear 1	4 J1	5 V_{CC}	6 Clock 2	7 Preset 2	8 Clear 2	9 J2	10 $\overline{Q}$ 2	11 Q2	12 K2	13 GND	14 $\overline{Q}$ 1	15 Q1	16 K1	Meas. terminal	Test limits Min	Max	Unit
7 2/ 4/			87	B	A	A	B	4.5 V	B	A	A	B	L 3/	H 3/	A	GND	L 3/	H 3/	A	All	H or L		
T_C = 25°C			88	A	A	A	B	"	A	A	A	B	L	H	A	"	L	H	A	Output	as shown 3/		
"			89	B	A	A	B	"	B	A	A	B	H	L	A	"	H	L	A	"	"		
"			90	B	A	A	A	"	B	A	A	A	H	L	A	"	H	L	A	"	"		
"			91	A	A	A	A	"	A	A	A	A	H	L	A	"	H	L	A	"	"		
"			92	B	A	A	A	"	B	A	A	A	L	H	A	"	L	H	A	"	"		
"			93	A	A	A	A	"	A	A	A	A	L	H	A	"	L	H	A	"	"		
"			94	B	A	A	A	"	B	A	A	A	H	L	A	"	H	L	A	"	"		
"			95	A	B	B	B	"	A	B	B	B	H	H	B	"	H	H	B	"	"		
"			96	A	B	A	A	"	A	B	A	A	L	H	A	"	L	H	A	"	"		
"			97	A	A	A	A	"	A	A	A	A	L	H	A	"	L	H	A	"	"		
"			98	A	A	A	A	"	A	A	A	A	L	H	B	"	L	H	B	"	"		
"			99	A	A	A	B	"	A	A	A	B	L	H	B	"	L	H	B	"	"		
"			100	B	A	A	B	"	B	A	A	B	H	L	B	"	H	L	B	"	"		
"			101	A	A	A	A	"	A	A	A	A	H	L	A	"	H	L	A	"	"		
"			102	A	A	A	B	"	A	A	A	B	H	L	A	"	H	L	A	"	"		
"			103	A	A	A	B	"	A	A	A	B	H	L	B	"	H	L	B	"	"		
"			104	B	A	A	B	"	B	A	A	B	L	H	B	"	L	H	B	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55ºC.																						
9	F_{MAX}	(Fig. 9)	105	IN	5.0 V		2.4 V	5.0 V								GND		OUT	2.4 V	Q1	10		MHz
T_C = 25°C	"	5/	106	IN	5.0 V		2.4 V	"								"	OUT		2.4 V	$\overline{Q}$ 1	"		"
"	"	"	107					"	IN	5.0 V		2.4 V		OUT	2.4 V	"				Q2	"		"
"	"	"	108					"	IN	5.0 V		2.4 V	OUT		2.4 V	"				$\overline{Q}$ 2	"		"
"	t_{PLH1}	3003 (Fig 8)	109	2.4 V	5.0 V	IN	2.4 V	"								"	OUT		2.4 V	Clear 1 to $\overline{Q}$ 1	5	25	ns
"	"	"	110	2.4 V	IN	5.0 V	2.4 V	"								"		OUT	2.4 V	Preset 1 to Q1	"	"	"
"	"	"	111					"	2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	112					"	2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	"	"
"	t_{PHL1}	"	113	2.4 V	5.0 V	IN	2.4 V	"								"		OUT	2.4 V	Clear 1 to Q1	"	40	"
"	"	"	114	2.4 V	IN	5.0 V	2.4 V	"								"	OUT		2.4 V	Preset 1 to $\overline{Q}$ 1	"	"	"
"	"	"	115					"	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q2	"	"	"
"	"	"	116					"	2.4 V	IN	5.0 V	2.4 V	OUT		2.4 V	"				Preset 2 to $\overline{Q}$ 2	"	"	"
"	t_{PLH2}	3003 (Fig 9)	117	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	5	30	ns
"	"	"	118	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	"	119					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	120					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL2}	"	121	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	40	"

See notes at end of device type 04.

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 Clock 1	2 Preset 1	3 Clear 1	4 J1	5 V_{CC}	6 Clock 2	7 Preset 2	8 Clear 2	9 J2	10 $\overline{Q}$ 2	11 Q2	12 K2	13 GND	14 $\overline{Q}$ 1	15 Q1	16 K1	Meas. terminal	Test limits Min	Max	Unit
9 T_C = 25°C	t_{PHL2}	3003 (Fig 8)	122	IN	5.0 V		2.4 V	5.0 V								GND	OUT	OUT	2.4 V	Clock 1 to $\overline{Q}$ 1	5	40	ns
"	"	"	123					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	124					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}$ 2	"	"	"
10 T_C = 125°C	F_{MAX} 5/	(Fig 9)	125	IN	5.0 V		2.4 V	"								"		OUT	2.4 V	Q1	10		MHz
"	"	"	126	IN	5.0 V		2.4 V	"								"	OUT		2.4 V	$\overline{Q}$ 1	"		"
"	"	"	127					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
"	"	"	128					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				$\overline{Q}$ 2	"		"
"	t_{PLH1}	3003 (Fig 8)	129	2.4 V	5.0 V	IN	2.4 V	"								"	OUT		2.4 V	Clear 1 to $\overline{Q}$ 1	5	39	ns
"	"	"	130	2.4 V	IN	5.0 V	2.4 V	"								"		OUT	2.4 V	Preset 1 to Q1	"	"	"
"	"	"	131					"	2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	132					"	2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	"	"
"	t_{PHL1}	"	133	2.4 V	5.0 V	IN	2.4 V	"								"		OUT	2.4 V	Clear 1 to Q1	"	50	"
"	"	"	134	2.4 V	IN	5.0 V	2.4 V	"								"	OUT		2.4 V	Preset 1 to $\overline{Q}$ 1	"	"	"
"	"	"	135					"	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V	"				Clear 2 to Q2	"	"	"
"	"	"	136					"	2.4 V	IN	5.0 V	2.4 V	OUT		2.4 V	"				Preset 2 to $\overline{Q}$ 2	"	"	"
"	t_{PLH2}	3003 (Fig 9)	137	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	5	39	ns
"	"	"	138	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	"	139					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	140					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL2}	"	141	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1 to Q1	"	50	"
"	"	"	142	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	"	143					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	144					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2 to $\overline{Q}$ 2	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																						

See notes at end of device type 04.

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
C = This note has been deleted.
E = Momentary ground, then 2.4 V.
F = Momentary ground, then 5.5 V.
** = Test time limit ≤ 100 ms.
J = This note has been deleted.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open.)
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
1 T_C = 25°C	V_{OH}	3006	1	A	2.0 V		4.5 V							GND		-.4 mA		Q1	2.4		V
"	"	"	2	A	0.8 V		"							"	-.4 mA			$\overline{Q}$ 1	"		"
"	"	"	3	GND		0.8 V	"							"	-.4 mA		GND	$\overline{Q}$ 1	"		"
"	"	"	4			GND	"							"		-.4 mA	0.8 V	Q1	"		"
"	"	"	5				"		2.0 V	A		-.4 mA		"				Q2	"		"
"	"	"	6				"		0.8 V	A			-.4 mA	"				$\overline{Q}$ 2	"		"
"	"	"	7				"	0.8 V		GND	GND		-.4 mA	"				$\overline{Q}$ 2	"		"
"	"	"	8				"	GND			0.8 V	-.4 mA		"				Q2	"		"
"	V_{OL}	3007	9	A	2.0 V		"							"	16 mA			$\overline{Q}$ 1		0.4	"
"	"	"	10	A	0.8 V		"							"		16 mA		Q1		"	"
"	"	"	11			0.8 V	"							"		16 mA	2.0 V	Q1		"	"
"	"	"	12			2.0 V	"							"	16 mA		0.8 V	$\overline{Q}$ 1		"	"
"	"	"	13				"		2.0 V	A			16 mA	"				$\overline{Q}$ 2		"	"
"	"	"	14				"		0.8 V	A		16 mA		"				Q2		"	"
"	"	"	15				"	0.8 V			2.0 V	16 mA		"				Q2		"	"
"	"	"	16				"	2.0 V			0.8 V		16 mA	"				$\overline{Q}$ 2		"	"
"	V_{IC}		17		-12 mA		"							"				D1		-1.5	"
"	"		18	-12 mA			"							"				Clock 1		"	"
"	"		19			-12 mA	"							"				Clear 1		"	"
"	"		20				"							"			-12 mA	Preset 1		"	"
"	"		21				"		-12 mA					"				D2		"	"
"	"		22				"			-12 mA				"				Clock 2		"	"
"	"		23				"	-12 mA						"				Clear 2		"	"
"	"		24				"				-12 mA			"				Preset 2		"	"
"	I_{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							"			GND	D1	-0.7	-1.6	mA
"	"	"	26				"	4.5 V	0.4 V	4.5 V	GND			"				D2	-0.7	-1.6	"
"	"	"	27	GND	GND	GND	"							"			0.4 V	Preset 1	-1.4	-3.2	"
"	"	"	28				"	GND	GND	GND	0.4 V			"				Preset 2	-1.4	-3.2	"
"	I_{IL2}	"	29	0.4 V	GND	4.5 V	"							"			GND	Clock 1	-1.4	-3.2	"
"	"	"	30 7/	4.5 V	4.5 V	0.4 V	"							"			GND	Clear 1	-2.1	-4.8	"
"	"	"	31				"	4.5 V	GND	0.4 V	GND			"				Clock 2	-1.4	-3.2	"
"	"	"	32 7/				"	0.4 V	4.5 V	4.5 V	GND			"				Clear 2	-2.1	-4.8	"
"	I_{IH1}	3010	33	4.5 V	2.4 V	GND	"							"			4.5 V	D1		40	µA
"	I_{IH1}	"	34				"	GND	2.4 V	4.5 V	4.5 V			"				D2		40	"
"	I_{IH2}	"	35	4.5 V	5.5 V	GND	"							"			4.5 V	D1		100	"
"	I_{IH2}	"	36				"	GND	5.5 V	4.5 V	4.5 V			"				D2		100	"
"	I_{IH3}	"	37	2.4 V	4.5 V	GND	"							"			4.5 V	Clock 1		80	"
"	"	"	38	B	4.5 V	4.5 V	"							"			2.4 V	Preset 1		"	"
"	"	"	39				"	GND	4.5 V	2.4 V	4.5 V			"				Clock 2		"	"
"	"	"	40				"	4.5 V	4.5 V	B	2.4 V			"				Preset 2		"	"
"	I_{IH4}	"	41	5.5 V	4.5 V	GND	"							"			4.5 V	Clock 1		200	"
"	"	"	42	B	4.5 V	4.5 V	"							"			5.5 V	Preset 1		"	"
"	"	"	43				"	GND	4.5 V	5.5 V	4.5 V			"				Clock 2		"	"
"	"	"	44				"	4.5 V	4.5 V	B	5.5 V			"				Preset 2		"	"
"	I_{IH5}	"	45	B	GND	2.4 V	"							"			4.5 V	Clear 1		120	"
"	I_{IH5}	"	46				"	2.4 V	GND	B	4.5 V			"				Clear 2		120	"
"	I_{IH6}	"	47	B	GND	5.5 V	"							"			4.5 V	Clear 1		300	"
"	I_{IH6}	"	48				"	5.5 V	GND	B	4.5 V			"				Clear 2		300	"

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
1	I_{OS}	3011	49				5.5 V							GND		GND	GND	Q1	-20	-57	mA
T_C = 25°C	"	"	50			GND	"							"	GND			$\overline{Q}$ 1	"	"	"
"	"	"	51				"				GND	GND		"				Q2	"	"	"
"	"	"	52				"	GND					GND	"				$\overline{Q}$ 2	"	"	"
"	I_{CC}	3005	53	GND	GND		"		GND	GND	GND			"			GND	V_{CC}		30	"
"	I_{CC}	3005	54	GND	GND	GND	"	GND	GND	GND				"				V_{CC}		30	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				
7 2/ 4/			55	B	B	B	4.5 V	B	B	B	B	H 3/	H 3/	GND	H 3/	H	B	All outputs	H or L as shown 3/		
T_C = 25°C			56	B	B	B	"	B	B	B	A	L	H	"	H	L	A				
"			57	B	B	A	"	A	B	B	A	L	H	"	H	L	A	"	"		
"			58	B	B	A	"	A	B	B	B	H	L	"	L	H	B	"	"		
"			59	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			60	A	B	B	"	B	B	A	B	H	H	"	H	H	B	"	"		
"			61	A	A	B	"	B	A	A	B	H	H	"	H	H	B	"	"		
"			62	A	A	B	"	B	A	A	A	L	H	"	H	L	A	"	"		
"			63	A	A	A	"	A	A	A	A	L	H	"	H	L	A	"	"		
"			64	A	A	A	"	A	A	A	B	H	L	"	L	H	B	"	"		
"			65	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			66	B	A	A	"	A	A	B	A	H	L	"	L	H	A	"	"		
"			67	B	B	A	"	A	B	B	A	H	L	"	L	H	A	"	"		
"			68	A	B	A	"	A	B	A	A	L	H	"	H	L	A	"	"		
"			69	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			70	A	A	B	"	B	A	A	B	H	H	"	H	H	B	"	"		
"			71	A	B	B	"	B	B	A	B	H	H	"	H	H	B	"	"		
"			72	A	B	B	"	B	B	A	A	L	H	"	H	L	A	"	"		
"			73	A	B	A	"	A	B	A	A	L	H	"	H	L	A	"	"		
"			74	B	A	A	"	A	A	B	A	L	H	"	H	L	A	"	"		
"			75	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			76	A	A	A	"	A	A	A	B	H	L	"	L	H	B	"	"		
"			77	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			78	A	A	B	"	B	A	A	A	L	H	"	H	L	A	"	"		
"			79	A	A	A	"	A	A	A	A	L	H	"	H	L	A	"	"		
"			80	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			81	A	B	A	"	A	B	A	A	H	L	"	L	H	A	"	"		
"			82	A	B	B	"	B	B	A	A	L	H	"	H	L	A	"	"		
"			83	A	B	A	"	A	B	A	A	L	H	"	H	L	A	"	"		
"			84	A	A	A	"	A	A	A	A	L	H	"	H	L	A	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55ºC.																				
9	F_{MAX} 6/	(Fig. 11)	85	IN	E		5.0 V							GND		OUT	5.0 V	Q1	10		MHz
T_C = 25°C	"	"	86	IN	E		"							"	OUT		5.0 V	$\overline{Q}$ 1	"		"
"	"	"	87				"		E	IN	5.0 V	OUT		"				Q2	"		"
"	"	"	88				"		E	IN	5.0 V		OUT	"				$\overline{Q}$ 2	"		"

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
9 T_C = 25°C	t_{PLH1}	3003 (Fig 10)	89			IN	5.0 V							GND	OUT		J	Clear 1 to $\overline{Q}$ 1	5	25	ns
"	"	"	90			J	"							"		OUT	IN	Preset 1 to Q1	"	"	"
"	"	"	91				"	IN			J		OUT	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	92				"	J			IN	OUT		"				Preset 2 to Q2	"	40	"
"	t_{PHL1}	"	93			IN	"							"		OUT	J	Clear 1 to Q1	"	"	"
"	"	"	94			J	"							"	OUT		IN	Preset 1 to $\overline{Q}$ 1	"	"	"
"	"	"	95				"	IN			J	OUT		"				Clear 2 to Q2	"	"	"
"	"	"	96				"	J			IN		OUT	"				Preset 2 to $\overline{Q}$ 2	"	"	"
"	t_{PLH2}	3003 5/ (Fig 11)	97	IN	IN (A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	5	30	ns
"	"	(Fig 12)	98	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig 11)	99				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig 12)	100				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL2}	(Fig 12)	101	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	40	"
"	"	(Fig 11)	102	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig 12)	103				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig 11)	104				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
10 T_C = 125°C	F_{MAX} 6/	(Fig 11)	105	IN	E		"							"		OUT	5.0 V	Q1	10	"	MHz
	"	"	106	IN	E		"							"	OUT		5.0 V	$\overline{Q}$ 1	"	"	"
"	"	"	107				"		E	IN	5.0 V	OUT		"				Q2	"	"	"
"	"	"	108				"		E	IN	5.0 V		OUT	"				$\overline{Q}$ 2	"		"
"	t_{PLH1}	3003 (Fig 10)	109			IN	"							"	OUT		J	Clear 1 to $\overline{Q}$ 1	5	39	ns
"	"	"	110			J	"							"		OUT	IN	Preset 1 to Q1	"	"	"
"	"	"	111				"	IN			J		OUT	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	112				"	J			IN	OUT		"				Preset 2 to Q2	"	"	"
"	t_{PHL1}	"	113			IN	"							"		OUT	J	Clear 1 to Q1	"	50	"
"	"	"	114			J	"							"	OUT		IN	Preset 1 to $\overline{Q}$ 1	"	"	"
"	"	"	115				"	IN			J	OUT		"				Clear 2 to Q2	"	"	"
"	"	"	116				"	J			IN		OUT	"				Preset 2 to $\overline{Q}$ 2	"	"	"

See notes at end of device type 05.

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B, D Case C Test No.	1 Clock 1	2 D1	3 Clear 1	4 V_{CC}	5 Clear 2	6 D2	7 Clock 2	8 Preset 2	9 Q2	10 $\overline{Q}$ 2	11 GND	12 $\overline{Q}$ 1	13 Q1	14 Preset 1	Meas. terminal	Test limits Min	 Max	 Unit
10 T_C = 125°C	t_{PLH2}	3003 5/ (Fig 11)	117	IN	IN (A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	5	39	ns
	"	(Fig 12)	118	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig 11)	119				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig 12)	120				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL2}	(Fig 12)	121	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	40	"
"	"	(Fig 11)	122	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig 12)	123				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig 11)	124				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
E = Input D connected to $\overline{Q}$.
J = Input pulse, $t_p \geq 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Tests shall be performed for both D input pulses (A and B).
6 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
7/ CKT C limits are –0.7 to -4.8 mA for these tests.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11				
			Test No.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J*	$\overline{Q}$	GND	Q	K*	K2		Min	Max	Unit
1	V_{OH}	3006	1	0.8 V	A		4.5 V			2.0 V	2.0 V	0.8 V		GND	-.4 mA	2.0 V	0.8 V	Q	2.4		V
T_C = 25°C	"	"	2	2.0 V	A		"			0.8 V	0.8 V	2.0 V	-.4 mA	"		0.8 V	2.0 V	$\overline{Q}$	"		"
"	"	"	3		GND	2.0 V	"	0.8 V				GND	-.4 mA	"		GND		$\overline{Q}$	"		"
"	"	"	4		GND	0.8 V	"	2.0 V				GND		"	-.4 mA	GND		Q	"		"
"	V_{OL}	3007	5	2.0 V	A		"			0.8 V	0.8 V	2.0 V		"	16 mA	0.8 V	2.0 V	Q		0.4	"
"	"	"	6	0.8 V	A		"			2.0 V	2.0 V	0.8 V	16 mA	"		2.0 V	0.8 V	$\overline{Q}$		"	"
"	"	"	7		GND	0.8 V	"	2.0 V				GND	16 mA	"				$\overline{Q}$		"	"
"	"	"	8		GND	2.0 V	"	0.8 V				GND		"	16 mA			Q		"	"
"	V_{IC}		9				"			-12 mA				"				J1		-1.5	"
"	"		10				"				-12 mA			"				J2		"	"
"	"		11				"					-12 mA		"				J*		"	"
"	"		12	-12 mA			"							"				K1		"	"
"	"		13				"							"			-12 mA	K2		"	"
"	"		14				"							"		-12 mA		K*		"	"
"	"		15		-12 mA		"							"				Clock		"	"
"	"		16			-12 mA	"							"				Preset		"	"
"	"		17				"	-12 mA						"				Clear		"	"
"	I_{IL1}	3009	18		GND		5.5 V	B		0.4 V	4.5 V	0.4 V		"				J1	-0.7	-1.6	mA
"	"	"	19		GND		"	B		4.5 V	0.4 V	0.4 V		"				J2	"	"	"
"	"	"	20				"					0.4 V		"				J*	"	"	"
"	"	"	21	0.4 V	GND	B	"							"		0.4 V	4.5 V	K1	"	"	"
"	"	"	22	4.5 V	GND	B	"							"		0.4 V	0.4 V	K2	"	"	"
"	"	"	23				"							"		0.4 V		K*	"	"	"
"	"	"	24		0.4 V		"							"				Clock	"	"	"
"	"	"	25	4.5 V	GND	0.4 V	"							"		0.4 V	4.5 V	Preset	"	"	"
"	"	"	26		GND		"	0.4 V		4.5 V	4.5 V	0.4 V		"				Clear	"	"	"
"	I_{IH1}	3010	27				"	GND		2.4 V	GND	4.5 V		"				J1		40	µA
"	"	"	28				"	GND		GND	2.4 V	4.5 V		"				J2		"	"
"	"	"	29				"					2.4 V		"				J*		"	"
"	"	"	30	2.4 V		GND	"							"		4.5 V	GND	K1		"	"
"	"	"	31	GND		GND	"							"		4.5 V	2.4 V	K2		"	"
"	"	"	32				"							"		2.4 V		K*		"	"
"	"	"	33		2.4 V		"							"				Clock		"	"
"	I_{IH2}	"	34				"	GND		5.5 V	GND	4.5 V		"				J1		100	"
"		"	35				"	GND		GND	5.5 V	4.5 V		"				J2		"	"
"		"	36				"					5.5 V		"				J*		"	"
"	"	"	37	5.5 V		GND	"							"		4.5 V	GND	K1		"	"
"	"	"	38	GND		GND	"							"		4.5 V	5.5 V	K2		"	"
"	"	"	39				"							"		5.5 V		K*		"	"
"	"	"	40		5.5 V		"							"				Clock		"	"
"	I_{IH3}	"	41	GND	A	2.4 V	"			4.5 V	4.5 V	GND		"		4.5 V	GND	Preset		80	"
"	"	"	42	4.5 V	A		"	2.4 V		GND	GND	4.5 V		"		GND	4.5 V	Clear		80	"
"	I_{IH4}	"	43	GND	A	5.5 V	"			4.5 V	4.5 V	GND		"		4.5 V	GND	Preset		200	"
"	"	"	44	4.5 V	A		"	5.5 V		GND	GND	4.5 V		"		GND	4.5 V	Clear		200	"
"	I_{OS}	3011	45		GND	GND	"					GND		"	GND	GND		Q	-20	-57	mA
"	"	"	46		GND		"	GND				GND	GND	"		GND		$\overline{Q}$	-20	-57	"
"	I_{CC}	3005	47				"	GND						"				V_{CC}		30	"
"	"	"	48			GND	"							"				V_{CC}		30	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				

See notes at end of device type 06.

TABLE III. Group A inspection for device type 06. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11				
			Test No.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J*	$\overline{Q}$	GND	Q	K*	K2		Min	Max	Unit
7 2/ 4/			49	B	B	A	4.5 V	B	B	B	B	A	H 3/	GND	L 3/	A	B	All	H or L		
T_C = 25°C			50	B	B	B	"	A	B	B	B	A	L	"	H	A	B	output	as shown 3/		
"			51	B	B	A	"	A	B	B	B	A	L	"	H	B	A	"	"		
"			52	B	A	A	"	A	B	B	B	A	L	"	H	B	A	"	"		
"			53	B	B	A	"	A	B	B	B	A	L	"	H	B	A	"	"		
"			54	A	B	A	"	A	B	B	B	A	L	"	H	B	B	"	"		
"			55	A	A	A	"	A	B	B	B	A	L	"	H	B	B	"	"		
"			56	A	B	A	"	A	B	B	B	A	L	"	H	B	B	"	"		
"			57	A	B	A	"	A	B	B	B	A	L	"	H	A	A	"	"		
"			58	A	A	A	"	A	B	B	B	A	L	"	H	A	A	"	"		
"			59	A	B	A	"	A	B	B	B	A	L	"	H	A	A	"	"		
"			60	A	B	A	"	B	B	B	B	A	H	"	L	A	A	"	"		
"			61	B	B	A	"	A	B	A	B	B	H	"	L	A	B	"	"		
"			62	B	A	A	"	A	B	A	B	B	H	"	L	A	B	"	"		
"			63	B	B	A	"	A	B	A	B	B	H	"	L	A	B	"	"		
"			64	B	B	A	"	A	B	B	A	B	H	"	L	A	B	"	"		
"			65	B	A	A	"	A	B	B	A	B	H	"	L	A	B	"	"		
"			66	B	B	A	"	A	B	B	A	B	H	"	L	A	B	"	"		
"			67	B	B	A	"	A	B	A	A	A	H	"	L	A	B	"	"		
"			68	B	A	A	"	A	B	A	A	A	H	"	L	A	B	"	"		
"			69	B	B	A	"	A	B	A	A	A	H	"	L	A	B	"	"		
"			70	A	B	A	"	A	B	A	A	B	H	"	L	B	A	"	"		
"			71	A	A	A	"	A	B	A	A	B	L	"	H	B	A	"	"		
"			72	A	B	A	"	A	B	A	A	B	L	"	H	B	A	"	"		
"			73	A	A	A	"	A	B	A	A	B	H	"	L	B	A	"	"		
"			74	A	B	A	"	A	B	A	A	B	H	"	L	B	A	"	"		
"			75	A	B	A	"	B	B	A	A	B	H	"	L	B	A	"	"		
"			76	A	A	A	"	B	B	A	A	B	H	"	L	B	A	"	"		
"			77	A	B	A	"	B	B	A	A	B	H	"	L	B	A	"	"		
"			78	A	B	B	"	B	B	A	A	B	L	"	L	B	A	"	"		
"			79	A	A	B	"	B	B	A	A	B	L	"	L	B	A	"	"		
"			80	A	B	B	"	B	B	A	A	B	L	"	L	B	A	"	"		
"			81	B	B	A	"	B	B	B	B	A	H	"	L	A	B	"	"		
"			82	B	B	A	"	A	B	B	B	A	H	"	L	A	B	"	"		
"			83	B	A	A	"	A	B	B	B	A	H	"	L	A	B	"	"		
"			84	B	A	B	"	A	B	B	B	A	L	"	L	A	B	"	"		
"			85	B	B	B	"	A	B	B	B	A	L	"	H	A	B	"	"		
"			86	B	B	A	"	A	B	B	B	A	L	"	H	A	B	"	"		
"			87	B	A	A	"	A	B	B	B	A	L	"	H	A	B	"	"		
"			88	B	A	A	"	B	B	B	B	A	L	"	L	A	B	"	"		
"			89	B	A	A	"	A	B	B	B	A	L	"	H	A	B	"	"		
"			90	A	B	A	"	A	B	A	A	B	L	"	H	B	A	"	"		
"			91	A	B	B	"	A	B	A	A	B	L	"	H	B	A	"	"		
"			92	A	A	B	"	A	B	A	A	B	L	"	H	B	A	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55°C.																				

See notes at end of device type 06.

TABLE III. Group A inspection for device type 06. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11				
			Test No.	K1	Clock	Preset	V_{CC}	Clear	NC	J1	J2	J*	$\overline{Q}$	GND	Q	K*	K2		Min	Max	Unit
9	F_{MAX} 5/	(Fig. 14)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	GND		GND	OUT	GND	2.4 V	Q	20		MHz
T_C = 25°C	F_{MAX} 5/	(Fig. 14)	94	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND	OUT	"		GND	2.4 V	$\overline{Q}$	20		MHz
"	t_{PLH}	3003 (Fig. 13)	95	5.0 V	0.8 V	IN	"	IN		5.0 V	5.0 V	GND	OUT	"		GND	5.0 V	Clear to $\overline{Q}$	5	50	ns
"	t_{PLH}	"	96	"	"	"	"	"		"	"	"		"	OUT	"	"	Preset to Q	"	"	"
"	t_{PHL}	"	97	"	"	"	"	"		"	"	"		"	OUT	"	"	Clear to Q	"	"	"
"	t_{PHL}	"	98	"	"	"	"	"		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	"	"
"	(Fig. 15)	3003 (Fig. 14)	99	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	50	ns
"	t_{PLH}		100	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	"	"
"	t_{PHL}	"	101	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	"	"
"	t_{PHL}	"	102	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	"	"
10	F_{MAX} 5/	(Fig. 14)	103	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Q	15		MHz
T_C = 125°C	F_{MAX} 5/	(Fig. 14)	104	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND	OUT	"		GND	2.4 V	$\overline{Q}$	15		MHz
"	t_{PLH}	3003 (Fig. 13)	105	5.0 V	0.8 V	IN	"	IN		5.0 V	5.0 V	GND	OUT	"		GND	5.0 V	Clear to $\overline{Q}$	5	62	ns
"	t_{PLH}	"	106	"	"	"	"	"		"	"	"		"	OUT	"	"	Preset to Q	"	"	"
"	t_{PHL}	"	107	"	"	"	"	"		"	"	"		"	OUT	"	"	Clear to Q	"	"	"
"	t_{PHL}	"	108	"	"	"	"	"		"	"	"	OUT	"		"	"	Preset to $\overline{Q}$	"	"	"
"	t_{PLH}	3003 (Fig. 14)	109	2.4 V	IN	5.0 V	"	5.0 V		5.0 V	5.0 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	62	ns
"	t_{PLH}		110	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	"	"
"	t_{PHL}	"	111	"	"	"	"	"		"	"	"		"	OUT	"	"	Clock to Q	"	"	"
"	t_{PHL}	"	112	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to $\overline{Q}$	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 07. 1/

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	Unit
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1				
1	V_{OH}	3006	1	A	2.0 V		4.5 V							GND		-.4 mA		Q1	2.4		V
T_C = 25°C	"	"	2	A	0.8 V		"							"	-.4 mA			$\overline{Q}$ 1	"		"
"	"	"	3			0.8 V	"							"	-.4 mA		2.0 V	$\overline{Q}$ 1	"		"
"	"	"	4			2.0 V	"							"		-.4 mA	0.8 V	Q1	"		"
"	"	"	5				"		2.0 V	A		-.4 mA		"				Q2	"		"
"	"	"	6				"		0.8 V	A			-.4 mA	"				$\overline{Q}$ 2	"		"
"	"	"	7				"	0.8 V			2.0 V		-.4 mA	"				$\overline{Q}$ 2	"		"
"	"	"	8				"	2.0 V			0.8 V	-.4 mA		"				Q2	"		"
"	V_{OL}	3007	9	A	2.0 V		"							"	16 mA			$\overline{Q}$ 1		0.4 V	"
"	"	"	10	A	0.8 V		"							"		16 mA		Q1		"	"
"	"	"	11			0.8 V	"							"		16 mA	2.0 V	$\overline{Q}$ 1		"	"
"	"	"	12			2.0 V	"							"	16 mA		0.8 V	Q1		"	"
"	"	"	13				"		2.0 V	A			16 mA	"				$\overline{Q}$ 2		"	"
"	"	"	14				"		0.8 V	A		16 mA		"				Q2		"	"
"	"	"	15				"	0.8 V			2.0 V	16 mA		"				Q2		"	"
"	"	"	16				"	2.0 V			0.8 V		16 mA	"				$\overline{Q}$ 2		"	"
"	V_{IC}		17		-12 mA		"							"				D1		-1.5	"
"	"		18	-12 mA			"							"				Clock 1		"	"
"	"		19			-12 mA	"							"				Clear 1		"	"
"	"		20				"							"			-12 mA	Preset 1		"	"
"	"		21				"		-12 mA					"				D2		"	"
"	"		22				"			-12 mA				"				Clock 2		"	"
"	"		23				"	-12 mA						"				Clear 2		"	"
"	"		24				"				-12 mA			"				Preset 2		"	"
"	I_{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							"			0.4 V	D 1	-0.5	-1.6	mA
"	"	"	26	0.4 V	0.4 V	4.5 V	"							"			0.4 V	Preset 1	"	"	"
"	"	"	27				"	4.5 V	0.4 V	4.5 V	0.4 V			"				D 2	"	"	"
"	"	"	28				"	4.5 V	0.4 V	0.4 V	0.4 V			"				Preset 2	"	"	"
"	I_{IL2}	"	29	0.4 V	0.4 V	4.5 V	"							"			GND	Clock 1	-1.0	-3.2	"
"	"	"	30	0.8 V	4.5 V	0.4 V	"							"			4.5 V	Clear 1	"	"	"
"	"	"	31				"	4.5 V	0.4 V	0.4 V	GND			"				Clock 2	"	"	"
"	"	"	32				"	0.4 V	4.5 V	0.8 V	4.5 V			"				Clear 2	"	"	"
"	I_{IH1}	3010	33	4.5 V	2.4 V	GND	"							"			GND	D1		40	µA
"	"	"	34				"	GND	2.4 V	4.5 V	GND			"				D2		40	"
"	I_{IH2}	"	35	4.5 V	5.5 V	GND	"							"			GND	D1		100	"
"	"	"	36				"	GND	5.5 V	4.5 V	GND			"				D2		100	"
"	I_{IH3}	"	37	2.4 V		B	"							"			GND	Clock 1		80	"
"	"	"	38	B	4.5 V	4.5 V	"							"			2.4 V	Preset 1		"	"
"	"	"	39				"	B		2.4 V	GND			"				Clock 2		"	"
"	"	"	40				"	4.5 V	4.5 V	B	2.4 V			"				Preset 2		"	"
"	I_{IH4}	"	41	5.5 V		B	"							"			GND	Clock 1		200	"
"	"	"	42	B	4.5 V	4.5 V	"							"			5.5 V	Preset 1		"	"
"	"	"	43				"	B		5.5 V	GND			"				Clock 2		"	"
"	"	"	44				"	4.5 V	4.5 V	B	5.5 V			"				Preset 2		"	"
"	I_{IH5}	"	45	GND	GND	2.4 V	"							"				Clear 1		120	"
"	"	"	46				"	2.4 v	GND	GND				"				Clear 2		120	"
"	I_{IH6}	"	47	GND	GND	5.5 V	"							"				Clear 1		300	"
"	"	"	48				"	5.5 V	GND	GND				"				Clear 2		300	"

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
1	I_{OS}	3011	49				5.5 V							GND		GND	GND	Q1	-20	-57	mA
T_C = 25°C	"	"	50			GND	"							"	GND			$\overline{Q}$ 1	"	"	"
"	"	"	51				"				GND	GND		"				Q2	"	"	"
"	"	"	52				"	GND					GND	"				$\overline{Q}$ 2	"	"	"
"	I_{CC}	3005	53	GND	GND		"		GND	GND	GND	GND		"			GND	V_{CC}		30	"
"	I_{CC}	3005	54	GND	GND	GND	"	GND	GND	GND	GND			"				V_{CC}		30	"
2	Same tests, terminal conditions and limits as subgroup 1, except T_C = 125ºC and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as subgroup 1, except T_C = -55ºC and V_{IC} tests are omitted.																				
7 2/ 4/			55	B	B	B	4.5 V	B	B	B	B	H 3/	H 3/	GND	H 3/	H 3/	B	All outputs	H or L as shown 3/		
T_C = 25°C			56	B	B	B	"	B	B	B	A	L	H	"	H	L	A	"	"		
"			57	B	B	A	"	A	B	B	A	L	H	"	H	L	A	"	"		
"			58	B	B	A	"	A	B	B	B	H	L	"	L	H	B	"	"		
"			59	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			60	A	B	B	"	B	B	A	B	H	H	"	H	H	B	"	"		
"			61	A	A	B	"	B	A	A	B	H	H	"	H	H	B	"	"		
"			62	A	A	B	"	B	A	A	A	L	H	"	H	L	A	"	"		
"			63	A	A	A	"	A	A	A	A	L	H	"	H	L	A	"	"		
"			64	A	A	A	"	A	A	A	B	H	L	"	L	H	B	"	"		
"			65	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			66	B	A	A	"	A	A	B	A	H	L	"	L	H	A	"	"		
"			67	B	B	A	"	A	B	B	A	H	L	"	L	H	A	"	"		
"			68	A	B	A	"	A	B	A	A	L	H	"	H	L	A	"	"		
"			69	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			70	A	A	B	"	B	A	A	B	H	H	"	H	H	B	"	"		
"			71	A	B	B	"	B	B	A	B	H	H	"	H	H	B	"	"		
"			72	A	B	B	"	B	B	A	A	L	H	"	H	L	A	"	"		
"			73	A	B	A	"	A	B	A	A	L	H	"	H	L	A	"	"		
"			74	B	A	A	"	A	A	B	A	L	H	"	H	L	A	"	"		
"			75	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			76	A	A	A	"	A	A	A	B	H	L	"	L	H	B	"	"		
"			77	A	A	A	"	A	A	A	A	H	L	"	L	H	A	"	"		
"			78	A	A	B	"	B	A	A	A	L	H	"	H	L	A	"	"		
"			79	A	A	A	"	A	A	A	A	L	H	"	H	L	A	"	"		
"			80	A	B	A	"	A	B	A	B	H	L	"	L	H	B	"	"		
"			81	A	B	A	"	A	B	A	A	H	L	"	L	H	A	"	"		
8 2/ 4/	Same tests, terminal conditions and limits as for subgroup 7, except T_C = 125ºC and -55°C.																				

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
9	F_{MAX}	(Fig. 11)	82	IN	E	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MHz
T_C = 25°C	"	"	83	IN	E	5.0 V	"							"	OUT		5.0 V	$\overline{Q}$ 1	"		"
"	"	"	84				"	5.0 V	E	IN	5.0 V	OUT		"				Q2	"		"
"	"	"	85				"	5.0 V	E	IN	5.0 V		OUT	"				$\overline{Q}$ 2	"		"
"	t_{PLH}	3003 ((Fig. 10)	86			IN	"							"	OUT		IN	Clear 1 to $\overline{Q}$ 1	5	25	ns
"	"	"	87			IN	"							"		OUT	IN	Preset 1 to Q1	"	"	"
"	"	"	88				"	IN			IN		OUT	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	89				"	IN			IN	OUT		"				Preset 2 to Q2	"	"	"
"	t_{PHL}	"	90			IN	"							"		OUT	IN	Clear 1 to Q1	"	33	"
"	"	"	91			IN	"							"	OUT		IN	Preset 1 to $\overline{Q}$ 1	"	36	"
"	"	"	92				"	IN			IN		OUT	"				Clear 2 to $\overline{Q}$ 2	"	36	"
"	"	"	93				"	IN			IN	OUT		"				Preset 2 to Q2	"	33	"
"	t_{PLH}	3003 5/ (Fig. 11)	94	IN	IN (A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	5	25	ns
"	"	(Fig. 12)	95	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig. 11)	96				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig. 12)	97				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL}	(Fig. 12)	98	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	33	"
"	"	(Fig. 11)	99	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig. 12)	100				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig. 11)	101				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"

See notes at end of device type 07.

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4				
			Test No.	Clock 1	D1	Clear 1	V_{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1		Min	Max	Unit
10 T_C = 125°C	F_{MAX} 6/	(Fig. 11)	102	IN	E	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MHz
"	"	"	103	IN	E	5.0 V	"							"	OUT		5.0 V	$\overline{Q}$ 1	"		"
"	"	"	104				"	5.0 V	E	IN	5.0 V	OUT		"				Q2	"		"
"	"	"	105				"	5.0 V	E	IN	5.0 V		OUT	"				$\overline{Q}$ 2	"		"
"	t_{PLH}	3003 ((Fig. 10)	106			IN	"							"	OUT		IN	Clear 1 to $\overline{Q}$ 1	5	31	ns
	"	"	107			IN	"							"		OUT	IN	Preset 1 to Q1	"		"
"	"	"	108				"	IN			IN		OUT	"				Clear 2 to $\overline{Q}$ 2	"	"	"
"	"	"	109				"	IN			IN	OUT		"				Preset 2 to Q2	"	"	"
"	t_{PHL}	"	110			IN	"							"		OUT	IN	Clear 1 to Q1	"	39	"
"		"	111			IN	"							"	OUT		IN	Preset 1 to $\overline{Q}$ 1	"	42	"
"	"	"	112				"	IN			IN		OUT	"				Preset 2 to $\overline{Q}$ 2	"	42	"
"	"	"	113				"	IN			IN	OUT		"				Clear 2 to Q2	"	39	"
"	t_{PLH}	3003 5/ (Fig. 11)	114	IN	IN (A)	B	"							"		OUT	5.0 V	Clock 1 to Q1	5	31	ns
"	"	(Fig. 12)	115	IN	IN (A)	5.0 V	"							"	OUT		B	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig. 11)	116				"	B	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig. 12)	117				"	5.0 V	IN (A)	IN	B		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
"	t_{PHL}	(Fig. 12)	118	IN	IN (B)	5.0 V	"							"		OUT	B	Clock 1 to Q1	"	39	"
"	"	(Fig. 11)	119	IN	IN (B)	B	"							"	OUT		5.0 V	Clock 1 to $\overline{Q}$ 1	"	"	"
"	"	(Fig. 12)	120				"	5.0 V	IN (B)	IN	B	OUT		"				Clock 2 to Q2	"	"	"
"	"	(Fig. 11)	121				"	B	IN (B)	IN	5.0 V		OUT	"				Clock 2 to $\overline{Q}$ 2	"	"	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																				

NOTES:
A = Normal clock pulse.
B = Momentary GND, then 4.5 V.
E = Input D connected to $\overline{Q}$.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
4/ Tests shall be performed in sequence.
5/ Tests shall be performed for both D input pulses (A and B).
6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

I Requirements for "JAN" marking.

j. Packaging Requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ..... Electrical ground (common terminal)
V_{IN} ..... Voltage level at an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	SN5472 (Circuit A)
01	DM5472 (Circuit B)
01	MC5472 (Circuit C)
02	SN5473 (Circuit A)
02	DM5473 (Circuit B)
02	S5473 (Circuit C)
03	SN54107 (Circuit A)
03	DM54107 (Circuit B)
03	S54107 (Circuit C)
04	SN5476 (Circuit A)
04	DM5476 (Circuit B)
04	S5476 (Circuit C)
05	5474 (Circuit A)
05	DM5474 (Circuit B)
06	5470
07	SN5479 (Circuit A)
07	MC5479 (Circuit B)

6.8 Change from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

Review activities:
Army – SM, MI
Navy - AS, CG, MC, SH TD
Air Force – 03, 19, 99

(Project 5962-2096)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.