INCH-POUND
MIL-M-38510/2G
8 February 2005
SUPERSEDING
MIL-M-38510/2E
24 December 1974
MIL-M-0038510/2F (USAF)
24 OCTOBER 1975

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

- 1. SCOPE
- 1.1 <u>Scope.</u> This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outlines/lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).
 - 1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.
 - 1.2.1 <u>Device types</u>. The device types are as follows:

Device type	<u>Circuit</u>
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil

AMSC N/A FSC 5962

1.2.3 <u>Case outlines.</u> The case outlines are as designated in MIL-STD-1835 and as follows:

B C D E	Descriptive designator	<u>Terminals</u>	Package style
Α	GDFP5-F14 or CDFP6-F14	14	Flat pack
В	GDFP4-F14	14	Flat pack
С	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.3 Absolute maximum ratings.

Supply voltage rangeInput voltage range	
Storage temperature range	
Maximum power dissipation, (P _D)	440
flip-flop, 1/	
Lead temperature (soldering, 10 seconds)	
Thermal resistance, junction to case (0)()	0.08°C/mW for dual-in-line pack
Junction temperature (T _J)	•

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	
	5.5 V dc maximum
Minimum high-level input voltage (V _{IH})	2.0 V dc
Maximum low-level input voltage (V _{IL})	0.8 V dc
Normalized fanout (each output) 2/	10 maximum
Case operating temperature range (T _C)	-55 °C to +125 °C
Input set up time:	
Device type 01, 02, 03 and 04,	≥ clock pulse width
Device type 05, 06, and 07	20 ns
Input hold time	
Device types 01, 02, 03 and 04	0 ns
Device type 05, 06 and 07	5 ns

2. APPLICABLE DOCUMENTS

2.1 <u>General</u>. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

^{1/} Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration

^{2/} Device will fanout in both high and low levels to the specified number of I_{IL1}/I_{IH1} inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 <u>Specifications and Standards</u>. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 <u>Order of precedence.</u> In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Qualification</u>. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).
- 3.2 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 3.3 <u>Design, construction, and physical dimensions.</u> The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
- 3.3.1 <u>Terminal connections and logic diagrams</u>. The terminal connections and logic diagrams shall be as specified on figures 1.
 - 3.3.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.
- 3.3.3 <u>Schematic circuits.</u> The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.
 - 3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
- 3.4 <u>Lead material and finish.</u> The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
- 3.5 <u>Electrical performance characteristics</u>. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
- 3.6 <u>Electrical test requirements.</u> The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III. Subgroups 7 and 8 testing requires only a summary of attributes data.
 - 3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 9/	Device	Lim	nits	Units
		_	Type	Min	Max	
High-level output voltage	V _{OH}	V _{CC} =4.5 V	All	2.4		Volts
		$I_{OH} = -400 \mu A$				
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, I_{OL} = 16 \text{ mA}$	All		0.4	Volts
Input clamp voltage	V _{IC}	$V_{CC} = 4.5 \text{ V}, I_{IC} = -12 \text{ mA}$ $T_{C} = 25^{\circ}\text{C}$	All		-1.5	Volts
Low-level input current	I _{IL1}	$V_{CC} = 5.5 \text{ V}$	01, 02, 03, 04,	-0.7	-1.6	mA
, , , , , , , , , , , , , , , , , , , ,	121	$V_{IN} = 0.4 \text{ V } 1/$	05, 06			
		_	07	-0.5	-1.6	mA
Low-level input current	I _{IL2}	V _{CC} = 5.5 V	01, 02, 03, 04,	-1.4	-3.2	mA
		$V_{IN} = 0.4 \text{ V } \underline{2}/$	05			
			07	-1.0	-3.2	mA
Low-level input current	I _{IL3}	V _{CC} = 5.5 V	01, 02, 03, 04	-0.7	-3.2	mA
		$V_{IN} = 0.4 \text{ V } \underline{6}/$				
High-level input current	I _{IH1}	V _{CC} = 5.5 V	All		40	μΑ
		V _{IN} = 2.4 V <u>5</u> /				
High-level input current	I _{IH2}	$V_{CC} = 5.5 \text{ V}$	All		100	μΑ
		V _{IN} = 5.5 V <u>5</u> /				
High-level input current	I _{IH3}	V _{CC} = 5.5 V	All <u>11</u> /		80	μΑ
		$V_{IN} = 2.4 \text{ V} \underline{3}/$ $V_{CC} = 5.5 \text{ V}$				
High-level input current	I _{IH4}	$V_{CC} = 5.5 \text{ V}$ $V_{IN} = 5.5 \text{ V} 3 / 7 /$	All		200	μΑ
High-level input current	I _{IH5}	V _{CC} = 5.5 V	01, 02, 03, 04,	-50	-850	μА
g	-1110	V _{IN} = 2.4 V <u>7</u> / <u>8</u> /	05, 07		120	μΑ
High-level input current	I _{IH6}	V _{CC} = 5.5 V	05, 07		300	μΑ
riigir iovoi iripat carront	ino	V _{IN} = 5.5 V <u>8</u> /	00, 01		000	μΛ
Short-circuit output current	Ios	V _{CC} = 5.5 V	All	-20	-57	mA
	100	$V_{IN} = 0 \underline{4}/$				
Supply current per device	I _{cc}	V _{CC} = 5.5 V	01		20	mA
		V _{IN} = 5 V	02, 03, 04		40	
			05, 06, 07		30	
Maximum clock frequency 10/	f _{MAX}		01, 02, 03	10		MHz
			04, 05, 07			
			06	15		
Propagation delay to high logic level	t _{PLH}		01, 02, 03, 04,	5	39	ns
(clear or preset to output)			05			
, ,			06	5	62	
			07	5	31	
Propagation delay to low logic level	t _{PHL}	$V_{CC} = 5 V$	01, 02, 03, 04,	5	50	ns
(clear or preset to output)		CL = 50 pF minimum	05			
, ,		$RL = 390\Omega \pm 5\%$	06	5	62	
			07	5	39	
Propagation delay to high logic level	t _{PLH}	7	06	5	62	ns
(clock to output)			01, 02, 03, 04,	5	39	1
			05			
			07	5	31	
Propagation delay to low logic level	t _{PHL}	7	06	5	62	ns
(clock to output)			01, 02, 03, 04,	5	50	
			05			
			07	5	39	

^{1/} Input condition – J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.

^{2/} Input condition – Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.

^{3/} Input condition – Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.

^{4/} No more than one output should be shorted at a time.

^{5/} Input condition – J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.

^{6/} Input condition – Clear or preset for device types 01, 02, 03 and 04.

^{7/} Input condition – Clock for device types 01, 02, 03 and 04.

- 8/ Input condition Clear for device types 05 and 07.
- 9/ See table III for complete terminal conditions.
- <u>10/</u> Minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- 11/ For device types 02 and 03, limits are 0 to 120 μ A.

TABLE II. Electrical test requirements.

	Subgroups	(see table III)
MIL-PRF-38535	Class S	Class B
test requirements	devices	devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 8, 9	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7 9
Group B test when using the method 5005 QCI option	1, 2, 3,	N/A
Group C end-point electrical parameters	1, 2, 3,	1, 2, 3
Additional electrical subgroups for Group C periodic inspections	N/A	10, 11
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

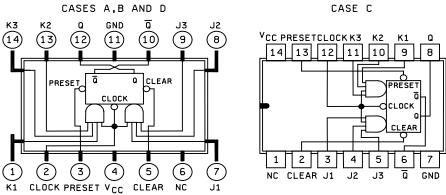
^{*}PDA applies to subgroup 1.

4. VERIFICATION

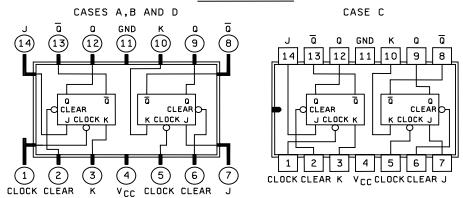
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
- 4.2 <u>Screening.</u> Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
 - a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
 - c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
 - 4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.
- 4.4 <u>Technology Conformance inspection (TCI).</u> Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

- 4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 shall be omitted.
 - 4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.
- 4.4.3 <u>Group C inspection.</u> Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burnin test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- 4.4.4 <u>Group D inspection.</u> Group D inspection shall be in accordance with table V of MIL-PRF-38535. Endpoint electrical parameters shall be as specified in table II herein.
 - 4.5 Methods of inspection. Methods of inspection shall be specified and as follows:
- 4.5.1 <u>Voltage and current.</u> All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 03

CASE C

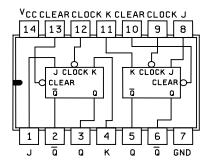
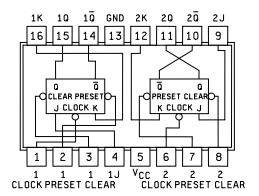
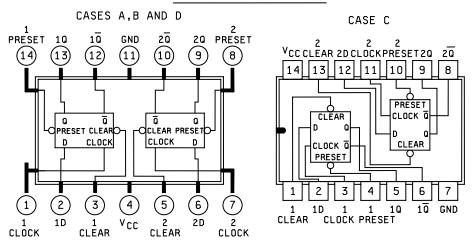


FIGURE 1. Logic diagram and terminal connections.

DEVICE TYPE 04 CASES E AND F



DEVICE TYPES 05 AND 07



DEVICE TYPE 06

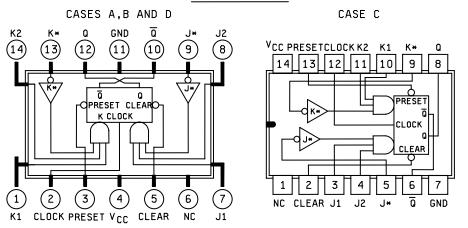


FIGURE 1. Logic diagram and terminal connections - Continued.

Device type 01

Truth table						
t	t _n					
J	J K					
L	L L					
L	L H					
Н	L	Н				
Н	Н	\overline{Q}_n				

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate regardless of the state of clock or J of K inputs.

NOTES: $1. J = J1 \bullet J2 \bullet J3$

2. K = K1 • K2 • K3

3. t_n = Bit time before clock pulse.

4. $t_n + 1$ = Bit time after clock pulse.

Device type 02 and 03

Truth table each flip-flop							
t_n $t_n + 1$							
J	J K						
L	L L						
L	L H						
Н	H L						
Н	Н	Q _n					

Positive logic: Low input to clear sets Q to low-level

Clear is independent of clock and dominate regardless of the state of clock or J or K inputs.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. Truth tables.

Device type 04

Truth table each flip-flop							
t	t _n						
J	J K						
L	Qn						
L	Н	L					
Н	L	Н					
Н	Н	$\overline{\overline{Q}}_n$					

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate

regardless of the state of clock or J of K inputs.

NOTES: 1. t_n = Bit time before clock pulse. 2. t_n + 1 = Bit time after clock pulse.

Device type 05 and 07

Truth table each flip-flop								
t _n t _n + 1								
INPUT D	OUTPUT Q	OUTPUT Q						
L	L	Н						
Н	Н	L						

Positive logic: Low input to preset sets Q to high-level

Low input to clear sets Q to low-level

Preset and clear are independent of clock and dominate

regardless of the state of clock or D input.

NOTES: 1. t_n = Bit time before clock pulse.

2. $t_n + 1 = Bit time after clock pulse.$

FIGURE 2. <u>Truth tables</u> – Continued.

Device type 06

Truth table						
t	t _n + 1					
J	J K					
L	L L					
L	L H					
Н	L	Н				
Н	Н	$\overline{\overline{Q}}_n$				

Positive logic: Low input to preset sets Q to high-level

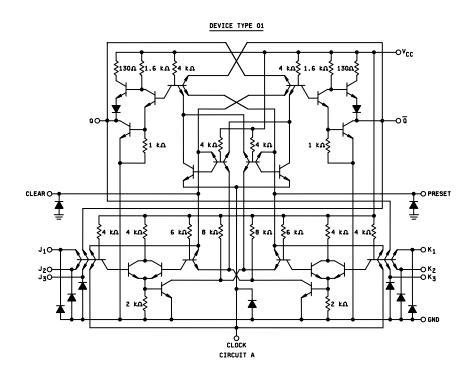
Low input to clear sets Q to low-level Preset or clear function can occur only

When clock input is low.

NOTES: 1. J = J1 • J2 • $\overline{J^*}$

- 2. K = K1 K2 \overline{K}^* 3. t_n = Bit time before clock pulse.
- 4. $t_n + 1$ = Bit time after clock pulse.
- 5. If inputs J* or K* are not used must be grounded.

FIGURE 2. <u>Truth tables</u> – Continued.



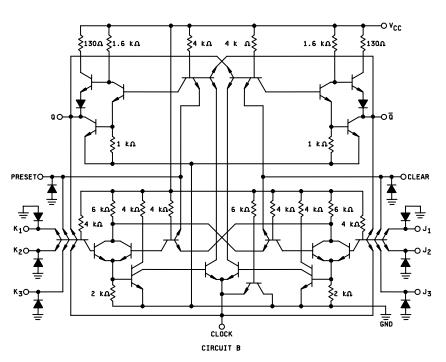


FIGURE 3. Schematic circuits.

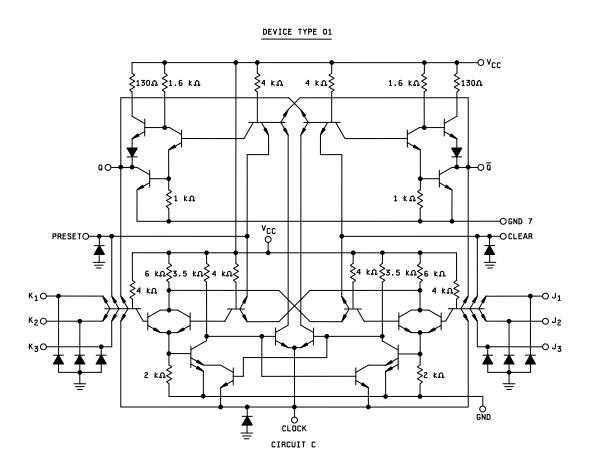


FIGURE 3. <u>Schematic circuits</u> – Continued.

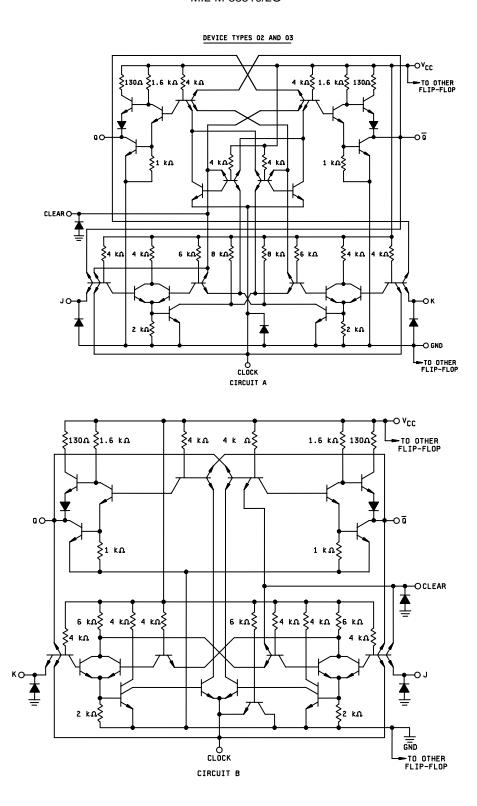
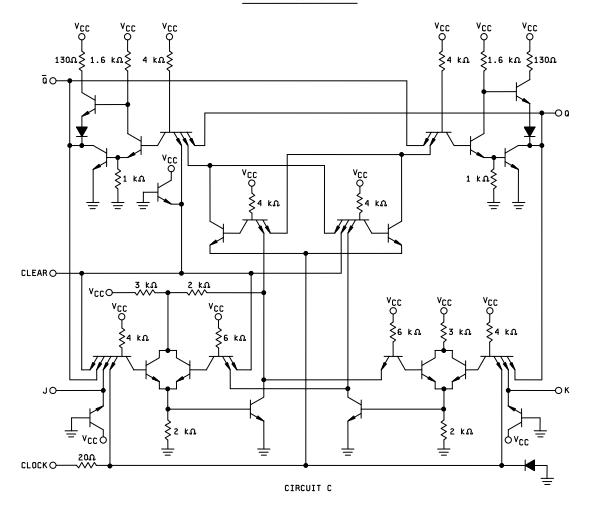


FIGURE 3. Schematic circuits - Continued.

DEVICE TYPES 02 AND 03



- 1. Circuits A, B, and C are the only acceptable variations for device types 02 and 03.
- 2. All resistance values shown are nominal.

FIGURE 3. Schematic circuits - Continued.

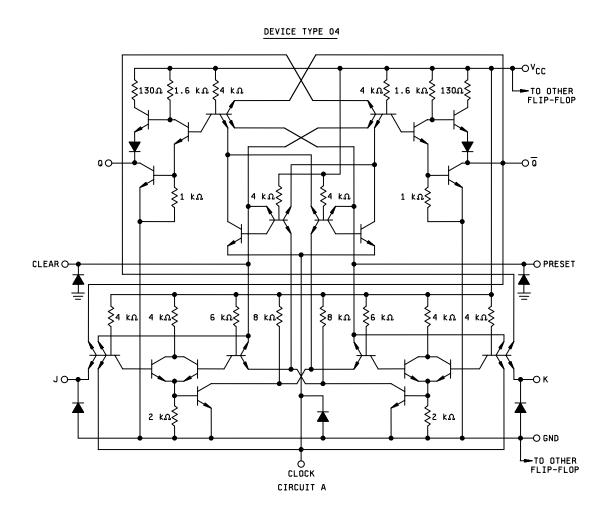


FIGURE 3. <u>Schematic circuits</u> – Continued.

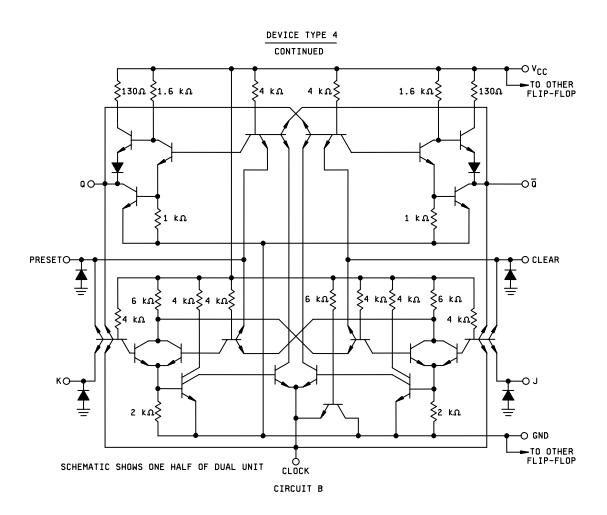
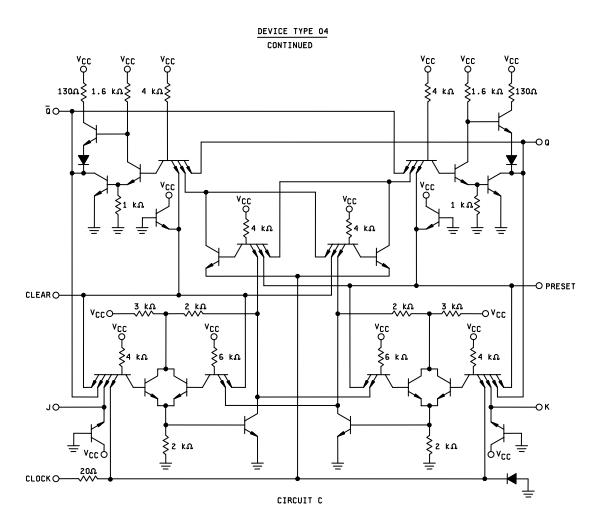
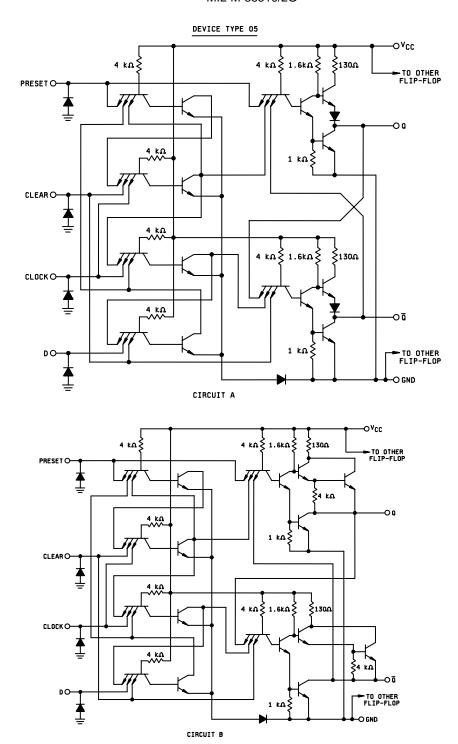


FIGURE 3. Schematic circuits – Continued.



- 1. Circuits A, B and C are the only acceptable variation for device type 04.
- 2. All resistance values shown are nominal.

FIGURE 3. <u>Schematic circuits</u> – Continued.



- Circuits A, B, and C are the only acceptable variations for device type 05. All resistance values shown are nominal.
- 2.

FIGURE 3. Schematic circuits - Continued.

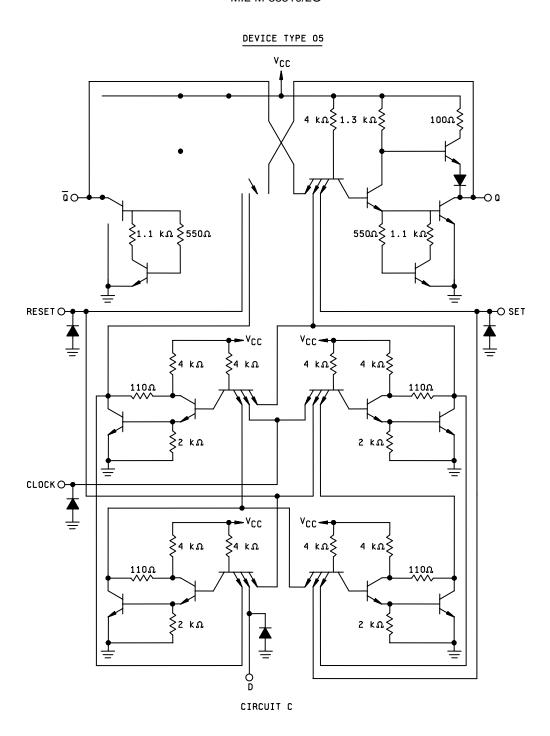
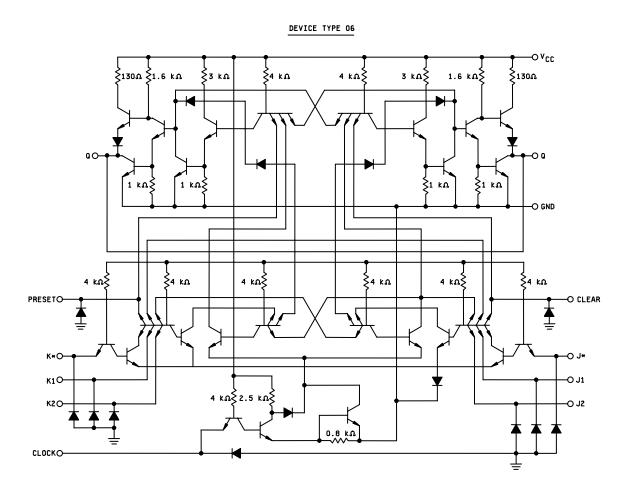
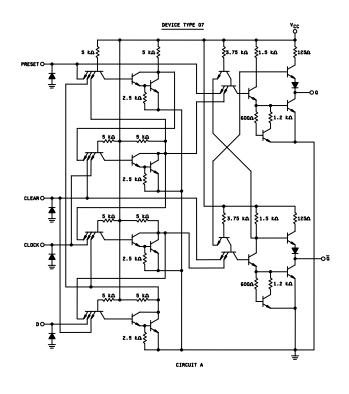


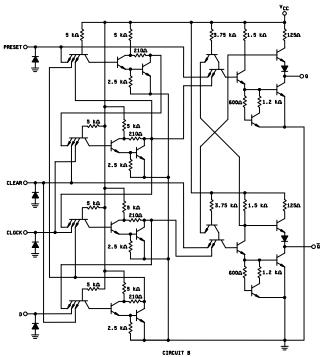
FIGURE 3. <u>Schematic circuits</u> – Continued.



NOTE: All resistance values shown are nominal.

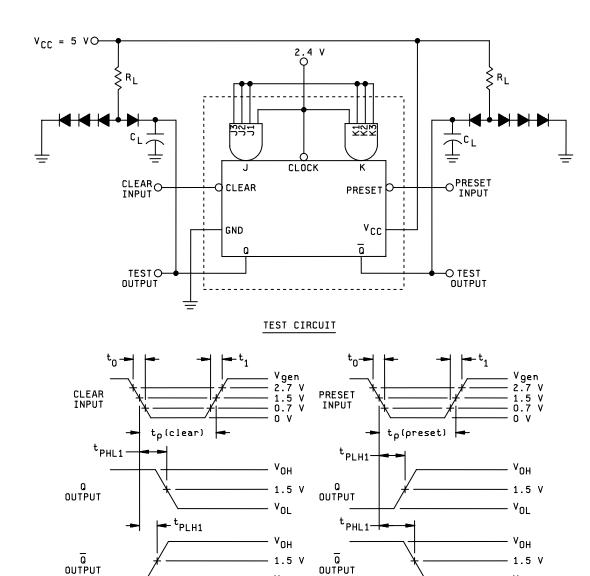
FIGURE 3. Schematic circuits – Continued.





- Circuits A and B are the only acceptable variations for device type 07.
 All resistance values shown are nominal.

FIGURE 3. Schematic circuits – Continued.



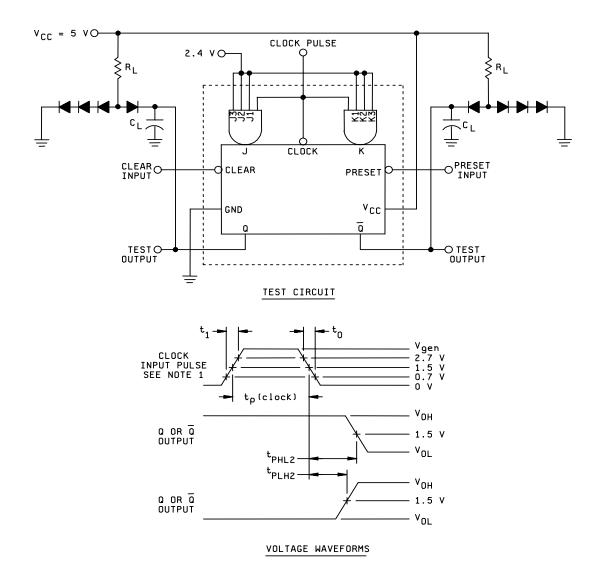
- 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (C_L includes probe and jig capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.
- 5. All diodes are 1N3064, or equivalent.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset output switching, clear shall have a negative pulse (see table III).

FIGURE 4. Clear and preset switching test circuit and waveforms for device type 01.

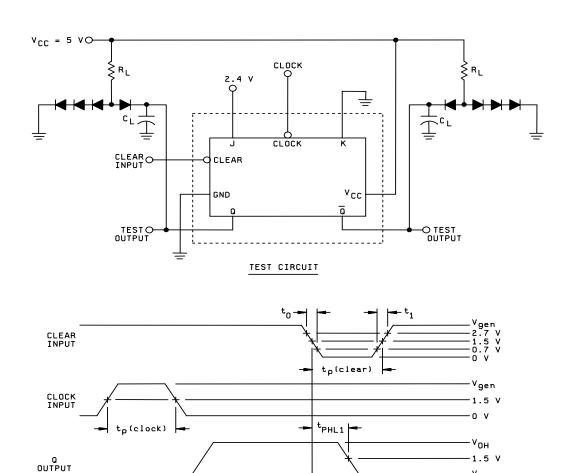
VOL

VOLTAGE WAVEFORMS

VOL



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing t_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. $J = J1 \cdot J2 \cdot J3$; and $K = K1 \cdot K2 \cdot K3$
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum } (C_L \text{ includes probe and jig capacitance}).$
- 5. $R_L = 390\Omega \pm 5\%$



VOLTAGE WAVEFORMS

^tPLH1

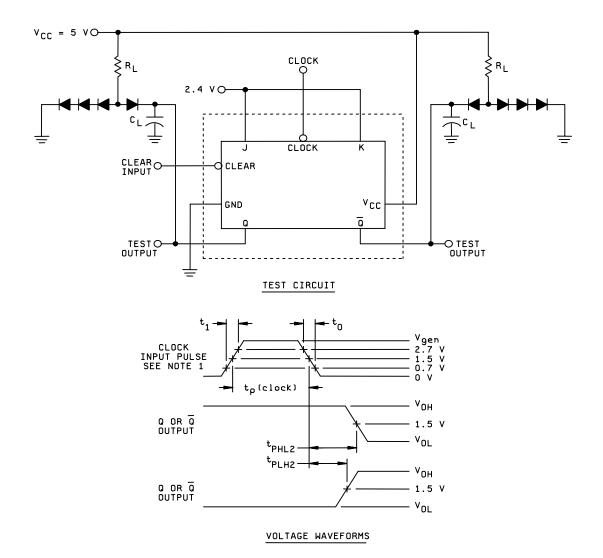
۷он 1.5 V

· V_{OL}

NOTES:

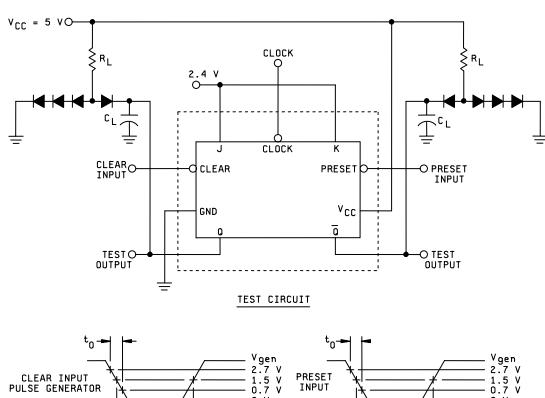
- Clear inputs dominate regardless of the state of clock or J-K inputs.
 Clear input pulse characteristics: V_{gen} = 3 V, t₀ = t₁ = 10 ns, t_p(clear) = 30 ns, PRR = 1 MHz.
 All diodes are 1N3064, or equivalent.
- 4. C_L = 50 pF, minimum (C_L includes probe and jig capacitance). 5. R_L = 390 Ω ±5%.
- 6. Clock input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_p \text{ (clock)} \ge 25 \text{ ns}$, PRR = 1 MHz.

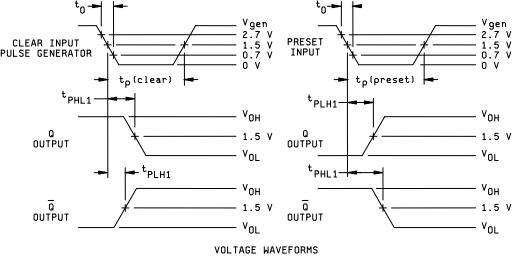
FIGURE 6. Clear switching test circuit and waveforms for device types 02 and 03.



- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing f_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0\leq 10$ ns, t_p (clock) = 20 ns, and PRR = 10 MHz for subgroups 9, 10, and 11.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$

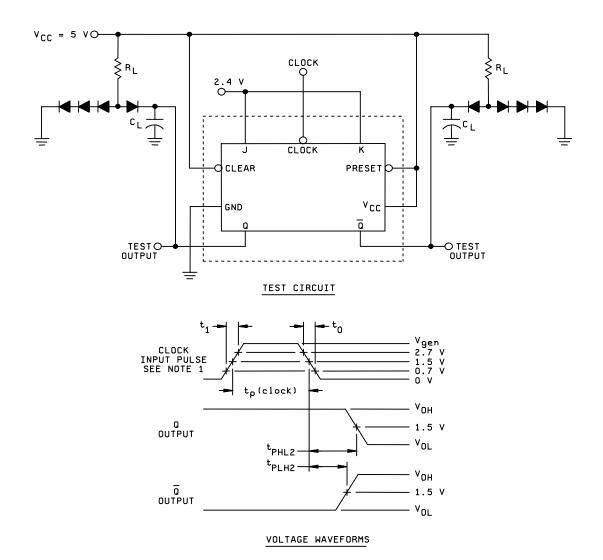
FIGURE 7. Synchronous switching test circuit for device type 02 and 03.





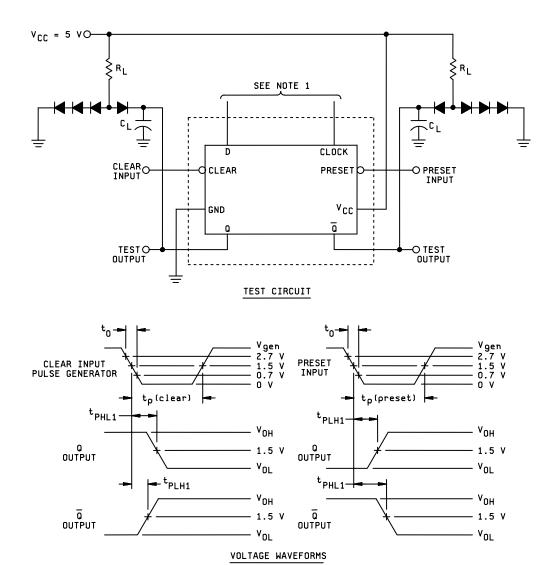
- 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
- 2. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_0 = t_1 = 10 \text{ ns}$, $t_p(clear) = t_p(preset) = 30 \text{ ns}$, PRR = 1 MHz, and $Z_{OUT} \approx 50\Omega$.
- 3. $C_L = 50$ pF, minimum (including jig and probe capacitance).
- 4. $R_L = 390\Omega \pm 5\%$.
- 5. All diodes are 1N3064, or equivalent.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 8. Clear and preset switching test circuit and waveforms for device type 04.



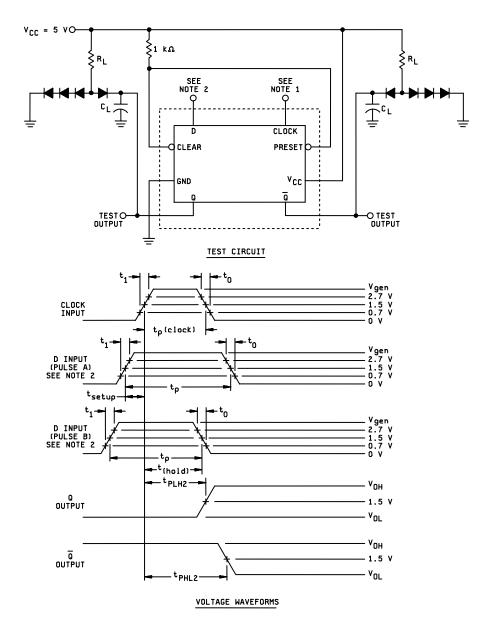
- 1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output), $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 25 ns, and PRR = 1 MHz. All J and K inputs are at 2.4 V. When testing t_{MAX} the clock input characteristics are $V_{gen}=3$ V, $t_1=t_0 \le 10$ ns, t_p (clock) = 20 ns, and PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 9. Synchronous switching test circuit for device type 04.



- 1. Clear and preset inputs dominate regardless of the state of clock or D inputs.
- 2. All diodes are 1N3064, or equivalent.
- 3. Clear or preset input pulse characteristics: $V_{gen} = 3 \text{ V}$, $t_o \le 7 \text{ ns}$, t_p (clear) = t_p (preset) = 35 ns, and PRR = 1 MHz.
- 4. $C_L = 50$ pF, minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$.
- 6. When testing clear to output switching, preset input shall have a negative pulse. When testing preset to output switching, clear input shall have a negative pulse (see table III).

FIGURE 10. Clear and preset switching test circuit and waveforms for device types 05 and 07.



- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 \le 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. D input (pulse A) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 \le 10$ ns, $t_{SETUP}=25$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen}=3$ V, $t_o=t_1 < 7$ ns, $t_{hold}=6$ ns, $t_p=60$ ns, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50 \text{ pF minimum (including jig and probe capacitance)}$.
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 11. Synchronous switching test circuit (high level data) for device types 05 and 07.

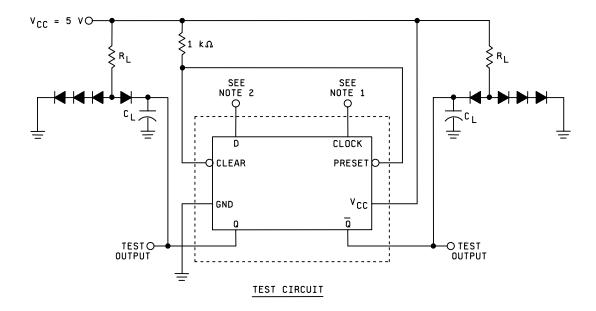
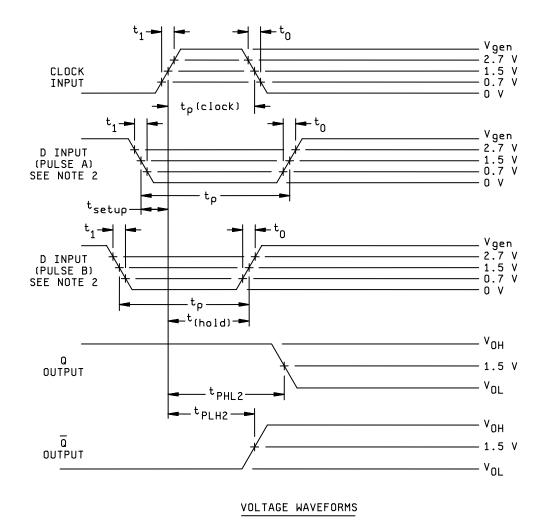
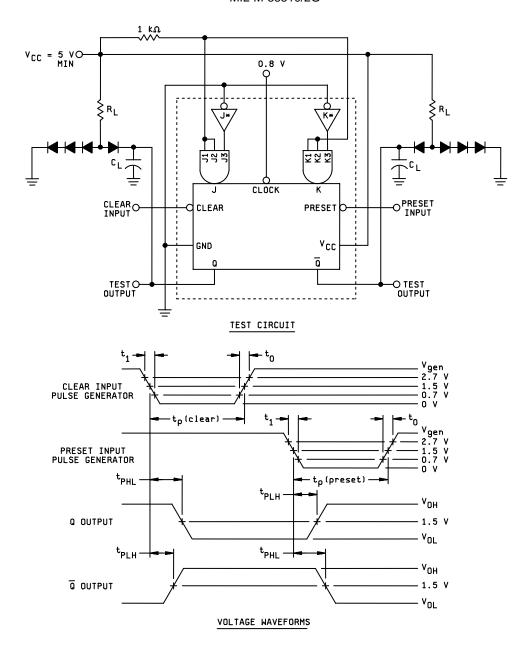


FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07.



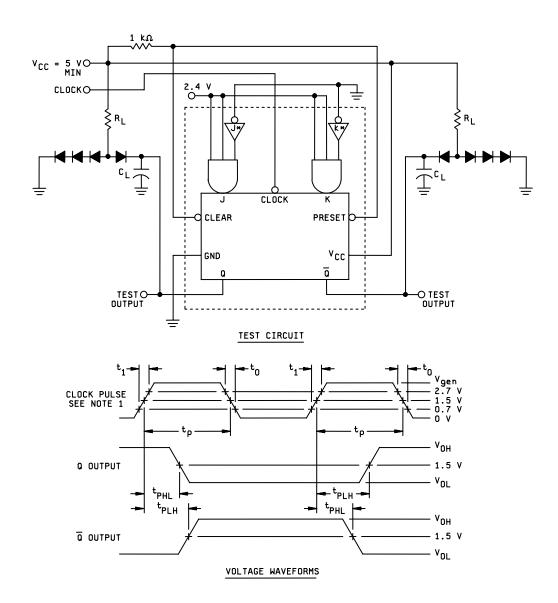
- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 < 10 \text{ ns}$, t_p (clock) = 30 ns, and PRR = 1 MHz.
- 2. D input (pulse A) has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 \leq 10 \text{ ns}$, $t_{SETUP} = 25 \text{ ns}$, $t_p = 60 \text{ ns}$, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_o = t_1 < 10 \text{ ns}$, $t_{hold} = 6 \text{ ns}$, $t_p = 60 \text{ ns}$, and PRR is 50% of the clock PRR.
- 3. All diodes are 1N3064, or equivalent.
- 4. $C_L = 50$ pF minimum (including jig and probe capacitance).
- 5. $R_L = 390\Omega \pm 5\%$

FIGURE 12. Synchronous switching test circuit (low-level data) for device types 05 and 07 – Continued.



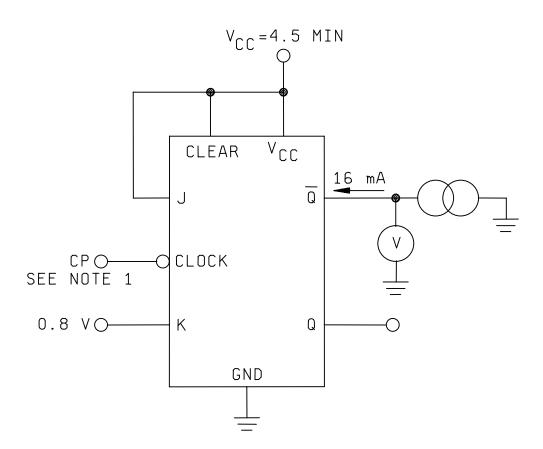
- 1. Preset or clear function can occur only when clock input is low. Gated inputs are inhibited.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF, minimum, including jig and probe capacitance.
- 4. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, t_o = 5 ns, $t_1 \le 10$ ns, t_p = 25 ns.
- 5. $R_L = 390\Omega \pm 5\%$.

FIGURE 13. Clear and preset switching test circuit and waveforms for device types 06.



- 1. Clock input pulse has the following characteristics: $V_{gen} = 3 \text{ V}$, $t_1 = t_0 \le 10 \text{ ns}$, $t_p = 30 \text{ ns}$, and PRR = 1 MHz. When testing f_{MAX} , PRR = see table III.
- 2. All diodes are 1N3064, or equivalent.
- 3. $C_L = 50$ pF minimum including jig and probe capacitance.
- 4. $R_L = 390\Omega \pm 5\%$

FIGURE 14. Synchronous switching test circuit for device type 06.



- 1. Apply normal clock pulse, then sink -12 mA on the clock input.
- 2. The output \overline{Q} is measured after -12 mA is applied to the clock to insure it is still in the low state.

FIGURE 15. Input clamp voltage test circuit for device types 01, 02, 03, and 04 (circuit B).

TABLE III. Group A inspection for device type 01. 1/

Subgroup	Symbol	MIL-	Case A. B. D	1 1	2	3	4	5	6	7	8	9	10	11	12	13	14		-	Test limits	
Subgroup	Syllibol	STD-883	Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11	Meas.		rest illillis	
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	Q	GND	Q	K2	K3	terminal	Min	Max	Unit
1 <u>2</u> /	V _{OH}	3006	1	0.8 V	Α		4.5 V			2.0 V	2.0 V	2.0 V		u	4 mA	0.8 V	0.8 V	Q	2.4		V
T _C = 25°C	"	"	2	2.0 V	A		u			0.8 V	0.8 V	0.8 V	4 mA	"		2.0 V	2.0 V	Q	и		и
"	"	"	3			0.8 V	u	2.0 V						ű	4 mA			Q	u		и
ű	и	"	4			2.0 V	и	0.8 V					4 mA	"				Ια	и		"
"	V _{OL}	3007	5	2.0 V	Α		"			0.8 V	0.8 V	0.8 V		"	16 mA	2.0 V	2.0 V	Q		0.4	"
и	"	"	6	0.8 V	Α		"			2.0 V	2.0 V	2.0 V	16 mA	"		0.8 V	0.8 V	ĪQ		"	"
"	"	"	7			0.8 V	"	2.0 V					16 mA	"				ī		"	"
"	"	"	8			2.0 V	"	0.8 V						"	16 mA			Q		"	"
"	V _{IC}	"	9				"			-12 mA				"				J1		-1.5	"
"	"	"	10				"				-12 mA			"				J2		"	и
"	"	"	11				"					-12 mA		ű				J3		"	u
"	"	"	12	-12 mA			"							"				K1		"	"
"	"	"	13				"							"		-12 mA		K2		"	"
	"	"	14				"							"			-12 mA	K3		"	
"		"	15			40. 4		-12 mA										Clear			"
"		"	16		40. 4	-12 mA								"				Preset		"	"
"			17	0.01/	-12 mA		"	4.5 V		4.5.1/	4.5.1/	4.5.1/		-		0.0.1/	0.01/	Clock			
"		3009	17 CKT B 18	0.8 V GND	A* 4.5 V		5.5 V	4.5 V B		4.5 V 0.4 V	4.5 V 4.5 V	4.5 V 4.5 V		"		0.8 V GND	0.8 V GND	Clock J1	-0.7	0.5 -1.6	A
"	I _{IL1}	3009	19	GND "	4.5 V		5.5 V	В		4.5 V	0.4 V	4.5 V 4.5 V	-	"		GND	GND	J2	-0.7	-1.0	mA "
"	"	"	20	"	"		"	В		4.5 V	4.5 V	0.4 V	1	"		GND	GND	J3	"	"	"
"	"	"	21	0.4 V	"	В	и	ь		GND	GND	GND		"		4.5 V	4.5 V	K1	"	"	и
"	и	"	22	4.5 V	u	В	и			GND	GND	GND		u		0.4 V	4.5 V	K2	и	u	и
"	"	"	23	4.5 V	"	В	"			GND	GND	GND		"		4.5 V	0.4 V	K3	u	"	u
"	I _{IL2}	"	24	4.5 V	0.4 V	В	и			4.5 V	4.5 V	4.5 V		u		4.5 V	4.5 V	Clock	-1.4	-3.2	mA
"	I _{II 2}	"	25	"	0.4 V		"	В		"	"	"		"		"	"	Clock	-1.4	-3.2	"
"	I _{II 3}	"	26 CKT A	u	4.5 V	0.4 V	"			"	"	"		"		"	"	Preset	-0.7	-1.6	"
"	"	"	26 CKT B	"	"	0.4 V	"			"	"	"		"		"	"	Preset	-1.4	-3.2	"
"	"	"	27 CKT A	"	"		"	0.4 V		"	"	"		"		"	"	Clear	-0.7	-1.6	"
"	"	"	27 CKT B	"	"		ű	0.4 V		"	"	"		"		"	"	Clear	-1.4	-3.2	и
"	I _{IH1}	3010	28		GND		"	GND		2.4 V	GND	GND		"				J1		40	μΑ
"	"	"	29		"		"	GND		GND	2.4 V	GND		"				J2		"	и
"	u	"	30		"		"	GND		GND	GND	2.4 V		"				J3		"	"
"	"	"	31	2.4 V	"	GND	"							"		GND	GND	K1		"	"
	"	"	32	GND	"	GND	"							u		2.4 V	GND	K2		"	и
"		"	33	GND	"	GND	"							"		GND	2.4 V	K3		"	"
	I _{IH2}	"	34				"	GND		5.5 V	GND	GND						J1		100	- "
		"	35		"		"	GND		GND	5.5 V	GND						J2		"	
	"	"	36	5.5.1	"	ONE	"	GND		GND	GND	5.5 V		"		ONE	ONE	J3		"	- "
	"		37 38	5.5 V GND	"	GND GND			1			 	-			GND 5.5 V	GND GND	K1 K2	1	"	
u	u	"	38	GND	"	GND	"		-			-		u		GND	5.5 V	K2 K3	-	"	и
"	 	"	40	4.5 V	Α	GIND	"	2.4 V	 	GND	GND	GND	1	"	1	4.5 V	4.5 V	Clear	1	80	и
"	I _{IH3}	"	41	GND	A	2.4 V	"	GND	 	4.5 V	4.5 V	4.5 V	1	"	1	GND	GND	Preset	1	80	"
"	I _{IH4}	"	42	GND	A	5.5 V	"	GND	 	4.5 V	4.5 V	4.5 V	1	"	1	GND	GND	Preset	1	200	"
и	'IH4 "	"	43	4.5 V	A	J.J V	u	5.5 V		GND	GND	GND		"		4.5 V	4.5 V	Clear		"	"
и	и	"	44	GND	5.5 V		"	GND	1	GND	GND	GND		"		GND	GND	Clock		"	и
u	u	"	45	GND	5.5 V	GND	и	OIVD	 	GND	GND	GND	1	u	 	GND	GND	Clock	 	u	и
	1	I	+5	GIND	J.J V	GIVD	1		I	GIND	GIND	GND	1	1	1	GIND	GIND	CIUCK	l		

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01. 1/- Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	I	-	Test limits	
Subgroup	Symbol	STD-883	Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11	Meas.		i est ilitilis	
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	Q	GND	Q	K2	K3	terminal	Min	Max	Unit
1	I _{IH5}	3010	46 CKT A	GND	2.4 V		5.5 V	GND		GND	GND	GND		GND		GND	GND	Clock	-50	-700	μА
T _C = 25°C	"	"	46 CKT B	u	"		u	GND		ű	"	"		"		"	u	"	-200	-850	"
u	"	"	46 CKT C	"	"		"	GND		"	"	"		"		"	"	"	-400	-1000	"
ű	"	"	47 CKT A	u	"	GND	u			"	"	"		u		и	"	ű	-50	-700	u
u	"	"	47 CKT B	"	"	GND	"			"	"	и		"		u	"	и	-200	-850	"
"		"	47 CKT C			GND	"			"	"			"			"	"	-400	-1000	
"	I _{os}	3011 3011	48 49	4.5 V 4.5 V	GND "	GND	5.5 V	GND		4.5 V 4.5 V	4.5 V 4.5 V	4.5 V 4.5 V	GND	"		4.5 V 4.5 V	4.5 V 4.5 V	Q Q	-20 -20	-57 -57	mA "
u								OND					OND	"					20		
"	I _{cc}	3005 3005	50 51	GND GND	"	GND	"	GND		GND GND	GND GND	GND GND		"		GND GND	GND GND	V _{CC}		20 20	- "
2	I _{CC}				roup 1 over	nt T _ 125	0C and V		mittad	GND	GND	GND	l	l		GND	GND	V _{CC}	1	20	
3			nditions and limits			•															
	Same test	s, terminai coi	nditions and limits																		
7 <u>2</u> / <u>4</u>			52	В	В	A	4.5 V	В	В	В	В	В	H <u>3</u> /	GND "	L <u>3/</u>	В	В	All	_	H or L	,
$T_C = 25^{\circ}C$			53 54	B B	B B	В	"	A A	B B	B B	B B	B B	L	"	H	B A	B A	output "	a	s shown <u>3</u>	
"			55	В	A	A A	"	A	В	В	В	В	L	"	H	A	A	66		"	
u			56	В	В	A	"	A	В	В	В	В	Ĺ	"	H	A	A	u		"	
"			57	A	В	A	u	A	В	В	В	В	Ē	u	H	В	A	"		"	
и			58	A	A	A	"	A	В	В	В	В	L	"	H	В	Α	"		"	
u			59	Α	В	Α	"	Α	В	В	В	В	L	"	Н	В	Α	"		"	
u			60	Α	В	Α	u	Α	В	В	В	В	L	"	Н	Α	В	"		"	
u			61	Α	Α	Α	"	Α	В	В	В	В	L	"	Н	A	В	и		u	
"			62	A	В	Α	"	Α	В	В	В	В	L	"	H	Α	В	u .		"	
"			63 64	A B	B B	A A	"	B A	B B	B B	B A	B A	H	"	L	A B	B B	u		"	
"			65	В	A	A	"	A	В	В	A	A	H	"	L	В	В	и		"	
ii .			66	В	В	A	"	A	В	В	A	A	H	и	<u> </u>	В	В	"		"	
"			67	В	В	A	ű	A	В	A	В	A	H	"	Ĺ	В	В	и		"	
u			68	В	Α	Α	"	Α	В	Α	В	Α	Н	"	L	В	В	ű		"	
"			69	В	В	Α	"	Α	В	Α	В	Α	Н	"	L	В	В	66		"	
u			70	В	В	Α	ű	Α	В	Α	Α	В	Η	u	L	В	В	"		u	
u			71	В	Α	Α	"	Α	В	Α	Α	В	Η	"	L	В	В	и		u	
"			72	В	В	A	"	A	В	A	A	В	Η:	"	L	В	В	u		"	
"			73 74	A	В	A A	"	A	В	A	A	A A	H H	"	L	A	A A	"		"	
"			75	A A	A B	A	"	A A	B B	A A	A A	A	L	"	H	A	A	и		"	
u			76	A	A	A	и	A	В	A	A	A	Ĺ	и	H	A	A	"		"	
44			77	A	В	A	u	A	В	A	A	A	H	u	L L	A	A	66		"	
"			78	Α	В	Α	u	В	В	Α	Α	Α	Н	"	L	Α	Α	"		"	
u			79	Α	Α	Α	u	В	В	Α	Α	Α	Н	u	L	Α	Α	"		"	
u			80	Α	В	Α	"	В	В	Α	Α	Α	Η	"	L	Α	Α	ii .		ű	
"		ļ	81	A	В	В	"	В	В	A	A	A	Н	"	Н	A	Α	"		"	
"		ļ	82	A	A	В	"	В	В	A	A	A	Н	"	Н	A	A	"		"	
"			83	A A	B A	B B	"	B	B B	A	A	A	H	"	H	A	A	"			
"	-	-	84 85	A	A	A A	"	A A	В	A A	A A	A	L	"	H	A	A A	"	-	"	
u		1	86	В	A	A	и	A	В	A	A	A	L	"	H	A	A	u		u	
u		 	87	В	A	A	u	A	В	В	A	A	Ĺ	"	H	A	A	ű	<u> </u>	и	
"			88	В	В	A	"	A	В	В	A	A	H	"	L	A	A	и		"	
u		İ	89	A	A	A	"	A	В	A	A	A	H	"	L	A	A	u		"	
u			90	Α	Α	Α	ű	Α	В	В	Α	Α	Н	"	L	Α	Α	u		"	

TABLE III. Group A inspection for device type 01. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	.s
	1	STD-883	Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{cc}	Clear	NC	J1	J2	J3	ā	GND	Q	K2	K3	terminal	Min	Max	Unit
7 <u>2</u> / <u>4</u> /			91	В	Α	Α	4.5 V	Α	В	В	Α	Α	Н	GND	L	Α	Α	All		H or L	
T _C = 25°C			92	В	В	Α	4.5 V	Α	В	В	Α	Α	L	GND	Н	Α	Α	output	,	As shown	<u>3</u> /
8 <u>2</u> / <u>4</u> /	Same test	s, terminal co	nditions and limits	as for sub	group 7, ex	cept T _C = 12	25 and -55	°C.													
9	F _{MAX} <u>5</u> /	(Fig. 5)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	2.4 V		GND	OUT	2.4 V	2.4 V	Q	10		MHz
$T_C = 25^{\circ}C$	F _{MAX} <u>5</u> /	(Fig. 5)	94	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"	Q	10		MHz
и	t _{PLH1}	3003	95	"	2.4 V	J	"	IN		"	"	"	OUT	"		"	"	Clear to Q	5	25	ns
u	t _{PLH1}	(Fig. 4)	96	"	"	IN	"	J		er.	"	"		"	OUT	"	"	Preset	и	25	u
44	4	"	97	"	"		"	IN		"	"	"		"	OUT	"	"	to Q Clear to Q	"	40	
u	t _{PHL1}	"	98	"	"	IN	"	IIN		"	"	"	OUT	"	001	"	"	Preset	и	40	
	PHL1		30										001					to Q		40	
"		3003	99	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"		"	30	ns
	t _{PLH2}	(Fig 5	99		IIN	3.0 V		5.0 V					001					Clock to Q		30	115
и	t _{PLH2}	"	100	"	"	u	"	"		"	u	"		u	OUT	u	"	Clock to Q	и	30	u
u	t _{PHL2}	"	101	"	"	"	"	"		"	"	"	OUT	"		"	"	Clock to Q	"	40	"
ű	t _{PHL2}	"	102	"	"	"	"	ű		ű	"	"		"	OUT	"	"	Clock to Q		40	u
10	F _{MAX} <u>5</u> /	(Fig 5)	103	"	"	"	"	"		"	"	"		"	OUT	"	"	Q	10		MHz
T _C = 125°C	F _{MAX} <u>5</u> /	(Fig 5)	104	"	"	"	"	"		"	"	"	OUT	"		"	"	Q	10		MHz
"	t _{PLH1}	3003 (Fig. 4)	105	"	2.4 V	J	"	IN		и	"	"	OUT	"		"	и	Clear to Q	5	39	ns
u	t _{PLH1}	"	106	"	"	IN	"	J		и	"	"		"	OUT	"	"	Preset to Q	и	39	u
"	t _{PHL1}	"	107	"	"	J	"	IN		"	"	"			OUT	"	"	Clear to Q	и	50	"
u	t _{PHL1}	"	108	"	"	IN	"	J		"	"	"	OUT	"		"	"	Preset to Q	"	50	"
ű	t _{PLH2}	(Fig 5)	109	"	IN	5.0 V	"	5.0 V		"	"	"	OUT	"		"	"		"	39	ns
	YFLFIZ	, ,									"							Clock to Q			
"	t _{PLH2}	"	110 111	"	"	"	"	"		"	"	"	OUT	"	OUT	"	"	Clock to Q	"	39 50	- "
	t _{PHL2}	**				-						-	001	-			-	Clock to Q	-		
u	t _{PHL2}	"	112	"	"	"	"	ű		ű		"		"	OUT	"	ű	Clock to Q	"	50	"

NOTES:

A = Normal clock pulse. B = Momentary GND, then 4.5 V.

 $J = Input pulse t_p = 100 ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V$

*After clock pulse apply –12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).

- $1\!/$ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open). $2\!/$ Input voltages shown are: A= 2.0 volts minimum and B = 0.8 volts maximum.
- $\frac{3}{2}$ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double camparator; or (b) $H \ge 1.5$ V and L < 1.5 V when using a high speed checker single comparator.
- 4/ Tests shall be performed in sequence.
 5/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		-	Test limits	
- 20g. 00p	,	STD-883	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas.			
		method	Test No.	Clock 1	Clear 1	K1	V _{cc}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
1	V _{OH}	3006	1	Α		0.8 V	4.5 V							GND	4 mA		2.0 V	Q	2.4		V
$T_C = 25^{\circ}C$	"	"	2	Α		2.0 V	"							"		4 mA	0.8 V	Q 1	"		"
и	и	"	3		0.8 V		"							"		4 mA		 Q 1	и		и
"	u	"	4				u	Α		2.0 V		4 mA	0.8 V	u				Q2	u		u
и	"	"	5				"	Α		0.8 V	4 mA		2.0 V	"				Q 2	"		"
ű	"	"	6				"		0.8 V		4 mA			"					"		"
"	Vol	3007	7	Α		2.0 V	u							"	16 mA		0.8 V	Q1		0.4	"
"	ű	"	8	Α		0.8 V	"							"		16 mA	2.0 V	Q 1		"	"
u	u	"	9		0.8 V		и							"	16 mA			Q1		"	"
"	"	"	10				u	Α		0.8 V		16 mA	2.0 V	u				Q2		u	и
"	"	"	11				"	Α		2.0 V	16 mA		0.8 V	"				Q 2		"	"
"	u	"	12				и		0.8 V			16 mA		u				Q2		u	"
"	V _{IC}		13				"							"			-12 mA	J1		-1.5	"
"	"		14			40. 4	"			-12 mA				"				J2		"	"
"			15 16			-12 mA	"						-12 mA	"				K1 K2		"	"
"	u		17		-12 mA		u						-12 IIIA	"				Clear 1		"	"
			18	-12 mA	12 117 (u							"				Clock 1		"	
u	"		18 CKT B	A*	4.5 V	0.8 V	"							"			4.5 V	Clock 1		-0.5	"
"	u		19				u		-12 mA					u				Clear 2		-1.5	"
"	"		20				"	-12 mA						"				Clock 2		-1.5	"
"	- "	0000	20 CKT B	F/	451/			A*	4.5 V	4.5 V			0.8 V	"			0.417	Clock 2	0.7	-0.5	4
"	I _{IL1}	3009	21 22	<u>5</u> /	4.5 V 4.5 V	0.4 V	5.5 V							"			0.4 V	J1 K1	-0.7	-1.6	mA "
"	"	"	23	<u> </u>	4.5 V	0. 4 V	"	5/	4.5 V	0.4 V				"				J2	"	"	"
"	"	"	24				"	5/	4.5 V				0.4 V	"				K2	"	"	"
и	I_{IL2}	11	25	0.4 V	В	4.5 V	и							ii .			4.5 V	Clock 1	-1.4	-3.2	"
"	I _{IL2}	"	26				"	0.4 V	В	4.5 V			4.5 V	"				Clock 2	-1.4	-3.2	"
"	I _{IL3}	"	27 CKT A, C 27 CKT B	4.5 V 4.5 V	0.4 V 0.4 V		"							"			4.5 V 4.5 V	Clear 1	-0.7 -1.4	-1.6 -3.2	- "
"	u	"	28 CKT A, C	4.5 V	0.4 V		"	4.5 V	0.4 V	4.5 V				"			4.5 V	Clear 1 Clear 2	-0.7	-3.2 -1.6	"
"	"	"	28 CKT B				"	4.5 V	0.4 V	4.5 V				"				Clear 2	-1.4	-3.2	"
"	I _{IH1}	3010	29	GND	GND		5.5 V		-					"			2.4 V	J1		40	μА
"	ű	44	30	GND	В	2.4 V	u							u				K1		u	и
"	"	"	31				"	GND	GND	2.4 V				"				J2		"	"
"		"	32	OND	OND			GND	В				2.4 V				F F \/	K2			- "
"	I _{IH2}	"	33 34	GND GND	GND B	5.5 V	"							"			5.5 V	J1 K1		100	"
"	u	"	35	0.10		0.0 *	"	GND	GND	5.5 V				"				J2		"	u
"	u	"	36				"	GND	В				5.5 V	"				K2		"	u
"	I _{IH3} 7/	"	37	GND	Е		"							"			GND	Clear 1		80	u
"	I _{IH3} <u>7</u> /	"	38				"	GND	E	GND				"				Clear 2		80	и
"	I _{IH4}	"	39	5.5 V	5.5 V	GND	"							"			GND	Clock 1		200	"
	"	"	40 41	GND	Е		"	5.5 V	5.5 V	GND			GND	"	-		GND	Clear 1 Clock 2		"	- "
"	"	"	42	<u> </u>			"	GND	5.5 V	GND			GIND	"				Clear 2		"	"
"	I _{IH5}	u	43 CKT A, C	2.4 V	Е	GND	и							ű			GND	Clock 1	-50	-700	"
u	"	"	43 CKT B	2.4 V	2.4 V	GND	"							ű			GND	Clock 1	-200	-850	u
"	"	"	44 CKT A, C				"	2.4 V	E	GND			GND	"				Clock 2	-50	-700	- "
"		"	44 CKT B		1			2.4 V	2.4 V	GND			GND		l	l		Clock 2	-200	-850	

TABLE III. Group A inspection for device type 02. 1/ - Continued.

ubgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		· ·	Test limits	S
		STD-883 method	Case C Test No.	1 Clock 1	2 Clear 1	3 K1	V _{CC}	5 Clock 2	6 Clear 2	7 J2	8	9 Q2	10 K2	11 GND	12 Q1	13 —	14 J1	Meas. terminal	Min	Max	1
								Olock 2	Oleai Z	32	Q ₂	QZ	11/2		Q i	Q 1					
1 = 25°C	I _{os}	3011	45	2.4 V	GND	2.4 V	5.5 V							GND		GND	2.4 V	Q 1	-20	-57	
"	u	3011**	46	Α	4.5 V	0	ű							"	GND		4.5 V	Q1	u	"	T
и	"	3011**	47				"	GND	4.5 V	4.5 V		GND	0 V	"				Q2	"	"	T
"	"	3011	48				"	2.4 V	GND	2.4 V	GND		2.4 V	u				Q 2	"	"	
и	I _{cc}	3005	49	D	4.5 V	GND	u	D	4.5 V	4.5 V			GND	u			4.5 V	V _{cc}		40	+
2	Same test	s, terminal cor	nditions and limits	as for subg	roup 1, exc	ept T _C = 12	5ºC and V	_{IC} tests are o	omitted.												
3	Same test	s, terminal cor	nditions and limits	as for subg	roup 1, exc	ept T _C = -5	5ºC and V₁	c tests are o	mitted.												
2/4/			50	В	В	В	4.5 V	В	В	Α	H 3/	L 3/	В	GND	L 3/	H 3/	Α	All		H or L	_
= 25°C			51	A	В	В	"	A	В	A	H		В	"	L L	H	A	output	а	s shown (3/
		1	52	В	В	В	"	В	В	A	Н	Ē	В	"	L	Н	A	"		"	_
"			53	В	В	A	"	В	В	A	Н	Ē	A	"	L	Н	A	u		"	_
"			54	Α	В	Α	u	Α	В	Α	Н	L	Α	"	L	Н	Α	"		"	Τ
"			55	В	В	Α	"	В	В	Α	Н	L	Α	"	L	Н	Α	"		"	_
"			56	В	Α	Α	"	В	Α	Α	Н	L	Α	"	L	Н	Α	"		"	
u			57	Α	Α	Α	u	Α	Α	Α	Н	L	Α	u	L	Н	Α	"		и	
"			58	В	Α	Α	"	В	Α	Α	L	Н	Α	"	Н	L	Α	"		"	
"			59	Α	Α	Α	"	Α	Α	Α	L	Н	Α	"	Н	L	Α	"		"	
"			60	В	Α	Α	u	В	Α	Α	Н	L	Α	"	L	Н	Α	и		"	
"			61	Α	Α	Α	"	Α	Α	Α	Н	L	Α	"	L	Н	Α	"		"	
"			62	В	Α	Α	"	В	Α	Α	L	Н	Α	"	Н	L	Α	"		"	
"			63	В	Α	В	"	В	A	В	L	Н	В	"	Н	L	В	"		"	_
u			64	Α	Α	В	"	Α	Α	В	L	Н	В	"	Н	L	В	"		"	
"			65	В	Α	В	"	В	Α	В	L	Н	В	"	Н	L	В	"		"	_
"			66	В	В	В	"	В	В	В	H	L.	В	"	<u> </u>	H	В	"		"	_
			67	В	A	В	"	В	A	В	Н	L	В	"	<u> </u>	H	В				_
"			68	A	A	В		A	A	В	Н	L	В	"	Ŀ	H	В	"			_
"			69	В	A	В	"	В	A	В	H	L	В	"	<u> </u>	H	В	"		"	_
			70	В	A	В	"	В	A	A	Н	L	В	"	<u> </u>	H	A	"		"	_
			71	A	A	В	"	A	A	A	Н	L	В	"	L	H	A	"			_
"			72	B B	A	B A	"	B B	A A	A B	L	H H	B A	"	H H	-	A B	"		"	_
и			73 74	A	A	A	"	A	A	В	L L	H	A	"	H	L L	В	"		и	_
"		+	75	В	A	A	"	В	A	В	H	L	A	"	I I	H	В	44		"	_
"			76	A	В	A	"	A	В	A	H	L I	A	"	-	H	A	"		"	-
u		 	77	A	A	A	u	A	A	A	Н	L	A	u	i	Н	A	и	 	"	-
"		-	78	A	A	A	"	A	A	В	H	Ŀ	A	"	i	H	В	u		"	-
"			79	A	A	В	"	A	A	В	H	ī	В	"	ī	H	В	"		"	-
"			80	В	A	В	"	В	A	В	Ĺ	H	В	"	H	i	В	"		"	_
u			81	Ā	A	A	"	A	A	A	L	H	A	"	H	L	A	"		"	_
íí .			82	A	A	В	u	A	A	A	L	H	В	u	H	Ŀ	A	"		"	-
"			83	A	A	В	u	A	A	В	L	H	В	u	H	L	В	"		"	-
u		1	84	В	A	В	u	В	A	В	H	Ľ	В	u	Ĺ	H	В	"		"	-
"			85	A	A	В	u	A	A	A	H	Ī	В	"	Ī	H	A	66		"	-
ii .			86	В	A	В	u	В	A	A	L	H	В	u	H	L L	A	"		"	-
"			87	A	A	В	u	A	A	A	Ĺ	H	В	u	H	Ĺ	A	"		"	_
"			88	Α	В	В	"	A	В	A	Н	-	В	u	-	H	A	"		"	_

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL- STD-883	Case A, B, D Case C	1	2	3	4	5 5	6	7	8	9	10 10	11 11	12 12	13 13	14 14	Meas.		Test limit	s
		method	Test No.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
9	F _{MAX} <u>6</u> /	(Fig 7)	89	IN		2.4 V	5.0 V				-			GND	OUT		2.4 V	Q ₁	10		MHz
$T_C = 25^{\circ}C$	u	"	90	IN		2.4 V	"							"		OUT	2.4 V	Q 1	"		"
u	u	u	91				u	IN		2.4 V		OUT	2.4 V	"				Q_2	и		"
"	"	"	92				"	IN		2.4 V	OUT		2.4 V	"				Q 2	"		"
и	t _{PLH1}	3003	93	IN	IN	GND	"							"		OUT	2.4 V	Clear 1	5	25	"
		(Fig 6)																to Q 1			
"	t _{PLH1}	"	94				44	IN	IN	2.4 V	OUT		GND	"				Clear 2 to Q 2	"	25	"
"	t _{PHL1}	"	95	IN	IN	GND	"							"	OUT		2.4 V	to Q 2 Clear 1	u	40	"
"		u				0.15	и	15.1	15.1	0.41/		O. I.	OND	"				to Q1	и		
-	t _{PHL1}	-	96					IN	IN	2.4 V		OUT	GND	-				Clear 2 to Q2	-	40	
u	t _{PLH2}	3003 (Fig 7)	97	IN	5.0 V	2.4 V	44							"	OUT		2.4 V	Clock 1 to Q1	u	30	"
"	и	(1.19.7)	98	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1	u	"	"
																		to Q 1			L
"	"	"	99				u	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2 to Q2	"	"	"
"	"	"	100				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	u	"	"
																		to Q 2			<u></u>
	t _{PHL2}		101	IN	5.0 V	2.4 V	"								OUT		2.4 V	Clock 1 to Q1		40	ı
u	и	"	102	IN	5.0 V	2.4 V	"							"		OUT	2.4 V	Clock 1	"	"	"
u	u	"	400				"	15.1	5.0.1/	0.41/		OUT	0.41/	"				to Q 1	u	"	
	-		103				-	IN	5.0 V	2.4 V		OUT	2.4 V	-				Clock 2 to Q2	-	-	
u	u	"	104				"	IN	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	"	"	"
10	F 6/	/F:~ 7\	105	IN		2.4 V	"							"	OUT		2.41/	to Q 2	10		MHz
10 T _C = 125°C	F _{MAX} <u>6</u> /	(Fig 7)	105 106	IN		2.4 V 2.4 V	и							и	001	OUT	2.4 V 2.4 V	Q1 Q 1	10		IVITZ
"	u	u	107				"	IN		2.4 V		OUT	2.4 V	"				Q1 Q2	и		"
u	и	и	108				и	IN		2.4 V	OUT	001	2.4 V	и				Q 2	и		"
"	t _{PLH1}	3003	109	IN	IN	GND	и							"		OUT	2.4 V	Clear 1	5	39	ns
		(Fig 6)																to Q 1			1
"	t _{PLH1}	"	110				"	IN	IN	2.4 V	OUT		GND	"				Clear 2	и	39	u
																		to Q 2			
"	t _{PHL1}	"	111	IN	IN	GND	"							"	OUT		2.4 V	Clear 1 to Q1	"	50	"
"	t _{PHL1}	"	112				и	IN	IN	2.4 V		OUT	GND	"				Clear 2	и	50	ii
ш	t _{PLH2}	3003	113	IN	5.0 V	2.4 V	и							"	OUT		2.4 V	to Q2 Clock 1	и	39	u
и	и	(Fig 7)	114	IN	5.0 V	2.4 V	и							"		OUT	2.4 V	to Q1 Clock 1	u	"	ш
				"'	0.0 .													to Q 1			ĺ
"	и	"	115				u	IN	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2	u	"	"
и	и	"	116				и	IN	5.0 V	2.4 V	OUT		2.4 V	"				to Q2 Clock 2	u	"	"
			110					",	0.0 1	2.7 V	001		2.7 0					to Q 2			İ

TABLE III. Group A inspection for device type 02. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	3
		STD-883	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas.			
		method	Test No.	Clock 1	Clear 1	K1	V _{cc}	Clock 2	Clear 2	J2	Q ₂	Q2	K2	GND	Q1	Q 1	J1	terminal	Min	Max	Unit
10 T _C = 125°C	t _{PHL2}	3003	117	IN	5.0 V	2.4 V	5.0 V							GND	OUT		2.4 V	Clock 1 to Q1	5	50	ns
66	и	и	118	IN	5.0 V	2.4 V	44							и		OUT	2.4 V	Clock 1 to Q 1	и	"	и
"	"	"	119				u	IN	5.0 V	2.4 V		OUT	2.4 V	и				Clock 2 to Q2	u	u	и
66	и	и	120				и	IN	5.0 V	2.4 V	OUT		2.4 V	и				Clock 2 to Q 2	и	"	и
11	Same test	s, terminal cor	nditions and limits	as for subg	roup 10, ex	cept T _C = -55	5°C.														

NOTES:

- A = Normal clock pulse.
- B = Momentary GND, then 4.5 V. C = This note has been deleted.
- D = Momentary 4.5 V, then GND.
- E = Momentary ground, then 2.4 V. F = Momentary ground, then 5.5 V.
- J = This note has been deleted.
- * After clock pulse apply -12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).
- ** Test time limit ≤ 100 ms.
- 1/ Terminal conditions (pins not designated may be H \geq 2.0 V, or L \leq 0.8 V, or open.) 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
- 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) $H \ge 1.5 \text{ V}$ and L < 1.5 V when using a high speed checker single comparator.
- 4/ Tests shall be performed in sequence.
 5/ Input shall be one normal clock pulse, then 4.5 V
- 6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall ge one-half of the input frequency. 7/ For CKT A, I_{IH3} limits are 0 to 120 µA.

TABLE III. Group A inspection for device type 03. 1/

Subgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	s
Subgroup	Cymbol	STD-883 method	Test No.	J1	Q 1	Q1	K1	Q2	Q ₂	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{cc}	Meas. terminal	Min	Max	Unit
1	V _{OH}	3006	1	2.0 V		4 mA	0.8 V			GND					Α		4.5 V	Q1	2.4		V
$T_C = 25^{\circ}C$	"	"	2	0.8 V	4 mA		2.0 V			"					Α		"	Q 1	"		"
и	и	"	3		4 mA					"						0.8 V	"	Q 1	"		"
"	"	"	4					4 mA		и	2.0 V	Α		0.8 V				Q2	и		££
"	"	"	5					1117 (4 mA	u	0.8 V	A		2.0 V			"	Q 2	u		"
"	u	"	6						4 mA	"			0.8 V						"		и
			U						4 111/4				0.8 V					Q 2			
и	V _{OL}	3007	7	0.8 V		16 mA	2.0 V			u					Α		"	Q1		0.4	"
"	"	"	8	2.0 V	16 mA		0.8 V			"					Α			Q 1		"	"
"	"	"	9			16 mA				"						0.8 V	"	Q1		"	"
u	"	"	10					16 mA		"	0.8 V	Α		2.0 V				Q2		"	"
ű	"	u	11						16 mA	"	2.0 V	Α		0.8 V			"	Q 2		**	"
"	"	"	12					16 mA		u			0.8 V					Q2		"	"
u	V _{IC}		13	-12 mA						"							"	J1	1	-1.5	-
44	"		14				-12 mA			"								K1		"	
"	и		15							и	-12 mA						"	J2		"	,
"	"		16							"				-12 mA				K2		"	
u	u		17							и						-12 mA	"	Clear 1		"	
"			18							"					-12 mA			Clock 1		44	
"	"		18 CKT B	4.5 V			0.8 V			"					A*	4.5 V	"	Clock 1		-0.5	
	"		19							"			-12 mA				"	Clear 2		-1.5	<u> </u>
"	"		20							"	4.5.7	-12 mA	4.5.1	0.01/			"	Clock 2		-1.5	<u> </u>
"		3009	20 CKT B	0.4 V						"	4.5 V	A*	4.5 V	0.8 V	5/	4.5 V	5.5 V	Clock 2 J1	0.7	-0.5 -1.6	<u> </u>
"	I _{IL1}	3009	21 22	0.4 V			0.4 V			"					<u>5</u> /	4.5 V	5.5 V	K1	-0.7	-1.6	m
u	"	"	23				0.4 V			"	0.4 V	<u>5</u> /	4.5 V		<u> </u>	4.5 V	"	J2	"	"	
u	и	и	24							и	0.4 V	<u>5</u> /	4.5 V	0.4 V			u	K2	"	"	-
"	I _{II 2}	"	25	4.5 V			4.5 V			"		<u> </u>	4.0 0	0.4 V	0.4 V	В	"	Clock 1	-1.25	-3.2	
"	I _{II 2}	"	26							"	4.5 V	0.4 V	В	4.5 V	****		"	Clock 2	-1.25	-3.2	_
"	I _{II.3}	"	27 CKT A, C	4.5 V						"					4.5 V	0.4 V	"	Clear 1	-0.7	-1.6	
u	и	"	27 CKT B	4.5 V						и					4.5 V	0.4 V	"	Clear 1	-1.4	-3.2	
u	u	"	28 CKT A, C							u	4.5 V	4.5 V	0.4 V				"	Clear 2	-0.7	-1.6	
"	"	u	28 CKT B							"	4.5 V	4.5 V	0.4 V				"	Clear 2	-1.4	-3.2	
"	I _{IH1}	3010	29	2.4 V						"					GND	GND	"	J1		40	μ
"	u	"	30				2.4 V			"					GND	В	"	K1		"	
"	"	"	31 32							"	2.4 V	GND GND	GND B	2.4 V				J2 K2			
"	-	u	33	5.5 V						и		GND	В	2.4 V	GND	GND	"	J1	<u> </u>	100	
"	I _{IH2}	44	34	3.5 V			5.5 V			"					GND	B	"	K1	1	"	_
"	"	"	35				J.J V			и	5.5 V	GND	GND		GIND	В	u	J2		и	-
"	"	"	36							"	0.0 1	GND	В	5.5 V			"	K2		"	
"	I _{IH3} 7/	u	37	GND						"			<u> </u>		GND	Е	"	Clear 1	1	80	
ш	I _{IH3} 7/	"	38							"	GND	GND	Е			- -	"	Clear 2		80	
"	I _{IH4}	"	39	GND			GND			"					5.5 V	GND	"	Clock 1		200	
"	"	"	40	GND						"					GND	F	"	Clear 1		"	
"	"	"	41							u	GND	5.5 V	GND	GND			"	Clock 2		"	
"	u	u	42							u	GND	GND	F				"	Clear 2		"	
"	I _{IH5}	"	43 CKT A, C	GND			GND			u					2.4 V	GND	"	Clock 1	-50	-700	
u	u	"	43 CKT B	GND			GND			"					2.4 V	GND	"	Clock 1	-200	-850	,
"	и	"	44 CKT A, C							"	GND	2.4 V	GND	GND			"	Clock 2	-50	-700	
"	"	"	44 CKT B	l	1			l	1	"	GND	2.4 V	GND	GND	l		"	Clock 2	-80	-850	1

TABLE III. Group A inspection for device type 03. 1/- Continued.

ubgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	
		STD-883 method	Test No.	J1	Q ₁	Q1	K1	Q2	\overline{Q}_2	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{cc}	Meas. terminal	Min	Max	U
1	Ios	3011	45	2.4 V	GND		2.4 V			"					2.4 V	GND	5.5 V	Q 1	-20	-57	n
= 25°C	"	3011 *	46	4.5 V	GND	GND	0 V			"					Α	4.5 V	"	Q1	"		1
"	"	3011 *	47					GND	GND	"	4.5 V	Α	4.5 V	2.4 V			"	Q2	"		+
"	u	3011	48						GND	u	2.4 V	2.4 V	GND	0 V				Q 2	"		
u	I _{CC}	3005	49	4.5 V			GND			"	4.5 V	D	4.5 V	GND	D	4.5 V	"	V _{CC}		40	+
2	Same test	s, terminal cor	ditions and limits	as for subg	roup 1, exc	ept T _C = 125	°C and V _{IC} t	ests are om	itted.												
3	Same test	s, terminal cor	ditions and limits	as for subg	roup 1, exc	ept T _C = -55°	C and V _{IC} te	ests are omi	itted.												
<u>2</u> / <u>4</u>			50	Α	H <u>3</u> /	L <u>3</u> /	В	L <u>3</u> /	H <u>3</u> /	GND	Α	В	В	В	В	В	4.5 V	All		H or L	
= 25°C			51	Α	Н	L	В	L	Н	"	Α	Α	В	В	Α	В	"	output	а	s shown	ı <u>3</u> /
"			52	A	Н	L	В	L	Н	"	Α	В	В	В	В	В	"	"		"	
"			53	Α	Н	L	Α	L	Н	ű	Α	В	В	Α	В	В	"	"		"	
u			54	Α	Н	L	Α	L	Н	"	Α	Α	В	Α	Α	В	"	"		"	
			55	A	Н	L	A	L	Н	"	A	В	В	A	В	В	"	"			
"			56	A	H	<u> </u>	A	L L	H		A	В	A	A	В	A		"		"	
"			57	A	H	L.	A	L	H	"	A	A	A	A	A	A	"	"			_
"			58 59	A	L	H H	A	H	L	"	A	В	A	A	В	A	"	"		"	
u			60	A	H	L	A	L	L H	"	A A	A B	A	A	A B	A	"	u		"	_
"			61	A	H	L	A	L	Н	"	A	A	A	A	A	A	"	"		"	
"			62	A	L	Н	A	H	L	"	A	В	A	A	В	A	"	44		"	_
u			63	В	-	H	В	H	L	"	В	В	A	В	В	A	"	44		"	_
"			64	В	-	H	В	H	i i	"	В	A	A	В	A	A	ű	"		"	_
u			65	В	ī	H	В	H	Ĺ	"	В	В	A	В	В	A	"	"		"	_
u			66	В	H	i.	В	L L	H	"	В	В	В	В	В	В	"	"		"	_
u			67	В	H	ī	В	Ī	H	"	В	В	A	В	В	A	u	"		"	_
"			68	В	Н	L	В	L	Н	"	В	A	A	В	A	Α	"	"		"	
"			69	В	Н	L	В	L	Н	"	В	В	A	В	В	Α	"	"		"	
u			70	Α	Н	L	В	L	Н	"	Α	В	Α	В	В	Α	"	"		"	
u			71	Α	Н	L	В	L	Н	"	Α	Α	Α	В	Α	Α	"	"		"	
"			72	Α	L	Н	В	Н	L	u	Α	В	Α	В	В	Α	"	"		"	
"			73	В	L	Н	Α	Н	L	"	В	В	Α	Α	В	Α	"	"		"	
u			74	В	L	Н	Α	Н	L	"	В	Α	Α	Α	Α	Α	"	"		u	
"			75	В	Н	L	Α	L	Н	"	В	В	Α	Α	В	Α	"	"		"	
"		ļļ	76	A	Н	L	A	L	Н	"	A	A	В	A	A	В	"	и		"	
			77	A	H	L.	A	L	Н	"	A	A	A	A	A	A					
u			78	В	H	L.	A	L L	H	"	В	A	A	A	A	A	"	"		"	
"			79	В	H	L	В	L	H		В	A	A	В	A	A				"	
"			80	В	L L	H	В	H	L		В	В	A	В	В	A	"	"			
"			81	A	L	H	A	H	L	"	A	A	A	A B	A	A	"	"	-	"	
"		 	82	A B	-	H	В	H	L		A	A	A		A	A	"	"	 	"	
u			83 84	В	H	H L	B B	H	H	и	<u>В</u> В	A B	A	B B	A B	A	"	"		"	
"			84 85	A	H	L	В	L	H	"	A	A	A	В	A	A	"	44		"	
"			86	A	<u>п</u>	H	В	H		u	A	В	A	В	В	A	"	"		"	
"			87	A	-	H	В	H	-	"	A	A	A	В	A	A	"	66		"	
	ı		88	A	Н	- !!	В	- !!	H		A	A	В	В	A	В				"	_

TABLE III. Group A inspection for device type 03. 1/- Continued.

Subgroup	Symbol	MIL-	Case C	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	is
		STD-883 method	Test No.	J1	Q ₁	Q1	K1	Q2	Q ₂	GND	J2	Clock 2	Clear 2	K2	Clock 1	Clear 1	V _{cc}	Meas. terminal	Min	Max	Unit
9	F_{MAX}	(Fig. 7) <u>6</u> /	89	2.4 V		OUT	2.4 V			GND					IN	5.0 V	5.0 V	Q1	10		MHz
$T_C = 25^{\circ}C$	"	"	90	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Q ₁	"		"
u	"	"	91					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Q2	"		"
u	"	"	92						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Q ₂	"		"
íí.	t _{PLH}	3003 (Fig. 6)	93	2.4 V	OUT		GND			"					Α	IN	"	Clr 1 to Q 1	5	25	ns
u	t _{PLH}	"	94						OUT	"	2.4 V	Α	IN	GND			"	Clr 2 to Q 2	u	25	"
u	t _{PHL}	"	95	2.4 V		OUT	GND			u					Α	IN	"	Clr 1 to Q1	и	40	и
u	t _{PHL}	и	96					OUT		"	2.4 V	Α	IN	GND			"	Clr 2 to Q2	u	40	"
и	t _{PLH}	3003	97	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	5	30	ns
"	"	(Fig. 7)	98	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to Q 1	u	44	"
"	"	"	99					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	ű	"	"
u	"	"	100						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	"	"	"
u	t _{PHL}	"	101	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	ű	40	u
и	"	"	102	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to Q 1	"	"	"
"	"	"	103					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
и	"	"	104						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	"	"	"
10	F_{MAX}	(Fig. 7) <u>6</u> /	105	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Q1	10		MHz
$T_C = 125^{\circ}C$	"	"	106	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Q ₁	"		"
u	"	"	107					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Q2	"		"
u	"	"	108						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Q ₂	u		"
"	t _{PLH}	3003 (Fig 6)	109	2.4 V	OUT		GND			и					А	IN	и	Clr 1 to Q 1	5	39	ns
u	t _{PLH}	(1 19 0)	110						OUT	"	2.4 V	Α	IN	GND			"	Clr 2 to Q 2	u	39	"
"	t _{PHI}	"	111	2.4 V		OUT	GND			"					Α	IN	"	Clr 1 to Q1	"	50	"
"	t _{PHI}	"	112					OUT		"	2.4 V	Α	IN	GND			"	Clr 2 to Q2	"	50	"
u	t _{PLH}	3003	113	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	5	39	ns
u	"	(Fig 7)	114	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to Q 1	"	"	"
u	"	"	115					OUT		и	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	и	"	ш
ű	"	"	116						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	"	"	"
u	t _{PHL}	u	117	2.4 V		OUT	2.4 V			"					IN	5.0 V	"	Clk 1 to Q1	u	50	"
ű	"	и	118	2.4 V	OUT		2.4 V			"					IN	5.0 V	"	Clk 1 to Q 1	"	"	"
и	"	u	119					OUT		"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q2	"	"	"
"	"	и	120						OUT	"	2.4 V	IN	5.0 V	2.4 V			"	Clk 2 to Q 2	**	"	"

NOTES:

- A = Normal clock pulse.

- A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.
 C = This note has been deleted.
 D = Momentary 4.5 V, then GND.
 E = Momentary ground, then 2.4 V.
 F = Momentary ground, then 5.5 V.
- * After clock pulse apply -12 mA to clock pin to insure \overline{Q} is still in the low state (see figure 15).
- ** Test time limit ≤100 ms.

- 1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b)
 H≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.
- 4/ Tests shall be performed in sequence.

- g/ Tests shall be performed in sequence.
 5/ One normal clock pulse, then 4.5 V.
 6 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
 7/ For CKT A, I_{IH3} limits are 0 to 120 μA.

TABLE III. Group A inspection for device type 04. 1/

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Т	est limits	
Cubgroup	Cymbol	STD-883	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas.	Min	Max	Unit
1	V _{OH}	method 3006	1	Α			2.0 V	4.5 V					~ -			GND	~ .	4 mA	0.8 V	terminal Q1	2.4		V
T _C = 25°C	"	"	2	Α			0.8 V	"								u	4 mA		2.0 V	Q 1	"		"
"	"	"	3		2.0 V	0.8 V		"								"	4 mA			Q 1	"		"
"	u	u	4		0.8 V	2.0 V		"								"		4 mA		Q 1 Q1	44		"
"	"	"	5		U.0 V	2.0 V		"	Α			2.0 V		4 mA	0.8 V	"		4 IIIA		Q2	"		"
"	"	"	6					"	Α			0.8 V	4 mA		2.0 V	"				Q 2	"		"
"	и	и	7					"		2.0 V	0.8 V		4 mA			"					44		u
"	u	"	8					"		0.8 V	2.0 V			4 mA		u				Q2	"		"
"	V _{OL}	3007	9	Α			0.8 V	"		0.0 +	2.0 1					и		16 mA	2.0 V	Q1		0.4	"
u	"	u	10	A			2.0 V	и								u	16 mA		0.8 V	Q 1		"	"
u	и	44	11		0.8 V	2.0 V		"								"	16 mA			Q 1		"	"
и	и	и	12		2.0 V	0.8 V		и								u		16 mA		Q1		"	"
"	u	"	13					"	Α			0.8 V		16 mA	2.0 V	u				Q2		"	"
"	"	"	14					"	Α			2.0 V	16 mA		0.8 V	"				Q 2		"	и
"	"	"	15					"		0.8 V	2.0 V		16 mA			"				Q 2		"	и
"	u	и	16					"		2.0 V	0.8 V			16 mA		и				Q2		"	"
u	V _{IC}		17				-12 mA	"								"				J1		-1.5	"
"	u		18					"								u			-12 mA	K1		"	"
"	и		19					"				-12 mA				ű				J2		"	"
"	u		20					"							-12 mA	ű				K2		"	"
"	"		21	-12 mA				"								u				Clock 1		"	"
"	"		22		-12 mA	40 4		"								"				Preset 1		"	- "
	"		23			-12 mA		"	40 m A							"	 			Clear 1		"	
"	и		24 25					"	-12 mA	-12 mA						и				Clock 2 Preset 2		"	"
"	и		26					"		-12 IIIA	-12 mA					и				Clear 2		**	"
u	I _{II 1}	3009	27	4.5 V		В	0.4 V	5.5 V			-12111/4					и				J1	-0.7	-1.6	mA
"	"IL1	"	28	4.5 V	В	4.5 V	0.4 0	"								"			0.4 V	K1	"	"	"
"	и	и	29					"	4.5 V		В	0.4 V				u				J2	"	"	"
"	"	"	30					"	4.5 V	В	4.5 V				0.4 V	и				K2	"	"	"
"	I _{IL2}	"	31	0.4 V	В		4.5 V	"								"			4.5 V	Clock 1	-1.25	-3.2	"
"	u	"	32	0.4 V		В	4.5 V	"								и			4.5 V	Clock 1	"	"	"
и	и	и	33					"	0.4 V	В		4.5 V			4.5 V	"				Clock 2	"	"	"
"	"	"	34					"	0.4 V		В	4.5 V			4.5 V	"				Clock 2	"	"	"
"	I _{IL3}	"	35 A, C	4.5 V		0.4 V	4.5 V	"								"			4.5 V	Clear 1	-0.7	-1.6	- "
44	u	"	35 B	4.5 V	0.417	0.4 V	4.5 V	"	ļ						ļ	"	ļ	ļ	4.5 V	Clear 1	-1.4	-3.2	
		"	36 A, C	4.5 V	0.4 V		4.5 V	"	 					1	 	"	1	-	4.5 V	Preset 1	-0.7	-1.6	
"	"	"	36 B 37 A, C	4.5 V	0.4 V		4.5 V	"	4.5 V		0.4 V	4.5 V		-	4.5 V	"			4.5 V	Preset 1 Clear 2	-1.4 -0.7	-3.2 -1.6	u
"	"	"	37 A, C	1				"	4.5 V 4.5 V		0.4 V 0.4 V	4.5 V 4.5 V	 	-	4.5 V	"	}	 	 	Clear 2	-0.7	-3.2	"
"	"	и	38 A, C					"	4.5 V	0.4 V	U.4 V	4.5 V			4.5 V	и				Preset 2	-0.7	-3.2	ш
"	"	"	38 B	1				"	4.5 V	0.4 V		4.5 V		1	4.5 V	"	1			Preset 2	-1.4	-3.2	"
"	I _{IH1}	3010	39	GND		GND	2.4 V	u		0					,	и				J1	l	40	μА
"	u	"	40	GND	GND			"								"			2.4 V	K1		"	"
"	и	"	41					"	GND		GND	2.4 V				"				J2		"	"
"	и	u	42					"	GND	GND					2.4 V	и				K2		"	"
"	I _{IH2}	u	43	GND		GND	5.5 V	"								ű				J1		100	"
"	и	и	44	GND	GND			"								u			5.5 V	K1		"	"
"	и	и	45					"	GND		GND	5.5 V				ű				J2		"	"
"	"	"	46					"	GND	GND					5.5 V	"				K2		"	"

TABLE III. Group A inspection for device type 04. 1/- Continued.

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		-	est limits	
Subgroup	Symbol	STD-883 method	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas. terminal	Min	Max	Unit
1	I _{IH3}	3010	47	GND		Е	GND	5.5 V								GND			4.5 V	Clear 1		160	μА
T _C = 25°C	"IH3	"	48	GND	Е		4.5 V	"								"			GND	Preset 1		"	"
1 _C = 23 C	и	и	49	GIVD	_		7.5 V	"	GND		Е	GND			4.5 V	u			OND	Clear 2		"	"
и	u	u	50					"	GND	Е		4.5 V			GND	"				Preset 2		"	и
u	I _{IH4}	u	51	GND		F	GND	"	GIVD			T.5 V			OND	"			4.5 V	Clear 1		200	"
u	"IH4	u	52	GND	F	-	4.5 V	"								"			GND	Preset 1		"	"
u	"	"	53	OND			7.0 1	"	GND		F	GND			4.5 V	"			OND	Clear 2		"	"
u	"	"	54					"	GND	F	·	4.5 V			GND	"				Preset 2		"	"
u	и	u	55	5.5 V		GND	GND	"	0.15						0.15	íí.			GND	Clock 1		"	и
u	и	u	56					"	5.5 V		GND	GND			GND	íí.				Clock 2		"	и
и	I _{IH5}	и	57 CKT A, C	2.4 V		GND	GND	"	0.0							u			GND	Clock 1	-50	-700	"
и	"	и	57 CKT B	2.4 V		GND	GND	"								u			GND	Clock 1	-200	-850	"
u	и	и	58 CKT A, C					"	2.4 V		GND	GND			GND	ű				Clock 2	-50	-700	"
u u	и	u	58 CKT B					"	2.4 V		GND	GND			GND	"				Clock 2	-200	-850	"
"	los	3011	59 **	2.4 V	GND	4.5 V	2.4 V	"								"		GND	2.4 V	Q1	-20	-57	mA
"	"	и	60	2.4 V	4.5 V	GND	2.4 V	"								u	GND		2.4 V	Q 1	66	"	"
"	"	"	61**					"	2.4 V	GND	4.5 V	2.4 V		GND	2.4 V	"				Q2	"	"	"
"	"	"	62					"	2.4 V	4.5 V	GND	2.4 V	GND		2.4 V	u				Q 2	44	44	"
		0005	63	GND	4.5 V	GND	GND	"	GND	4.5 V	GND	GND			GND	u			GND	Vcc		40	"
u	lcc.	3005	03																				
2	I _{CC}	3005	64 nditions and lin	GND	GND	4.5 V	GND	" and V _{IC} t	GND	GND	4.5 V	GND			GND	и			GND	V _{CC}		40	и
2	I _{CC} Same test	3005 s, terminal co	64 nditions and lin	GND nits as for nits as for	GND subgroup 1 subgroup 1	4.5 V 1, except T 1, except T	GND _C = 125°C	and V _{IC} to	GND ests are o	GND mitted. mitted.	4.5 V	GND			GND								и
" 2 3 7 <u>2</u> / <u>4</u> /	I _{CC} Same test	3005 s, terminal co	64 nditions and lin nditions and lin 65	GND nits as for nits as for B	GND subgroup 1 subgroup 1	4.5 V 1, except T 1, except T B	$\frac{\text{GND}}{\text{C}} = 125^{\circ}\text{C}$ $\frac{\text{C}}{\text{C}} = -55^{\circ}\text{C}$ A		GND ests are o	GND mitted. mitted.	4.5 V	GND A	H <u>3</u> /	L <u>3</u> /	GND	" GND	H <u>3</u> /	L <u>3</u> /	В	All		H or L	66
2	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the following of the following and line of following following for the following	GND nits as for nits as for B A	GND subgroup 1 subgroup 1 A A	4.5 V 1, except T 1, except T B B	GND C = 125°C C = -55°C A A	and V _{IC} to	GND ests are o ests are o B A	GND mitted. mitted. A A	4.5 V B B	GND A A	Н	Ĺ	GND B B		Н	L <u>3</u> / L	B B		as		" /
" 2 3 7 <u>2</u> / <u>4</u> /	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the following o	GND nits as for nits as for B A B	GND subgroup 1 subgroup 1 A A A	4.5 V 1, except T 1, except T B B B	GND T _C = 125°C A A A	and V _{IC} to	GND eests are coests are o	GND mitted. mitted. A A	4.5 V B B	GND A A A	H		GND B B B		H		B B B	All	as	H or L s shown <u>3</u>	, ,
2 3 7 <u>2</u> / <u>4</u> / T _C = 25°C	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the following o	GND nits as for nits as for A B B B	subgroup 1 Subgroup 1 A A A A	4.5 V 1, except T 1, except T B B B B	GND Cc = 125°C A A A A	and V _{IC} to	GND ests are constant are of the state of th	GND mitted. A A A A	4.5 V B B B B	A A A A	H H H	Ĺ	B B B	GND "	H H		B B B	All	as	H or L	, /
2 3 7 <u>2/4/</u> T _C = 25°C	I _{CC} Same test	3005 s, terminal co	64 Inditions and lin Inditions	GND nits as for nits as for B A B B A	GND subgroup 1 subgroup 1 A A A A	4.5 V 1, except T 1, except T B B B B B B	GND Cc = 125°C A A A A	and V _{IC} to	GND ests are o ests are o B A B B A	GND mitted. A A A A A	4.5 V B B B B B	A A A A A	H H H	L L	B B B A	GND "	H H H		B B B A	All output "	as	H or L s shown <u>3</u> "	, , , , , , , , , , , , , , , , , , ,
3 7 2/ 4/ T _C = 25°C " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line 65 66 67 68 69 70	GND nits as for nits as for B A B A B B A	GND subgroup 1 subgroup 1 A A A A A A	4.5 V 1, except T 1, except T B B B B B B B B	GND C = 125°C A A A A A A A	and V _{IC} to	GND ests are coests are o	GND mitted. A A A A A A	4.5 V B B B B B B	A A A A A	H H H H	L L L	B B B A A	GND "	H H		B B B A A	All output "	as	H or L s shown <u>3</u>	, ,
" 2 3 7 2/4/ T _C = 25°C " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and lin Inditions	GND nits as for nits as for B A B B B B B B B	GND subgroup 1 subgroup 1 A A A A A B	4.5 V 1, except T 1, except T B B B B B B A	GND $C_{C} = 125^{\circ}C$ A A A A A A A	and V _{IC} to	GND ests are consists are of the state of th	GND mitted. A A A A A B	4.5 V B B B B B A	A A A A A A	H H H H	L L L L	B B B A A A	GND " " " "	H H H H	L L L	B B B A A	All output "	as	H or L s shown <u>3</u> "	/
3 7 2/ 4/ T _C = 25°C " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and lim Inditions	GND nits as for nits as for B A B B B A B A B A	subgroup 1 Subgroup 1 A A A A B B B	4.5 V 1, except T 1, except T B B B B B A A	GND Cc = 125°C A A A A A A A A	and V _{IC} to	ests are of ests a	GND mitted. A A A A A B B B	4.5 V B B B B A A	A A A A A A A	H H H H	L L L L H	B B B A A A	GND "	H H H H	L L L H	B B B A A A	All output	as	H or L s shown <u>3</u>	/
" 2 3 7 2/4/ T _C = 25°C " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line line line line line line line line	GND nits as for nits as for B A B B B A B B B B B B B B B B B B B	subgroup 1 subgroup 1 A A A A B B B B	4.5 V 1, except T 1, except T B B B B B A A A	GND C = 125°C A A A A A A A A	and V _{IC} to	GND ests are o ests are o B A B B B A B B A B B B B B B B B B B	GND mitted. A A A A A B B B B B	8 B B B B A A	GND A A A A A A A A A A A A A A A A A A	H H H H L	L L L H H	B B B A A A A	GND " " " " " " " " " "	H H H H	L	B B B A A A A	All output "	as	H or L s shown <u>3</u>	/
3 7 2/4/ T _C = 25°C " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the following state	GND nits as for B A B B A B A B B B B B B B B B B B B	GND subgroup 1 A A A A A B B B B B	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A	GND C = 125°C A A A A A A A A A A A A B B	and V _{IC} to	GND ests are coests are of B A B A B A B A B B A B B B B B B B B B	GND mitted. A A A A B B B B B	B B B B B A A A A	A A A A A A A A B B	H H H H L L	L L L H H	B B B A A A A A A A A	GND " " " "	H H H H	L L L H H	B B A A A A A	All output	a	H or L s shown <u>3</u>	/
3 7 2/4/ T _C = 25°C " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and lin Inditions	GND nits as for nits as for B A B B A B A B A B A A B A A B A A B A A A B A A A B A A A B A A A B A A A B A A A B A A B A A B A A B A A B A A B A A B A A B A A B A A B A B A A B A B A A B A B A B A A B B A A B B A A B B A A B B A A B B A B B A A B B B A A B B B A A B B B A A B B B A B B B A B B B A B B B B A B B B B A B	GND subgroup 1 A A A A A B B B B B B	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A	GND C = 125°C A A A A A A A B B B	and V _{IC} to	ests are o ests are o ests are o B A B B A B B A B A B A A B A A B A A A B A A A B A A A B A A A B A A A B A A B A A B A A B A A B A A B A A B A A B A A B A A B B A A B B A A B B A A B B B A A B B B A A B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B A A B B B B B A A B B B B B B A A B	GND mitted. A A A A B B B B B B	B B B B A A A A A	A A A A A A A B B B	H H H H L	L L L L H H H	B B B A A A A A A	GND " " " " " " " " " "	H H H H	L L L H H H	B B B A A A A A A	All output	as	H or L s shown <u>3</u>	, ,
" 2 3 7 2/4/ T _C = 25°C " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the second of the s	GND nits as for B A B B A B B A B B A B B B B A B	GND subgroup 1 A A A A A B B B B B B B B B B B B B B B	4.5 V 1, except T 1, except T 1, except T B B B B B B A A A A A	GND C = 125°C A A A A A A A B B B B	and V _{IC} to	ests are of ests a	GND mitted. mitted. A A A A B B B B B B B B B	B B B B A A A A A A A	A A A A A A B B B B	H H H H L L	L L L H H H	B B B A A A A A A A	GND " " " " " " " " " "	H H H H	L L L L H H H	B B B A A A A A A A A A A A A A A A A A	All output	as	H or L s shown <u>3</u>	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " " " " " " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line 65 66 67 68 69 70 71 72 73 74 75 76	GND nits as for B A B B A B B A B B A B B B B B B B B	subgroup 1 subgroup 1 A A A A B B B B B A	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A A A A	GND C = 125°C A A A A A A B B B B	and V _{IC} to	GND ests are constant of the c	GND mitted. A A A A B B B B B B B B A A	B B B B A A A A A A A A	A A A A A A B B B B B B	H H H H L L	L L L L H H H H	B B B A A A A A A A B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H	L L L L H H H H	B B B A A A A A A A B	All output	as	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the control	GND nits as for B B A B B B A B B A B B A A B B A A B B A A B B A A B A A B A A B A A B A A B A A B A A B A A B A A B A A B A B A A B A B A A B B A A B B A A B B A A B B A A B B A A B B A B A B B A A B B B A A B B B A A B B B A A B B B A A B B B A B B A B B B A B B B A B B B A B B B B A B B B B A B B B B A B B B B B A B B B B B A B	GND subgroup 1 A A A A B B B B B B A A A A	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A A A A A	GND C = 125°C A A A A A A B B B B	and V _{IC} t	GND ests are coests are of B B A B B B A B B B A B B B A B B B A B B B A B B B A B B B A B B B B A B B B B A B B B B A B B B B A B B B B B A B	GND mitted. A A A A B B B B B B B A A A	B B B B A A A A A A A A	A A A A A A A B B B B B B B B B B B B B	H H H H L L L		B B B A A A A A A A B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H		B B B A A A A A A A B B B B	All output	as	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and lin Inditions	GND nits as for B A B B A B B A B B A B B A B B A B B A B B A B B B B A B	GND subgroup 1 A A A A A B B B B B A A A A A A A A A	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A A A A A A A A A A A	GND C = 125°C A A A A A B B B B B	and V _{IC} t	GND ests are coests are of B A B B A B B A B B A B B A B B A B B A B B A B B B B A B	GND mitted. A A A A B B B B B A A A A A A A A A A	B B B B B A A A A A A A A A A A A A A A	A A A A A A A B B B B B B B B B B B B B	H H H H L L L L L L L L L L L L L L L L	L L L L H H H H	B B B A A A A A A B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L	L L L L H H H H	B B B A A A A A A A B B B B	All output	at	H or L s shown 3	J
" 2 3 7 2/4/ T _C = 25°C " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the second s	GND nits as for B A B B A B B B B A B B B A B B B B B	subgroup 1 subgroup 1 A A A A B B B B B A A A A	4.5 V 1, except T 1, except T 1, except T 1, except T B B B B B A A A A A A A B B	GND C = 125°C A A A A A A A A B B B B B B B B B B B	and V _{IC} t	GND ests are c ests are o B A B A B B A B B B A B B A B B B A B	GND mitted. A A A A A B B B B B B B A A A A A A A	B B B B B A A A A A A A A B B	A A A A A A A B B B B B B B B B B B B B	H H H H L L L L L L H H H H H H H H H H		B B B A A A A A A B B B B B B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L L L L L L L L L L L L L		B B B A A A A A A A B B B B B B	All output	as	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81	GND nits as for B A B B A B B A B B A B B A B B B A B B B B A B	GND subgroup 1 A A A A A B B B B B A A A A A A A A A	4.5 V 1, except T	GND C = 125°C A A A A A A A A B B B B B B B B B B B	and V _{IC} t	GND ests are coests are of the state of the	GND mitted. A A A A B B B B B B A A A A A A A A A	B B B B B A A A A A A A A A A A A A A A	A A A A A A B B B B B B B B B B B B B B	H H H H L L L L L L H H H H H H H H H H		B B B A A A A A A B B B B B B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L L L L L L L L L L L L L		B B B A A A A A A A B B B B B B B B B B	All output	as	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " " " " " " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line of the second of the s	GND nits as for B A B B A B B B B A B B B A B B B B B	GND subgroup 1 A A A A A B B B B B B A A A A A A A A	4.5 V 1, except T 1, except T 1, except T B B B B B A A A A A A A A A A A A A A	GND C = 125°C A A A A A B B B B B B B B	and V _{IC} t	GND ests are c ests are o B A B A B B A B B B A B B A B B B A B	GND mitted. A A A A B B B B B A A A A A A A A A A	B B B B A A A A A A A A A A A A A A A A	A A A A A A A B B B B B B B B B B B B B	H H H H L L L L L L L L L H H H H H H H		B B B A A A A A A B B B B B B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L L L L L L L L L L L L L		B B B A A A A A A A B B B B B B B B B B	All output	as	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " " " " " " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81	GND nits as for B A B B B A B B B A B B B A B B B A B B B B A B B B B A B B B B B A B	GND subgroup 1 A A A A A B B B B B A A A A A A A A A	4.5 V 1, except T	GND C = 125°C A A A A A A A A B B B B B B B B B B B	and V _{IC} t	GND ests are o ests are o B A B B B A B B B A B B B A B B B B A B B B B A B B B B B B A B	GND mitted. A A A A B B B B B B A A A A A A A A A	B B B B B A A A A A A A A A A A A A A A	A A A A A A B B B B B B B B B B B B B B	H H H H L L L L L L H H H H H H H H H H		B B B A A A A A A B B B B B B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L L L L L L L L L L L L L		B B B A A A A A A A B B B B B B B B B B	All output	at	H or L s shown 3	/
" 2 3 7 2/4/ T _C = 25°C " " " " " " " " " " " " " " " " " " "	I _{CC} Same test	3005 s, terminal co	64 Inditions and line ditions are ditionally dist	GND nits as for B A B A B B A B B A B B B A B B B A B B B B B B A B	GND subgroup 1 A A A A A B B B B B A A A A A A A A A	4.5 V 1, except T	GND C = 125°C A A A A A A A A B B B B B B B B B B B	and V _{IC} t	GND ests are constant of the c	GND mitted. A A A A A B B B B A A A A A A A A A A	B B B B B A A A A A A A A A A A A A A A	A A A A A A A B B B B B B B B B B B B B	H H H H L L L L L L L L L L L L L L L L		B B B A A A A A A A B B B B B B B B B B	GND 4 4 4 4 4 4 4 4 4 4 4 4 4	H H H H L L L L L L L L L L H H H H H H		B B B A A A A A A A B B B B B B B B B B	All output	as	H or L s shown 3 " " " " " " " " " " " " " " " " " "	J

TABLE III. Group A inspection for device type 04. $\underline{1}$ / - Continued.

Subgroup	Symbol	MIL-	Case E & F	<u> </u>	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			Test limits	
Subgroup	Symbol	STD-883	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{CC}	Clock 2	Preset 2	Clear 2	J2		Q2	K2	GND	Q 1	Q1	K1	Meas.	Min	Max	Unit
		method	10011101	Oldon I	1 10001 1	0.00.	0.	• (()	0.00.02		0.00. 2	91	Q 2	Ψ.		0.10	Q 1	;		terminal		max	
7 <u>2</u> / <u>4</u> /			87	В	Α	Α	В	4.5 V	В	Α	Α	В	L <u>3</u> /	H <u>3</u> /	Α	GND	L <u>3</u> /	H <u>3</u> /	Α	All		H or L	
$T_C = 25^{\circ}C$			88	Α	Α	Α	В	"	Α	Α	Α	В	L	Н	Α	"	L	Н	A	Output	a	as shown (3/
"			89	В	A	A	В	"	В	A	A	В	H	Ŀ	A	"	H	Ļ	A	"		"	
			90 91	В	A	A	A	"	В	A	A	A	H H	L	A		H	_	A	"			
"			92	A B	A A	A A	A A	"	A B	A A	A A	A A		H	A	"	H	H	A A	"		и	
u			93	A	Ā	A	A	"	A	A	A	A	- i	H	Ä	"	i	H	A	и		"	
"			94	В	A	A	A	u	В	A	A	A	H	Ĺ	A	u	H	Ĺ	A	"		и	
"			95	Α	В	В	В	"	Α	В	В	В	Н	Н	В	"	Н	Н	В	и		"	
"			96	Α	В	Α	Α	"	Α	В	Α	Α	L	Н	Α	"	L	Н	Α	и		u	
"			97	Α	Α	Α	Α	u	Α	Α	Α	Α	L	Н	Α	u	L	Н	Α	"		u	
"			98	Α	Α	Α	Α	"	Α	Α	Α	Α	L	Н	В	ii .	L	Н	В	"		и	
"			99	A	Α	A	В	"	A	Α	Α	В	L	Н	В	"	L	H	В	"		"	
"	+	1	100	В	A	A	B	"	В	A	A	В	H	L L	В	"	H	<u> </u>	В	"		"	
"	+		101 102	A	A	A A	A B	"	A	A	A A	A B	H H	-	A	"	H	<u> </u>	A A	и		"	
"	+		102	A	A	A	В	и	A	A	A	В	H	-	В	и	Н	1	В	u		и	
"			103	В	A	A	В	"	В	A	A	В	ï	H	В	"	ï	H	В	u		"	
0.2/ 4/	Sama taat	torminal ac						and EE					_					•					
8 <u>2</u> / <u>4</u> /			nditions and lin			, ехсері т			U.														
9	F _{MAX}	(Fig. 9)	105	IN	5.0 V		2.4 V	5.0 V								GND "	OUT	OUT	2.4 V	Q1	10		MHz "
$T_C = 25^{\circ}C$		<u>5</u> /	106	IN	5.0 V		2.4 V									-	OUT		2.4 V	Q 1			
"	ű	"	107					"	IN	5.0 V		2.4 V		OUT	2.4 V	"				Q2	u		"
"	"	и	108					"	IN	5.0 V		2.4 V	OUT		2.4 V	"					"		"
"		3003	109	2.4 V	5.0 V	IN	2.4 V	"								"	OUT		2.4 V	Clear 1	5	25	ns
	t _{PLH1}	(Fig 8)	109	2.4 V	3.0 V	IIN	2.4 V										001		2.4 V	_	3	25	115
		(i ig 0)																		to Q 1			<u> </u>
"	44	"	110	2.4 V	IN	5.0 V	2.4 V	"								"		OUT	2.4 V	Preset 1	u	"	"
"	"	"	444					"	0.41/	501/	INI	0.41/	OUT		0.41/	"				to Q1	и	"	
-	-		111					-	2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V	-				Clear 2			
																				to Q 2			<u> </u>
"	"	"	112					"	2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V	"				Preset 2	"	"	"
"		,,						"												to Q2			
	t _{PHL1}		113	2.4 V	5.0 V	IN	2.4 V											OUT	2.4 V	Clear 1 to Q1		40	
"	"	"	114	2.4 V	IN	5.0 V	2.4 V	"								и	OUT		2.4 V	Preset 1	и	и	"
				2.7 0		0.0 1	2.→ V										001		2.7 4	to Q 1			
,,		,,																					
			115					. "	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V					Clear 2 to Q2		. "	
"	44	"	116					"	2.4 V	IN	5.0 V	2.4 V	OUT	1	2.4 V	"				Preset 2	и	"	"
			'''						2.7 V		J.0 V	2.7 V	001		2.7 V					_			'
			1																	to Q 2			
"	t _{PLH2}	3003	117	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1	5	30	ns
"	"	(Fig 9)	118	IN	5.0 V	5.0 V	2.4 V	"	-	-	-				 	"	OUT		2.4 V	to Q1 Clock 1	и	"	"
			110	IIN	J.U V	J.U V	∠.+ V				1				1		001		∠. + V	_		1	1
	1		1																	to Q 1			
"	"	"	119					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Clock 2	"	"	"
"	"	"	420		-			"	INI	F 0 1/	5.01/	2.4.1/	OUT		2.41/	и				to Q2	"	"	"
		-	120						IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	-				Clock 2	-		
																				to Q 2			
44	t _{PHL2}	"	121	IN	5.0 V	5.0 V	2.4 V	"			1				1	"		OUT	2.4 V	Clock 1	ű	40	"
]		I	l				l					to Q1		l	1

TABLE III. Group A inspection for device type 04. 1/ - Continued.

Subgroup	Symbol	MIL-	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			Test limits	s
		STD-883 method	Test No.	Clock 1	Preset 1	Clear 1	J1	V _{cc}	Clock 2	Preset 2	Clear 2	J2	Q 2	Q2	K2	GND	Q 1	Q1	K1	Meas. terminal	Min	Max	Unit
9	t _{PHL2}	3003	122	IN	5.0 V		2.4 V	5.0 V								GND	OUT	OUT	2.4 V	Clock 1	5	40	ns
$T_C = 25^{\circ}C$		(Fig 8)																		to Q 1			
и	"	u	123					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	и				Clock 2 to Q2	и	и	u
u	"	u	124					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	и	"	"
																				to Q 2			
10	F _{MAX} <u>5</u> /	(Fig 9)	125	IN	5.0 V		2.4 V	"								"		OUT	2.4 V	Q1	10		MHz
T _C = 125°C	"	"	126	IN	5.0 V		2.4 V	"								"	OUT		2.4 V	Q 1	и		"
и	ű	ű	127					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	"				Q2	"		"
"	u	и	128					"	IN	5.0 V	5.0 V	2.4 V	OUT	001	2.4 V	"				Q 2	"		"
и		0000	400	0.41/	501/	INI	0.41/	"								"	OUT		0.41/		_	00	
	t _{PLH1}	3003 (Fig 8)	129	2.4 V	5.0 V	IN	2.4 V										OUT		2.4 V	Clear 1 to Q 1	5	39	ns
и	"	u	130	2.4 V	IN	5.0 V	2.4 V	"								и		OUT	2.4 V	Preset 1 to Q1	и	и	"
и	"	u	131					"	2.4 V	5.0 V	IN	2.4 V	OUT		2.4 V	"				Clear 2	"	"	u
																				to Q 2			
u	u	u	132					"	2.4 V	IN	5.0 V	2.4 V		OUT	2.4 V	"				Preset 2 to Q2	"	u	"
u	t _{PHL1}	u	133	2.4 V	5.0 V	IN	2.4 V	"								и		OUT	2.4 V	Clear 1 to Q1	и	50	u
и	"	"	134	2.4 V	IN	5.0 V	2.4 V	и								"	OUT		2.4 V	Preset 1	u	u	"
																				to Q 1			
и	u	u	135					"	2.4 V	5.0 V	IN	2.4 V		OUT	2.4 V	и				Clear 2 to Q2	"	и	"
"	"	u	136					"	2.4 V	IN	5.0 V	2.4 V	OUT		2.4 V	"				Preset 2	и	и	"
																				to Q 2			
u	t _{PLH2}	3003 (Fig 9)	137	IN	5.0 V	5.0 V	2.4 V	"								ш		OUT	2.4 V	Clock 1 to Q1	5	39	ns
ű	ű	(Fig 9)	138	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	Clock 1	"	u	u
																				to Q 1			
u	"	"	139					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	ш				Clock 2 to Q2	и	и	и
u	"	u	140					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	"	"	"
																				to Q 2			
u	t _{PHL2}	и	141	IN	5.0 V	5.0 V	2.4 V	"								"		OUT	2.4 V	Clock 1	и	50	"
u	и	и	142	IN	5.0 V	5.0 V	2.4 V	"								"	OUT		2.4 V	to Q1 Clock 1	"	"	"
																				to Q 1			
"	"	u	143					"	IN	5.0 V	5.0 V	2.4 V		OUT	2.4 V	и				Clock 2 to Q2	и	и	"
и	и	u	144					"	IN	5.0 V	5.0 V	2.4 V	OUT		2.4 V	"				Clock 2	"	"	"
																				to Q 2			

NOTES:

- A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.
 C = This note has been deleted.
- E = Momentary ground, then 2.4 V. F = Momentary ground, then 5.5 V.

- ** = Test time limit ≤ 100 ms. J = This note has been deleted.

- 1/ Terminal conditions (pins not designated may be H \geq 2.0 V, or L \leq 0.8 V, or open.)
 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum.
 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H \geq 1.5 V and L < 1.5 V when using a high speed checker single comparator.
 4/ Tests shall be performed in sequence.
 5 F_{MAX} , minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Т	est limits	
Oubgroup	Cyllibol	883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.	,	est iiiiiis	
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
1	V _{OH}	3006	1	Α	2.0 V		4.5 V							GND		4 mA	-	Q1	2.4		V
T _C = 25°C	"	"	2	A	0.8 V		"							"	4 mA			Q 1	"		"
"	"	"	3	GND		0.8 V	"							"	4 mA		GND		"		и
				GIND											4 IIIA			Q 1			
"	"	"	4			GND	"			<u>. </u>				"		4 mA	0.8 V	Q1	"		"
	"	"	5				"		2.0 V	A		4 mA						Q2	"		
			6						0.8 V	Α			4 mA					Q 2			1
и	"	"	7				"	0.8 V		GND	GND		4 mA	"				Q 2	"		"
"	"	"	8				"	GND			0.8 V	4 mA		ű				Q2	"		"
u	V _{OL}	3007	9	Α	2.0 V		"							"	16 mA			Q 1		0.4	"
"	"	u	4.0		0.01/		"							u		40. 4				"	
"	"	"	10 11	Α	0.8 V	0.01/	"			1				- "		16 mA	2.0.1/	Q1		"	
u	"	"	12			0.8 V 2.0 V	"							"	16 mA	16 mA	2.0 V 0.8 V	Q1		"	и
			12			2.0 V									16 IIIA		0.8 V	Q 1			l
u	"	"	13				"		2.0 V	Α			16 mA	"				Q 2		"	"
u	"	и	14				"		0.8 V	Α		16 mA		"				Q2		"	"
u	"	"	15				"	0.8 V			2.0 V	16 mA		"				Q2		"	"
u	"	"	16				"	2.0 V			0.8 V		16 mA	"				Q 2		"	"
u	V _{IC}		17		-12 mA		"							u				D1		-1.5	"
"	"		18	-12 mA			"							u				Clock 1		"	"
u	"		19			-12 mA	"							"				Clear 1		"	"
u	"		20				"							"			-12 mA	Preset 1		"	"
ű	"		21				"		-12 mA					"				D2		"	"
	"		22				"			-12 mA				"				Clock 2		"	
"	"		23				"	-12 mA			40. 4			"				Clear 2		"	
"		3009	24 25	4.5 V	0.4 V	4.5 V	5.5 V				-12 mA			"			GND	Preset 2 D1	-0.7	-1.6	mA
u	I _{IL1}	3009	26	4.5 V	0.4 V	4.5 V	3.3 V	4.5 V	0.4 V	4.5 V	GND			"			GND	D1	-0.7	-1.6	"
"	"	"	27	GND	GND	GND	"	7.5 V	0. 4 V	7.5 V	OIVD			"	1		0.4 V	Preset 1	-1.4	-3.2	"
"	"	"	28	CITE	OND	OND	"	GND	GND	GND	0.4 V			u			0.4 V	Preset 2	-1.4	-3.2	"
u	I _{II 2}	"	29	0.4 V	GND	4.5 V	"							"			GND	Clock 1	-1.4	-3.2	"
"	"	"	30 <u>7</u> /	4.5 V	4.5 V	0.4 V	"							"			GND	Clear 1	-2.1	-4.8	"
u	u	"	31				"	4.5 V	GND	0.4 V	GND			ű				Clock 2	-1.4	-3.2	u
и	и	"	32 <u>7</u> /				"	0.4 V	4.5 V	4.5 V	GND			"				Clear 2	-2.1	-4.8	"
"	I _{IH1}	3010	33	4.5 V	2.4 V	GND	"							"			4.5 V	D1		40	μΑ
"	I _{IH1}	"	34			0115	"	GND	2.4 V	4.5 V	4.5 V		ļ	"				D2		40	
"	I _{IH2}	"	35	4.5 V	5.5 V	GND	"	ONE	5.5.1/	4.5.1	451/		-	"	1		4.5 V	D1		100	
	I _{IH2}	"	36 37	2.4.1/	1 E \/	CND	"	GND	5.5 V	4.5 V	4.5 V		 	"		-	4 5 \/	D2 Clock 1		100	
"	I _{IH3}	"	38	2.4 V B	4.5 V 4.5 V	GND 4.5 V	"	-		-			-	"	-		4.5 V 2.4 V	Clock 1 Preset 1		80	"
и	"	и	39	В	4.5 V	4.5 V	"	GND	4.5 V	2.4 V	4.5 V		<u> </u>	"	1		Z.4 V	Clock 2		u	"
u	"	"	40	1			"	4.5 V	4.5 V	B B	2.4 V			"	<u> </u>			Preset 2		"	"
"	I _{IH4}	"	41	5.5 V	4.5 V	GND	"				v			"	1		4.5 V	Clock 1		200	и
u	"	"	42	В	4.5 V	4.5 V	"							"	1		5.5 V	Preset 1		"	"
"	u	"	43				"	GND	4.5 V	5.5 V	4.5 V			u				Clock 2		"	u
"	"	"	44				"	4.5 V	4.5 V	В	5.5 V			"				Preset 2		"	"
"	I _{IH5}	"	45	В	GND	2.4 V	"							"			4.5 V	Clear 1		120	и
"	I _{IH5}	"	46				"	2.4 V	GND	В	4.5 V			"				Clear 2		120	"
"	I _{IH6}	"	47	В	GND	5.5 V	"	551:	OND		4.5.1		ļ	"			4.5 V	Clear 1		300	"
**	I _{IH6}	"	48					5.5 V	GND	В	4.5 V							Clear 2		300	

TABLE III. Group A inspection for device type 05. 1/- Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		1	est limits	.s
0 .	1	883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{cc}	Clear 2	D2	Clock	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
1	Ios	3011	49				5.5 V							GND		GND	GND	Q1	-20	-57	mA
$T_C = 25^{\circ}C$	"	"	50			GND	"							"	GND			Q 1	"	"	и
"	и	"	51				"				GND	GND		"				Q2	"	"	"
"	"	"	52				"	GND					GND	u				Q 2	"	"	"
"	Icc	3005	53	GND	GND		"		GND	GND	GND			"			GND	V _{CC}		30	
"	Icc	3005	54	GND	GND	GND	"	GND	GND	GND	OND			и			GIVD	V _{CC}		30	"
2		•	ditions and limits	as for sub	ogroup 1, e		125°C aı	nd V _{IC} test									•				
3			ditions and limits																		
7 <u>2</u> / <u>4</u> /	eame teete	T	55	В	В	В	4.5 V	В	В	В	В	H 3/	H <u>3</u> /	GND	H <u>3</u> /	Н	В	All		H or L	
T _C = 25°C			56	В	В	В	4.5 V	В	В	В	A	<u>пз</u> /	<u>пз</u> /	"	<u>пз</u> /	L	A	outputs	as	shown:	3/
10-230			57	В	В	A	"	A	В	В	A	L	H	"	Н.	L	A	"	a	"	<u>u</u>
"			58	В	В	A	"	A	В	В	В	Н	L.	"	L.	Н	В	"		"	
"			59	A	В	A	"	A	В	A	В	H	Ĺ	"	Ē	H	В	"		"	
и			60	Α	В	В	"	В	В	Α	В	Н	Н	"	H	Н	В	ű		"	
"			61	Α	Α	В	"	В	Α	Α	В	Н	Н	"	Н	Н	В	"		"	
"			62	Α	Α	В	"	В	Α	Α	Α	L	Н	"	Н	L	Α	"		"	
"			63	Α	Α	Α	"	Α	Α	Α	Α	L	Н	u	Н	L	Α	u		"	
и			64	Α	Α	Α	"	Α	Α	Α	В	Н	L	"	L	Н	В	и		"	
"			65	Α	Α	Α	"	Α	Α	Α	Α	Н	L	"	L	Н	Α	ű		"	
"			66	В	Α	Α	"	Α	Α	В	Α	Ι	L	"	L	Н	Α	"		"	
"			67	В	В	Α	"	Α	В	В	Α	Н	L	"	L	Н	Α	"		"	
			68	A	В	A	"	A	В	A	A	L	H	"	H	L	A	"		"	
"			69	A	В	A B	"	A	В	A	B B	H	L		L	Н	B B	"			
"			70 71	A A	A B	В	"	B B	A B	A	В	H	H	"	H	H	В	"		"	
"			72	A	В	В	"	В	В	A	A	L	H	"	Н	I	A	"		"	
"			73	A	В	A	"	A	В	A	A	L	H	u	Н	L	A	"		"	
ű			74	В	A	A	"	A	A	В	A	ī	H	u	H	i	A	"		"	
"			75	A	A	A	"	A	A	A	A	H	i i	"	i	H	A	и		"	
и			76	A	A	A	"	A	A	A	В	H	Ĺ	"	Ĺ	H	В	и		"	
ű			77	A	A	A	"	A	A	A	A	H	Ĺ	"	Ĺ	H	Ā	u		"	
и			78	Α	Α	В	"	В	Α	Α	Α	L	Н	u	Н	L	Α	u		"	
"			79	Α	Α	Α	"	Α	Α	Α	Α	L	Н	"	Н	L	Α	и		"	
"			80	Α	В	Α	"	Α	В	Α	В	Н	L	u	L	Н	В	"		u	
"			81	Α	В	Α	"	Α	В	Α	Α	Н	L	"	L	Н	Α	и		"	
"			82	Α	В	В	"	В	В	Α	Α	L	Н	"	Н	L	Α	ш		"	
"			83	A	В	A	"	A	В	A	A	<u> </u>	Н	"	Н	L	A	u u		"	
	_	l	84	Α	Α	A		Α	Α	Α	Α	L	Н		Н	<u>L</u>	Α			"	
8 <u>2</u> / <u>4</u> /			ditions and limits		•	xcept T _C =		nd -55ºC.		1	1		1	ONE	1	OUT.	L = 0.1/		40		T
9	F _{MAX} <u>6</u> /	(Fig. 11)	85	IN	E		5.0 V	1						GND "	OLIT.	OUT	5.0 V	Q1	10	1	MHz "
$T_C = 25^{\circ}C$	-	-	86	IN	Е		-								OUT		5.0 V	Q 1	-		
u	и	"	87				"		Е	IN	5.0 V	OUT		"				Q2	u		u
"	"	"	88	l			"		E	IN	5.0 V		OUT	"				Q 2	"		"

TABLE III. Group A inspection for device type 05. 1/ - Continued.

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	
J	-,	STD-883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
9	t _{PLH1}	3003	89			IN	5.0 V							GND	OUT		J	Clear 1	5	25	ns
$T_C = 25^{\circ}C$		(Fig 10)																to Q 1			
u	"	"	90			J	"							"		OUT	IN	Preset 1	14	"	"
и	"	u	91				"	IN			J		OUT	"				to Q1 Clear 2	"	"	**
			91					IIN			J		001					to Q 2			
и	ű	ű	92				"	J			IN	OUT		"				Preset 2	и	40	"
								Ů				001						to Q2		40	
"	t _{PHL1}	"	93			IN	"							"		OUT	J	Clear 1 to Q1	"	"	**
"	"	"	94			J	"							"	OUT		IN	Preset 1	"	"	"
																		to Q 1			
u	u	u	95				u	IN			J	OUT		"				Clear 2	"	"	"
																		to Q2	,,		
			96					J			IN		OUT					Preset 2			
		0000.5/	07	18.1	INI (A)	_	"							"		OUT	5.0 V	to Q 2		30	
	t _{PLH2}	3003 <u>5</u> / (Fig 11)	97	IN	IN (A)	В										001	5.0 V	to Q1	5	30	ns
66	"	(Fig 12)	98	IN	IN (A)	5.0 V	"							"	OUT		В	Clock 1	"	"	"
																		to Q 1			
"	u	(Fig 11)	99				"	В	IN (A)	IN	5.0 V	OUT		"				Clock 2	44	"	"
66	"	(Fig 12)	100				"	5.0 V	IN (A)	IN	В		OUT	"				to Q2 Clock 2	"	"	"
		(3)							()									to Q 2			
"	t _{PHL2}	(Fig 12)	101	IN	IN (B)	5.0 V	"							"		OUT	В	Clock 1	"	40	"
	"						.,							,,				to Q1	,,		
-	-	(Fig 11)	102	IN	IN (B)	В									OUT		5.0 V	Clock 1	_		
"	"	(Fig 12)	103				"	5.0 V	IN (B)	IN	В	OUT		"				to Q 1	"	"	"
		(FIG 12)	103					5.0 V	IIN (D)	IIN	В	001						to Q2			
"	"	(Fig 11)	104				"	В	IN (B)	IN	5.0 V		OUT	"				Clock 2	"	"	"
																		to Q 2			
10 T _C = 125°C	F _{MAX} <u>6</u> /	(Fig 11)	105	IN	Е		"							"		OUT	5.0 V	Q1	10	44	MHz
1 _C = 125°C	"	u	106	IN	E		"							"	OUT		5.0 V	Q 1	"	"	"
"	"	u					"			INI	F 0 \/	OUT		"				Q 1 Q2	"	"	u
"	"	u	107 108				u		E	IN IN	5.0 V 5.0 V	001	OUT	"				Q2 Q 2	и		"
"		3003	109			IN	"							"	OUT		J	Q 2 Clear 1	5	39	ns
	t _{PLH1}	(Fig 10)	109			IIN									001		J	to Q 1	5	39	ns
"	"	"	110			J	"							"		OUT	IN	Preset 1	"	"	"
						3										001	1111	to Q1			
"	u	u	111				"	IN			J		OUT	"				Clear 2	"	"	"
							<u> </u>											to Q 2			
"	"	"	112				ш	J			IN	OUT		"				Preset 2 to Q2	"	**	ш
"	t _{PHL1}	u	113			IN	"							"		OUT	J	Clear 1	"	50	"
"		"				L									OUT			to Q1	"	"	- "
-		"	114			J	. "								OUT		IN	Preset 1	"		
"	"	"	115				"	INI	ļ		ļ	OUT		"				to Q 1	"	"	
			115]	IN			J	OUT						to Q2			
ű	ű	u	116				"	J			IN		OUT	"				Preset 2	"	"	"
		I			1											1	1	to Q 2	1		1

Subgroup	Symbol	MIL-	Case A, B, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	,
		STD-883	Case C															Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
10 T _C = 125°C	t _{PLH2}	3003 <u>5</u> / (Fig 11)	117	IN	IN (A)	В	"							"		OUT	5.0 V	Clock 1 to Q1	5	39	ns
-	"	(Fig 12)	118	IN	IN (A)	5.0 V	"							"	OUT		В	Clock 1 to Q 1	u	и	"
u	"	(Fig 11)	119				"	В	IN (A)	IN	5.0 V	OUT		"				Clock 2 to Q2	ű	"	"
и	"	(Fig 12)	120				"	5.0 V	IN (A)	IN	В		OUT	и				Clock 2 to Q 2	u	и	"
u	t _{PHL2}	(Fig 12)	121	IN	IN (B)	5.0 V	"							"		OUT	В	Clock 1 to Q1	ű	40	"
u	и	(Fig 11)	122	IN	IN (B)	В	и							"	OUT		5.0 V	Clock 1 to Q 1	и	"	"
u	"	(Fig 12)	123				и	5.0 V	IN (B)	IN	В	OUT		и				Clock 2 to Q2	ű	"	"
и	"	(Fig 11)	124				"	В	IN (B)	IN	5.0 V		OUT	"				Clock 2 to Q 2	"	и	"
11	Same tests	s, terminal co	nditions and limi	ts as for su	bgroup 10	, except T	_C = -55°C			•		•	•	•	•	•				•	

NOTES:

- A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.
- E = Input D connected to \overline{Q} .
- J = Input pulse, $t_p \ge 100$ ns, PRR = 1 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open). 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b)
- H ≥ 1.5 V and L < 1.5 V when using a high speed checker single comparator.

- 4/ Tests shall be performed in sequence.
 5/ Tests shall be performed in sequence.
 6/ Tests shall be performed for both D input pulses (A and B).
 6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
 7/ CKT C limits are -0.7 to -4.8 mA for these tests.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test lim	its
		883 method	Case C Test No.	10 K1	12 Clock	13 Preset	V _{CC}	2 Clear	1 NC	3 J1	4 J2	5 J*	6 Q	7 GND	8 Q	9 K*	11 K2	Meas. terminal	Min	Max	Unit
4	\ /	2000		0.01/						0.01/	0.01/	0.01/	Q	OND	4 4	0.01/	0.01/	_	0.4		
1	V _{OH}	3006	2	0.8 V 2.0 V	A A		4.5 V			2.0 V 0.8 V	2.0 V 0.8 V	0.8 V 2.0 V	4 mA	GND "	4 mA	2.0 V 0.8 V	0.8 V 2.0 V	Q _	2.4		V
T _C = 25°C				2.0 V						0.6 V	0.6 V						2.0 V	Q			
"	"	"	3		GND	2.0 V	"	0.8 V				GND	4 mA	"		GND		Q	"		"
u	"	"	4		GND	0.8 V	"	2.0 V				GND		"	4 mA	GND		Q	"		"
ű	V _{OL}	3007	5	2.0 V	Α		"			0.8 V	0.8 V	2.0 V		"	16 mA	0.8 V	2.0 V	Q		0.4	"
u	"	u u	6	0.8 V	Α		"			2.0 V	2.0 V	0.8 V	16 mA	"		2.0 V	0.8 V	Q		"	"
"	"	u	7		GND	0.8 V	"	2.0 V				GND	16 mA	"				Q		"	"
и	"	"	8		GND	2.0 V	"	0.8 V				GND		"	16 mA			Q		"	"
u	V _{IC}		9				u			-12 mA				u				J1		-1.5	u
"	"		10				"				-12 mA			"				J2		"	"
"	"		11	40 4			"					-12 mA		"				J*		"	+ "
"	"		12 13	-12 mA			"							"			-12 mA	K1 K2		"	
"	"		14				"							"		-12 mA	-12111/4	K*		"	"
u	"		15		-12 mA		"							"				Clock		"	"
u	"		16			-12 mA	"							"				Preset		"	"
"	"		17				"	-12 mA						"				Clear		"	"
"	I _{IL1}	3009	18 19		GND GND		5.5 V	B B		0.4 V 4.5 V	4.5 V 0.4 V	0.4 V 0.4 V		"				J1 J2	-0.7	-1.6	m,
"	"	"	20		GND		"	В		4.5 V	0.4 V	0.4 V		"				J2 J*	"	"	
ű	44	"	21	0.4 V	GND	В	"					0. 4 V		"		0.4 V	4.5 V	K1	"	"	"
ű	"	"	22	4.5 V	GND	В	"							"		0.4 V	0.4 V	K2	"	"	"
u	"	"	23				"							"		0.4 V		K*	"	"	"
"	"	"	24		0.4 V		"							"				Clock	"	"	"
"	"	"	25 26	4.5 V	GND GND	0.4 V	"	0.4 V		4.5 V	4.5 V	0.4 V		"		0.4 V	4.5 V	Preset	"	"	"
u	I _{IH1}	3010	27		GIND		"	GND		2.4 V	GND	4.5 V		"				Clear J1		40	μA
u	"	"	28				u	GND		GND	2.4 V	4.5 V		"				J2		"	μr "
u	ű	"	29				"					2.4 V		"				J*		"	"
u	"	"	30	2.4 V		GND	u							"		4.5 V	GND	K1		"	"
"	"	"	31	GND		GND	"							"		4.5 V	2.4 V	K2		"	"
	"	"	32 33		2.4 V		"							"		2.4 V		K* Clock		"	
"	I _{IH2}	"	34		2.4 V		"	GND		5.5 V	GND	4.5 V		"				J1		100	"
и	IIIZ	"	35				"	GND		GND	5.5 V	4.5 V		"				J2		"	"
и		"	36				"					5.5 V		"				J*		"	"
"	"	"	37	5.5 V		GND	"							"		4.5 V	GND	K1		"	"
"	"	"	38	GND		GND	"							"		4.5 V	5.5 V	K2		"	"
"	"	"	39 40		5.5 V		"							"		5.5 V		K* Clock		"	- "
"	I _{IH3}	"	41	GND	3.5 V	2.4 V	"			4.5 V	4.5 V	GND	1	"		4.5 V	GND	Preset		80	"
u	"III3	"	42	4.5 V	A		и	2.4 V		GND	GND	4.5 V		"		GND	4.5 V	Clear		80	"
u	I _{IH4}	ű	43	GND	Α	5.5 V	и			4.5 V	4.5 V	GND		"		4.5 V	GND	Preset		200	u
"		"	44	4.5 V	A		"	5.5 V		GND	GND	4.5 V		"		GND	4.5 V	Clear		200	"
u	I _{OS}	3011	45 46		GND GND	GND	"	GND				GND GND	GND	"	GND	GND GND		Q -	-20 -20	-57 -57	m/
					GIAD		"					OND	CIAD	"		CIND		ā	-20		<u> </u>
"	I _{CC}	3005	47 48	-	-	GND	"	GND					-	"				V _{CC}		30 30	- "
		I		<u> </u>	<u> </u>			<u> </u>		<u> </u>			1					V _{CC}	<u> </u>	30	ــــــــــــــــــــــــــــــــــــــ
2	Same tests	terminal cond	ditions and limits	as for sub	paroup 1. e	$xcept T_c =$: 125°C aı	nd V _{ic} test	s are omitte	ed.											

TABLE III. Group A inspection for device type 06. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Test I	imits
		883	Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11	Meas.		
		method	Test No.	K1	Clock	Preset	V _{cc}	Clear	NC	J1	J2	J*	Q	GND	Q	K*	K2	terminal	Min Max	(U
7 <u>2</u> / <u>4</u> /			49	В	В	Α	4.5 V	В	В	В	В	Α	H 3/	GND	L <u>3</u> /	Α	В	All	Но	r L
= 25°C			50	В	В	В	"	Α	В	В	В	Α	L	"	Н	Α	В	output	as sho	wn <u>3</u> /
u			51	В	В	Α	u	Α	В	В	В	Α	L	"	Н	В	Α	ü	"	
"			52	В	Α	Α	"	Α	В	В	В	Α	L	"	Н	В	Α	"	"	
"			53	В	В	Α	"	Α	В	В	В	Α	L	"	Н	В	Α	"	u	
u			54	Α	В	Α	ű	Α	В	В	В	Α	L	"	Н	В	В	"	u	
"			55	Α	Α	Α	"	Α	В	В	В	Α	L	"	Н	В	В	"	u	
"			56	Α	В	Α	"	Α	В	В	В	Α	L	"	Н	В	В	"	"	
"			57	Α	В	Α	"	Α	В	В	В	Α	L	"	Н	Α	Α	"	"	
"			58	Α	Α	Α	"	Α	В	В	В	Α	L	"	Н	Α	Α	"	"	
"			59	Α	В	Α	"	Α	В	В	В	Α	L	"	Н	Α	Α	"	u	
"			60	Α	В	Α	"	В	В	В	В	Α	Н	"	L	Α	Α	"	u	
"			61	В	В	Α	"	Α	В	Α	В	В	Н	"	L	Α	В	"	"	
"			62	В	Α	Α	"	Α	В	Α	В	В	Н	"	L	Α	В	"	ű	
u			63	В	В	Α	"	Α	В	Α	В	В	Н	"	L	Α	В	"	u	
"			64	В	В	Α	"	Α	В	В	Α	В	Н	"	L	Α	В	"	"	
"			65	В	Α	Α	"	Α	В	В	Α	В	Н	"	L	Α	В	"	"	
"			66	В	В	Α	"	Α	В	В	Α	В	Н	"	L	Α	В	"	"	
"			67	В	В	Α	"	Α	В	A	Α	Α	Н	"	L	Α	В		"	
			68	В	Α	Α		A	В	A	A	Α	Н	"	L	A	В	"	"	
"			69	В	В	Α	"	Α	В	Α	Α	A	Н	"	L	A	В	"	"	
"			70	A	В	A	"	A	В	A	A	В	Н	"	L	В	A	"	"	
"			71	Α	A	A	- "	A	В	A	A	В	L		Н	В	A	"		
			72	Α	В	A	"	A	В	A	A	В	L	"	Н	В	A	"		
"			73	A	A	A	"	A	В	A	A	В	H	"	<u> </u>	В	A	"	"	
"			74	A	В	A	"	A	В	A	A	В	H	"	L	В	A	"		
"			75	A	В	A	"	В	В	A	A	В	Н	- "	L	В	A	"		
			76	A	A	A	"	В	В	A	A	В	H	"	L	В	A	"	"	
"			77	A	В	A	"	В	В	A	A	В	H	"	L	В	A	"	"	
"			78 79	A	В	B B	"	B B	B B	A	A	B B		"	L	B B	A	"	"	
"				A A	A B	В	"	В		A	A		L	"	L	В	A	"	ű	
"			80 81	B	В	A	"	В	B B	A B	A B	B A	Н	"	L	A	A B	"	44	
"			82	В	В		"		В	В	В		H	"	L	A	В	"	44	
"	-		83	В	A	A A	"	A A	В	В	В	A A	H	"	L	A	В	"	"	
"			84	В	A	В	"	A	В	В	В	A	L	"	L	A	В	"	"	
"		 	85	В	В	В	"	A	В	В	В	A	L	"	H	A	В	"	u	
"		1	86	В	В	A	"	A	В	В	В	A	L	"	H	A	В	"	"	
"		1	87	В	A	A	"	A	В	В	В	A	L	"	H	A	В	"	"	
"		1	88	В	A	A	"	В	В	В	В	A	L	"	L	A	В	"	"	
"		 	89	В	A	A	"	A	В	В	В	A	<u> </u>	"	H	A	В	"	u	
u		 	90	A	В	A	"	A	В	A	A	В	L	"	H	В	A	"	"	
u		 	91	A	В	В	"	A	В	A	A	В	i	"	H	В	A	"	"	
"		1	92	A	A	В	"	A	В	A	A	В	L	"	H	В	A	"	"	

TABLE III. Group A inspection for device type 06. 1/- Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	is
		883	Case C	10	12	13	14	2	1	3	4	5	6	7	8	9	11	Meas.			
		method	Test No.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J*	Ια	GND	Q	K*	K2	terminal	Min	Max	Unit
9	F _{MAX} <u>5</u> /	(Fig. 14)	93	2.4 V	IN	5.0 V	5.0 V	5.0 V		2.4 V	2.4 V	GND		GND	OUT	GND	2.4 V	Q	20		MHz
$T_C = 25^{\circ}C$	F _{MAX} <u>5</u> /	(Fig. 14)	94	2.4 V	IN	5.0 V	u	5.0 V		2.4 V	2.4 V	GND	OUT	и		GND	2.4 V	Q	20		MHz
es	t _{PLH}	3003 (Fig. 13)	95	5.0 V	0.8 V	IN	и	IN		5.0 V	5.0 V	GND	OUT	u		GND	5.0 V	Clear to Q	5	50	ns
u	t _{PLH}	"	96	"	"	"	"	"		"	"	"		"	OUT	"	"	Preset to Q	"	"	"
u	t _{PHL}	"	97	u	u	"	u	u		и	"	"		"	OUT	"	u	Clear to Q	"	u	и
"	t _{PHL}	"	98	"	"	"	"	"		"	"	"	OUT	"		"	"	Preset to Q	"	"	"
u	(Fig. 15)	3003	99	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	50	ns
"	t _{PLH}	(Fig. 14)	100	"	"	"	u	"		"	44	"	OUT	"		"	"	Clock to Q	"	"	"
u	t _{PHL}	"	101	u	u	"	u	u		и	"	"		"	OUT	"	u	Clock to Q	"	u	и
u	t _{PHL}	"	102	u	u	"	u	u		"	"	и	OUT	"		"	u	Clock to Q	"	u	"
10	F _{MAX} <u>5</u> /	(Fig. 14)	103	2.4 V	IN	5.0 V	"	5.0 V		2.4 V	2.4 V	GND		"	OUT	GND	2.4 V	Q	15		MHz
T _C = 125°C	F _{MAX} <u>5</u> /	(Fig. 14)	104	2.4 V	IN	5.0 V	u	5.0 V		2.4 V	2.4 V	GND	OUT	"		GND	2.4 V	Q	15		MHz
u	t _{PLH}	3003 (Fig. 13)	105	5.0 V	0.8 V	IN	"	IN		5.0 V	5.0 V	GND	OUT	"		GND	5.0 V	Clear to Q	5	62	ns
u	t _{PLH}	"	106	"	"	"	"	u		u	"	"		"	OUT	"	u	Preset to Q	"	u	u
"	t _{PHL}	"	107	"	u	"	"	u		"	"	"		"	OUT	"	ű	Clear to Q	"	u	"
"	t _{PHL}	"	108	44	44	"	u	44		"	44	"	OUT	"		"	44	Preset to Q	"	**	"
"	t _{PLH}	3003	109	2.4 V	IN	5.0 V	u	5.0 V		5.0 V	5.0 V	GND		"	OUT	GND	2.4 V	Clock to Q	5	62	ns
u	t _{PLH}	(Fig. 14)	110	u	u	"	u	u		"	"	"	OUT	"		"	u	Clock to Q	"	u	"
"	t _{PHL}	"	111	u	u	u	u	u		u	u	u		"	OUT	u	u	Clock to Q	"	u	и
u	t _{PHL}	ш	112	и	и	"	"	ii .		"	"	"	OUT	"		"	"	Clock to Q	"	ii .	"

NOTES:

- A = Normal clock pulse.
 B = Momentary GND, then 4.5 V.

- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open). 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b)
- H≥1.5 V and L < 1.5 V when using a high speed checker single comparator.

 4/ Tests shall be performed in sequence.

 5 F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

	Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limits	
Test No. Clock Display 5· P																						
Tr = 2°C			method				Clear 1	V _{CC}	Clear				Q2	Q 2	GND				terminal	Min	Max	Unit
	1	V _{OH}	3006	1	Α	2.0 V		4.5 V							GND		4 mA		Q1	2.4		V
*** * * * * * * * * * * * * * * * * *	$T_C = 25^{\circ}C$	"	"	2	Α	0.8 V		"							"	4 mA			Q 1	"		и
** * * * * * * * * * * * * * * * * * *	u	"	u	3			0.8 V	"							"	4 mA		2.0 V	Q 1	"		"
	u	"	"				2.0 V	"							"		4 mA	0.8 V		"		"
	u	"	"					"					4 mA		"					"		"
. V. V. V. S. 100	u	"	ű					44		0.8 V	Α			4 mA	"					ű		"
Vo	u	"	"	7				"	0.8 V			2.0 V		4 mA	"				Q 2	"		"
** 190 A 0.8V 0.8V	u	"						"	2.0 V			0.8 V	4 mA							"		
10	"	V _{OL}	3007	9	Α	2.0 V		"							"	16 mA			Q 1		0.4 V	"
** * * * * * * * * * * * * * * * * * *	u	"	"	10	Α	0.8 V		u							u						u	"
	u	"	"	11			0.8 V	"							"		16 mA	2.0 V	Q 1		"	"
. " " 14	"	"	"	12			2.0 V	"							"	16 mA		0.8 V	Q1		"	"
" " 15	u	"	"	13				"		2.0 V	Α			16 mA	"				Q 2		"	"
* V _{1C}	"	"	"	14				"		0.8 V	Α		16 mA		"				Q2		"	"
- V _C 177	u	и	"					"					16 mA		"				Q2		u	и
	u	"	"	16				"	2.0 V			0.8 V		16 mA	"				Q 2		"	"
19	и	V _{IC}		17		-12 mA		"							"				D1		-1.5	"
"	u	"			-12 mA			u							"						"	"
12 12 12 12 12 12 12 12	"	"					-12 mA	"							"						"	
	"	"						"		10 1					"			-12 mA			"	- "
" " 23	"	"						"		-12 MA	-12 mA				"						"	"
	и	"						и	-12 m∆		-12 IIIA				"						и	"
	и	"						"	12 110 1			-12 mA			"						"	"
	"	I _{IL1}	3009	25	4.5 V	0.4 V	4.5 V	5.5 V							"			0.4 V		-0.5	-1.6	mA
" " " 28	u	"	"		0.4 V	0.4 V	4.5 V	u										0.4 V		"	"	"
	и	"																		"	"	"
" " " 30 0.8 V 4.5 V 0.4 V " 4.5 V 0.4 V " " 4.5 V 0.4 V GND " " Clock 2 " " " " " Clear 1 " " " " " " Clear 2 " " " " " " " " " " " " " " " " " "	"	."			0.41/	0.41/	451/		4.5 V	0.4 V	0.4 V	0.4 V						OND		4.0	"	- "
" " " 31	"	I _{IL2}	"					"							"					-1.0	-3.2	"
" " " 32	и	"	"		U.6 V	4.5 V	0.4 V	"	45 V	0.4.1/	041/	GND			"			4.5 V		"	"	"
I I I 3010 33 4.5 V 2.4 V GND	"	"	"					u							"					"	u	**
"	"	I _{IH1}	3010		4.5 V	2.4 V	GND	"							"			GND			40	цΑ
" " " 36	"	"	"	34				u	GND	2.4 V	4.5 V	GND			"				D2		40	"
" II II II II II II II II II II II II II	u	I _{IH2}	"		4.5 V	5.5 V	GND	"							"			GND				"
" 38 B 4.5 V 4.5 V " B 2.4 V GND " Clock 2 " " " " I I I I I I I I I I I I I I I	"	"	"		L			"	GND	5.5 V	4.5 V	GND			"							"
" " 39	"	I _{IH3}				451/		"							"							- "
"		"			В	4.5 V	4.5 V		D		2.4.1/	CND						2.4 V				
" I _{IH4} " 41 5.5 V B " GND Clock 1 200 " " " 42 B 4.5 V 4.5 V " B " 5.5 V GND " S.5 V Preset 1 " " " " 43 Clock 2 " " " " 44 Clock 2 " " " " 45 GND GND 2.4 V " Freset 2 " " " " " 46 Clock 2 " " " " " 46 GND GND 5.5 V " " Clear 1 120 " " I _{IH6} " 47 GND GND 5.5 V " " Clear 1 300 "	66				1	1				45 V				1								"
" 42 B 4.5 V 4.5 V " 5.5 V Preset 1 " " " " " " " " " " " " " " " " " "	u	lua	"		5.5 V		В	"	4.5 V	4.5 V		2.4 V			"			GND			200	"
" 43	и		"			4.5 V		"							"							"
" " 44	u	"						"			5.5 V	GND			"						u	"
" " 46	и	ű	"					"	4.5 V	4.5 V	В	5.5 V			"							"
" I _{IH6} " 47 GND GND 5.5 V " " " Clear 1 300 "	"	I _{IH5}	"		GND	GND	2.4 V	"							"							"
11H6 47 CND CND 3.3 V	"		"		ONE	OND	5.5.1	"	2.4 v	GND	GND				"							- "
		I _{IH6}	"	47	GND	GND	5.5 V	"	5.5 V	GND	GND				"				Clear 1 Clear 2		300	

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	.s
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	Vcc	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	U
1	Ios	3011	49				5.5 V							GND		GND	GND	Q1	-20	-57	n
_C = 25°C	"	"	50			GND	"							"	GND			Q 1	"	"	
u	"	"	51				"				GND	GND		"				Q2	"	"	+
"	"	"	52				"	GND			GND	GND	GND	"				Q 2	"	"	+
"																					_
"	I _{cc}	3005 3005	53 54	GND GND	GND GND	GND	"	GND	GND GND	GND	GND GND	GND		"			GND	V _{cc}		30 30	+-
2	Icc		ditions and limits								GND						<u> </u>	V _{CC}		30	
3	Same tests	, terminal con	ditions and limits					-													_
7 <u>2</u> / <u>4</u> /			55	В	В	В	4.5 V	В	В	В	В	H <u>3</u> /	H <u>3</u> /	GND "	H <u>3</u> /	H <u>3</u> /	В	All		H or L	۰,
Γ _C = 25°C			56 57	B B	В	В	"	В	B B	B B	A	<u>L</u>	H	"	H H	<u>L</u>	A	outputs "	-	as shown	3/
"			58	В	B B	A	"	A	В	В	A B	L H	Н	"		L H	A B	"		"	
"			59	A	В	A	и	A A	В	A	В	H	L	u	<u>L</u>	H	В	"		и	
u			60	A	В	B	"	В	В	A	В	H	Н	"	<u> </u>	H	В	"		"	
u			61	A	A	В	"	В	A	A	В	H	H	"	H	H	В	u		"	_
u			62	A	A	В	u	В	A	A	A	- i	H	u	H	L L	A	"		u	
u			63	A	Α	A	"	A	A	A	Α	Ē	Н	"	Н	Ĺ	A	"		"	
"			64	Α	Α	Α	"	Α	Α	Α	В	Н	L	"	L	Н	В	u		"	
"			65	Α	Α	Α	u	Α	Α	Α	Α	Н	L	"	L	Н	Α	"		"	
"			66	В	Α	Α	u	Α	Α	В	Α	Н	L	"	L	Н	Α	"		u	
"			67	В	В	Α	"	Α	В	В	Α	H	L	"	L	Н	Α	u		"	
"			68	A	В	A	"	A	В	A	A	<u> </u>	H	"	<u> </u>	L.	A	"		"	
			69 70	A	В	A B	"	A B	В	A	B B	H	H	"	<u>L</u>	H	B B	"			
"			70	A	A B	В	"	В	A B	A	В	H	Н	"	H	H	В	"		"	
"			72	A	В	В	u	В	В	A	A		H	u	H	i i	A	u		и	
"			73	A	В	A	u	A	В	A	A	Ī	H	u	H	Ī	A	"		u	
"			74	В	A	Α	"	A	A	В	Α	Ī	Н	"	H	Ī	A	"		"	
u			75	Α	Α	Α	"	Α	Α	Α	Α	Н	L	"	L	Н	Α	"		"	
ű			76	Α	Α	Α	"	Α	Α	Α	В	Н	L	"	L	Н	В	"		"	
u			77	Α	Α	Α	"	Α	Α	Α	Α	Н	L	"	L	Н	Α	u		и	
"			78	Α	Α	В	u	В	Α	Α	Α	L	Н	"	Н	L	Α	"		"	
"			79	Α	Α	Α	"	Α	Α	Α	Α	L	Н	"	H	L	Α	u		"	
"			80	A	В	A	"	A	В	A	В	<u>H</u>	L	"	<u>Ļ</u>	Н	В	"		"	
"	l		81	Α	В	Α	"	Α	В	Α	Α	Н	L	"	L	Н	Α	"		"	

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	:S
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			
		method	Test No.	Clock 1	D1	Clear 1	V _{cc}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
9	F _{MAX}	(Fig. 11)	82	IN	Е	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MHz
$T_C = 25^{\circ}C$	и	"	83	IN	E	5.0 V	"							"	OUT		5.0 V	Q 1	"		"
u	"	"	84				u .	5.0 V	Е	IN	5.0 V	OUT		u				Q2	и		и
"	и	"	85				"	5.0 V	E	IN	5.0 V		OUT	"				Q 2	"		"
ss .	t _{PLH}	3003 ((Fig. 10)	86			IN	"							"	OUT		IN	Clear 1 to Q 1	5	25	ns
и	и	и	87			IN	"							"		OUT	IN	Preset 1 to Q1	"	u	"
"	u	"	88				"	IN			IN		OUT	u				Clear 2	"	"	"
																		to Q 2			
"	"	"	89				"	IN			IN	OUT		"				Preset 2 to Q2	"	u	и
"	t _{PHL}	"	90			IN	"							"		OUT	IN	Clear 1 to Q1	"	33	"
"	u	"	91			IN	"							u	OUT		IN	Preset 1	"	36	"
																		to Q 1			
"	u	"	92				"	IN			IN		OUT	и				Clear 2	"	36	"
																		to Q 2			
"	и	"	93				"	IN			IN	OUT		"				Preset 2 to Q2	"	33	"
"	t _{PLH}	3003 <u>5</u> / (Fig. 11)	94	IN	IN (A)	В	"							"		OUT	5.0 V	Clock 1 to Q1	5	25	ns
"	"	(Fig. 12)	95	IN	IN (A)	5.0 V	"							"	OUT		В	Clock 1	"	"	"
																		to Q 1			
"	"	(Fig. 11)	96				"	В	IN (A)	IN	5.0 V	OUT		u				Clock 2	"	"	"
"	u	(Fig. 12)	97				и	5.0 V	IN (A)	IN	В		OUT	и				to Q2 Clock 2	"	и	"
		(1.19.12)	0.					0.0 1	(/ .)									to Q 2			
u	t _{PHL}	(Fig. 12)	98	IN	IN (B)	5.0 V	и							u		OUT	В	Clock 1	и	33	и
"	и	(Fig. 11)	99	IN	IN (B)	В	"							"	OUT		5.0 V	to Q1 Clock 1	"	"	"
		(5)			(=/	_												to Q 1			
"	и	(Fig. 12)	100				и	5.0 V	IN (B)	IN	В	OUT		и				Clock 2 to Q2	"	u	"
ű	u	(Fig. 11)	101				"	В	IN (B)	IN	5.0 V		OUT	и				Clock 2	"	"	"
																		to Q 2			

TABLE III. Group A inspection for device type 07. 1/ - Continued.

Subgroup	Symbol	MIL-STD-	Case A, B D	1	2	3	4	5	6	7	8	9	10	11	12	13	14			Test limit	.S
		883	Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4	Meas.			T
		method	Test No.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	Q 2	GND	Q 1	Q1	Preset 1	terminal	Min	Max	Unit
10	F _{MAX} <u>6</u> /	(Fig. 11)	102	IN	Е	5.0 V	5.0 V							GND		OUT	5.0 V	Q1	10		MHz
T _C = 125°C	u	u	103	IN	Е	5.0 V	"							и	OUT		5.0 V	Q 1	"		"
u	u	и	104				"	5.0 V	Е	IN	5.0 V	OUT		"				Q2	"		"
u	u	u	105				"	5.0 V	E	IN	5.0 V		OUT	и				_ Q 2	"		и
u	t _{PLH}	3003	106			IN	"							u	OUT		IN	Clear 1	5	31	ns
		((Fig. 10)																to Q 1			
	u	"	107			IN	"							"		OUT	IN	Preset 1 to Q1	"		"
u	u	u	108				"	IN			IN		OUT	u				Clear 2	"	"	"
																		to Q 2			
u	u	u	109				"	IN			IN	OUT		и				Preset 2	"	"	u
u	t _{PHL}	и	110			IN	"							и		OUT	IN	to Q2 Clear 1	"	39	и
	THE																	to Q1			
u		u	111			IN	"							u	OUT		IN	Preset 1 to Q 1	"	42	"
"	"	u	112				"	IN			INI		OUT	и					"	42	
			112					IIN			IN		001					Preset 2 to Q 2		42	
u	u	и	113				"	IN			IN	OUT		и				Clear 2	и	39	и
,,							"							"				to Q2	_		
	t _{PLH}	3003 <u>5</u> / (Fig. 11)	114	IN	IN (A)	В										OUT	5.0 V	Clock 1 to Q1	5	31	ns
u	u	(Fig. 12)	115	IN	IN (A)	5.0 V	"							"	OUT		В	Clock 1	"	"	"
																		to Q 1			
u	"	(Fig. 11)	116				"	В	IN (A)	IN	5.0 V	OUT		и				Clock 2 to Q2	"	"	и
u	u	(Fig. 12)	117				"	5.0 V	IN (A)	IN	В		OUT	"				Clock 2	"	"	"
																		to Q 2			
u	t _{PHL}	(Fig. 12)	118	IN	IN (B)	5.0 V	ш							и		OUT	В	Clock 1 to Q1	и	39	и
u	u	(Fig. 11)	119	IN	IN (B)	В	"							и	OUT		5.0 V	Clock 1	"	"	и
																		to Q 1			
u	и	(Fig. 12)	120				и	5.0 V	IN (B)	IN	В	OUT		и				Clock 2 to Q2	"	"	"
u	u	(Fig. 11)	121		 		"	В	IN (B)	IN	5.0 V		OUT	и			+	Clock 2	"	"	"
		, , ,							` ′									to Q 2			

- NOTES: A = Normal clock pulse.
- B = Momentary GND, then 4.5 V.
- E = Input D connected to \overline{Q} .

- 1/ Terminal conditions (pins not designated may be $H \ge 2.0 \text{ V}$, or $L \le 0.8 \text{ V}$, or open). 2/ Input voltages shown are: A = 2.0 V minimum and B = 0.8 V maximum. 3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b)
- $H \geq 1.5 \ V$ and L < 1.5 V when using a high speed checker single comparator.

- 4/ Tests shall be performed in sequence.
 5/ Tests shall be performed for both D input pulses (A and B).
 6/ F_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

5. PACKAGING

5.1 <u>Packaging requirements</u>. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

- 6.1 <u>Intended use.</u> Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
 - 6.2 Acquisition requirements. Acquisition documents should specify the following:
 - a. Title, number, and date of the specification.
 - b. PIN and compliance identifier, if applicable_ (see 1.2).
 - c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
 - d. Requirements for certificate of compliance, if applicable.
 - e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
 - f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
 - g. Requirements for product assurance options.
 - h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
 - I Requirements for "JAN" marking.
 - j. Packaging Requirements (see 5.1)
- 6.3 <u>Qualification</u>. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.
- 6.4 <u>Superseding information</u>. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 <u>Abbreviations, symbols, and definitions.</u> The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal

- 6.6 <u>Logistic support.</u> Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
- 6.7 <u>Substitutability.</u> The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type_
01	SN5472 (Circuit A)
01	DM5472 (Circuit B)
01	MC5472 (Circuit C)
02	SN5473 (Circuit A)
02	DM5473 (Circuit B)
02	S5473 (Circuit C)
03	SN54107 (Circuit A)
03	DM54107 (Circuit B)
03	S54107 (Circuit C)
04	SN5476 (Circuit A)
04	DM5476 (Circuit B)
04	S5476 (Circuit C)
05	5474 (Circuit A)
05	DM5474 (Circuit B)
06	5470
07	SN5479 (Circuit A)
07	MC5479 (Circuit B)

6.8 <u>Change from previous issue.</u> Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army - CR Navy - EC Air Force - 11 DLA - CC Preparing activity: DLA - CC

Review activities:

Army – SM, MI Navy - AS, CG, MC, SH TD Air Force – 03, 19, 99 (Project 5962-2096)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.