Quad Isolated Precision Gate Driver, 0.1 A Output

ADuM1420

FEATURES

Quad outputs isolated from input and each other
- **Input-to-output differential: ±700 V peak**
- **Output-to-output differential: ±700 V peak**

0.1 A peak output current
High frequency operation: 5 MHz maximum
High common-mode transient immunity: >75 kV/µs
High temperature operation: 105°C
Wide body, 28-lead SOIC

APPLICATIONS

Plasma display modules

GENERAL DESCRIPTION

The ADuM1420[1] is a quad isolated gate driver that employs Analog Devices, Inc. *i*Coupler® technology to provide independent and isolated high-side and low-side outputs.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM1420 offers the benefit of true, galvanic isolation between the input and each of the four outputs. Each output can be operated up to ±700 V peak relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between any two outputs can be as high as 700 V peak.

[1] Protected by U.S. Patents 5,952,849; 6,291,907; and 7,075,329.

FUNCTIONAL BLOCK DIAGRAM

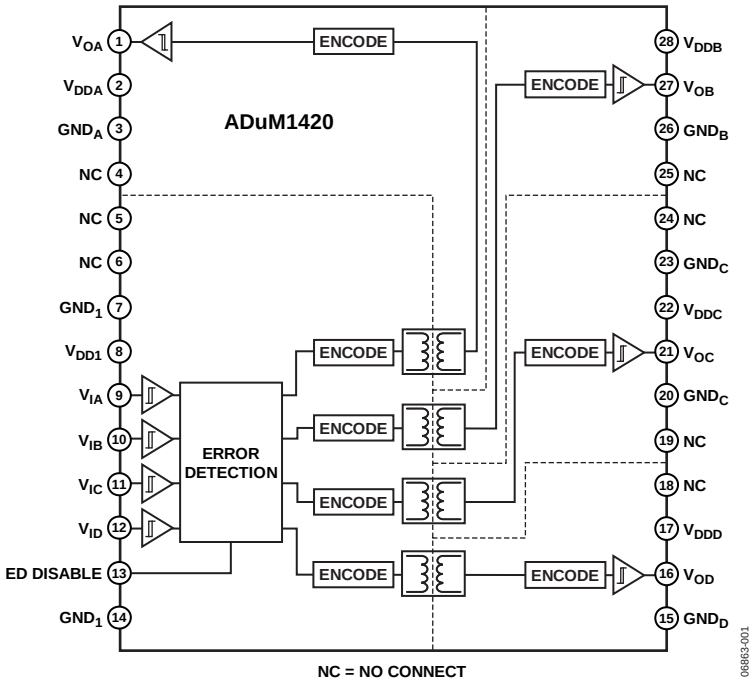

Figure 1.

Rev. A
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TABLE OF CONTENTS

REVISION HISTORY

2/08—Revision A: Initial Version

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 12 V ≤ V_{DDA} ≤ 18 V, 12 V ≤ V_{DDB} ≤ 18 V, 12 V ≤ V_{DDC} ≤ 18 V, 12 V ≤ V_{DDD} ≤ 18 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI (Q)}$		5.1	8.0	mA	
Output Supply Current (A, B, C, or D), Quiescent	$I_{DDA (Q)}$, $I_{DDB (Q)}$, $I_{DDC (Q)}$, $I_{DDD (Q)}$		0.3	1.2	mA	
Input Supply Current, 10 Mbps	$I_{DDI (10)}$		12	16	mA	
Output Supply Current (A, B, C, or D), 10 Mbps	$I_{DDA (10)}$, $I_{DDB (10)}$, $I_{DDC (10)}$, $I_{DDD (10)}$		16	22	mA	C_L = 200 pF
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, $I_{DISABLE}$	−10	+0.01	+10	μA	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.1, V_{DDB} − 0.1, V_{DDC} − 0.1, V_{DDD} − 0.1	V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}		V	I_{OA}, I_{OB}, I_{OC}, I_{OD} = −1 mA
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}			0.1	V	I_{OA}, I_{OB}, I_{OC}, I_{OD} = 1 mA
Output Short-Circuit Pulsed Current[1]	$I_{OA (SC)}$, $I_{OB (SC)}$, $I_{OC (SC)}$, $I_{OD (SC)}$	100			mA	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 200 pF, ED DISABLE = 0
Maximum Switching Frequency[3]		5			Mbps	C_L = 200 pF, ED DISABLE = 0
Propagation Delay[4]	t_{PHL}, t_{PLH}	99	110	128	ns	C_L = 200 pF, ED DISABLE = 0
Change vs. Temperature			85		ps/°C	C_L = 200 pF, ED DISABLE = 0
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			8	ns	C_L = 200 pF, ED DISABLE = 0
Channel-to-Channel Matching, Rising vs. Rising Edges[5]				5	ns	C_L = 200 pF, ED DISABLE = 0
Channel-to-Channel Matching, Falling vs. Falling Edges[5]				9	ns	C_L = 200 pF, ED DISABLE = 0
Channel-to-Channel Matching, Rising vs. Falling Edges[6]				13	ns	C_L = 200 pF, ED DISABLE = 0
Part-to-Part Matching, Rising or Falling Edges[7]				10	ns	C_L = 200 pF, ED DISABLE = 0, input t_R = 3 ns
Part-to-Part Matching, Rising vs. Falling Edges[8]				18	ns	C_L = 200 pF, ED DISABLE = 0, input t_R = 3 ns
Output Rise/Fall Time (10% to 90%)	t_R/t_F			25	ns	C_L = 200 pF, ED DISABLE = 0

[1] Short-circuit duration of less than 1 second. Average power must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.
[3] The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] Channel-to-channel matching, rising, or falling edges is the magnitude of the propagation delay difference between any two channels of the same part when the inputs are either both rising or falling edges. The supply voltages and the loads on each channel are equal.
[6] Channel-to-channel matching, rising vs. falling edges is the magnitude of the propagation delay difference between any two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.
[7] Part-to-part matching, rising, or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.
[8] Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

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PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		54		°C/W	
IC Junction-to-Case Thermal Resistance	θ_{JC}		13		°C/W	
Moisture Sensitivity Level				3		

[1] The device is considered a 2-terminal device: Pin 1 through Pin 14 are shorted together, and Pin 15 through Pin 28 are shorted together.

REGULATORY INFORMATION

The ADuM1420 will be approved by the organization listed in Table 3.

Table 3.

UL[1] (Pending)
Recognized under 1577 component recognition program, basic insulation, 1667 V rms isolation voltage.

[1] In accordance with UL 1577, each ADuM1420 is proof tested by applying an insulation test voltage ≥ 2000 V rms for 1 second (current leakage detection limit = 5 µA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		1667	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	2.1 min	mm	Measured from input terminals to output terminals B-D, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	2.1 min	mm	Measured from input terminals to output terminals B-D, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	4.5	5.5	V
Output Supply Voltages[1]	V_{DDA}, V_{DDB}	12	18	V
Input Signal Rise and Fall Times			100	ns
Common-Mode Transient Immunity, Input to Output[2]		−75	+75	kV/µs
Common-Mode Transient Immunity, Between Outputs[2]		−75	+75	kV/µs
Transient Immunity, Supply Voltages[2]		−75	+75	kV/µs

[1] All voltages are relative to their respective ground.
[2] See the Common-Mode Transient Immunity section for additional data.

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ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Input Supply Voltage (V_{DD1})[1]	−0.5 V to +7.0 V
Output Supply Voltage (V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD})[1]	−0.5 V to +27 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1]	−0.5 V to V_{DDA} + 0.5 V, V_{DDB} + 0.5 V, V_{DDC} + 0.5 V, V_{DDD} + 0.5 V
Input-to-Output Voltage[2]	−700 V peak to +700 V peak
Output Differential Voltage[3]	700 V peak
Output DC Current (I_{OA}, I_{OB})	−20 mA to +20 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] Input-to-output voltage is defined as GND_x − GND_1 where x is either A, B, C, or D.
[3] Output differential voltage is defined as GND_x − GND_y where x and y differ from each other and are either A, B, C, or D.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Table 7. Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{IC} Input	V_{ID} Input	ED DISABLE	V_{OA} Output	V_{OB} Output	V_{OC} Output	V_{OD} Output	V_{DD1} State[1]
L	L	L	L	L	L	L	L	L	Powered
L	L	L	H	L	L	L	L	H	Powered
L	L	H	L	L	L	L	H	L	Powered
L	L	H	H	L	L	L	L	L	Powered
L	H	L	L	L	L	H	L	L	Powered
L	H	L	H	L	L	L	L	L	Powered
L	H	H	L	L	L	H	H	L	Powered
L	H	H	H	L	L	L	L	L	Powered
H	L	L	L	L	H	L	L	L	Powered
H	L	L	H	L	H	L	L	H	Powered
H	L	H	L	L	L	L	L	L	Powered
H	L	H	H	L	L	L	L	L	Powered
H	H	L	L	L	L	L	L	L	Powered
H	H	L	H	L	L	L	L	L	Powered
H	H	H	L	L	L	L	L	L	Powered
H	H	H	H	L	L	L	L	L	Powered
L	L	L	L	NC or H	L	L	L	L	Powered
L	L	L	H	NC or H	L	L	L	H	Powered
L	L	H	L	NC or H	L	L	H	L	Powered
L	L	H	H	NC or H	L	L	H	H	Powered
L	H	L	L	NC or H	L	H	L	L	Powered
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H	L	H	L	NC or H	H	L	H	L	Powered
H	L	H	H	NC or H	H	L	H	H	Powered
H	H	L	L	NC or H	H	H	L	L	Powered
H	H	L	H	NC or H	H	H	L	H	Powered
H	H	H	L	NC or H	H	H	H	L	Powered
H	H	H	H	NC or H	H	H	H	H	Powered
X	X	X	X	X	L	L	L	L	Unpowered[2]

[1] Powered refers to the situation in which V_{DD1} is within the recommended operating conditions. Unpowered refers to the situation in which $V_{DD1} \leq 2.0$ V. Operation outside the recommended operating conditions is not recommended. See the Power-Up/Power-Down Considerations section for more information.
[2] Output returns to input state within 1 µs of V_{DD1} power restoration.

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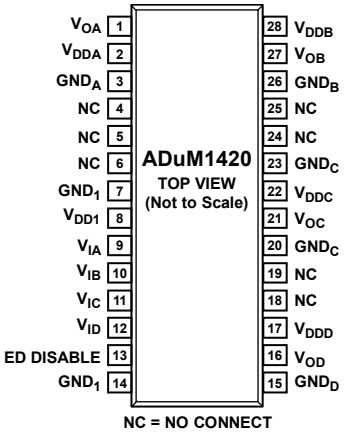
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
PIN 7 AND PIN 14 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 20 AND PIN 23 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_C IS RECOMMENDED. PIN 4, PIN 5, PIN 6, PIN 18, PIN 19, PIN 24, AND PIN 25 ARE FLOATING AND SHOULD BE LEFT UNCONNECTED.

06863-002

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OA}	Output A.
2	V_{DDA}	Output A Supply Voltage, 12 V to 18 V.
3	GND_A	Ground Reference for Output A.
4 to 6, 18, 19, 24, 25	NC	No Connection.
7, 14	GND_1	Ground Reference for Input Logic Signals.
8	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V.
9	V_{IA}	Logic Input A.
10	V_{IB}	Logic Input B.
11	V_{IC}	Logic Input C.
12	V_{ID}	Logic Input D.
13	ED DISABLE	Error Detection Disable. Disables the internal error detection function so that the logic outputs always match the logic inputs.
15	GND_D	Ground Reference for Output D.
16	V_{OD}	Output D.
17	V_{DDD}	Output D Supply Voltage, 12 V to 18 V.
20, 23	GND_C	Ground Reference for Output C.
21	V_{OC}	Output C.
22	V_{DDC}	Output C Supply Voltage, 12 V to 18 V.
26	GND_B	Ground Reference for Output B.
27	V_{OB}	Output B.
28	V_{DDB}	Output B Supply Voltage, 12 V to 18 V.

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TYPICAL PERFORMANCE CHARACTERISTICS

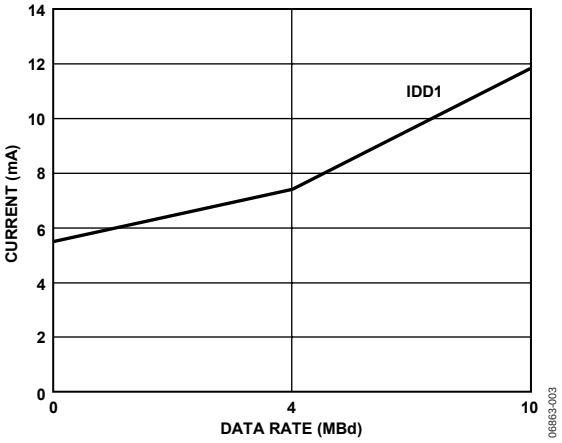

Figure 3. Typical Input Supply Current Variation with Data Rate

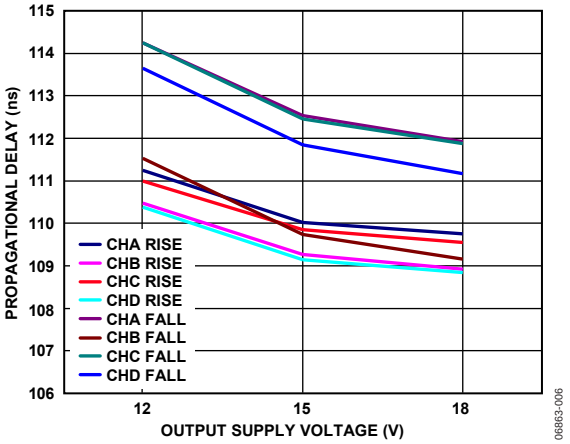

Figure 6. Typical Propagation Delay Variation with Output Supply Voltage (Input Supply Voltage = 5.0 V)

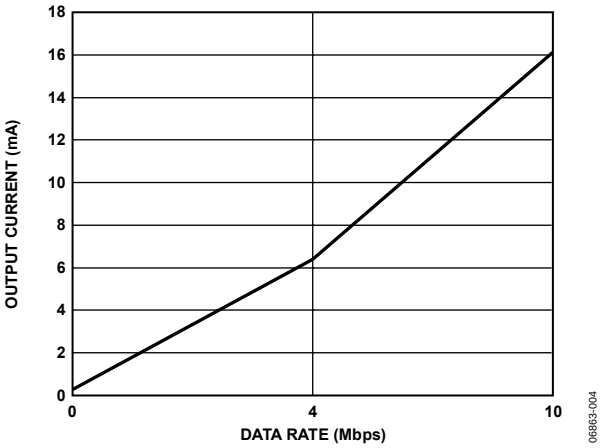

Figure 4. Typical Output Supply Current Variation with Data Rate

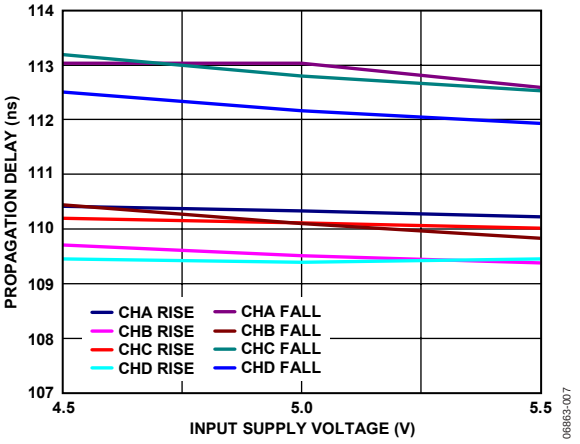

Figure 7. Typical Propagation Delay Variation with Input Supply Voltage (Output Supply Voltage = 15.0 V)

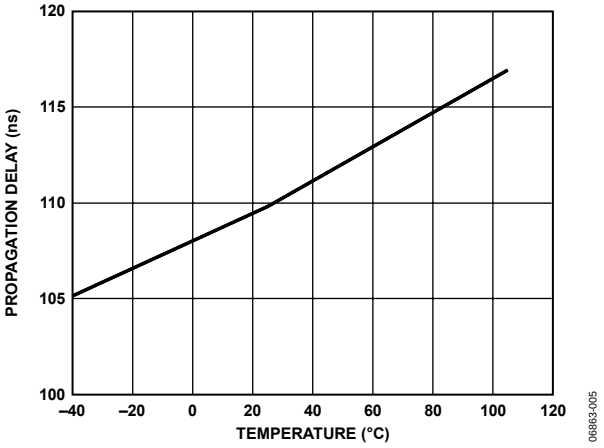

Figure 5. Typical Propagation Delay Variation with Temperature

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APPLICATION INFORMATION

COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM,\,linear} = (\Delta V/\Delta t)\ t$$

where $\Delta V/\Delta t$ is the slope of the transient shown in Figure 8 and Figure 9.

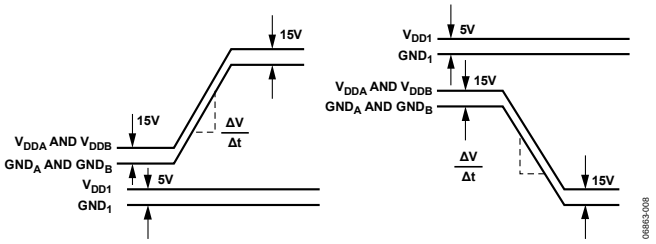

Figure 8. Common-Mode Transient Immunity Waveforms, Input to Output

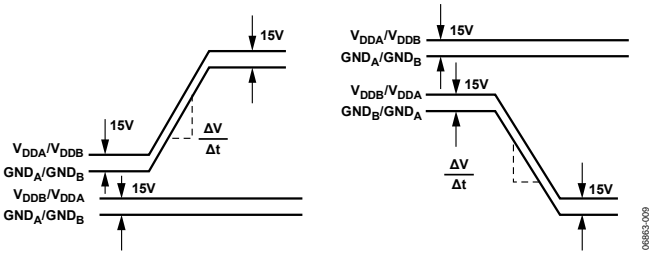

Figure 9. Common-Mode Transient Immunity Waveforms Between Outputs

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

The ability of the ADuM1420 to operate correctly in the presence of linear transients is characterized by the data in Figure 10. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM1420 can tolerate without an operational error. This data shows a higher level of robustness than what is shown in Table 5 because the transient immunity values obtained in Table 5 use measured data and apply allowances for measurement error and margin.

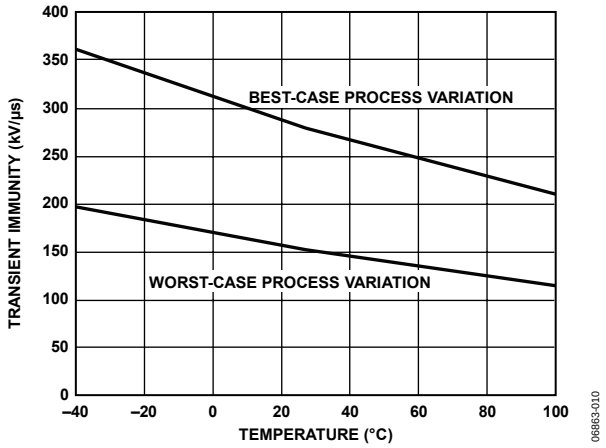

Figure 10. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM,\,sinusoidal} = V_0 \sin(2\pi ft)$$

where:
V_0 is the magnitude of the sinusoidal.
f is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f\ V_0$$

The ability of the ADuM1420 to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 11 and Figure 12. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f\ V_0$) that the ADuM1420 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 5 because measurements to obtain such values have not been possible.

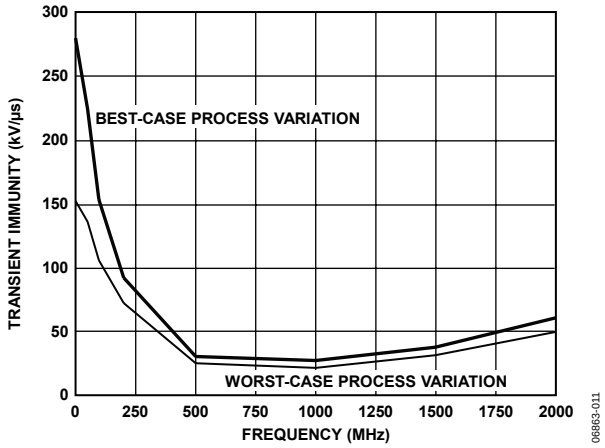

Figure 11. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

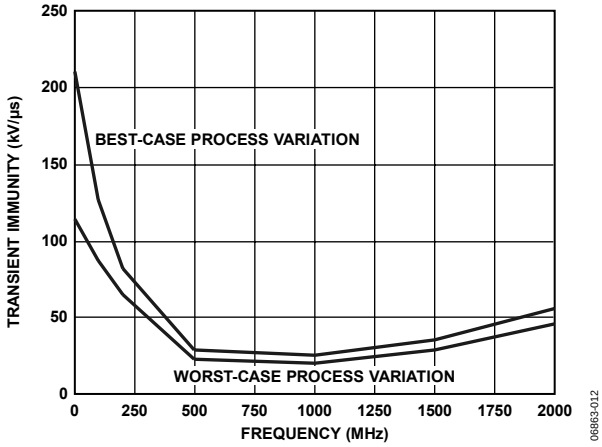

Figure 12. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

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POWER-UP/POWER-DOWN CONSIDERATIONS

Given that the ADuM1420 has separate supplies on either side of the isolation barrier for each channel, the power-up/power-down characteristics relative to each supply voltage need to be considered individually.

As shown in Table 7, when V_{DD1} input power is off, the ADuM1420 outputs take on a default low logic state. As the V_{DD1} supply is increased/decreased, the output of each channel transitions from/to a logic low to/from the state matching its respective input (see Figure 13 and Figure 14).

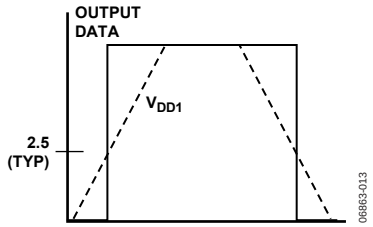

Figure 13. V_{DD1} Power-Up/Power-Down Characteristics, Input Data = High

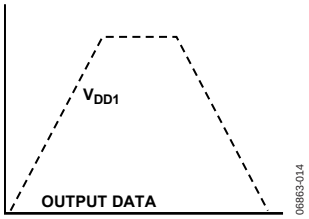

Figure 14. V_{DD1} Power-Up/Power-Down Characteristics, Input Data = Low

When V_{DD1} crosses the threshold for activating the refresh function (approximately 2.5 V), there can be a delay of up to 2 µs before the output is updated to the correct state, depending on the timing of the next refresh pulse. When V_{DD1} is reduced from an on state to below the 2.0 V threshold, there can be a delay of up to 5 µs before the output takes on its default low state.

In addition, during power-up/power-down, there is a range of V_{DD1} values within which erroneous outputs can occur if the input data either is a logic high or is in transition between logic states. This range is between 2.5 V and 2.7 V. The recommended practice is to set all the input logic levels to low during power-up/power-down.

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OUTLINE DIMENSIONS

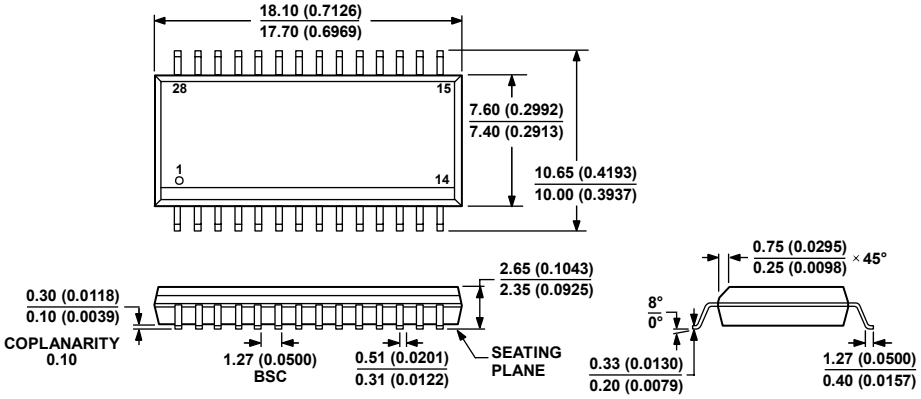

Figure 15. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM1420BRWZ[1]	4	0.1	15	−40°C to +105°C	28-Lead SOIC_W	RW-28
ADuM1420BRWZ-RL[1]	4	0.1	15	−40°C to +105°C	28-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units)	RW-28

[1] Z = RoHS Compliant Part.

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NOTES

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