

4-BIT SINGLE-CHIP MICROCONTROLLER FOR SMALL GENERAL-PURPOSE INFRARED REMOTE CONTROLLER

The μ PD17P236 is a model of the μ PD17236 with a one-time PROM instead of an internal mask ROM.

Since the user can write programs to the μ PD17P236, it is ideal for experimental production or small-scale production of the μ PD17230, 17231, 17232, 17233, 17234, 17235, or 17236 systems.

When reading this document, also read the documents related to the μ PD17230, 17231, 17232, 17233, 17234, 17235, and 17236.

Detailed functions are described in the following user's manual. Read this manual when designing your system.

μ PD172 $\times\times$ Series User's Manual: U12795E

FEATURES

- Pin compatible with μ PD17230, 17231, 17232, 17233, 17234, 17235, and 17236 (except PROM programming function)
- Carrier generator circuit for infrared remote controller (REM output)
- 17K architecture: General-purpose register method
- Program memory (one-time PROM): 32 Kbytes ($16,384 \times 16$)
- Data memory (RAM): 223×4 bits
- Low-voltage detection circuit
- Input/output of P1A₀ pin, clock selection for carrier generation

	μ PD17P236M1	μ PD17P236M2	μ PD17P236M3	μ PD17P236M4
Input/output of P1A ₀ pin	Output	Input	Output	Input
Clock (Rfx) selection for carrier generation	Rfx = fx/2		Rfx = fx	

- Supply voltage: $V_{DD} = 2.2$ to 3.6 V (fx = 4 MHz: high-speed mode, 4 μ s)
 $V_{DD} = 3.0$ to 3.6 V (fx = 8 MHz: high-speed mode, 2 μ s)

APPLICATIONS

Preset remote controllers, toys, and portable systems

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

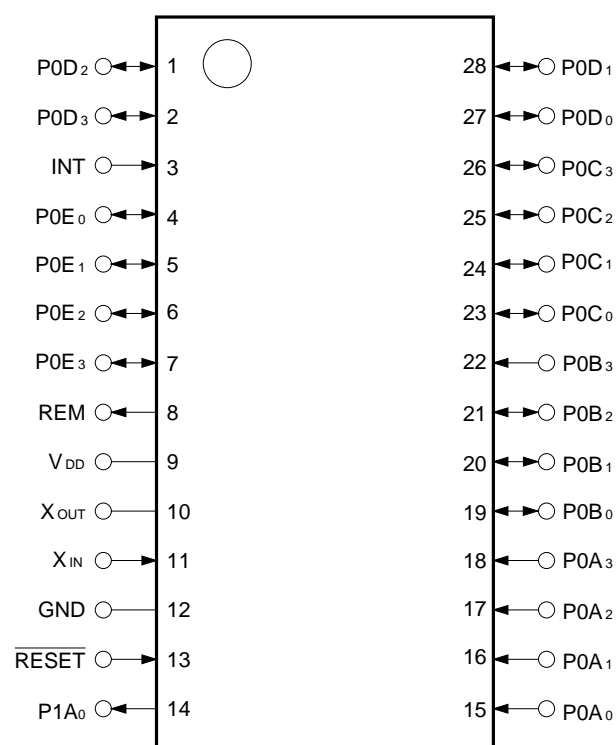
Part Number	Package
μPD17P236M1GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M1MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M2GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M2MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M3GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M3MC-5A4	30-pin plastic SSOP (7.62 mm (300))
μPD17P236M4GT	28-pin plastic SOP (9.53 mm (375))
μPD17P236M4MC-5A4	30-pin plastic SSOP (7.62 mm (300))

PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode

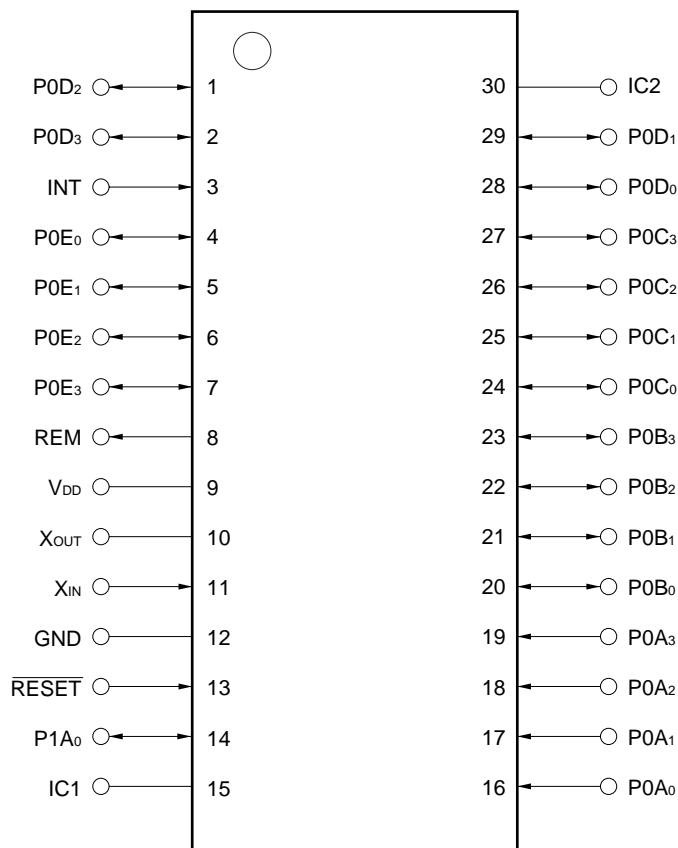
• 28-pin plastic SOP (9.53 mm (375))

μPD17P236M1GT, 17P236M2GT, 17P236M3GT, 17P236M4GT



• 30-pin plastic SSOP (7.62 mm (300))

μPD17P236M1MC-5A4, 17P236M2MC-5A4, 17P236M3MC-5A4, 17P236M4MC-5A4



- GND : Ground
- IC1, IC2 : Internally connected^{Note 1}
- INT : External interrupt request signal input
- P0A₀-P0A₃ : Input port (CMOS input)
- P0B₀-P0B₃ : Input/output port (CMOS input/N-ch open-drain output)
- P0C₀-P0C₃ : Input/output port (CMOS input/N-ch open-drain output)
- P0D₀-P0D₃ : Input/output port (CMOS input/N-ch open-drain output)
- P0E₀-P0E₃ : Input/output port (CMOS push-pull output)
- P1A₀ : Input port (CMOS input) or output port (N-ch open-drain output)^{Note 2}
- REM : Remote controller output (CMOS push-pull output)
- RESET : Reset input
- V_{DD} : Power supply
- X_{IN}, X_{OUT} : Resonator connection

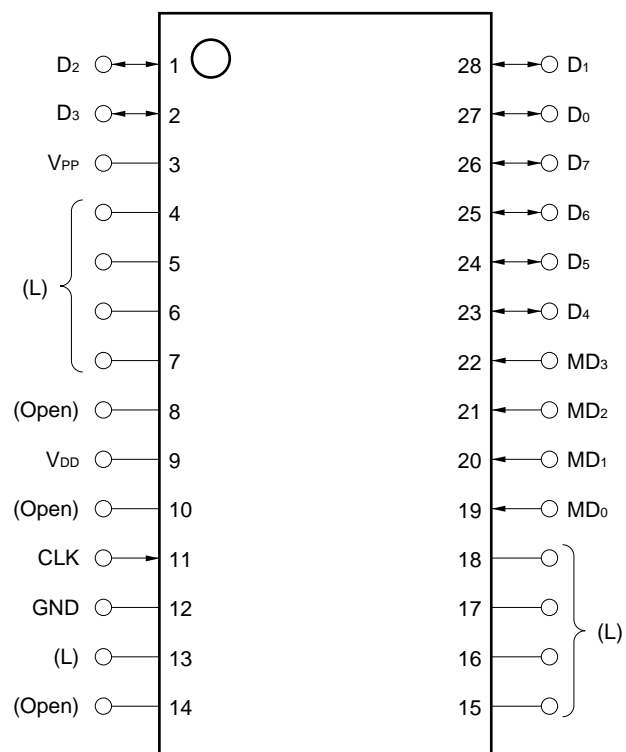
Notes 1. This pin cannot be used. Leave open.

2. Input port or output port is selected depending on the product (see 2. **PIN FUNCTIONS**).

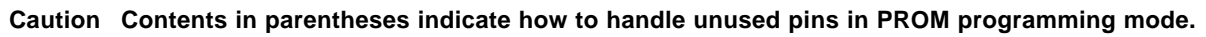
(2) PROM programming mode

• 28-pin plastic SOP (9.53 mm (375))

μPD17P236M1GT, 17P236M2GT, 17P236M3GT, 17P236M4GT



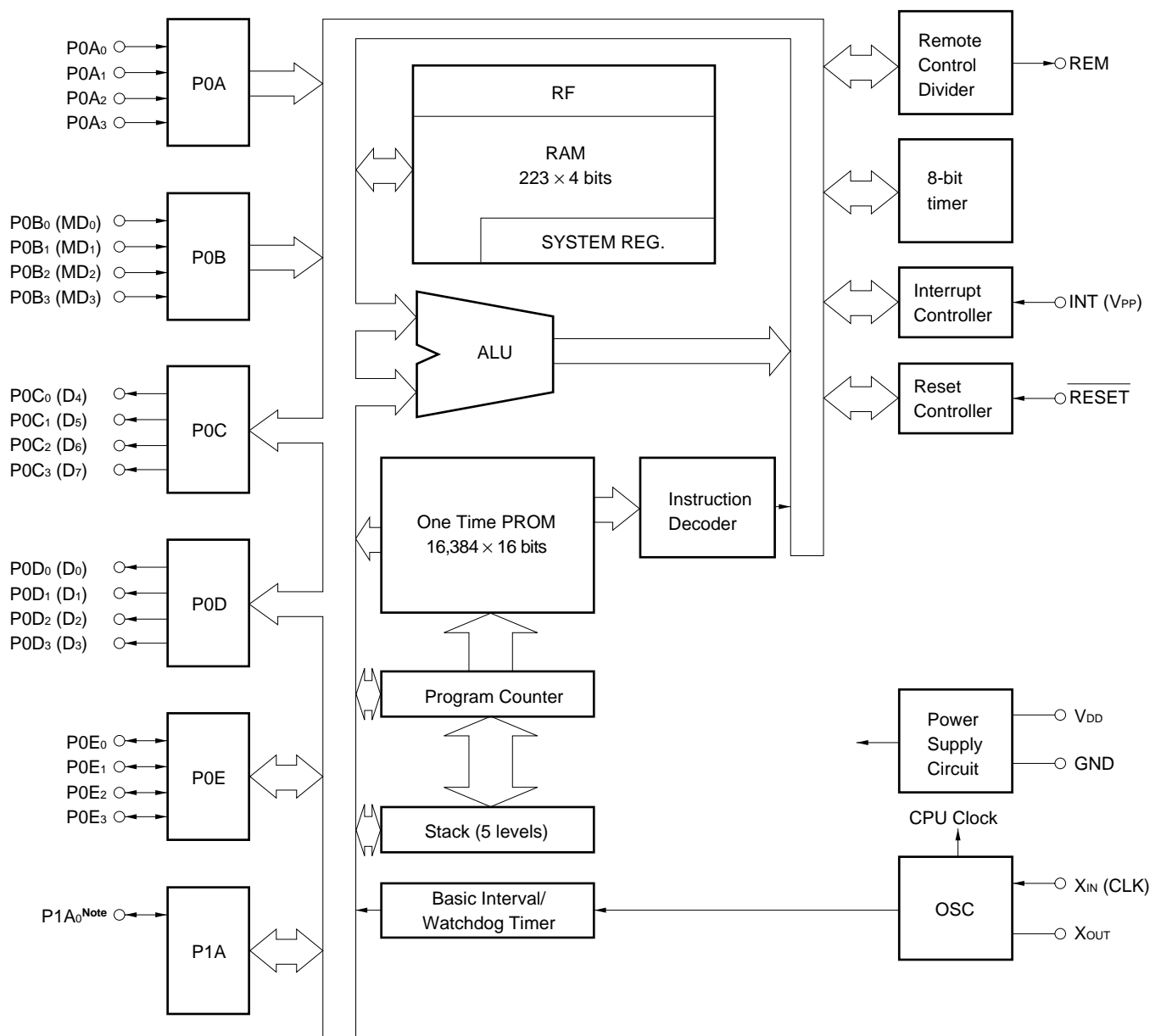
μ PD17P236M1MC-5A4, 17P236M2MC-5A4, 17P236M3MC-5A4, 17P236M4MC-5A4



Open : Leave unconnected.

Data Sheet U14776EJ1V0DS00

BLOCK DIAGRAM



Note Input port or output port is selected depending on the product (see 2. PIN FUNCTIONS).

Remark (): During PROM programming mode

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1. DIFFERENCES BETWEEN μ PD17236 AND μ PD17P236

μ PD17P236 is equipped with PROM to which data can be written by the user instead of the internal mask ROM (program memory) of the μ PD17236.

Table 1-1 shows the differences between the μ PD17236 and μ PD17P236.

The CPU functions and internal hardware of the μ PD17P236, 17230, 17231, 17232, 17233, 17234, 17235, and 17236 are identical. Therefore, the μ PD17P236 can be used to evaluate the program developed for the μ PD17230, 17231, 17232, 17233, 17234, 17235, and 17236 system. **Note, however, that some of the electrical specifications such as supply current and low-voltage detection voltage of the μ PD17P236 are different from those of the μ PD17230, 17231, 17232, 17233, 17234, 17235, and 17236.**

Table 1-1. Differences among μ PD17236 and μ PD17P236

Product Name Item	μ PD17P236 (μ PD17P236M1, 17P236M2, 17P236M3, 17P236M4)	μ PD17236
Program memory	One-time PROM 32 Kbytes ($16,384 \times 16$) (0000H-3FFFH)	Mask ROM
Data memory	223 \times 4 bits	
Input/output of P1A ₀ pin	<ul style="list-style-type: none"> Input (μPD17P236M2, 17P236M4) Output (μPD17P236M1, 17P236M3) 	Any (mask option)
Clock (Rf _x) selection for carrier generation	<ul style="list-style-type: none"> Rf_x = f_x/2 (μPD17P236M1, 17P236M2) Rf_x = f_x (μPD17P236M3, 17P236M4) 	Any (mask option)
Low-voltage detection circuit ^{Note}	Provided	Any (mask option)
Instruction execution time	<ul style="list-style-type: none"> 2 μs ($V_{DD} = 3.0$ to 3.6 V) 4 μs ($V_{DD} = 2.2$ to 3.6 V) 	<ul style="list-style-type: none"> 2 μs ($V_{DD} = 2.2$ to 3.6 V) 4 μs ($V_{DD} = 2.0$ to 3.6 V)
Supply voltage	$V_{DD} = 2.2$ to 3.6 V	$V_{DD} = 2.0$ to 3.6 V
Package	<ul style="list-style-type: none"> 28-pin plastic SOP (9.53 mm (375)) 30-pin plastic SSOP (7.62 mm (300)) 	

Note Although the circuit configuration is identical, its electrical characteristics differ depending on the product.

2. PIN FUNCTIONS

2.1 Normal Operation Mode (1/2)

Pin No.	Symbol	Function	Output Format	At Reset	
27 (28) 28 (29) 1 (1) 2 (2)	P0D ₀ P0D ₁ P0D ₂ P0D ₃	These pins constitute a 4-bit I/O port which can be set in the input or output mode in 4-bit units (group I/O). In the input mode, these pins serve as CMOS input pins with a pull-up resistor, and can be used as key return input lines of a key matrix. The standby status must be released when at least one of the input lines goes low. In the output mode, these pins are used as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Low-level output	
3 (3)	INT	External interrupt request signal. This signal releases the standby status if an external interrupt request signal is input to it when the INT pin interrupt enable flag (IP) is set.	—	Input	
4 (4) 5 (5) 6 (6) 7 (7)	P0E ₀ P0E ₁ P0E ₂ P0E ₃	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units. In the output mode, this port functions as a high current CMOS output port. In the input mode, function as CMOS input and can be specified to connect pull-up resistor by program.	CMOS push-pull	Input	
8 (8)	REM	Outputs transfer signal for infrared remote controller. Active-high output.	CMOS push-pull	Low-level output	
9 (9)	V _{DD}	Power supply	—	—	
10 (10) 11 (11)	X _{OUT} X _{IN}	Connects ceramic resonator for system clock oscillation	—	(Oscillation stops)	
12 (12)	GND	Ground	—	—	
13 (13)	$\overline{\text{RESET}}$	Turns ON pull down resistor if POC or watchdog timer overflows and if the stack pointer overflows or underflows, and resets the system. Usually, the pull-down resistor is ON.	—	Input	
14 (14)	P1A ₀	μ PD17P136M1, μ PD17P136M3	This pin is 1-bit output port (N-ch open-drain output) and can be used as the output lines of a key matrix.	N-ch open-drain	High-impedance output
		μ PD17P136M2, μ PD17P136M4	This pin is 1-bit input port (CMOS input). However, it cannot release the STOP mode.	—	Input
15 (16) 16 (17) 17 (18) 18 (19)	P0A ₀ P0A ₁ P0A ₂ P0A ₃	These pins are CMOS input pins with a 4-bit pull-up resistor. They can be used as the key return input lines of a key matrix. If any one of these pins goes low, the standby status is released.	—	Input	
19 (20) 20 (21) 21 (22) 22 (23)	P0B ₀ P0B ₁ P0B ₂ P0B ₃	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 1-bit units. In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low. In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Input	

Remark The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

2.1 Normal Operation Mode (2/2)

Pin No.	Symbol	Function	Output Format	At Reset
23 (24) 24 (25) 25 (26) 26 (27)	P0C ₀ P0C ₁ P0C ₂ P0C ₃	These pins constitute a 4-bit I/O port that can be set in the input or output mode in 4-bit units (group I/O). In the input mode, these pins are CMOS input pins with a pull-up resistor, and can be used as the key return input lines of a key matrix. The standby status is released when at least one of these pins goes low. In the output mode, they serve as N-ch open-drain output pins and can be used as the output lines of a key matrix.	N-ch open-drain	Low-level output
(15) (30)	IC1 IC2	These pins cannot be used. Leave open.	—	—

Remark The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

2.2 PROM Programming Mode

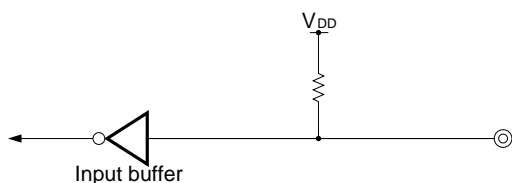
Pin No.	Symbol	Function	Output Format	At Reset
3	V _{PP}	Power supply for PROM programming. Apply +12.5 V to this pin as the program voltage when writing/verifying program memory.	—	—
9	V _{DD}	Power supply. Apply +6 V to this pin when writing/verifying program memory.	—	—
11	CLK	Inputs clock for PROM programming.	—	—
12	GND	Ground.	—	—
19 (20) 22 (23)	MD ₀ MD ₃	Input pins used to select operation mode when PROM is programmed.	—	Input
23 (24) 26 (27) 27 (28) 28 (29) 1 2	D ₄ D ₇ D ₀ D ₁ D ₂ D ₃	Input/output 8-bit data for PROM programming	CMOS push-pull	Input

- Remarks**
1. The other pins are not used in the PROM programming mode. How to handle the other opins are described in **PIN CONFIGURATION (2) PROM programming mode**.
 2. The number in parenthesis in the Pin No. column indicates the pin numbers of the 30-pin plastic SSOP.

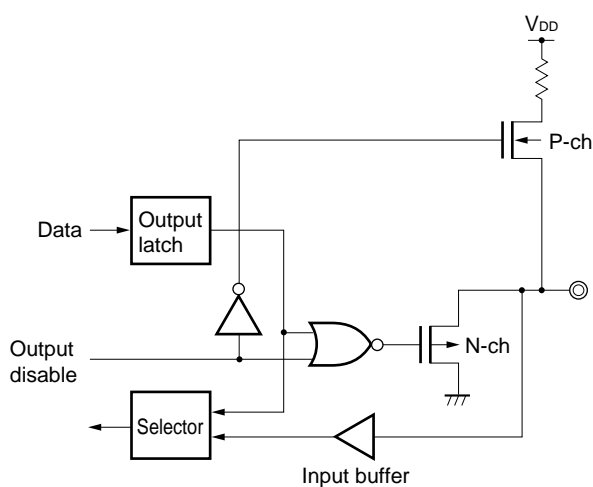
2.3 Input/Output Circuits

The equivalent input/output circuit for each μPD17P236 pin is shown below.

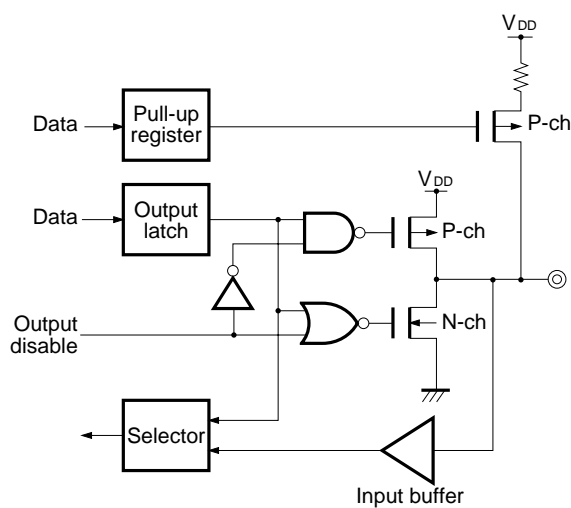
(1) P0A



(2) P0B, P0C, P0D

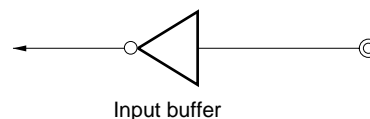


(3) P0E

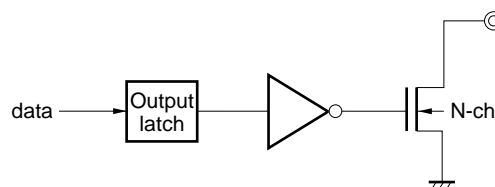


(4) P1A

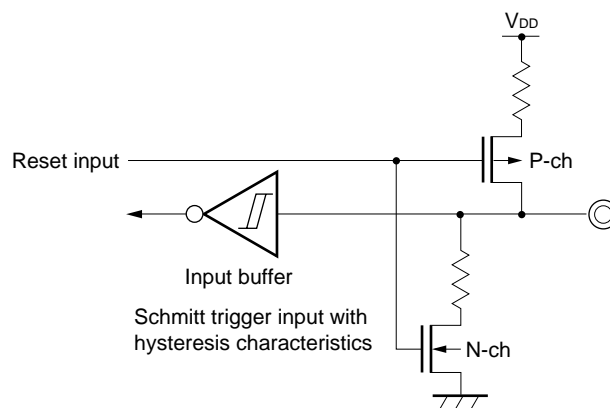
- Input mode (μPD17P236M2, 17P236M4)



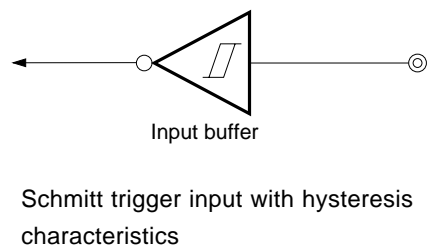
- Output mode (μPD17P236M1, 17P236M3)



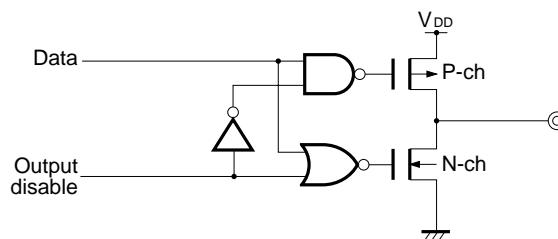
(5) RESET



(6) INT



(7) REM



2.4 Processing of Unused Pins

Process the unused pins as follows:

Table 2-1. Processing of Unused Pins

Pin	Recommended Connection
P0A ₀ -P0A ₃	Leave open.
P0B ₀ -P0B ₃	
P0C ₀ -P0C ₃	
P0D ₀ -P0D ₃	
P0E ₀ -P0E ₃	Input : Individually connect to V _{DD} or GND via resistor. Output : Leave open.
P1A ₀	Connect to GND.
REM	Leave open.
INT	Connect to GND.
IC1, IC2	These pins cannot be used. Leave open.

2.5 Notes on Using the RESET and INT Pins

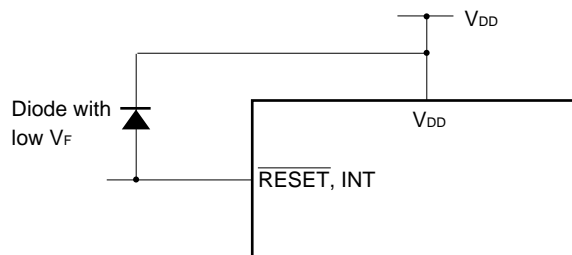
In addition to the functions shown in 2. PIN FUNCTIONS, the RESET pin also has the function of setting a test mode (for IC testing) in which the internal operations of the μPD17P236 are tested.

When a voltage higher than V_{DD} is applied to either of these pins, the test mode is set. This means that, even during normal operation, the μPD17P236 may be set in the test mode if noise exceeding V_{DD} is applied.

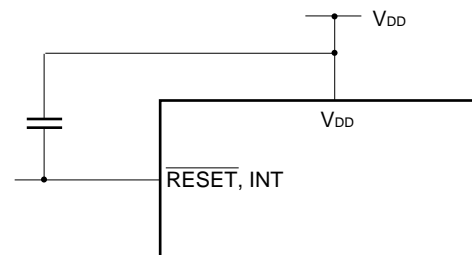
For example, if the wiring length of the RESET or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- Connect diode with low V_F between V_{DD} and RESET/INT pin



- Connect capacitor between V_{DD} and RESET/INT pin



3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μ PD17P236 is a one-time PROM of $16,384 \times 16$ bits.

To write or verify this one-time PROM, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

Table 3-1. Pins Used to Write/Verify Program Memory

Pin Name	Function
V _{PP}	Supplies voltage when writing/verifying program memory. Apply +12.5 V to this pin.
V _{DD}	Power supply. Supply +6 V to this pin when writing/verifying program memory.
CLK	Inputs clock to update address when writing/verifying program memory. By inputting pulse four times to CLK pin, address of program memory is updated.
MD ₀ -MD ₃	Input to select operation mode when writing/verifying program memory.
D ₀ -D ₇	Inputs/outputs 8-bit data when writing/verifying program memory.

3.1 Operating Mode When Writing/Verifying Program Memory

The μ PD17P236 is set in the program memory write/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after the μ PD17P236 has been in the reset status (V_{DD} = 5 V, $\overline{\text{RESET}} = 0$ V) for a specific time. In this mode, the operating modes shown in Table 3-2 can be set by setting the MD₀ through MD₃ pins. Leave all the pins other than those shown in Table 3-1 unconnected or connect them to GND via pull-down resistor (470 Ω). (See **PIN CONFIGURATION (2) PROM programming mode.**)

Table 3-2. Setting Operation Mode

Setting of Operating Mode						Operating Mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

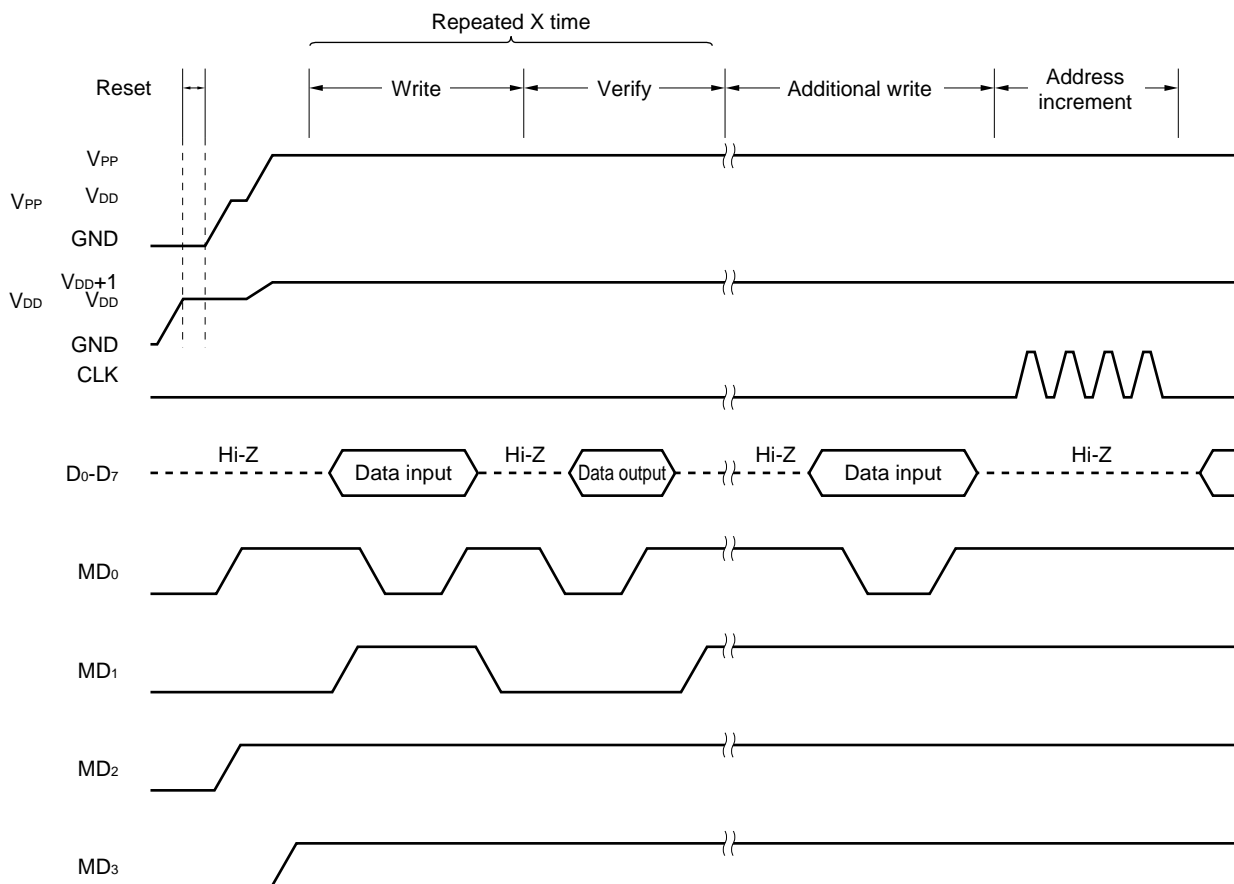
×: don't care (L or H)

3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μ s.
- (4) Set the program memory address 0 clear mode by using the mode setting pins.
- (5) Supply +6 V to V_{DD} and +12.5 V to V_{PP} .
- (6) Set the program inhibit mode.
- (7) Write data to the program memory in the 1-ms write mode.
- (8) Set the program inhibit mode.
- (9) Set the verify mode. If the data have been written to the program memory, proceed to (10). If not, repeat steps (7) through (9).
- (10) Additional writing of (number of times of writing in (7) through (9): X) \times 1 ms.
- (11) Set the program inhibit mode.
- (12) Input a pulse to the CLK pin four times to update the program memory address (+1).
- (13) Repeat steps (7) through (12) up to the last address.
- (14) Set the 0 clear mode of the program memory address.
- (15) Change the voltages on the V_{DD} and V_{PP} pins to 5 V.
- (16) Turn off power.

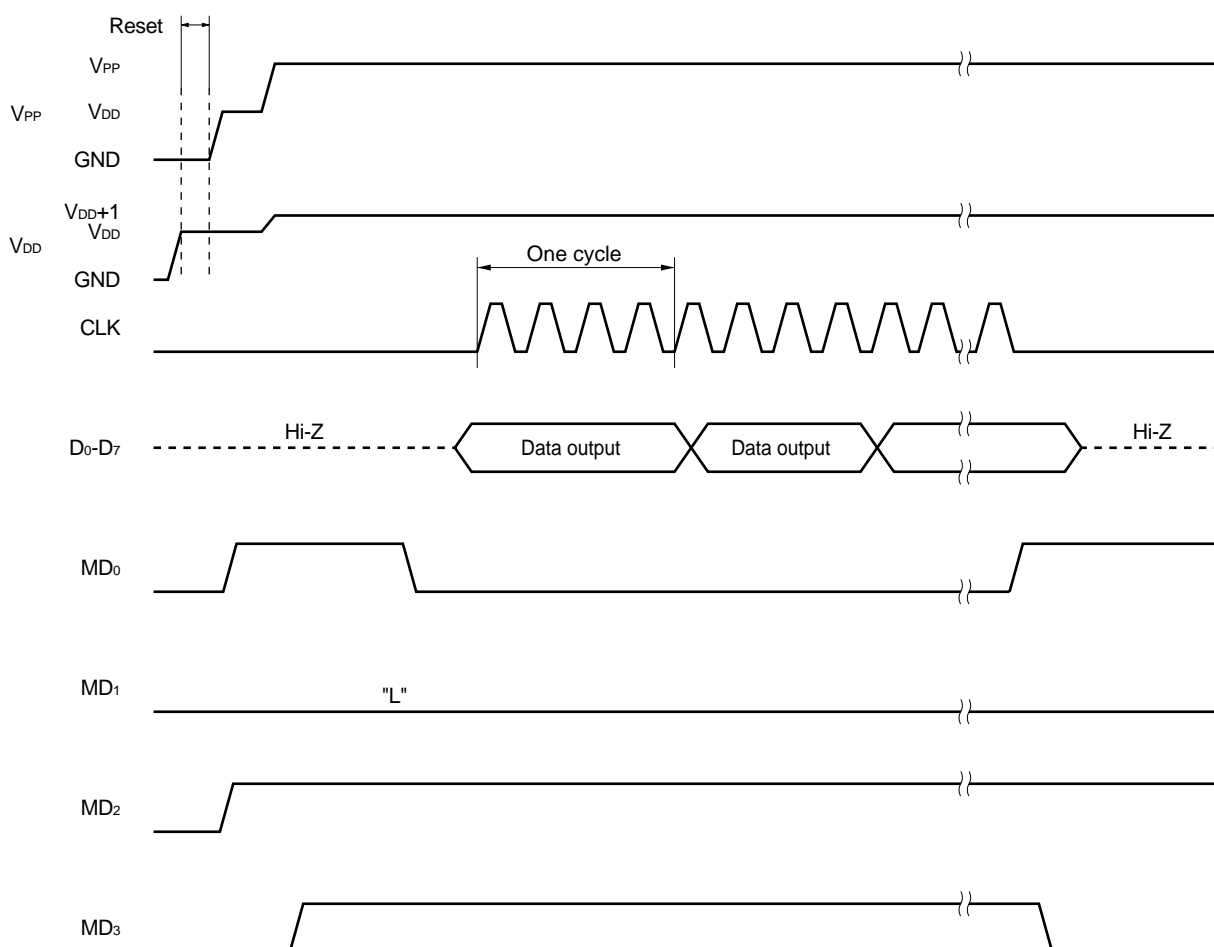
The following figure illustrates steps (2) through (12) above.



3.3 Program Memory Reading Procedure

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μ s.
- (4) Set the program memory address 0 clear mode by using the mode setting pins.
- (5) Supply +6 V to V_{DD} and +12.5 V to V_{PP} .
- (6) Set the program inhibit mode.
- (7) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
- (8) Set the program inhibit mode.
- (9) Set the program memory address 0 clear mode.
- (10) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
- (11) Turn off power.

The following figure illustrates steps (2) through (9) above.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Conditions		Ratings	Unit
Supply voltage	V _{DD}			−0.3 to +7.0	V
PROM power supply	V _{PP}			−0.3 to +13.5	V
Input voltage	V _I			−0.3 to V _{DD} + 0.3	V
Output voltage	V _O			−0.3 to V _{DD} + 0.3	V
High-level output current ^{Note}	I _{OH}	REM pin	Peak value	−36.0	mA
			rms value	−24.0	mA
		1 pin (P0E pin)	Peak value	−7.5	mA
			rms value	−5.0	mA
		Total of P0E pins	Peak value	−22.5	mA
			rms value	−15.0	mA
Low-level output current ^{Note}	I _{OL}	1 pin (P0B, P0C, P0D, P0E, P1A ₀ , or REM pin)	Peak value	7.5	mA
			rms value	5.0	mA
		Total of P0B, P0C, P0D, P1A ₀ , REM pins	Peak value	22.5	mA
			rms value	15.0	mA
		Total of P0E pins	Peak value	30.0	mA
			rms value	20.0	mA
Operating temperature	T _A			−40 to +85	°C
Storage temperature	T _{stg}			−65 to +150	°C
Power dissipation	P _d	T _A = 85°C		180	mW

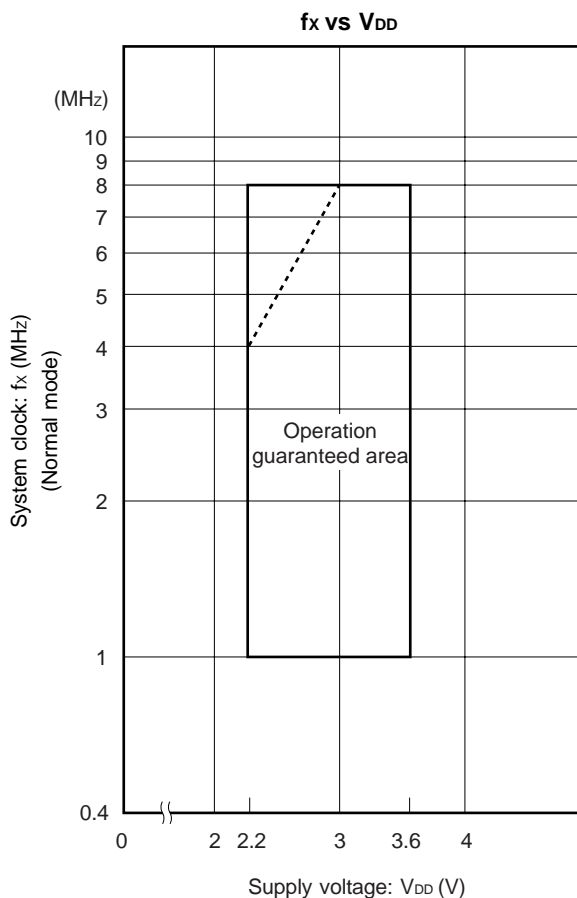
Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Ranges ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.2$ to 3.6 V)

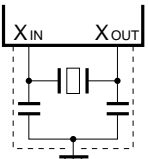
Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	$f_x = 1$ MHz	High-speed mode (Instruction execution time: $16\ \mu s$)	2.2		3.6	V
	V_{DD2}	$f_x = 4$ MHz	High-speed mode (Instruction execution time: $4\ \mu s$)				
	V_{DD3}	$f_x = 8$ MHz	Ordinary mode (Instruction execution time: $4\ \mu s$)				
	V_{DD4}		High-speed mode (Instruction execution time: $2\ \mu s$)	3.0		3.6	V
Oscillation frequency	f_x			1.0	4.0	8.0	MHz
Operating temperature	T_A			-40	+25	+85	°C
Low-voltage detector circuit ^{Note}	t_{CY}			4		32	μs

Note Reset if the status of $V_{DD} = 2.05$ V (TYP.) lasts for 1 ms or longer. Program hang-up does not occur even if the voltage drops, until the reset function is effected. Some oscillators stop oscillating before the reset function is effected.



Remark The region indicated by the broken line in the above figure is the guaranteed operating range in the high-speed mode.

System Clock Oscillator Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.2$ to 3.6 V)

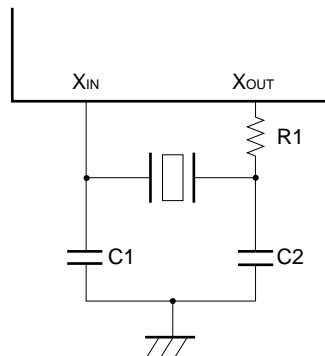
Resonator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_x) ^{Note 1}		1.0	4.0	8.0	MHz
		Oscillation stabilization time ^{Note 2}	After V_{DD} reached MIN. in oscillation voltage range			4	ms

Notes 1. The oscillation frequency only indicates the oscillator characteristics.

2. The oscillation stabilization time is necessary for oscillation to be stabilized, after V_{DD} application or STOP mode release.

Caution To use a system clock oscillator circuit, perform the wiring in the area enclosed by the dotted line in the above figure as follows, to avoid adverse wiring capacitance influences:

- Keep wiring length as short as possible.
- Do not cross a signal line with some other signal lines. Do not route the wiring in the vicinity of lines through which a large current flows.
- Always keep the oscillator capacitor ground at the same potential as GND. Do not ground the capacitor to a ground pattern, through which a large current flows.
- Do not extract signals from the oscillator.

External circuit example

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.2$ to 3.6 V)

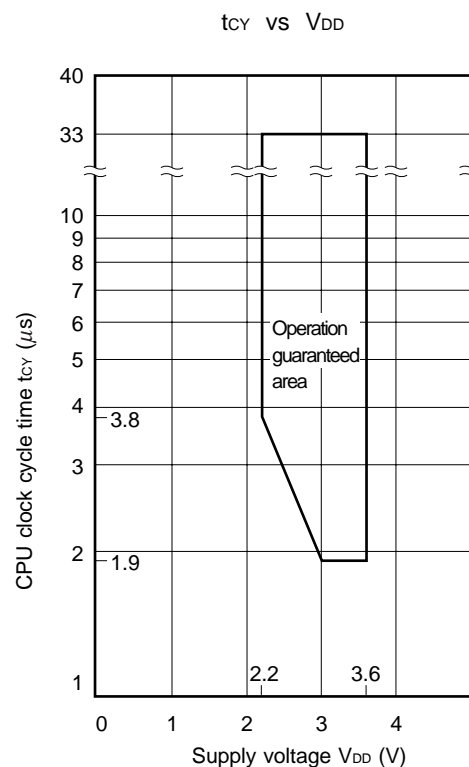
Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
High-level input voltage	V _{IH1}	P1A ₀ (input), $\overline{\text{RESET}}$, INT			0.8V _{DD}		V _{DD}	V
	V _{IH2}	P0A, P0B, P0C, P0D			0.7V _{DD}		V _{DD}	V
	V _{IH3}	P0E			0.8V _{DD}		V _{DD}	V
Low-level input voltage	V _{IL1}	P1A ₀ (input), $\overline{\text{RESET}}$, INT			0		0.2V _{DD}	V
	V _{IL2}	P0A, P0B, P0C, P0D			0		0.3V _{DD}	V
	V _{IL3}	P0E			0		0.35V _{DD}	V
High-level input leakage current	I _{LH}	P0A, P0B, P0C, P0D, P0E, P1A ₀ , $\overline{\text{RESET}}$, INT	V _{IH} = V _{DD}				3	μA
Low-level input leakage current	I _{LIL1}	INT, P1A ₀	V _{IL} = 0 V				−3	μA
	I _{LIL2}	P0E	V _{IL} = 0 V w/o pull-up resistor				−3	μA
Internal pull-up resistor	R ₁	P0E, $\overline{\text{RESET}}$ (pulled up)			25	50	100	kΩ
	R ₂	P0A, P0B, P0C, P0D			100	200	400	kΩ
Internal pull-down resistor	R ₃	$\overline{\text{RESET}}$ (pulled down)			2.5	5	10	kΩ
High-level output current	I _{OH1}	REM	V _{OH} = 1.0 V, V _{DD} = 3 V		−6	−13	−24	mA
High-level output voltage	V _{OH}	P0E, REM	I _{OH} = −0.5 mA		V _{DD} −0.3		V _{DD}	V
Low-level output voltage	V _{OL1}	P0B, P0C, P0D, P1A ₀ (output), REM	I _{OL} = 0.5 mA		0		0.3	V
	V _{OL2}	P0E	I _{OL} = 1.5 mA		0		0.3	V
Low-voltage detection voltage	V _{DT}	$\overline{\text{RESET}}$ pin pulled down, V _{DT} = V _{DD}				2.05	2.2	V
Data retention voltage	V _{DDDR}	$\overline{\text{RESET}}$ = low level or STOP mode			1.3		3.6	V
Supply current	I _{DD1}	Operating mode (high-speed)	V _{DD} = 3 V ±10%	f _X = 1 MHz		0.55	1.1	mA
				f _X = 4 MHz		1.0	2.0	mA
				f _X = 8 MHz		1.3	2.6	mA
	I _{DD2}	Operating mode (low-speed)	V _{DD} = 3 V ±10%	f _X = 1 MHz		0.5	1.0	mA
				f _X = 4 MHz		0.75	1.5	mA
				f _X = 8 MHz		0.9	1.8	mA
	I _{DD3}	HALT mode	V _{DD} = 3 V ±10%	f _X = 1 MHz		0.4	0.8	mA
				f _X = 4 MHz		0.5	1.0	mA
				f _X = 8 MHz		0.6	1.2	mA
	I _{DD4}	STOP mode	V _{DD} = 3 V ±10% built-in POC			2.0	20.0	μA
T _A = 25°C					2.0	5.0	μA	

AC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.2$ to 3.6 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU clock cycle time ^{Note} (instruction execution time)	t _{CY1}		3.8		33	μ s
	t _{CY2}	$V_{DD} = 3.0$ to 3.6 V	1.9		33	μ s
INT high/low level width	t _{INTH} , t _{INTL}		20			μ s
$\overline{\text{RESET}}$ low level lwidth	t _{RSL}		10			μ s

Note The CPU clock cycle time (instruction execution time) is determined by the oscillation frequency of the resonator connected and SYSCK (RF: address 02H) of the register file.

The figure on the right shows the CPU clock cycle time t_{CY} vs. supply voltage V_{DD} characteristics.



DC Programming Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Other than CLK	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	CLK	$V_{DD} - 0.5$		V_{DD}	V
Low-level input voltage	V_{IL1}	Other than CLK	0		$0.3V_{DD}$	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
High-level output voltage	V_{OH}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Low-level output voltage	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	$MD_0 = V_{IL}$, $MD_1 = V_{IH}$			30	mA

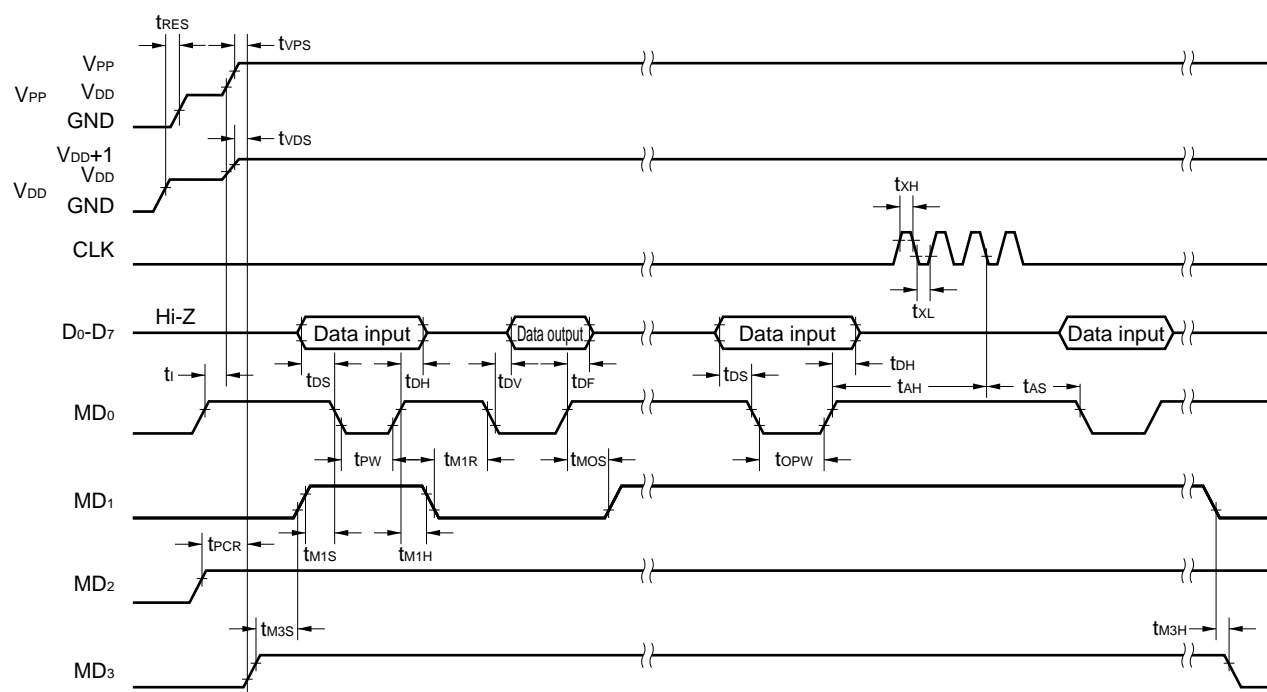
- Cautions**
1. Keep V_{PP} to within +13.5 V including overshoot.
 2. Apply V_{DD} before V_{PP} and turns it off after V_{PP} .

AC Programming Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

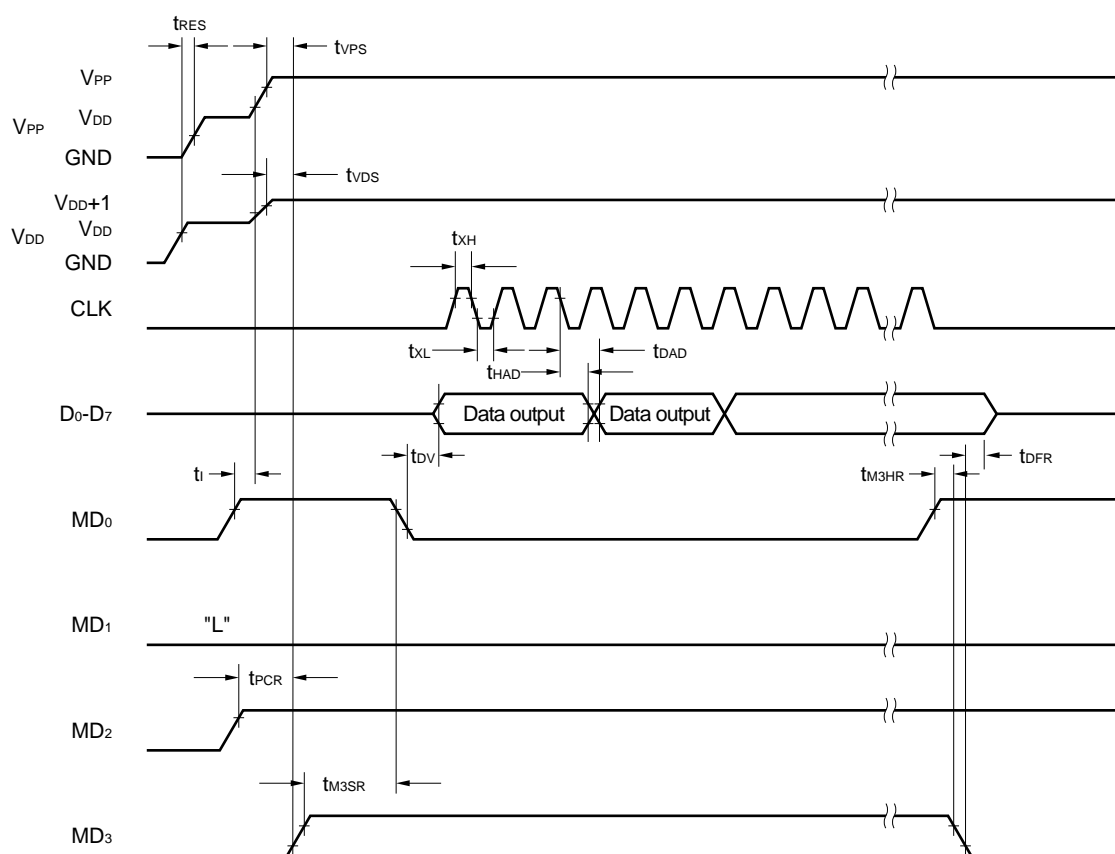
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time ^{Note} (vs. $MD_0\downarrow$)	t_{AS}		2			μs
MD_1 setup time (vs. $MD_0\downarrow$)	t_{M1S}		2			μs
Data setup time (vs. $MD_0\downarrow$)	t_{DS}		2			μs
Address hold time ^{Note} (vs. $MD_0\uparrow$)	t_{AH}		2			μs
Data hold time (vs. $MD_0\uparrow$)	t_{DH}		2			μs
$MD_0\uparrow \rightarrow$ data output float delay time	t_{DF}		0		130	ns
V_{PP} setup time (vs. $MD_3\uparrow$)	t_{VPS}		2			μs
V_{DD} setup time (vs. $MD_3\uparrow$)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD_0 setup time (vs. $MD_1\uparrow$)	t_{MOS}		2			μs
$MD_0\downarrow \rightarrow$ data output delay time	t_{DV}	$MD_0 = MD_1 = V_{IL}$			1	μs
MD_1 hold time (vs. $MD_0\uparrow$)	t_{M1H}	$t_{M1H} + t_{M1R} \geq 50\text{ }\mu\text{s}$	2			μs
MD_1 recovery time (vs. $MD_0\downarrow$)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-, low-level width	t_{XH} , t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode set time	t_i		2			μs
MD_3 setup time (vs. $MD_1\uparrow$)	t_{M3S}		2			μs
MD_3 hold time (vs. $MD_1\downarrow$)	t_{M3H}		2			μs
MD_3 setup time (vs. $MD_0\downarrow$)	t_{M3SR}	When program memory is read	2			μs
Address ^{Note} \rightarrow data output delay time	t_{DAD}	When program memory is read			2	μs
Address ^{Note} \rightarrow data output hold time	t_{HAD}	When program memory is read	0		130	ns
MD_3 hold time (vs. $MD_0\uparrow$)	t_{M3HR}	When program memory is read	2			μs
$MD_3\downarrow \rightarrow$ data output float delay time	t_{DFR}	When program memory is read			2	μs
Reset setup time	t_{RES}		10			μs

Note The internal address increment (+1) is performed on the fall of the 3rd clock, where 4 clocks comprise one cycle. The internal clock is not connected to a pin.

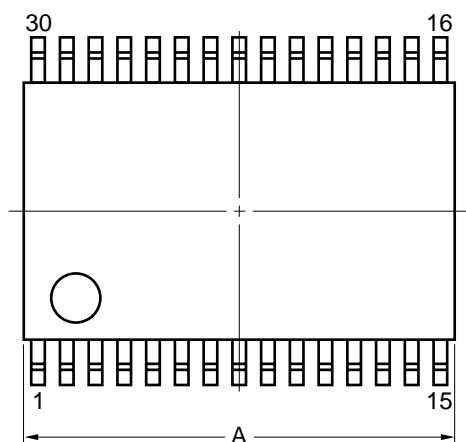
Program Memory Write Timing



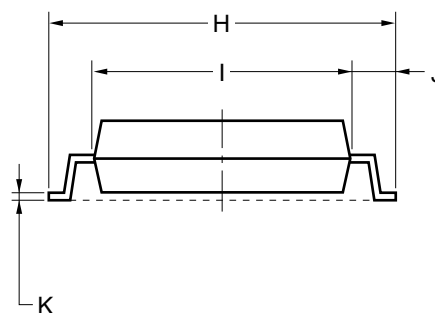
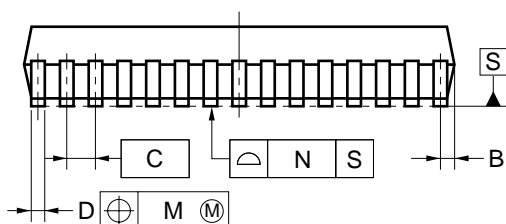
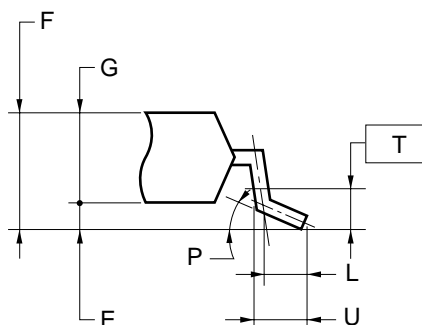
Program Memory Read Timing



30-PIN PLASTIC SSOP (7.62 mm (300))



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

6. RECOMMENDED SOLDERING CONDITIONS

For the μPD17P236 soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document "**Semiconductor Device Mounting Technology Manual**" (C10535E).

For other soldering methods, please consult with NEC personnel.

Table 6-1. Soldering Conditions of Surface Mount Type

(1) μPD17P236M1GT: 28-pin plastic SOP (9.35 mm (375))

μPD17P236M2GT: 28-pin plastic SOP (9.35 mm (375))

μPD17P236M3GT: 28-pin plastic SOP (9.35 mm (375))

μPD17P236M4GT: 28-pin plastic SOP (9.35 mm (375))

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max. Number of days: 7 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of days: 7 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max, Time: 10 seconds max., Number of times: once, preheating temperature: 120°C max. (package surface temperature) Number of days: 7 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	—

Note After opening the dry pack, store it at 25 °C or less and 6.5 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μ PD17P236M1MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

μ PD17P236M2MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

μ PD17P236M3MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

μ PD17P236M4MC-5A4: 30-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max. Number of days: 3 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max. Number of days: 3 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max, Time: 10 seconds max., Number of times: once, preheating temperature: 120°C max. (package surface temperature) Number of days: 3 ^{Note} (after that, prebaking is necessary at 125°C for 10 hours)	WS60-103-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	—

Note After opening the dry pack, store it at 25 °C or less and 6.5 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX. DEVELOPMENT TOOLS

To develop the programs for the μ PD17P236 subseries, the following development tools are available:

Hardware

Name	Remarks
In-circuit emulator (IE-17K, IE-17K-ET ^{Note 1})	IE-17K and IE-17K-ET are the in-circuit emulators used in common with the 17K series microcontroller. IE-17K and IE-17K-ET are connected to a PC-9800 series or IBM PC/AT TM compatible machines as the host machine with RS-232C. By using these in-circuit emulators with a system evaluation board corresponding to the microcomputer, the emulators can emulate the microcomputer. A higher level debugging environment can be provided by using man-machine interface <i>SIMPLEHOST</i> TM .
SE board (SE-17235)	This is an SE board for μ PD17236 subseries. It can be used alone to evaluate a system or in combination with an in-circuit emulator for debugging.
Emulation probe (EP-17K28GT)	EP-17K28GT is an emulation probe for 17K series 28-pin SOP (GM-375B). When used with EV9500GT-28 ^{Note 2} , it connects an SE board to the target system.
Emulation probe (EP-17K30GS)	EP-17K30GS is an emulation probe for 17K series 30-pin SSOP (MC-5A4). When used with EV-9500GT-30 ^{Note 3} , it connects an SE board to the target system.
Conversion adapter (EV-9500GT-28 ^{Note 2})	The EV-9500GT-28 is a conversion adapter for the 28-pin SOP (GM-375B). It is used to connect the EP-17K28GT and target system.
Conversion adapter (EV-9500GT-30 ^{Note 3})	The EV-9500GT-30 is a conversion adapter for the 30-pin SSOP (MC-5A4). It is used to connect the EP-17K30GS and target system.
PROM programmer (AF-9706 ^{Note 4} , AF-9708 ^{Note 4} , AF-9709 ^{Note 4})	AF-9706, AF-9708, and AF-9709 are PROM programmers corresponding to μ PD17P236. By connecting program adapter PA-17P236 to this PROM programmer, μ PD17P236 can be programmed.
Program adapter (PA-17P236)	PA-17P236 are adapters that is used to program μ PD17P236, and is used in combination with AF-9706, AF-9708, or AF-9709.

Notes 1. Low-cost model: External power supply type

2. Two EV-9500GT-28 are supplied with the EP-17K28GT. Five EV-9500GT-28 are optionally available as a set.
3. Two EV-9500GT-30 are supplied with the EP-17K30GS. Five EV-9500GT-30 are optionally available as a set.
4. These are products from Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd. (Tel: 03-3733-1166).

Software

Name	Outline	Host Machine	OS	Supply	Order Code
17K assembler (RA17K)	The RA17K is an assembler common to the 17K series products. When developing the program of devices, RA17K is used in combination with a device file (AS17235).	PC-9800 series	Japanese Windows™	3.5" 2HD	μ SAA13RA17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μ SAB13RA17K
			English Windows		μ SBB13RA17K
Device file (AS17235)	The AS17235 is a device file for μ PD17230, 17231, 17232, 17233, 17234, 17235, and 17236 and is used in combination with an assembler for the 17K series (RA17K).	PC-9800 series	Japanese Windows	3.5" 2HD	μ SAA13AS17235
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μ SAB13AS17235
			English Windows		μ SBB13AS17235
Support software (SIMPLEHOST)	SIMPLEHOST is a software package that enables man-machine interface on the Windows when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	Japanese Windows	3.5" 2HD	μ SAA13ID17K
		IBM PC/AT compatible machine	Japanese Windows	3.5" 2HC	μ SAB13ID17K
			English Windows		μ SBB13ID17K

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Hong Kong
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Fax: 2886-9022/9044

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United Square, Singapore 1130
Tel: 65-253-8311
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NEC do Brasil S.A.

Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
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