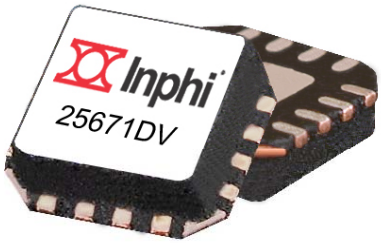
# 25671DV
# DC to 25 GHz Divide-by-2 Prescaler in QFN Plastic Package
# Data Sheet




## Applications

- Phase-locked loop (PLL) applications from DC to 25 GHz
- Point-to-point and point-to-multipoint digital radios
- Broadband test and measurement equipment

## Features

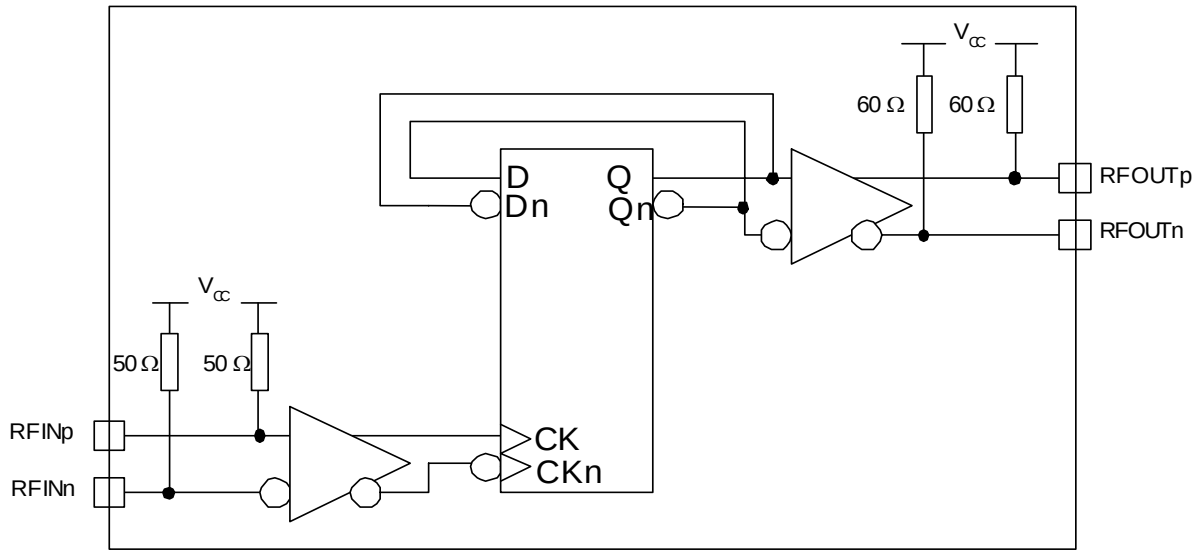
- Wide frequency range: DC to 25 GHz
- High input power sensitivity, –20 dBm typical
- Supports single-ended and differential operation
- Single +3.0 to +3.5 V power supply
- Low supply current: 76 mA typical
- Available in QFN plastic package
- Also available in die form or in LGA ceramic package
- Evaluation board available

## Description

The 25671DV-QFN divide-by-2 prescaler is designed for a wide range of communications and broadband test and measurement applications from DC to 25 GHz. It is typically used in high-frequency phase-locked loop (PLL) oscillator and signal-path down conversion circuits.

The 25671DV operates from a single +3.0 to +3.5 V power supply and is available in a 3 x 3 mm quad flat no lead (QFN) plastic package. This part is also available in die form or in a 7 x 7 mm ceramic package. Please contact Inphi to obtain data sheets for these versions. The packaged parts are also available on an evaluation board.

## Block Diagram




## Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | | –0.5 | +3.6 | V |
| CW RF Input Power | $P_{IN}$ (CW) | | --- | +5 | dBm |
| DC Input Voltage | $V_{RFIN}$ | | $V_{CC}$-2 | $V_{CC}$+0.6 | V |
| DC Output Voltage | $V_{RFOUT}$ | | $V_{CC}$-1.5 | $V_{CC}$+1.0 | V |
| Operating Temperature (Junction) | $T_J$ | | –40 | +175 | °C |
| Operating Temperature (Case) | $T_C$ | | –55 | +125 | °C |
| Shipping/Storage Temperature | $T_{STORE}$ | | –65 | +125 | °C |
| Humidity | RH | | 0 | 100 | % |

## Operating Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | | +3.0 | +3.3 | +3.5 | V |
| Supply Current | $I_{CC}$ | | --- | 76 | 98 | mA |
| Operating Temperature (Junction) | $T_J$ | | –20 | --- | +125 | °C |
| Operating Temperature (Case) | $T_C$ | | –40 | --- | +85 | °C |
| Thermal Resistance | $R_{JC}$ | | --- | --- | 54 | °C/W |

# Electrical Specifications

**WARNING** – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

| Electrical specifications guaranteed when the part is operated within the specified operating conditions | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Max Input Frequency | $F_{IN}$ (max) | | 25 | 26 | --- | GHz |
| Min Input Frequency[1] | $F_{IN}$ (min) | | --- | 0.5 | 1.0 | GHz |
| Input Return Loss | $RL_{IN}$ | < 25 GHz, $V_{CMIN} \leq V_{CC}$ | 10 | --- | --- | dB |
| Input Return Loss | $RL_{IN}$ | < 25 GHz, $V_{CMIN} > V_{CC}$ | 6 | --- | --- | dB |
| Output return Loss | $RL_{OUT}$ | < 13 GHz | 10 | --- | --- | dB |
| Input Power Range[2] | $P_{IN}$ | 2 – 4 GHz (sine wave) Single ended, AC coupled | - 4 | > - 10 | 4 | dBm |
| | | 4 – 8 GHz (sine wave) Single ended, AC coupled | - 10 | > - 20 | 4 | dBm |
| | | 8 – 20 GHz (sine wave) Single ended, AC coupled | - 16 | > - 25 | 4 | dBm |
| | | 20 – 24 GHz (sine wave) Single ended, AC coupled | - 8 | > - 15 | 4 | dBm |
| Output Power | $P_{OUT}$ | Single ended, AC coupled, $F_{IN}$ = 24 GHz | - 6 | 2 | --- | dBm |
| Reverse Leakage (output power appearing at input ports) | $P_{LEAKAGE}$ | Both RF outputs terminated (for Fin = 12.5 to 25 GHz). | --- | - 45 | - 43 | dBm |
| | | One RF output terminated | --- | - 40 | --- | dBm |
| Harmonics | $2F_{OUT}$<br>$3F_{OUT}$ | $P_{IN}$ = 0 dBm, $F_{IN}$ = 24 GHz | ---<br>--- | - 20<br>- 24 | ---<br>--- | dBc |
| Jitter rms | | $F_{IN}$ = 24 GHz | --- | 0.5 | --- | ps |
| Output Rise/Fall Time | $t_r/t_f$ | 20–80, $F_{IN}$ = 24 GHz | --- | 25 | --- | ps |
| SSB Phase Noise @ 100 kHz offset | Φ | $F_{IN}$ = 6 GHz<br>$F_{IN}$ = 18 GHz | --- | -150<br>-145 | --- | dBc/Hz |
| Spurious Output Power | | All input frequencies | --- | --- | none | dBc |

Notes:
[1] For sinewave input signal. Prescaler will operate down to DC with a square wave signal.
[2] For digital square was inputs, the minimum input amplitude should be 300 mVpp (differential or single-ended) over the frequency range of DC to 25 GHz. Note: the minimum slew rate needs to be 1V/ns.

# Typical Operating Characteristics

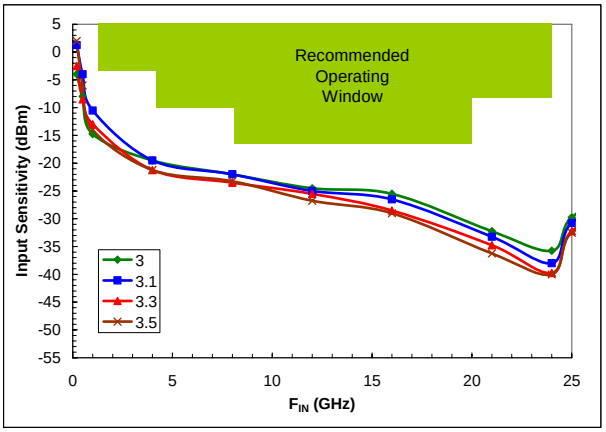



**Figure 1.** Input sensitivity vs. frequency, with parameter $V_{CC}$, T = -40 °C (die level data)

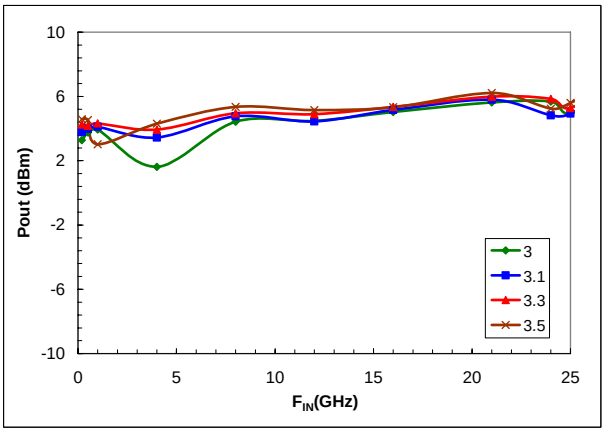



**Figure 2.** Output power vs. input frequency, with parameter $V_{CC}$, T = -40 °C (die level data)

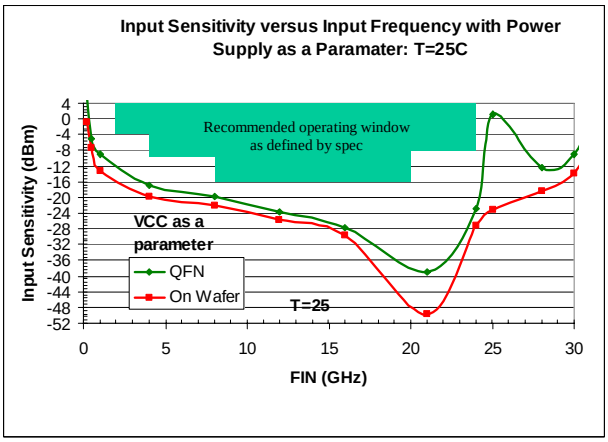



**Figure 3.** Input sensitivity vs. frequency, with parameter $V_{CC}$, T = 25 °C (QFN` level data)

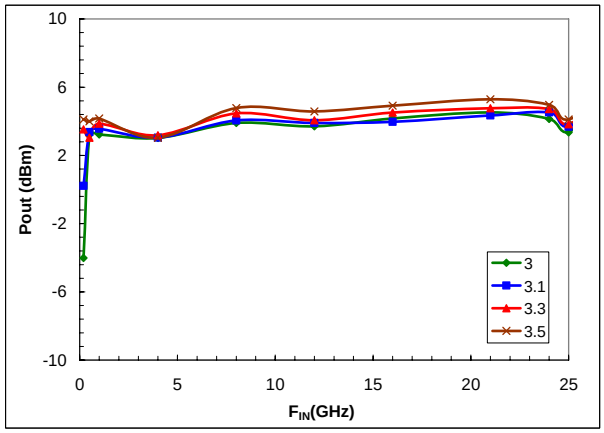



**Figure 4.** Output power vs. input frequency, with parameter $V_{CC}$, T = 25 °C (die level data)

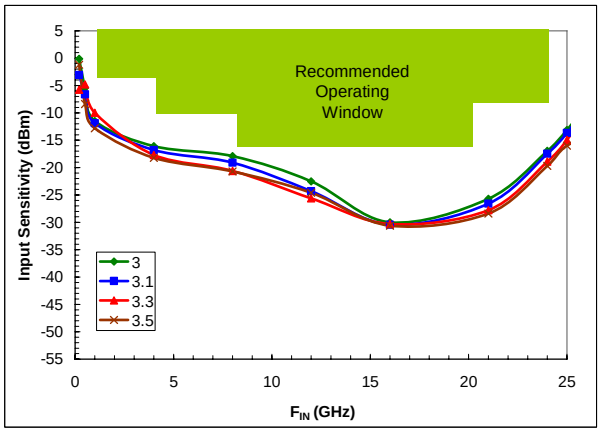



**Figure 5.** Input sensitivity vs. frequency,. With parameter $V_{CC}$, T = 85 °C (die level data)

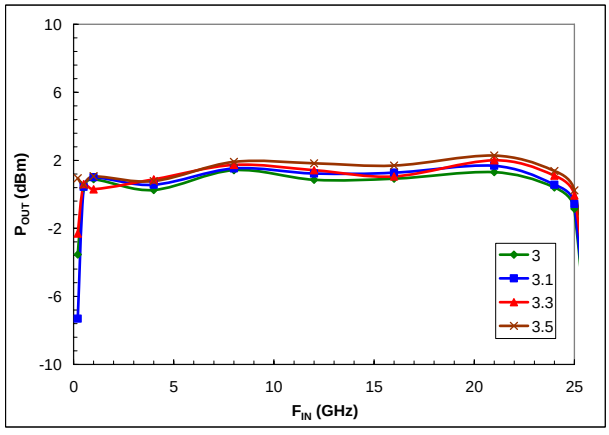



**Figure 6.** Output power vs. input frequency, with parameter $V_{CC}$, T = 85 °C (die level data)

## Typical Operating Characteristics (cont'd.)

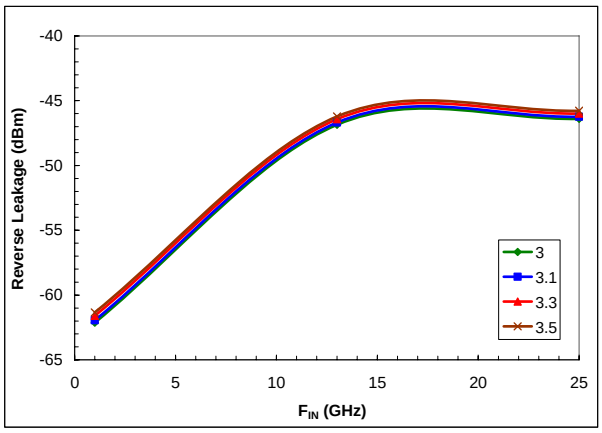



**Figure 7.** Reverse Leakage vs. frequency, with parameter $V_{CC}$, T = 25 °C (die level data)

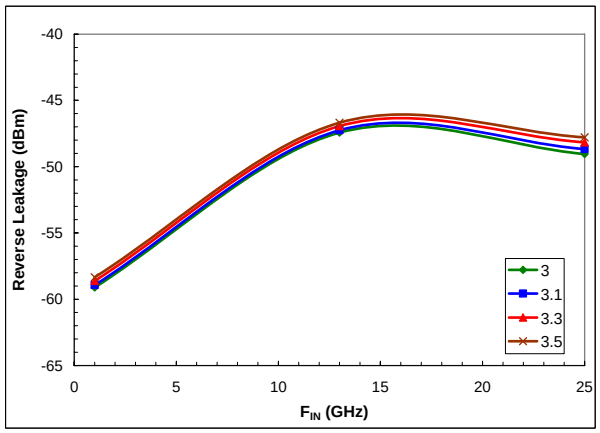



**Figure 8.** Reverse Leakage vs. frequency, with parameter $V_{CC}$, T = 85 °C (die level data)

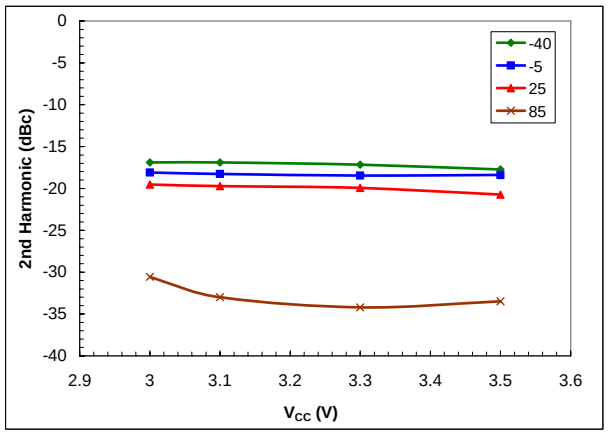



**Figure 9.** Harmonic content, 2nd Harmonic vs. Supply Voltage ($V_{CC}$), with temperature as a parameter, $P_{IN}$ = 0dBm and $F_{IN}$ = 25 GHz (die level data)

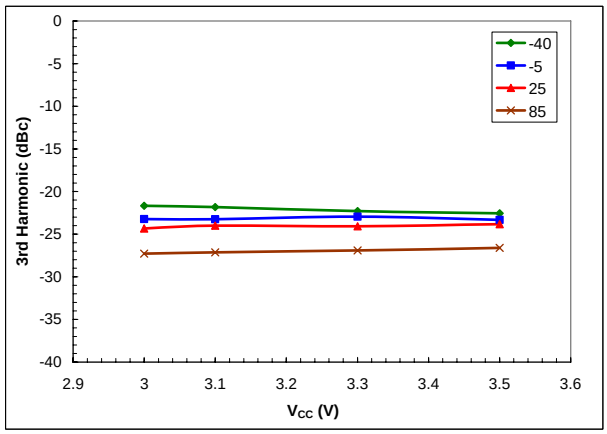



**Figure 10.** Harmonic content, 3rd Harmonic vs. Supply Voltage ($V_{CC}$), with temperature as a parameter, $P_{IN}$ = 0dBm and $F_{IN}$ = 25 GHz (die level data)

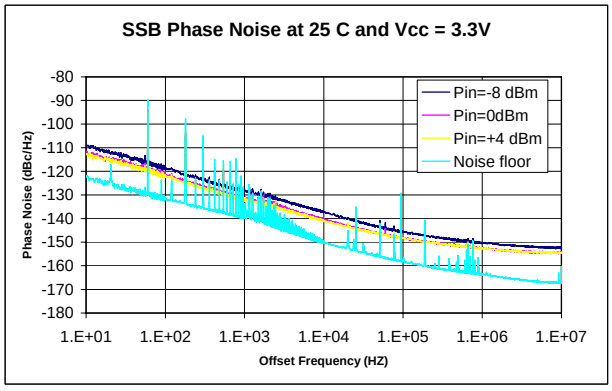



**Figure 11.** SSB phase noise, with $P_{IN}$ as a parameter, T = 25 °C and $V_{CC}$ = 3.3V (QFN level data)

### AC/DC Coupling and Termination

In a typical application, the RF inputs and outputs should be AC coupled via DC blocking capacitors mounted on a substrate or circuit board at each RF port. All unused RF outputs should be terminated with DC blocking capacitors and 50 Ω resistors to Vcc or ground for optimum performance. Unused RF output ports may be left open, but this configuration will result in additional power leakage from one RF port to the other.

All unused RF inputs should be terminated with DC blocking capacitors and 50 Ω resistors to Vcc or ground for optimum performance. Unused RF input ports may be left open, but this configuration will result in additional power leakage from one RF port to the other. The improvement from adding the 50 Ω terminations is small, and may not be noticeable in all cases. It may be possible to omit the termination if the part meets all the customer requirements without it.

In applications where the use of DC blocking capacitors is not desirable, the part may be directly DC coupled at the RF inputs and outputs. However, care must be taken to ascertain that the DC voltages at all RF input and output ports stay within the specified limits (see Absolute Maximum Ratings on page 2). All unused RF inputs and outputs should be terminated with 50 Ω resistors to Vcc (not ground) for optimum performance. Damage to the part may occur if the unused RF inputs and outputs are terminated directly to ground without the use of the DC blocking capacitors.

### Single-Ended Operation

The 25671DV-QFN is designed for either single-ended or differential operation. For single-ended operation, the unused RF input and output should be terminated in the manner described above.

### Input DC Offset

Under certain conditions, the 25671DV-QFN may self oscillate under no RF input power. This self-oscillation will produce an undesired output signal commonly referred to as "false trigger." To prevent false trigger, a small DC offset voltage between 20 and 100 mV may be applied between the RF input ports. Since the input has an internal 50 Ω resistor to $V_{CC}$ (nominally +3.3 V), adding a 10 KΩ resistor between the unused RF input to ground will result in an offset voltage of approximately 16.5 mV between the RF inputs and prevent the false trigger.

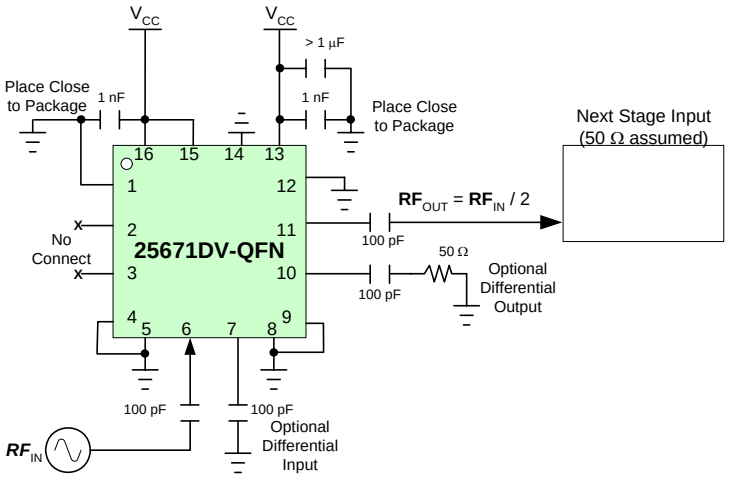
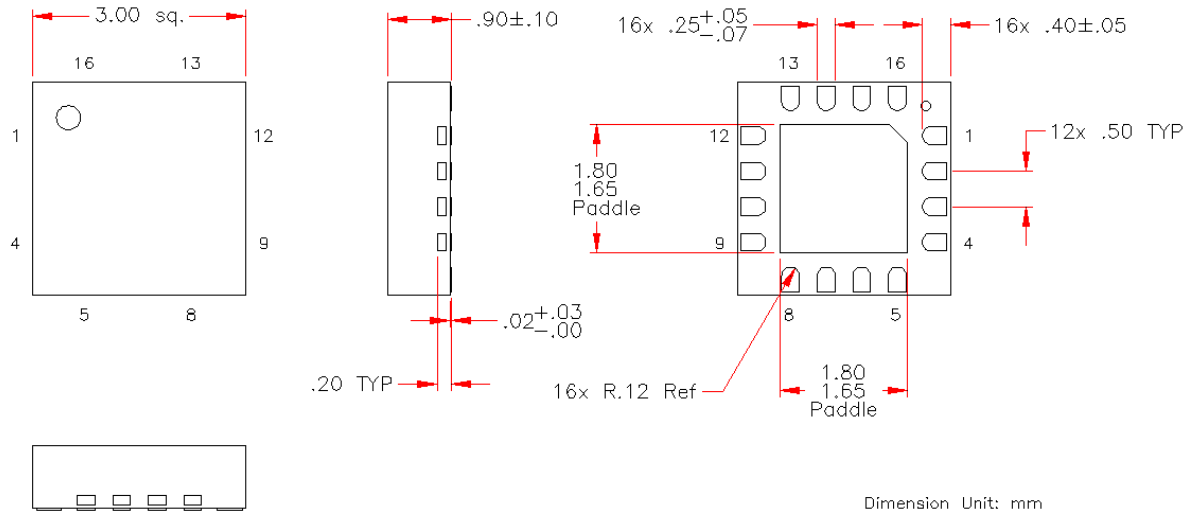



**Figure 12.** 25671DV-LGA suggested circuit configuration

# QFN Package Outline Drawing




| Name | Pin | Description | Function |
|---|---|---|---|
| RFINp | 6 | RF Input positive (non-inverting) | Input |
| RFINn | 7 | RF Input negative (inverting) | Input |
| RFOUTp | 11 | RF Output positive (non-inverting) | Output |
| RFOUTn | 10 | RF Output negative (inverting) | Output |
| GND | 1, 4, 5, 8, 9, 12, 14, Paddle | Ground | Supply |
| $V_{CC}$ | 13, 15, 16 | Power Supply: Connect to +3V to 3.5V Supply | Supply |
| NC | 2, 3 | Not Connected | NC |

**NOTE:** DC blocking capacitors are required at RF input and RF output ports for AC coupling.

## Order Information

| Part No. | Description |
|---|---|
| 25671DV-S03QFN | DC to 25 GHz Divide-by-2 Prescaler in Quad Flat No Lead Plastic Package |
| 25671DV-S03QFNEVB | DC to 25 GHz Divide-by-2 Prescaler in Quad Flat No Lead Plastic Package on an Evaluation Board with SMA Connectors |

## Related Products

| Part No. | Description |
|---|---|
| 25671DV-S03D | DC to 25 GHz Divide-by-2 Prescaler – Die |
| 25671DV-S03L | DC to 25 GHz Divide-by-2 Prescaler in LGA Ceramic Package |
| 25671DV-S03LEVB | DC to 25 GHz Divide-by-2 Prescaler in LGA Ceramic Package on an Evaluation Board with SMA Connectors |

## Contact Information

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## Qualification Notification

The 25671DV is fully qualified. Please contact Inphi for the qualification report.

**Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.**

## Radiation Tolerance

Inphi's High Speed Logic has been found to be radiation tolerant. Please contact Inphi for more details.

# Version Updates

**From Version 1.4 to Version 2.0 (dated 12/16/05):**

1. Changed Part number from 25671DV-S02 to 25671DV-S03 throughout datasheet.
2. Changes in "Features" section: Power supply current changed from 64 mA to 76 mA typical (page 1).
3. Changes to Block Diagram: removed the approximate symbols (~) from the output termination resistors.
4. Added the three comments on Absolute Maximum Ratings (at top of table on page 2.)
5. Changes to Operating Specifications (page 2):
    a. Power Supply Voltage maximum spec. = +3.5V.
    b. Power Supply Current spec.: typical = 76 mA, maximum = 98 mA.
6. Changes to Electrical Specification (page 3):
    a. Added Input Return Loss specifications.
    b. Added Output Return Loss specifications.
    c. Output Power specs: typical = -45 dBm, maximum = -43 dBm.
    d. Added Spurious Output Power spec. maximum = none.
7. Replaced figures 3, 4 and 8 in the Typical Operating Characteristics section (pages 4 & 5).
8. Changed Qualification Notification section to Limited Qualification Notification and changed statement from fully qualified (25671DV-S02) to not yet fully qualified (page 8).

**From Version 2.0 to 2.1 (dated 2007-04-10)**

1. Corrected typ reading for low supply current in the Features Section from 64 mA to 76 mA (page 1)
2. Updated Electrical Specifications Table (page 3):
    a. For Reverse Leakage condition, added note: "(for $F_{IN}$ = 12.5 to 25 GHz)" when both RF outputs are terminated.
    b. Added footnote #2, for Input Power Range ($P_{IN}$), the minimum input amplitude and slew rate needed for digital square wave inputs.
3. Updated Typical Operating Characteristics (pages 4 – 5)
    a. Updated figures 1 – 11 for input sensitivity, output power, reverse leakage, harmonic content and phase noise.
    b. Added note in figure captions that figures are die level data or QFN level data, as applicable.
4. Updated Application Notes to add information about optional 50Ω resistors on unused RF inputs. (page 6)
5. Added caption for Figure 12, suggested circuit configuration (page 6)
6. Updated table for the QFN Package Outline Drawing (page 7):
    a. Added "non-inverting" for the positive RF input and RF output
    b. Added "inverting" for the negative RF input and output.
    c. Provided separate rows in the table for each RF input and RF output.
    d. Corrected Power Supply voltage ($V_{CC}$) description from 3.4 V to 3.5 V
7. Updated Qualification Notification to indicate that this product is fully qualified. (page 8)
8. Added Radiation Tolerance Section (page 8)