

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LS273

## Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

REJ03D0473-0300  
Rev.3.00  
Jul.15.2005

The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

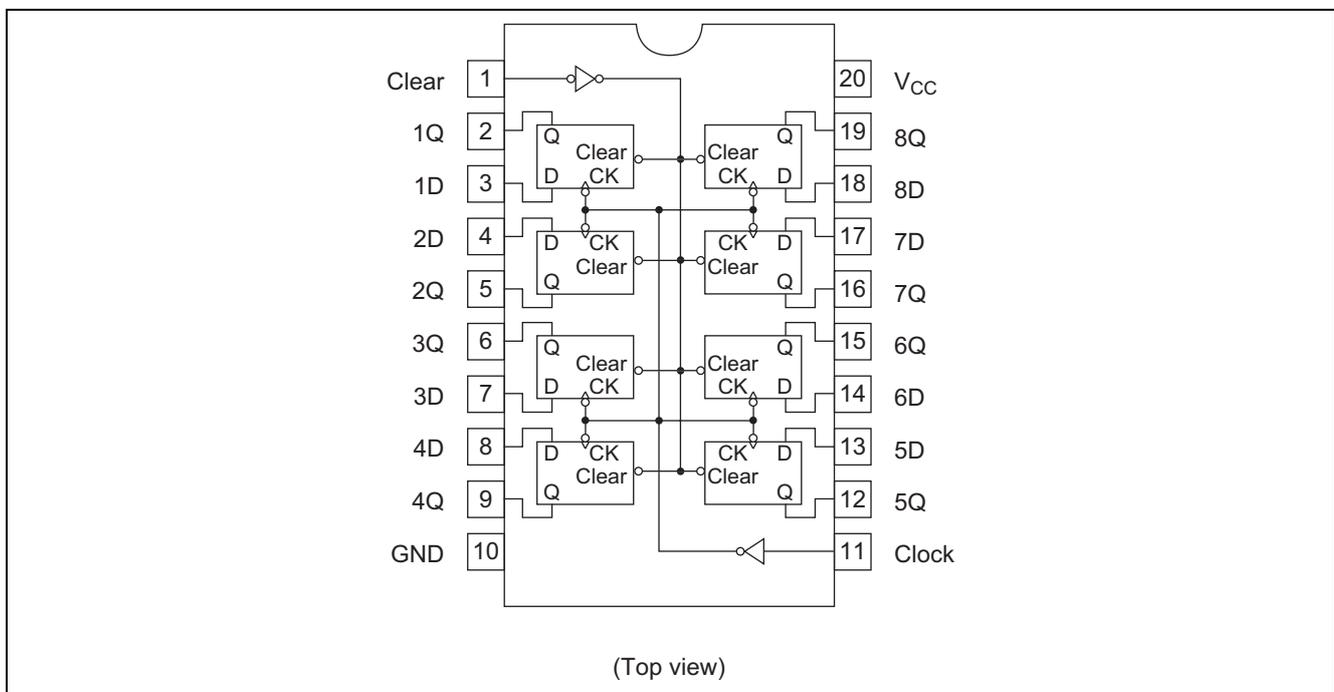
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS273P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS273FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS273RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement

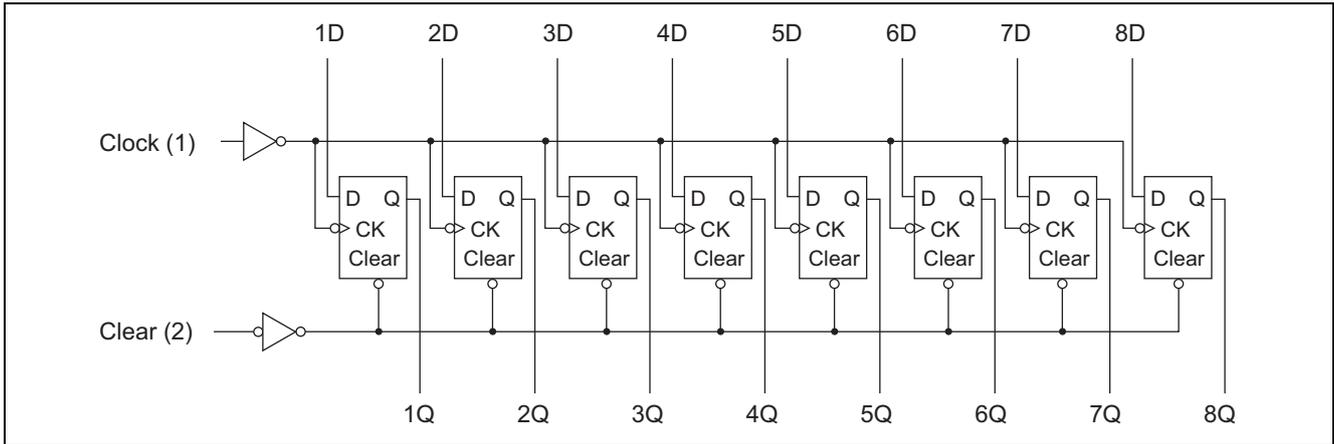


**Function Table**

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

Notes: H; high level, L; low level, X; irrelevant  
 ↑; transition from low to high level  
 Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established.

**Block Diagram**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output current	I <sub>OH</sub>	—	—	-400	μA
	I <sub>OL</sub>	—	—	8	mA
Operating temperature	Topr	-20	25	75	°C
Clock frequency	f <sub>clock</sub>	0	—	30	MHz
Clock pulse width	t <sub>w (clock)</sub>	20	—	—	ns
Clear pulse width	t <sub>w (clear)</sub>	20	—	—	ns
Data setup time	t <sub>su (data)</sub>	20↑	—	—	ns
Clear (inactive-state) setup time	t <sub>su (clear)</sub>	25↑	—	—	ns
Data hold time	t <sub>h (data)</sub>	5↑	—	—	ns

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
	V <sub>OL</sub>	—	—	0.5	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—		—	0.4			
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current	I <sub>CC</sub> **	—	17	27	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

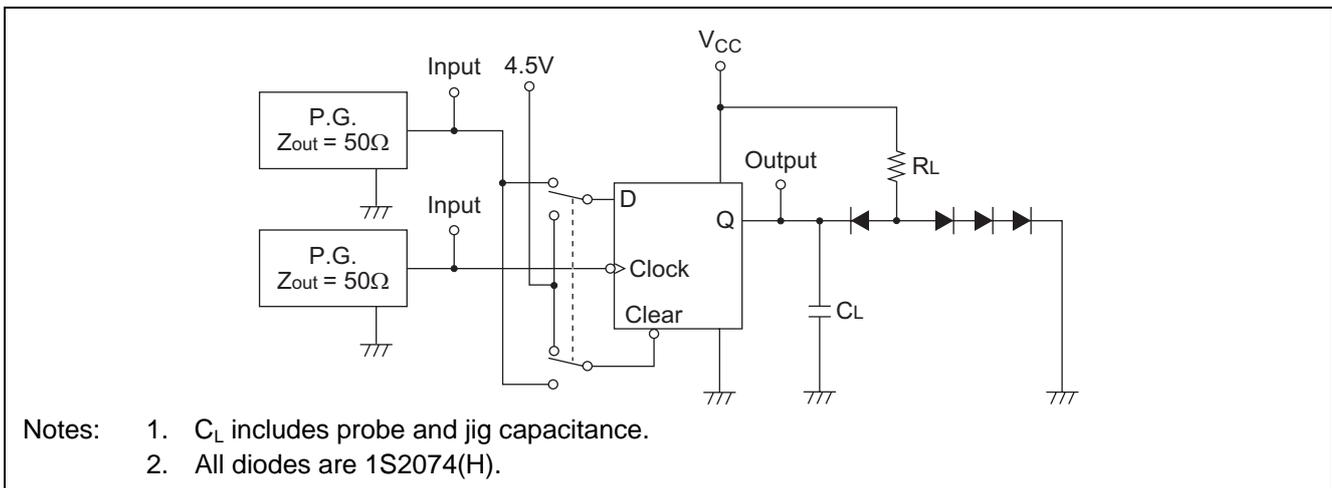
 Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C

 \*\* With all outputs open and 4.5 V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V is applied to clock.

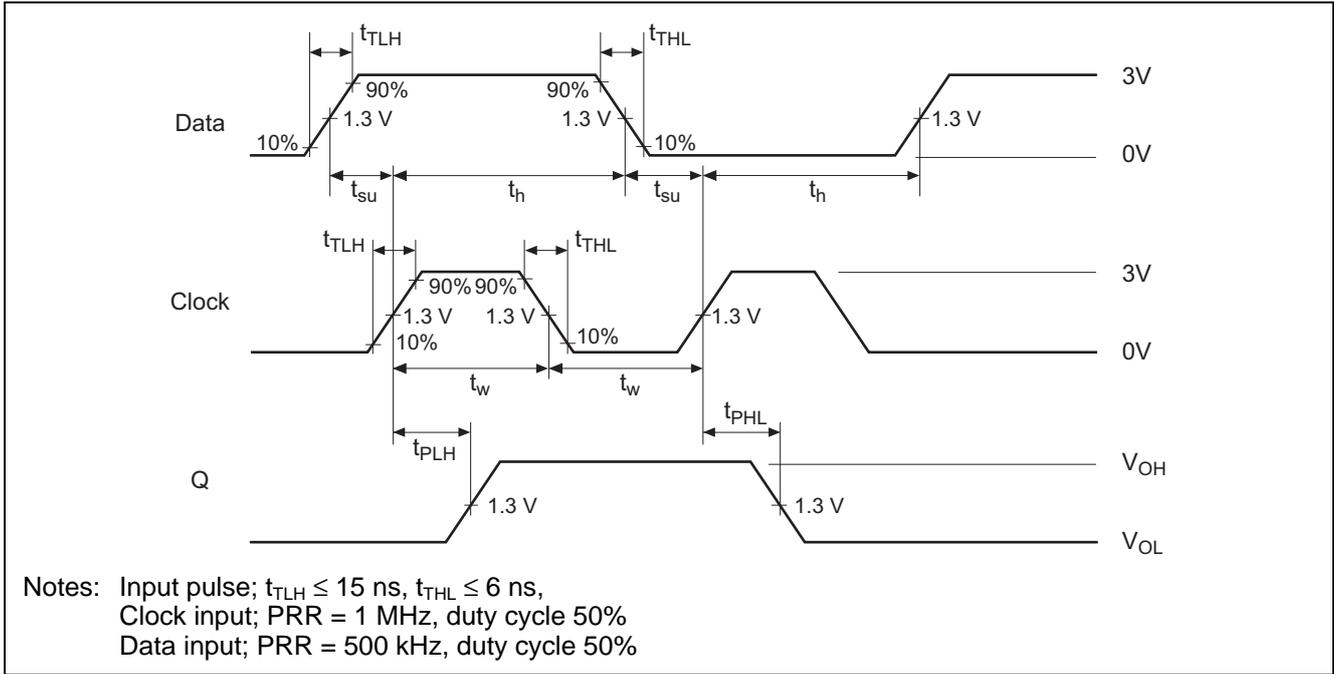
**Switching Characteristics**

 (V<sub>CC</sub> = 5 V, Ta = 25°C)

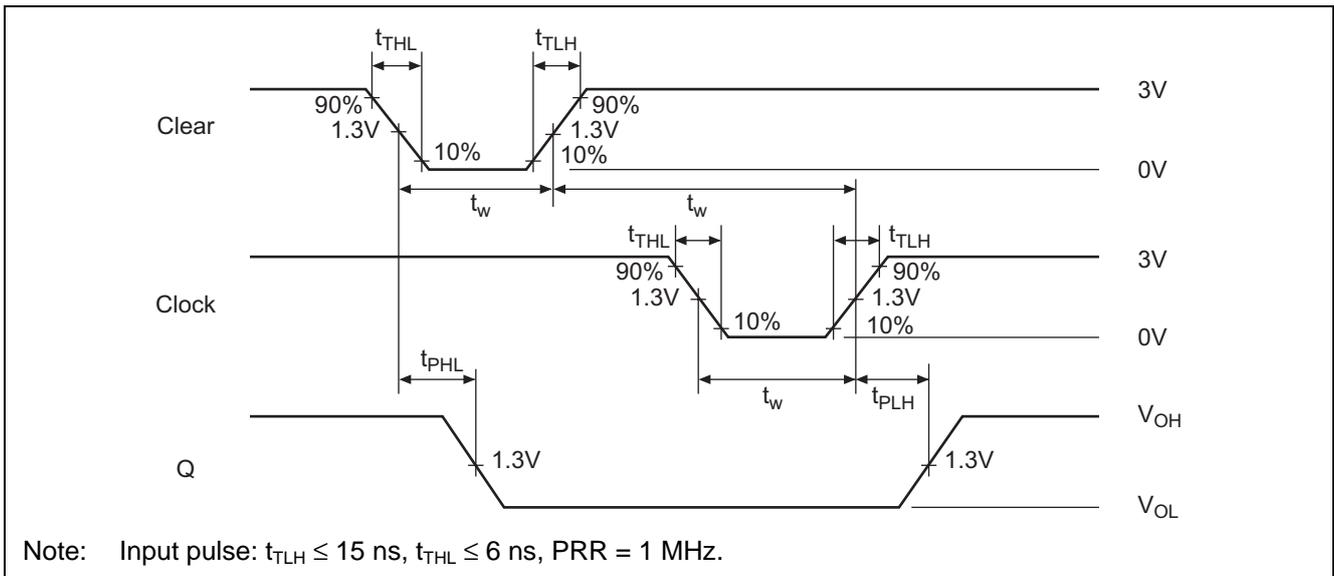
Item	Symbol	Inputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>	Clock	30	40	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
Propagation delay time	t <sub>PHL</sub>	Clear	—	18	27	ns	
	t <sub>PLH</sub>	Clock	—	17	27		
	t <sub>PHL</sub>			—	18	27	

**Testing Method**
**Test Circuit**


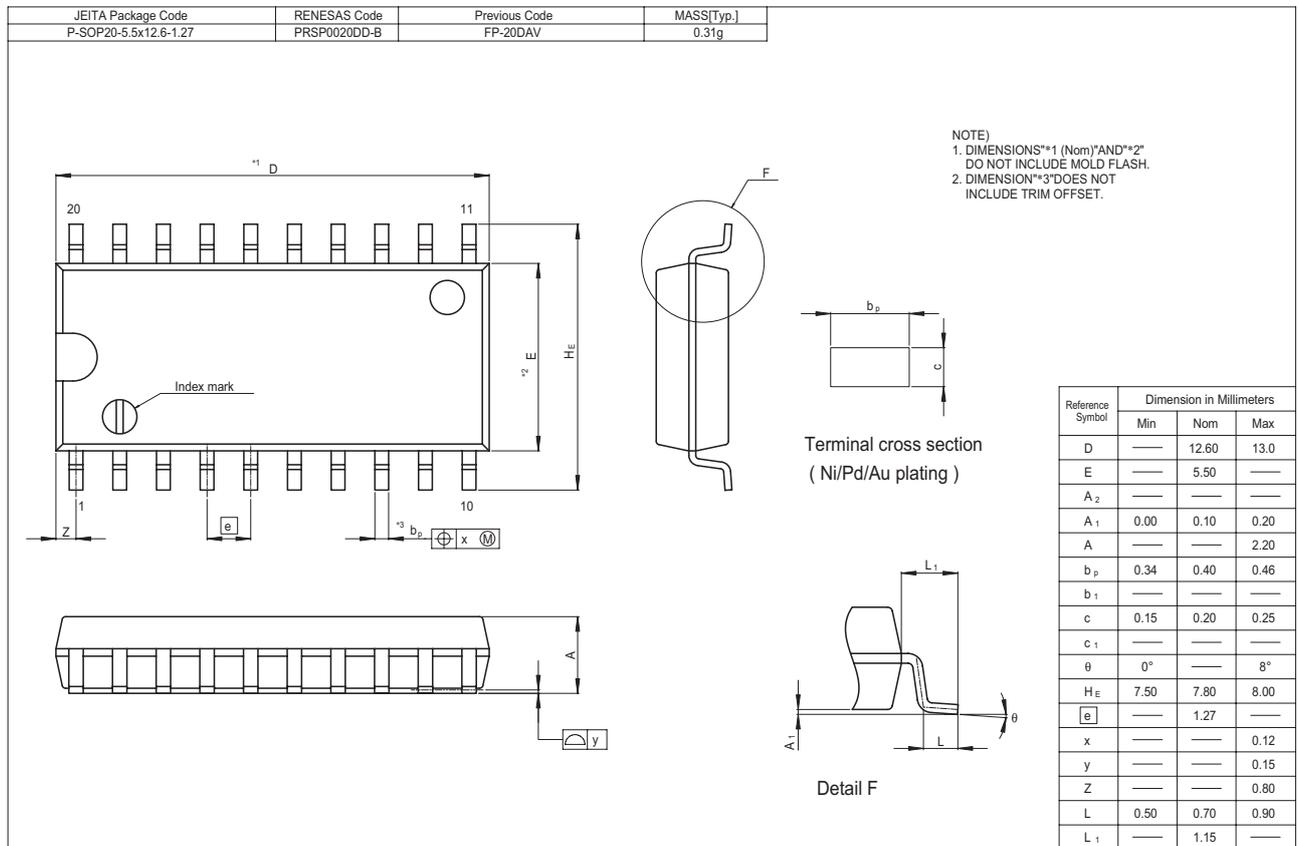
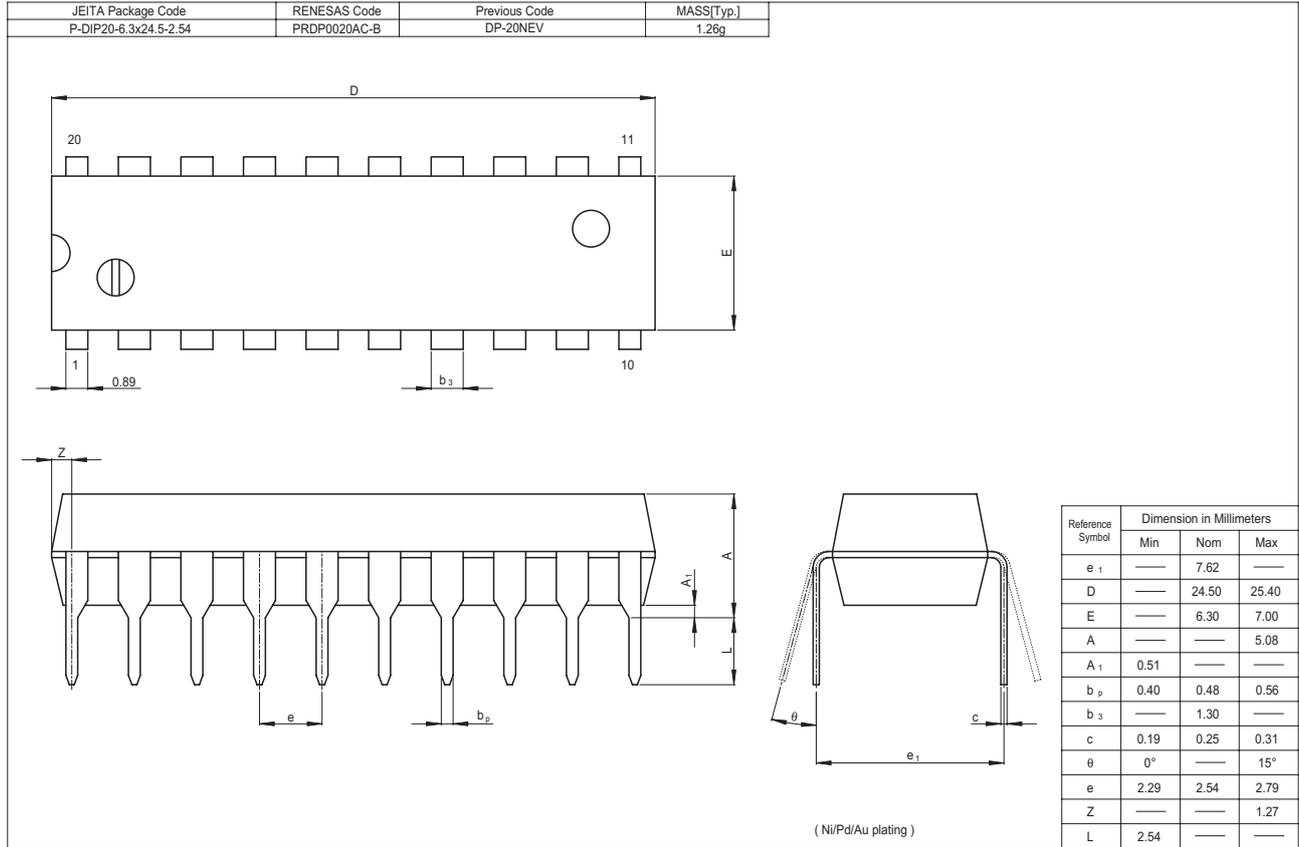
**Waveforms 1**



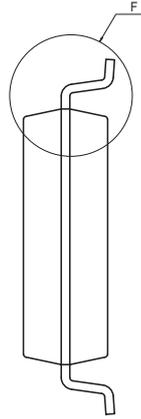
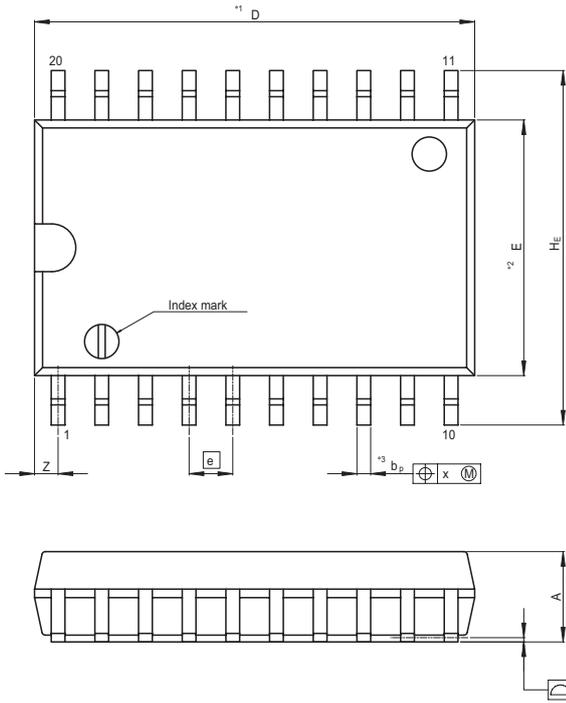
**Waveforms 2**



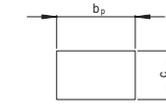
Package Dimensions



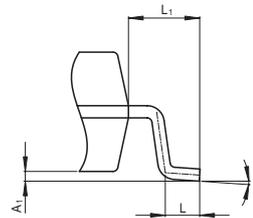
JEITA Package Code P-SOP20-7.5x12.8-1.27	RENESAS Code PRSP0020DC-A	Previous Code FP-20DBV	MASS[Typ.] 0.52g
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NOTE)  
1. DIMENSIONS<sup>\*\*1</sup> (Nom)<sup>\*\*AND<sup>\*\*2</sup></sup>  
@ DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION<sup>\*\*3</sup> DOES NOT  
@ INCLUDE TRIM OFFSET.



Terminal cross section  
( Ni/Pd/Au plating )



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.80	13.2
E	—	7.50	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.20	0.30
A	—	—	2.65
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.20	0.25	0.30
c <sub>1</sub>	—	—	—
$\theta$	0°	—	8°
H <sub>E</sub>	10.00	10.40	10.65
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.935
L	0.40	0.70	1.27
L <sub>1</sub>	—	1.45	—

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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

#### Renesas Technology Europe Limited

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Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

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Tel: <852> 2265-6688, Fax: <852> 2730-6071

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10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
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Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

#### Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510

