

LOW POWER STEP DOWN CONVERTERS

PRELIMINARY INFORMATION - JUL 2, 2012



Features

- ▶ Wide input voltage range 4.5V to 40V
- ▶ PFM regulator up to 1.33MHz
- ▶ Up to >92% efficiency
- ▶ Very low 8μA sleep mode current
- ▶ Ultra low 12μA standby current
- ▶ 100% duty cycle capability
- ▶ SOIC8-EP package
- ▶ Ambient temperature range up to +105°C

Applications

- ▶ Industry
- ▶ Consumer

General Description

The E522.71/72/73/74/75/76/77/78/79 product family provides ultra low quiescent current step down DC/DC converters with integrated power MOSFET.

The PFM (Pulse Frequency Modulation) regulator allows outstanding fast line- and load response time, stability and high efficiency over the full load current range. The integrated idle detection assures an ultra low idle current and high efficiency with low load currents down to <100μA for the completely powered application. A power-good signal is provided by a high-voltage open-drain low-side switch.

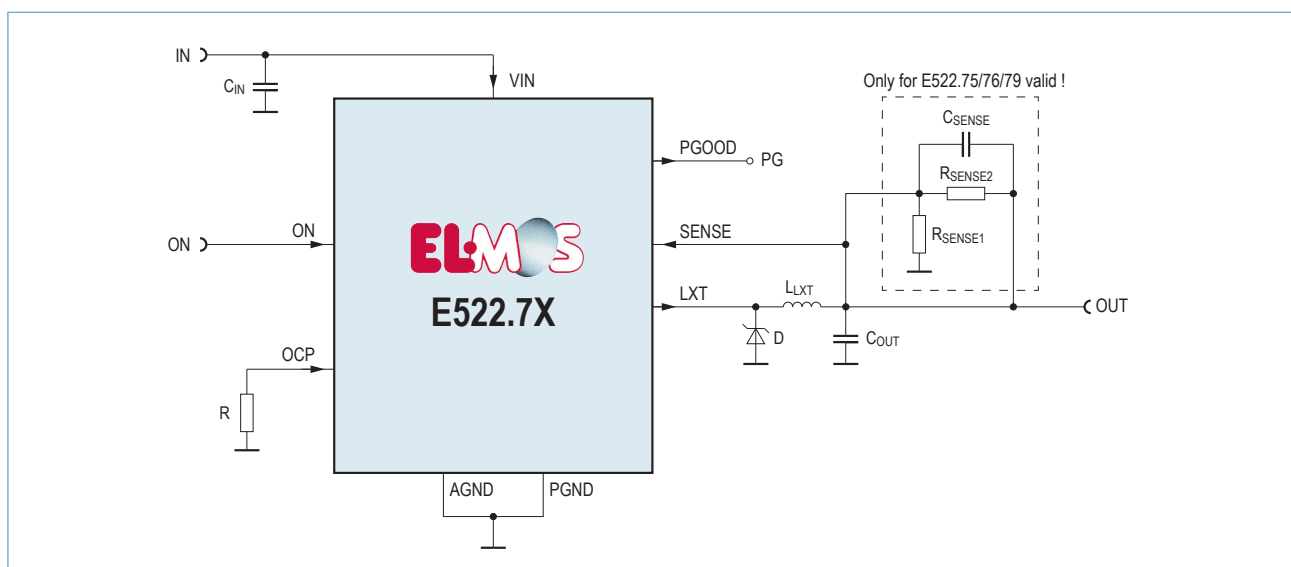
The E522.7x buck converter accommodates to common single supply micro controller applications. Low external component count and small exposed die pad SOIC 8-EP package allow compact PCB designs.

Ordering Information

Product ID	V _{OUT}	I _{OUT}	Ambient Temp. Range
E522.71	5V	500mA	-40°C to +105°C
E522.72	3.3V	500mA	-40°C to +105°C
E522.73	5V	350mA	-40°C to +105°C
E522.74	3.3V	350mA	-40°C to +105°C
E522.75	1.5 to 40V	500mA	-40°C to +105°C

Product ID	V _{OUT}	I _{OUT}	Ambient Temp. Range
E522.76	1.5 to 40V	350mA	-40°C to +105°C
E522.77	5V	1A	-40°C to +105°C
E522.78	3.3V	1A	-40°C to +105°C
E522.79	1.5 to 40V	1A	-40°C to +105°C

Ordering information continued at the end of this document.



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1 Functional Diagram

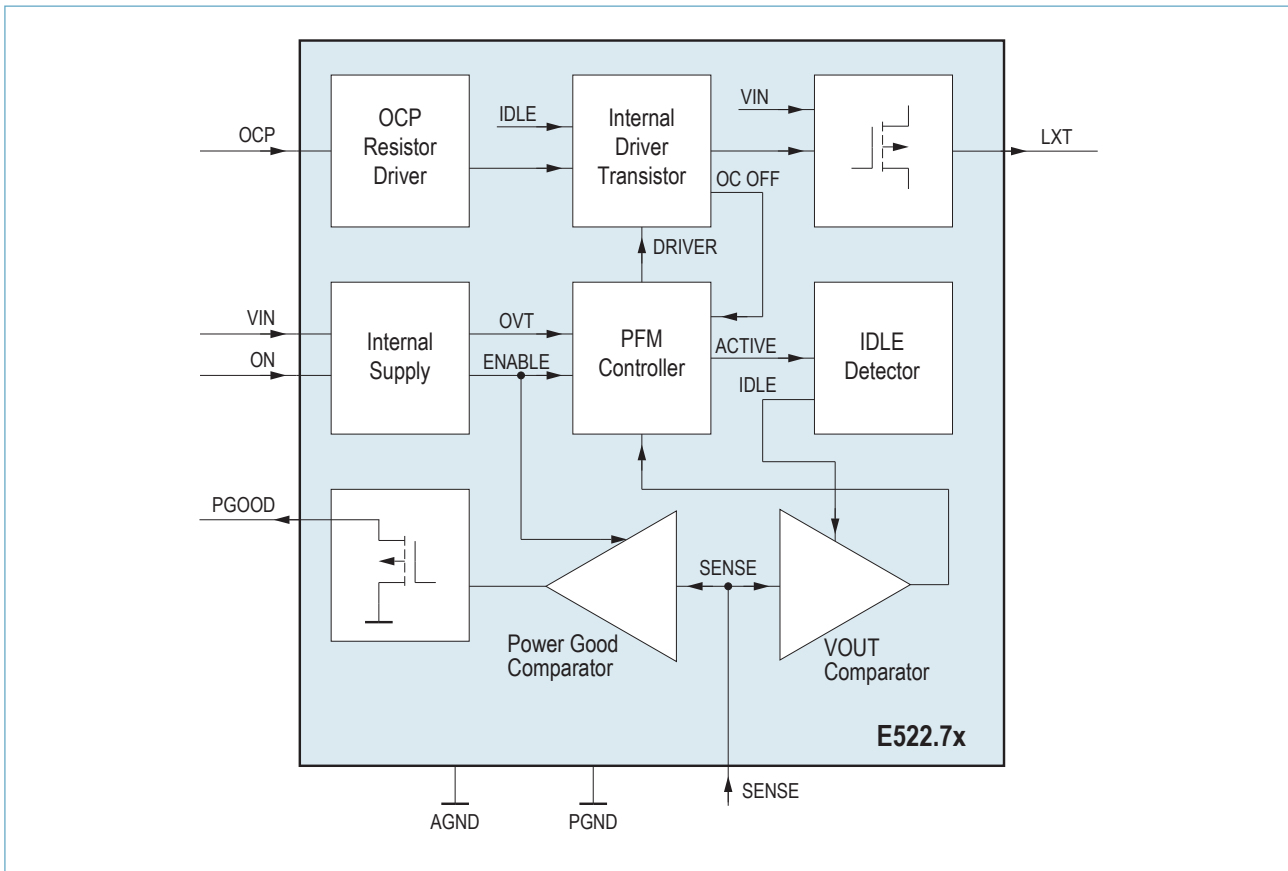


Figure 1: Block diagram

2 Pinout

2.1 Pin Configuration SOIC8-EP

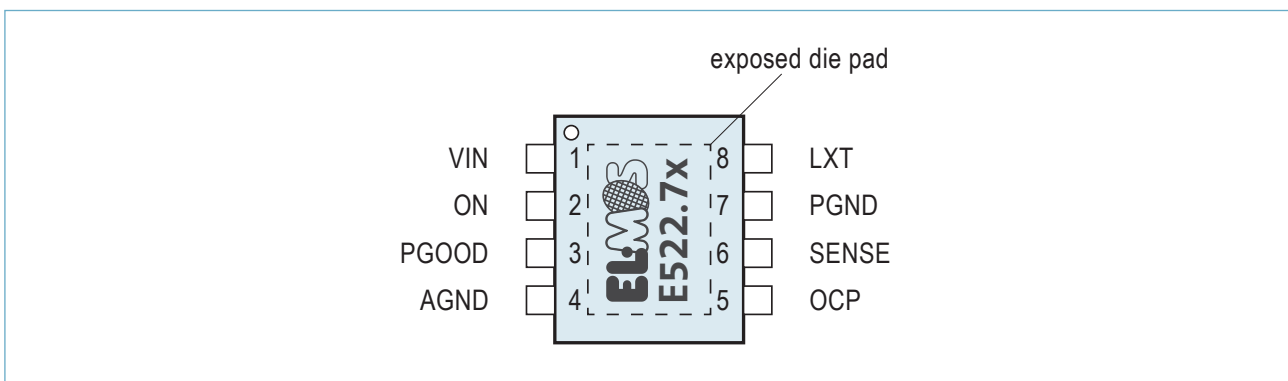


Figure 2: Package pinout, transparent top view, not to scale.

2.2 Pin Description

Table 1: Pin Description

Pin	Name	Type ¹⁾	Description	Remark
1	VIN	HV S	High-Voltage Supply input	bypass to GND with a low ESR capacitance >20μF
2	ON	HV AI	High-Voltage input to enable converter	
3	PGOOD	HV AO	High-Voltage capable low-side open-drain output for power good flag	
4	AGND	S	Signal ground connection	
5	OCP	AI	Over-current protection resistor input, connect to ground via resistor	
6	SENSE	AI	Feedback input for converter regulation, connect to output voltage	Redundant, connect both SENSE pins
7	PGND	S	Power ground connection	Open or GND
8	LXT	HV AO	Integrated high-side switch output, connect free-wheeling diode and inductor to this pin	

1) D = Digital, A = Analog, S = Supply, HV = High voltage (see max. ratings), I = Input, O = Output

Note: Pins with identical names have to be connected.

3 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to V_{GND} . Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Condition	Symbol	Min	Max	Unit
Supply voltage at pin VIN		V_{VIN}	-0.3	40	V
Voltage at pin ON		V_{ON}	-0.3	40	V
Voltage at pin PGOOD		V_{PGOOD}	-0.3	40	V
Current at pin PGOOD		I_{PGOOD}	0	5	mA
Voltage at pin SENSE		V_{SENSE}	-0.3	6	V
Voltage at pin OCP		V_{OCP}	-0.3	0.8	V
Voltage at pin LXT		V_{LXT}	-10	$V_{IN} + 0.3$	V
Storage / Junction temperature		T_{STG}	-50	+150	°C

4 ESD Protection

Description	Condition	Symbol	Min	Max	Unit
ESD HBM protection at pin VIN		$V_{ESD(HBM)}$	3		kV
ESD HBM protection at all other pins		$V_{ESD(HBM)}$	2		kV
ESD CDM protection at all pins		$V_{ESD(CDM)}$	500		V
ESD CDM protection at corner pins		$V_{ESD(CDM)C}$	750		V

5 Recommended Operating Conditions

Description	Condition	Symbol	Min	Max	Unit
Junction temperature		T_J	-40	+150	°C
Ambient temperature		T_{amb}	-40	+105 ²⁾	°C
Supply voltage at pin VIN		V_{VIN}	4.5 ¹⁾	40	V

1) For $V_{VIN} < V_{OUT}$, E522.7x enters 100% duty cycle mode

5.1 Package Thermal Resistance

Description	Condition	Symbol	Typ.	Unit
Junction - Ambient	Exposed die pad thermally connected to pcb ²⁾	RTHJA1	45	K/W
Junction - Ambient	Exposed die pad not thermally connected to pcb	RTHJA2	110	K/W
Junction – Exposed die pad		RTHJC	10	K/W

2) "Calculated from package in still air, mounted to 3" x 4.5" FR4 pcb with thermal vias under exposed pad per JESD51 standards"

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6 Electrical Characteristics

($V_{VIN} = 4.5V$ to $40V$, $T_{amb} = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $V_{VIN} = 14V$ and $T_{amb} = +25^{\circ}C$. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply						
Sleep mode quiescent current	$V_{ON} = 0$; non-switching	$I_{VIN,q,SLP}$		8		μA
Active mode quiescent current	$V_{ON} = V_{VIN} > 8V$; $I_{OUT} < 100\mu A$	$I_{VIN,q}$		12		μA
Active mode quiescent current	$V_{ON} = V_{VIN}$ L_{XT} driver OFF	$I_{VIN,q}$		150		μA
Input resistance at pin ON	$V_{ON} = V_{VIN} = 14V$	I_{ON}		7		$M\Omega$
Threshold voltage at pin ON	$V_{VIN} > 4.5V$	$V_{ON,th}$	1.40	1.48	1.56	V
Output Current Limit Programming						
Output voltage at OCP	$24k\Omega \leq R_{OCP} \leq 60k\Omega$	V_{OCP}		500		mV
OCP Selection Resistor		R_{OCP}	24		60	$k\Omega$
Load capacitance at OCP		C_{OCP}			100	pF
E522.71 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 500mA$ $V_{VIN} = 14V$	V_{OUT}	4.8	5.0	5.2	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.7	1.5	Ω
Over-current detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	740	830	930	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	300	350	410	mA
E522.72 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 500mA$ $V_{VIN} = 14V$	V_{OUT}	3.2	3.33	3.46	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.7	1.5	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	740	830	930	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	300	350	410	mA
E522.73 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 350mA$ $V_{VIN} = 14V$	V_{OUT}	4.8	5.0	5.2	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		1.1	2.5	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	490	550	620	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	190	230	280	mA
E522.74 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 350mA$ $V_{VIN} = 14V$	V_{OUT}	3.2	3.33	3.46	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		1.1	2.5	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	490	550	620	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	190	230	280	mA

1) Given value is switching threshold at pin SENSE, for $V_{VIN} < V_{OUT}$ regulator provides 100% conductance mode

2) Measured at $V_{VIN} = 14V$

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Electrical Characteristics (continued)

($V_{VIN} = 4.5V$ to $40V$, $T_{amb} = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $V_{VIN} = 14V$ and $T_{amb} = +25^{\circ}C$. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
E522.75 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 500mA$ $V_{VIN} = 14V$	V_{SENSE}	1.416	1.475	1.534	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.7	1.5	Ω
Over-current detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	740	830	930	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	300	350	410	mA
E522.76 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 350mA$ $V_{VIN} = 14V$	V_{SENSE}	1.416	1.475	1.534	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		1.1	2.5	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	490	550	620	mA
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	190	230	280	mA
E522.77 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 1A$ $V_{VIN} = 14V$	V_{OUT}	4.8	5.00	5.2	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.44	0.75	Ω
Over-current detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	1.3	1.45	1.61	A
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	0.5	0.6	0.71	A
E522.78 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 1A$ $V_{VIN} = 14V$	V_{OUT}	3.2	3.33	3.46	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.44	0.75	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	1.3	1.45	1.61	A
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	0.5	0.6	0.71	A
E522.79 Output						
Output regulation threshold ¹⁾	$I_{OUT} = 1A$ $V_{VIN} = 14V$	V_{SENSE}	1.416	1.475	1.534	V
On Resistance at LXT	$V_{VIN} = 14V$	$R_{DS(ON)}$		0.44	0.75	Ω
Overcurrent detection	$R_{OCP} = 24k\Omega$ ²⁾	$I_{OCP,24k\Omega}$	1.3	1.45	1.61	A
	$R_{OCP} = 60k\Omega$ ²⁾	$I_{OCP,60k\Omega}$	0.5	0.6	0.71	A

1) Given value is switching threshold at pin SENSE, for $V_{VIN} < V_{SENSE}$ regulator provides 100% conductance mode

2) Measured at $V_{VIN} = 14V$

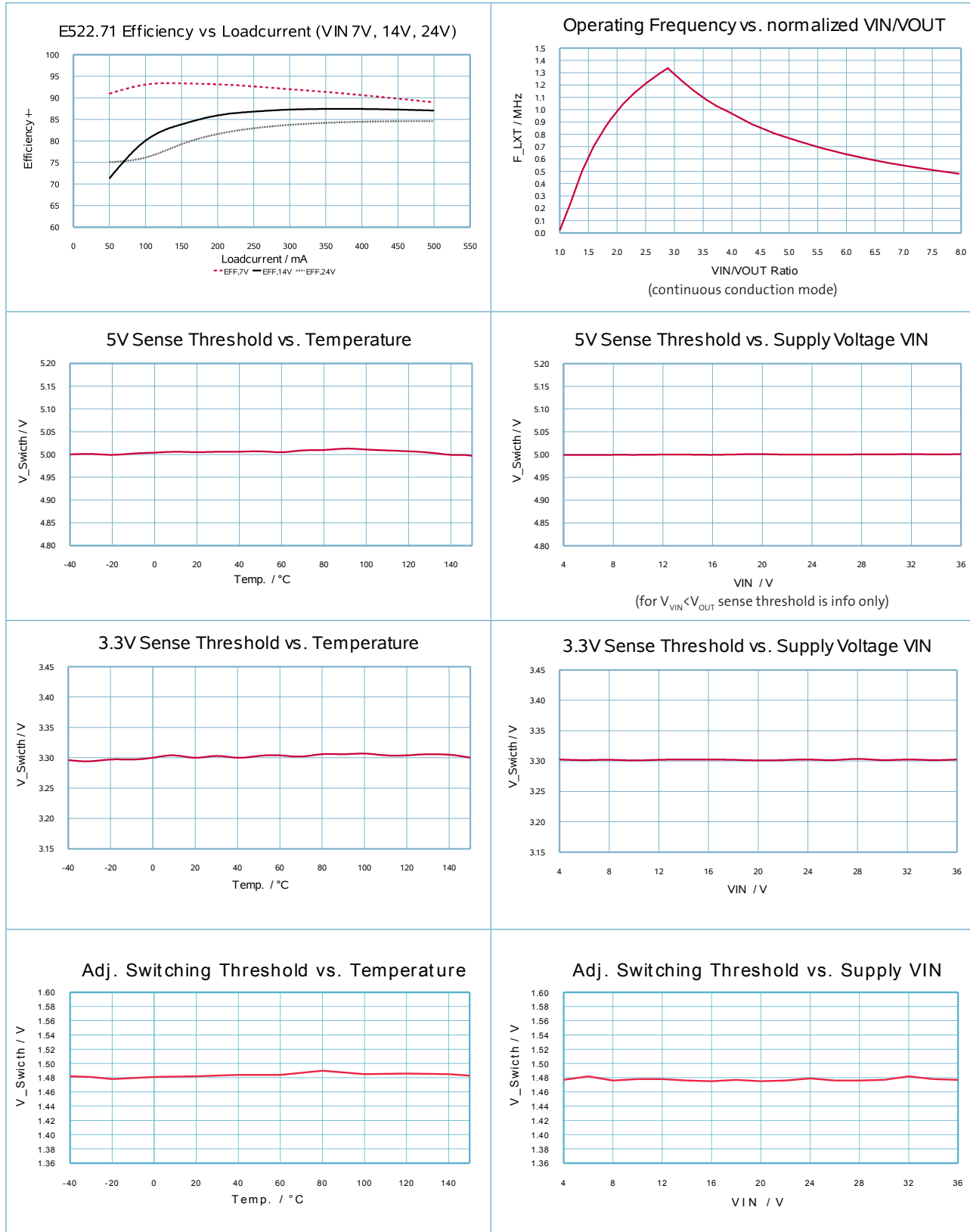
Electrical Characteristics (continued)

($V_{VIN} = 4.5V$ to $40V$, $T_{amb} = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $V_{VIN} = 14V$ and $T_{amb} = +25^{\circ}C$. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Switching						
Switching frequency		f_s	0		1.75	MHz
Minimum LXT on time	$I_{OUT} < I_{OCP}$	$t_{LXT}(ON)$		260		ns
	$I_{OUT} \geq I_{OCP}$	$t_{LXT}(ON)$		100		ns
Minimum LXT off time	PGOOD = '1'	$t_{LXT}(OFF)$		520		ns
	$I_{OUT} \geq I_{OCP}$, $V_{SENSE} > 1.2V$	$t_{LXT}(OFF)$		1330		ns
	$I_{OUT} \geq I_{OCP}$, $V_{SENSE} < 1.0V$	$t_{LXT}(OFF)$		2450		ns
Power Good Detector						
Power good detection threshold, rising edge		$V_{SENSE,th(LH)}/V_{OUT(NOM)}$		92.5		%
Power good detection threshold, falling edge		$V_{SENSE,th(HL)}/V_{OUT(NOM)}$		90		%
Output voltage at pin PGOOD	$V_{SENSE} < V_{SENSE,th(HL)}$ $I_{PGOOD} = 2mA$	V_{PGOOD}		0.2	0.4	V
Leakage at pin PGOOD	$V_{SENSE} = V_{OUT,NOM}$ $V_{PGOOD} = 5V$	$I_{PGOOD,lk}$			3	μA
IDLE Detector						
IDLE detection delay	no switching	T_{IDLE}	70	110	150	μs
Average LXT duty cycle for IDLE	Discontinuous operation	D_{IDLE}		1.38		%
Wake-up threshold during IDLE	relative to nominal V_{OUT} in %	$V_{SENSE,WU}$		95		%
Wake-up delay after IDLE	$V_{SENSE} < V_{SENSE,WU}$	$T_{DEL,ACTIVE}$		10	25	μs

7 Typical Operating Characteristics

Diagrams showing typical characteristics at $V_{VIN}=14V$ and $T_{AMB}=25^{\circ}$, unless otherwise noted

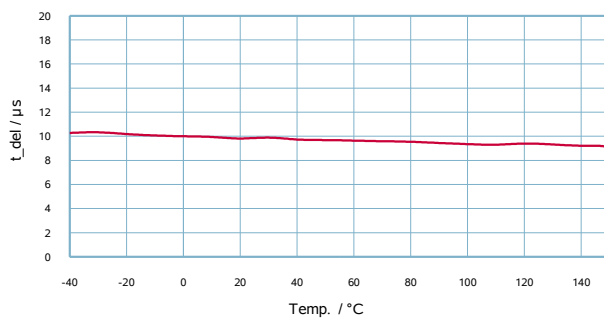


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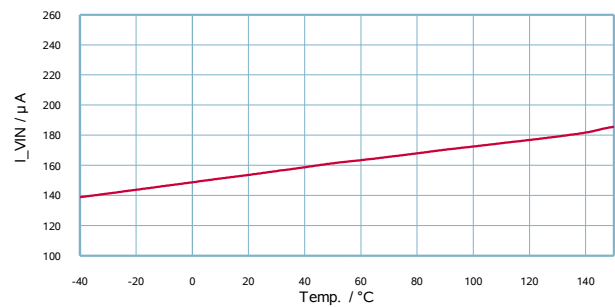
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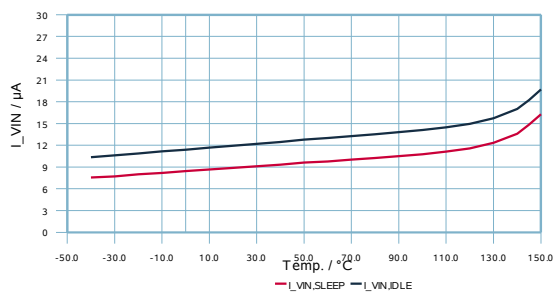
Re-Enable Delay vs. Temperature (Idle-to-Active)



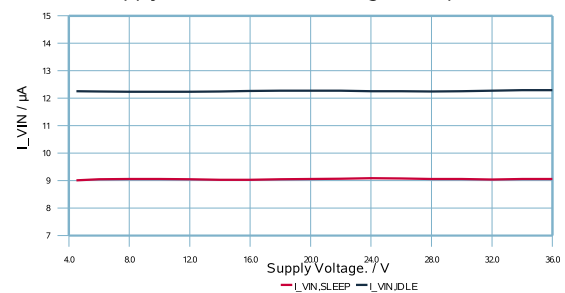
Supply Current vs. Temperature (Active Mode)



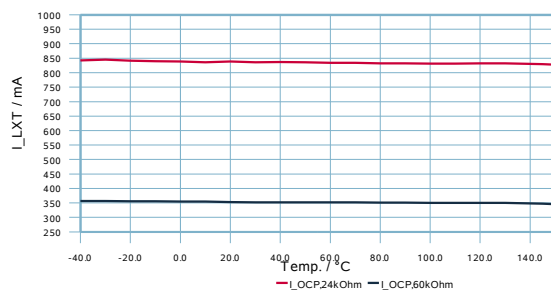
Supply Current vs. Temperature (Sleep & Idle Mode)



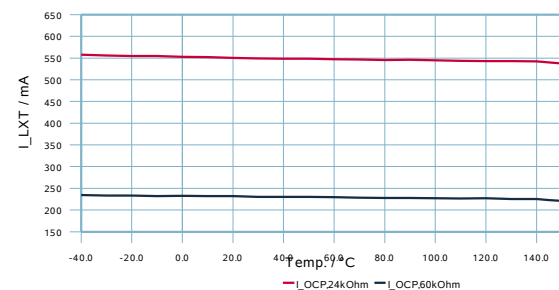
Supply Current vs. VIN Voltage (Sleep & Idle Mode)



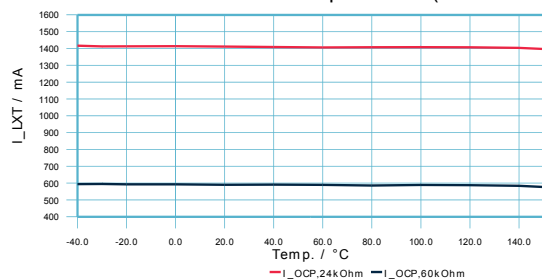
Current Limitation vs. Temperature (500mA Device)



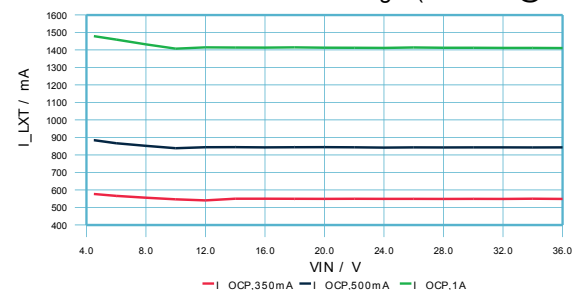
Current Limitation vs. Temperature (350mA Device)



Current Limitation vs. Temperature (1A Device)

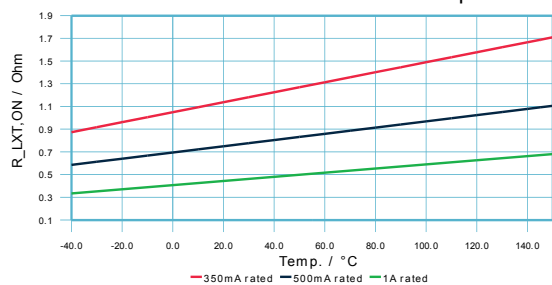


Current Limitation vs. VIN Voltage (24kOhm@OCP)

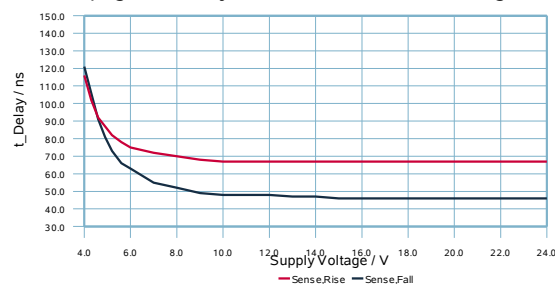


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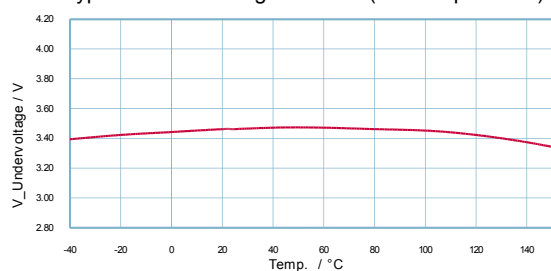
Internal FET On-Resistance vs. Temperature



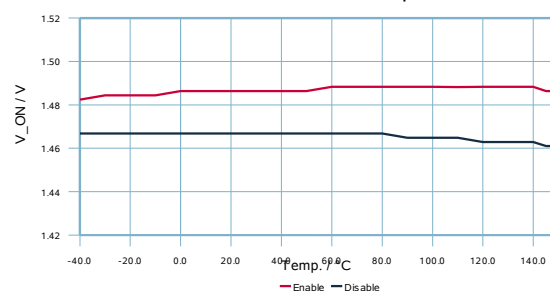
Propagation Delay Sense to LXT vs VIN Voltage



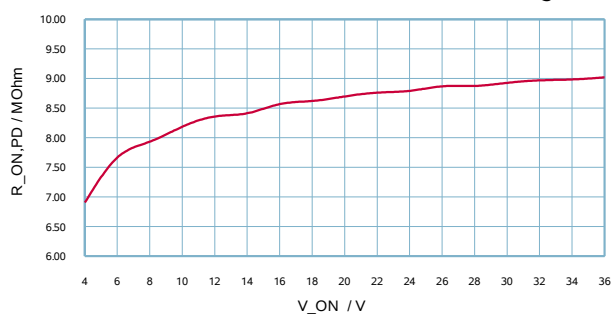
Typ. VIN Undervoltage Lockout (vs. Temperature)



Enable Threshold at ON vs Temperature



ON Pulldown Resistance vs ON Voltage



8 Functional Description

8.1 General Description

E522.7x product family is a fixed output voltage step-down converter family intended for current-sensitive industry and consumer applications, featuring open loop stability and short current limitation for the integrated driver transistor. High operating frequency allows the use of small-sized external components.

Integrated IDLE detection provides very low standby currents, significantly reducing the applications total current consumption. If the application supplied by E522.7x is set into low-current mode (typ. $\ll 1\text{mA}$), current consumption at V_{IN} is adapted to typical $12\mu\text{A}$ only.

The pulse frequency modulation (PFM) scheme does not need a clock signal for operation, providing minimum ON/OFF time regulation for the internal switch. Furthermore, the PFM scheme allows fastest transient line and load responses without the need for external compensation networks. Adjustable internal current measurement allows optimal adaption to the inductor without the need for a shunt resistor.

Pin ON	Load condition	Load condition	Internal Signal "IDLE"	Mode	V_{OUT}	I_{VIN}
$V_{\text{ON}} < V_{\text{ON,TH}}$				SLEEP	0V	$8\mu\text{A}$
$V_{\text{ON}} > V_{\text{ON,TH}}$	Nominal load	$D > D_{\text{IDLE}}$	"0"	NORMAL	3.3V or 5V	$150\mu\text{A}$
$V_{\text{ON}} > V_{\text{ON,TH}}$	Reduced load $\ll 1\text{mA}$	$D < D_{\text{IDLE}}$	"1"	IDLE	3.3V or 5V - 0%... -5%	$12\mu\text{A}$

8.2 Pulse Frequency Modulated Converter

The LXT switch control signal is based on a combination of output voltage V_{SENSE} , input voltage V_{VIN} and measured switch current. It provides adaptive frequency in the range of 0Hz up to typ. 1.33MHz as seen in typical performance figures.

To avoid unnecessary switching, a minimum ON time of typ. 260ns and OFF time of 520ns is used. ON time will be reduced below 260ns if over-current is detected. OFF time will automatically be increased in length to limit current flow during start-up or short circuit to GND at pin LXT or VOUT.

The figure below shows the typical normalized operating frequency in continuous conduction mode:

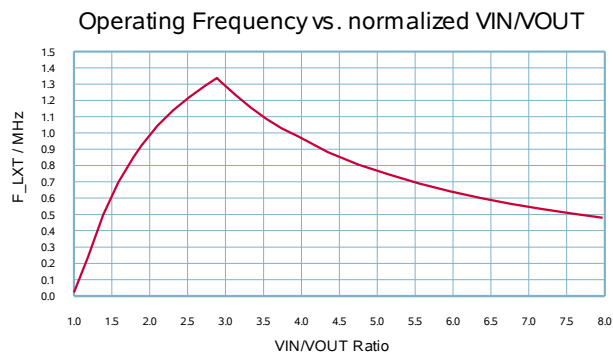


Figure 3: Operating Frequency vs normalized VIN/VOUT Ratio

8.3 Idle Detection

Idle operation basically is a sequence of standby periods followed by recharge cycles. During IDLE the application is supplied by the output capacitance. The reference is switched to typ. 95% of nominal value, at which the converter will be reactivated to high power operation. In this way, light load currents are compressed to short recharge phases, during which a high efficiency can be reached.

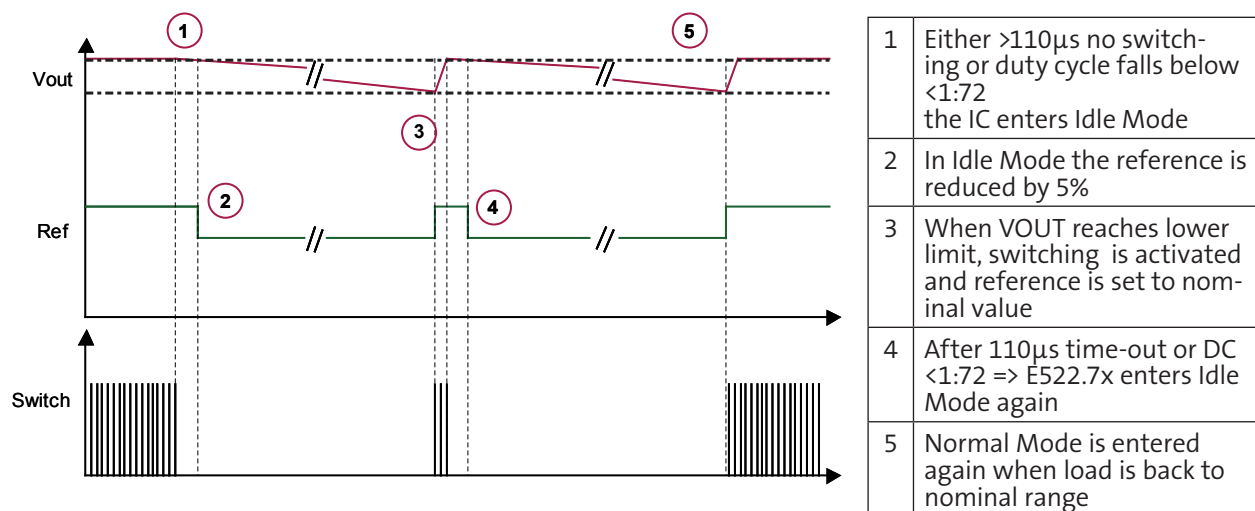


Figure 4: Behaviour in IDLE Mode

E522.7x automatically switches between IDLE and ACTIVE if no external load is applied to E522.7x. The criterion for the decision is that either no switching activity occurred for longer than typ. 110μs or the duty cycle of the converter falls below a limit of typically 1:72. (see figure 4)

9 Typical Operating Circuit

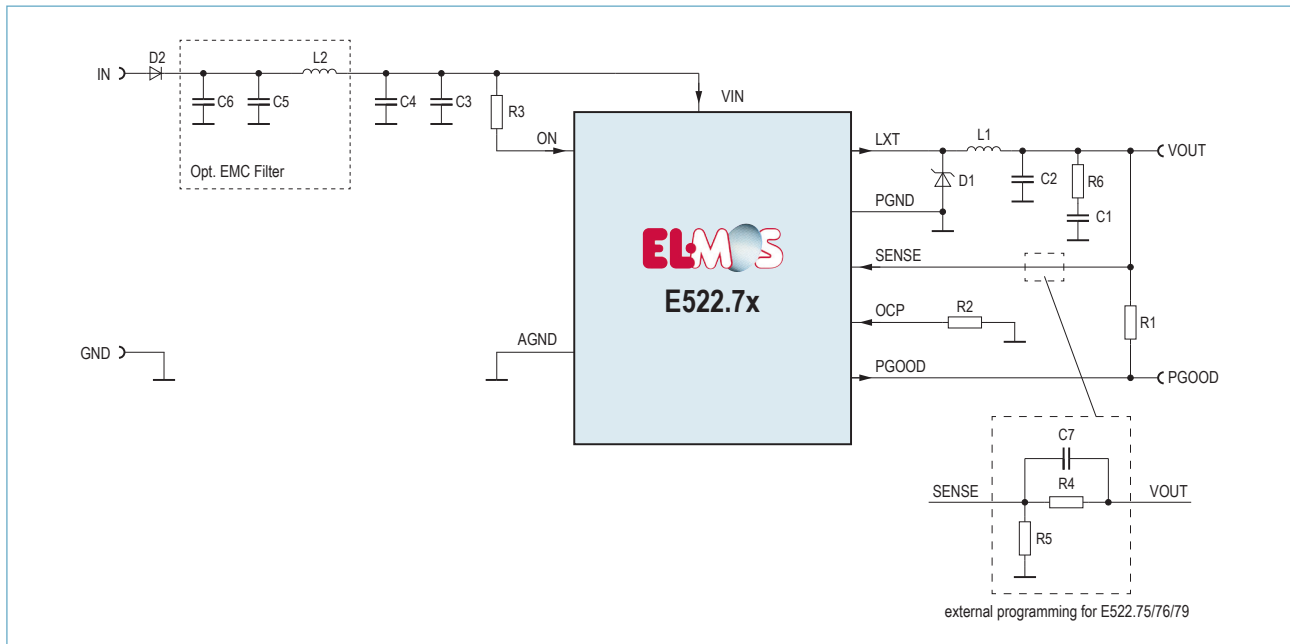


Figure 5: Typical operating circuit diagram

Table 2: External Components

Symbol	Min	Typ	Max	Unit	Description
R1		3.3		kΩ	Pull up resistor for PGOOD
R2	24		60	kΩ	OCP configuration resistor
R3		3.3		kΩ	Optional resistor for connection to VIN
R4		30 ¹⁾		kΩ	Resistor for output voltage programming
R5		30		kΩ	Resistor for output voltage programming
R6		0.2		Ω	Optional ESR-equivalent resistor
C1	47	100		μF	Output filter capacitor, low ESR
C2		33	100	nF	Output filter capacitor, low ESR, low ESL type
C3	20	33		μF	Input filter capacitor
C4		220		nF	Input filter capacitor, low ESR, low ESL type
C5		100		nF	EMC capacitor; low ESR, low ESL type
C6		1		nF	EMC capacitor; low ESR, low ESL type
C7					Optional AC-coupling capacitor (see chapter 9.2.5)
L1	18	33	82	μH	Inductor L _{LXT} @ E522.71-76
L1	10	22	82	μH	Inductor L _{LXT} @ E522.77-79
L2					EMC ferrite e.g. Würth 742-792-118
D1					Freewheeling diode for LXT, preferred Vishay SS14
D2					Optional reverse polarity protection diode

1) Select for V_{OUT} according to $R_4 = R_s \cdot \left(\frac{V_{OUT} - V_{SENSE}}{V_{SENSE}} \right)$

9.2 Application / Implementation Hints

The following chapter will give additional recommendations and advices for the implementation of E522.7x, giving starting values for components during prototyping.

9.2.1 Maximum Input Voltage in case of adjustable output voltage (E522.75/76/79)

The maximum input voltage is defined by the minimum $T_{ON,MIN}$ (during over-current limitation) and the requested output voltage. The following diagram shows the recommended area for the input voltage. If the input voltage is higher than recommended, due to transient effects the maximum current in the inductor may exceed the configured over-current limitation during start-up or in case of short circuit.

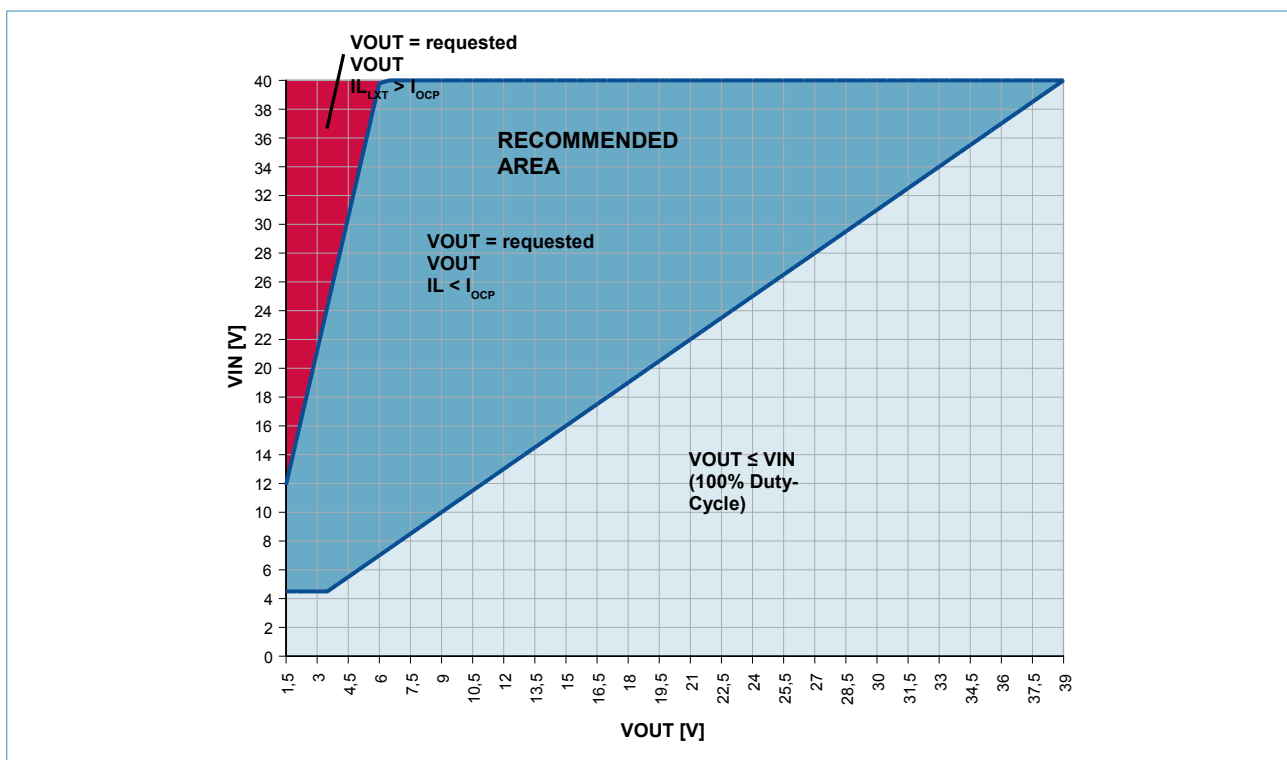


Figure 6: Maximum recommended V_{IN}

9.2.2 Maximum output current E522.75/76/79

E522.7x limits the inductor peak current. Lower end of inductor ripple current depends on $T_{OFF,MIN}$, the inductance value and the output voltage. The maximum available output current is less or equal to the average current flowing in the inductance.

The following graph visualizes the relation between these parameters.

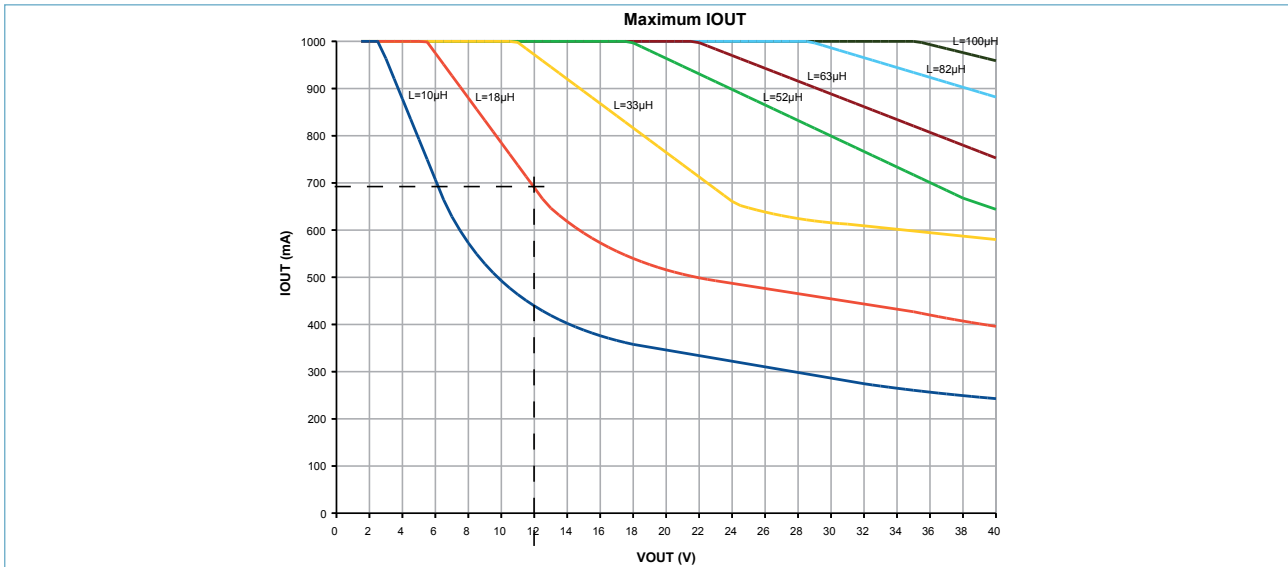


Figure 7: Maximum Output Current vs. Output Voltage (1A / E522.79)

For example, with an inductor of 18µH and an output voltage of 12V, the minimum available output current is 690mA.

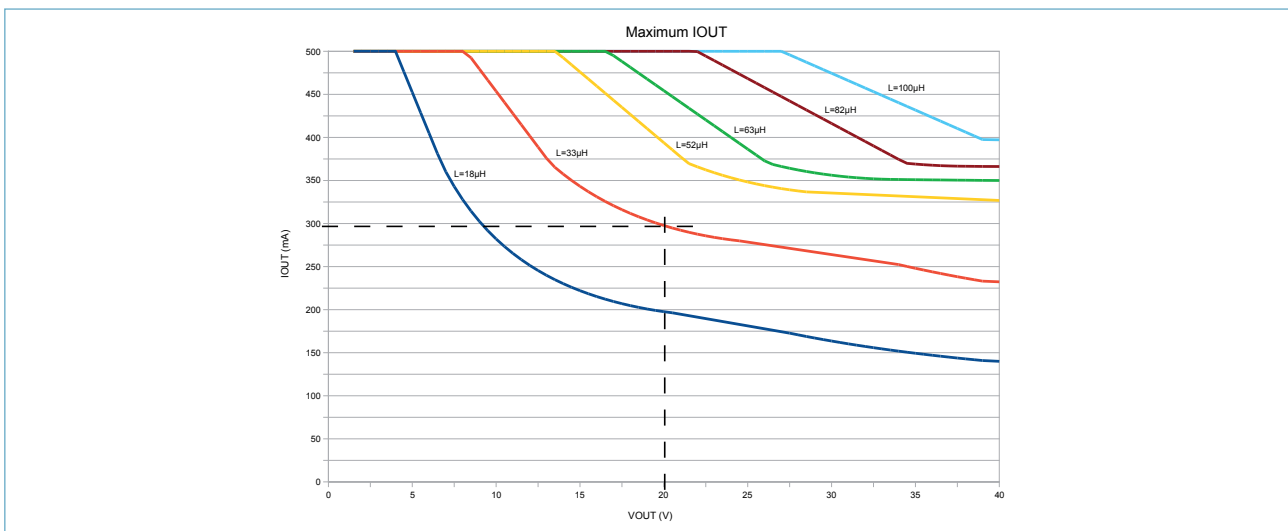


Figure 8: Maximum Output Current vs. Output Voltage (500mA / E522.75)

For example, with an inductor of 33µH and an output voltage of 20V, the minimum available output current is 295mA.

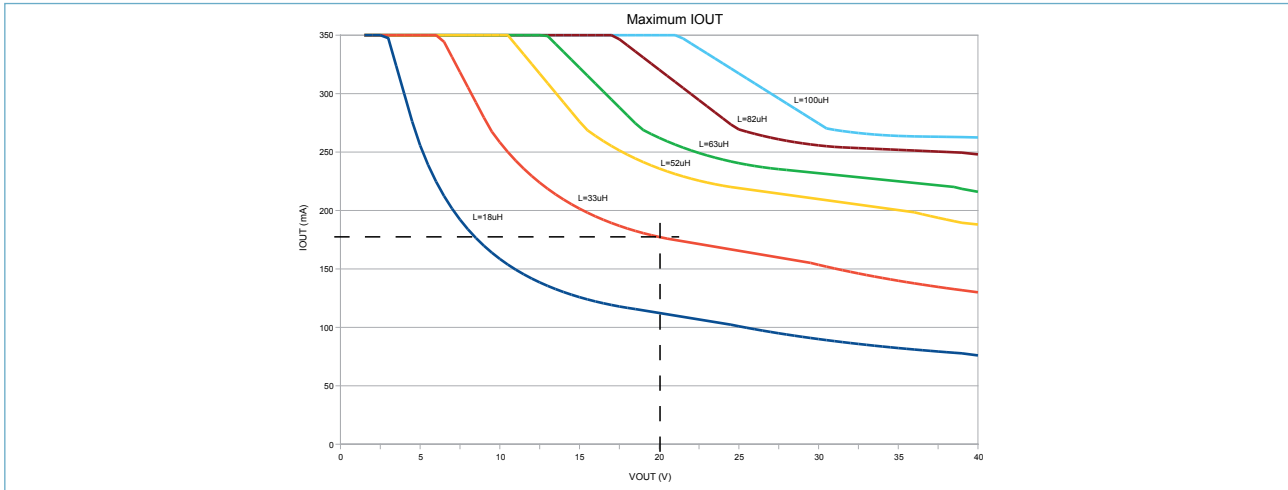


Figure 8: Maximum Output Current vs. Output Voltage (350mA / E522.76)

For example, with an inductor of 33µH and an output voltage of 20V, the minimum available output current is 175mA.

9.2.3 L_{LXT} Inductor Selection

For a given application (in continuous conducting mode), it is either recommended to choose an inductance value that is suitable for $\pm 15\%$ current ripple at the typical operating frequency or to use the following equations. Depending on V_{VIN} to V_{OUT} ratio, usually two equations describe the maximum peak-to-peak current ripple in the inductor L_{LXT} . It can either be calculated from the maximum input voltage at V_{IN} ($V_{VIN,MAX,APP}$)

$$a) \quad I_{RIPPLE, LXT, PP1} = \frac{T_{ON, MIN} \cdot (V_{VIN, MAX, APP} - V_{OUT, NOM})}{L_{LXT}}$$

or by the following equation (with V_{DIODE} being the forward voltage drop of the free-wheeling diode)

$$b) \quad I_{RIPPLE, LXT, PP2} = \frac{T_{OFF, MIN, NOM} \cdot (V_{OUT, NOM} + V_{DIODE})}{L_{LXT}}$$

Take the higher result of both equations into account during choice of the external capacitors ESR (see chapter 9.2.4). The minimum ripple may either occur at the maximum operation frequency or at the lowest input voltage that is required for the application. In most cases, the current ripple at peak-operating-frequency can also be calculated by equation b) above.

To choose a sufficiently high saturation current for the inductor L_{LXT} , consider

- the maximum application load current plus half of the maximum ripple current calculated above and
- the configured current limitation derived from R_{OCP} (to avoid degradation or other effects due to saturation of the inductor core - depending on the magnetic core material)

In general an additional saturation margin of $>25\%$ for the inductor current rating is recommended for transient effects, especially at extreme V_{VIN} to V_{OUT} voltage ratios.

DC resistance of L_{LXT} (referred here as $R_{LXT,DC}$) reduces efficiency and contributes to the losses in the inductor (combined with AC losses which may arise due the use of high frequency operation). A DC resistance $<0.5\Omega$ is recommended for E522.71-76 ($<0.25\Omega$ for E522.77-79). At a given load current I_{LOAD} , resistance affects minimum input voltage required to regulate V_{OUT} in the following way

$$V_{IN, MIN} = V_{OUT, NOM} + I_{LOAD} \cdot (R_{DS(ON)} + R_{LXT, DC})$$

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9.2.4 C_{OUT} Capacitor Selection

During nominal operation electrical serial resistance (ESR) of the capacitor is important to generate a minimum output voltage ripple of 10mV to 100mV. This ripple is necessary to provide a proper regulation information for E522.7x. It depends on peripheral elements chosen (L_{LXT} and C_{OUT}) and their parasitic behaviour as explained further on.

The ESR of the capacitor C_{OUT} (named R_{ESR,COUT}, see operating circuit R6) must be high enough to ensure a voltage ripple for V_{OUT} to provide high-frequency switching. The ripple voltage can basically be calculated using the inductor current ripple (see chapter 9.2.3) by

$$V_{RIPPLE,OUT} = R_{ESR,COUT} \cdot I_{RIPPLE,LXT,PP}$$

Electrical serial inductance should be kept as low as possible, what can be achieved by placing a parallel ceramic type capacitor of <100nF (typ. 33nF).

During IDLE, the application is supplied by the output capacitor C_{OUT}. The capacitance, which is necessary to power the application until E522.7x fully wakes up, can be calculated using the maximum load current step (I_{LOAD,MAX}) and a maximum tolerable voltage drop (U_{DROP,MAX}) in the following way:

$$C_{OUT} = \frac{I_{LOAD,MAX} \cdot 25\mu s}{U_{DROP,MAX} - R_{ESR,COUT} \cdot I_{LOAD,MAX}}$$

For example, assuming a maximum load step of 350mA, a tolerable voltage drop of 120mV and R_{ESR,COUT} being 120mΩ the output capacitance should be chosen >112μF. For proper active operation, it is necessary to choose capacitance values >22μF at V_{OUT}.

Take into account, that many capacitor types show a strong temperature and voltage dependency, or may be sensible to high peak currents. Make sure, that at extreme temperatures and voltages the capacitance value is reached.

9.2.5 R_{SENSE1}, C_{SENSE} Selection for adjustable E522.75/76/79

The resistors R_{SENSE1} and R_{SENSE2} have to be chosen high enough to avoid a reduction of the efficiency. A typical current of 50 μA is recommended to avoid sensitivity to noise. The capacitor C_{SENSE} helps to produce a correct ripple voltage at SENSE pin. Without enough ripple at SENSE pin, the regulation will not be optimal and you could observe burst pulses at LXT pin. When the ripple voltage is high enough, you should see a stable operating frequency. To choose C_{SENSE}, start without any capacitor and increase the value until you are satisfied with the regulation.

9.2.6 Rectification- / Freewheeling Diode Selection

The free-wheeling diode must have a low forward voltage (to increase efficiency) as well as a very low reverse recovery time of typically 10ns. In general, a fast Schottky type diode is recommended. High parasitic capacitance as well as long reverse recovery time may cause additional radiated emission at LXT. Parasitic capacitance of this diode decreases the overall efficiency and causes current spikes when the LXT driver turns on.

During IDLE, consider the leakage of the free-wheeling diode at nominal converter output voltage which will contribute to the overall current consumption (see IDLE adaption, chapter 9.2.9). In general, a bipolar diode can provide lower leakage current and parasitic capacitance, but may also have a negative impact on efficiency due to higher forward voltage drop. Reverse recovery time of the diode must be taken into account.

9.2.7 Over-Current Configuration at OCP

To adjust the internal over-current limitation of the LXT high-side driver to a value of I_{LIM} , the resistor between OCP and GND can be chosen by interpolation between the specified values (in the range of 24kΩ to 60kΩ) by

$$R_{OCP} = \frac{I_{OCP, 24k\Omega}}{I_{LIM}} \cdot 24k\Omega \quad | \quad I_{LIM} \leq I_{OCP, 24k\Omega}$$

Choice the current I_{LIM} with respect to the maximum usable current of the inductor L_{LXT} . Capacitive load at pin OCP has to be avoided due to stability reasons. It must not exceed 100pF.

9.2.8 VIN Capacitor Selection

VIN input capacitance value can be chosen from an acceptable voltage ripple $V_{VIN, RIPPLE, MAX}$ (defined by the overall application requirements) together with I_{LIM} (configured by R_{OCP}) and the ESR of VIN capacitor by

$$C_{VIN} = \frac{(I_{LIM} \cdot t_{ON, MIN})}{(V_{VIN, RIPPLE, MAX} - I_{LIM} \cdot R_{ESR, C_{VIN}})}$$

Both, the result of above equation, but also a minimum of 22μF are to be taken into account. Additionally, a parallel low ESR and low ESL ceramic capacitor type has to be placed (typ. 220nF).

Considerations regarding temperature and voltage dependency apply to VIN capacitors as well (see chapter 9.2.4), especially voltage dependency.

9.2.9 Idle Adaption Options

IDLE / ACTIVE state detection can be adapted to a given application by consideration of the following external influences:

a) During start-up, the energy within the inductor (approximately $0.5 \times L_{LXT} \times I_{LIM}^2$) has to be consumed by the load within the IDLE detection time-out (to stay in ACTIVE mode). It is proportional to the inductance L_{LXT} and to the square of configured OCP current limit.

b) At nominal operation, the power which is transferred to the output in discontinuous operation depends on the inductance at L_{LXT} , the current which is build up during $T_{ON, MIN}$ and the duty-cycle IDLE condition.

This detection mechanism allows to shift the detection threshold proportional to $1/L_{LXT}$. Note, that the output power in this case also depends on the square of charging voltage $V_{VIN-VOUT}$, which may require to adapt L_{LXT} to the typical application input voltage.

c) In general, cross-coupling between high voltage switching of LXT and input SENSE is to be avoided. In case that practically it may not be completely avoidable, a third effect based on the amount of coupling must be considered. Distortions can lead to self-excitation of the regulator, charging the output until the lower end of the output voltage ripple crosses the regulation point. The average of the output voltage ripple (1/2 for triangular ripple) has to be discharged by the load before a time-out is detected (typ. 110μs - to stay in ACTIVE mode).

Depending on choice of external components, the rectification / free-wheeling diode leakage current has to be taken into account, because it poses a load to E522.7x, too. If it generates sufficient switching activity to trigger the duty cycle IDLE condition, the converter will provide nominal output voltage.

Consider the leakage current of the free-wheeling diode for a reverse voltage of V_{OUT} and the maximum ambient temperature. The above described measures a,b,c (in most cases choice of inductance L_{LXT}) can be used to adapt the applications dimensioning to this additional load.

9.2.10 Misc Application Remarks

Optional, regarding VIN voltage supervision, the accurate threshold at pin ON can be used to implement under-voltage lock-out for the converter, automatically switching to sleep mode if necessary. In such cases a resistive divider between VIN and GND, connected to ON can be used. The threshold is defined by

$$V_{VIN,MIN} = V_{ON,TH} \cdot \left(1 + \frac{R2}{R1}\right)$$

Choose the divider impedance significantly lower than the typical input impedance of 7MΩ at pin ON to avoid inaccuracy. Note, that the divider current directly contributes to the application current consumption.

For reverse polarity protection a diode (or comparable reverse voltage protection measure) for VIN is recommended. In EMC sensitive environments additional decoupling measures at VIN are recommended.

10 Ordering Information

Product ID	V _{OUT}	I _{OUT}	Ambient Temp. Range	Package
E522.71	5V	500mA	-40°C to +105°C	SOIC8-EP
E522.72	3.3V	500mA	-40°C to +105°C	SOIC8-EP
E522.73	5V	350mA	-40°C to +105°C	SOIC8-EP
E522.74	3.3V	350mA	-40°C to +105°C	SOIC8-EP
E522.75	1.5V to 40V	500mA	-40°C to +105°C	SOIC8-EP
E522.76	1.5V to 40V	350mA	-40°C to +105°C	SOIC8-EP
E522.77	5V	1A	-40°C to +105°C	SOIC8-EP
E522.78	3.3V	1A	-40°C to +105°C	SOIC8-EP
E522.79	1.5V to 40V	1A	-40°C to +105°C	SOIC8-EP

11 Package Reference

11.1 Package Reference SOIC8-EP

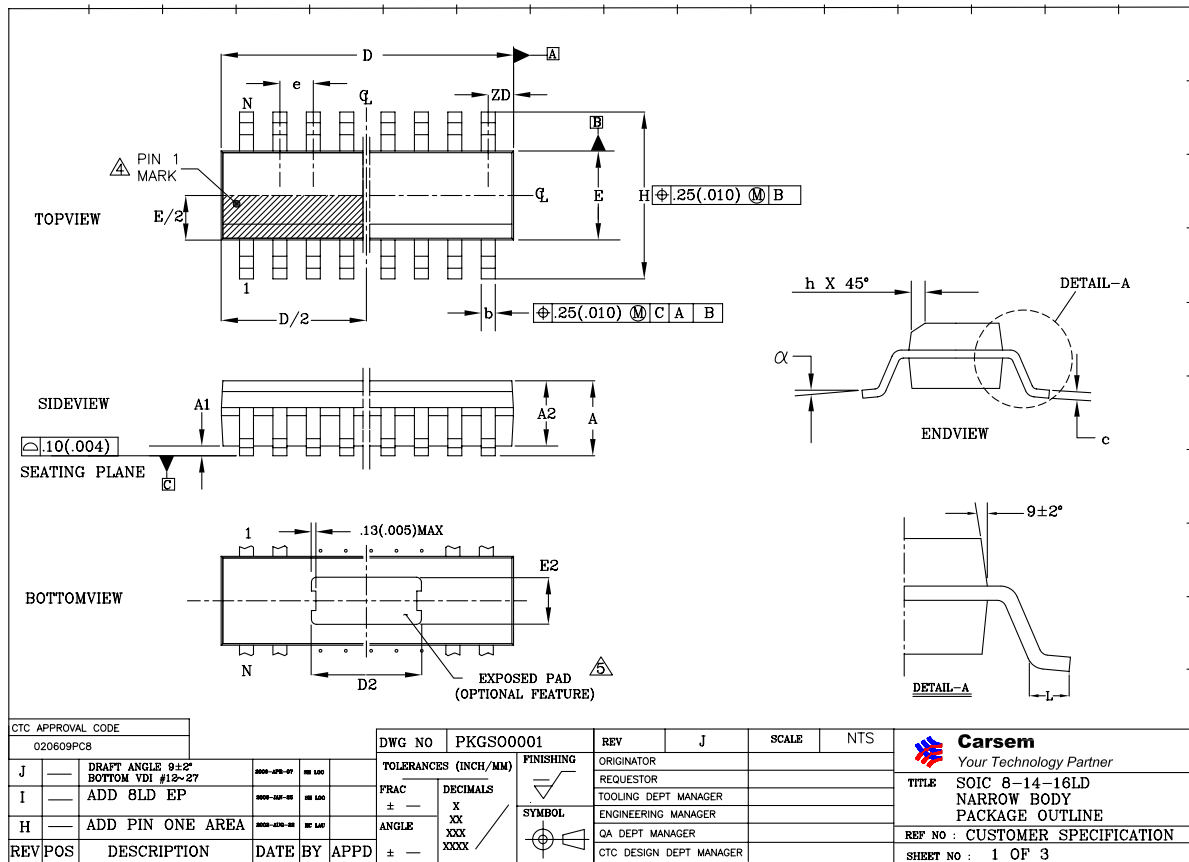
The E522.7x family members are available in a Pb free, RoHS compliant, SOIC8-EP package.

11.2 Marking Top Side

- ▶ Elmos Logo
- ▶ 52271
- ▶ XXXSL
- ▶ YWWR@

Signature	Explanation
52271	ELMOS project number
A	ELMOS project revision code
XXX	Production lot number
S	Assembler code
L	Production line code
YWW	Year and week of assembly
R	Mask revision code
@	ELMOS internal code

11.3 Package Outline SOIC8-EP



SYMBOL	SOIC-8LD	
	MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27	BSC
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.53	REF
A2	1.37	1.57

SYMBOL	SOIC-8-EP1	
	MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27	BSC
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.53	REF
A2	1.37	1.57
D2	3.00	3.50
E2	2.00	2.50

SYMBOL	SOIC-14LD	
	MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	8.56	8.74
E	3.81	3.99
e	1.27	BSC
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51	REF
A2	1.37	1.57

SYMBOL	SOIC-16LD	
	MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27	BSC
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51	REF
A2	1.37	1.57

NOTES :

- LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
- PACKAGE SURFACE FINISHING :
 (2.1) TOP : MATTE (CHARMILLES #18~30).
 (2.2) BOTTOM : MATTE (CHARMILLES #12~27).

- ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).
- DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- EXPOSED PAD FEATURE IS PRESENT ON VARIATIONS DESIGNATED WITH "-EP"
- REFERENCE TO JEDEC MS-012.

CTC APPROVAL CODE	DWG NO	PKGS00001	REV	J	SCALE	NTS
J	DRAFT ANGLE 9±2° BOTTOM VDI #12-27	TOLERANCES (INCH/MM)	ORIGINATOR			
I	ADD 8LD EP	FRAC ±	REQUESTOR			
H	ADD PIN ONE AREA	DECIMALS X XX XXX XXXX	TOOLING DEPT MANAGER			
REV	POS DESCRIPTION	DATE BY APPD	ENGINEERING MANAGER			
			QA DEPT MANAGER			
			CTC DESIGN DEPT MANAGER			

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 TITLE: SOIC 8-14-16LD NARROW BODY PACKAGE OUTLINE
 REF NO: CUSTOMER SPECIFICATION
 SHEET NO: 2 OF 3

LOW POWER STEP DOWN CONVERTERS

PRELIMINARY INFORMATION - JUL 2, 2012

SOIC-8LD			SOIC-8-EP1			SOIC-14LD			SOIC-16LD		
SYMBOL	INCHES		SYMBOL	INCHES		SYMBOL	INCHES		SYMBOL	INCHES	
	MIN	MAX		MIN	MAX		MIN	MAX		MIN	MAX
A1	.0040	.0098	A1	.0040	.0098	A1	.0040	.0098	A1	.0040	.0098
B	.014	.018	B	.014	.018	B	.014	.018	B	.014	.018
C	.0075	.0098	C	.0075	.0098	C	.0075	.0098	C	.0075	.0098
D	.189	.196	D	.189	.196	D	.337	.344	D	.386	.393
E	.150	.157	E	.150	.157	E	.150	.157	E	.150	.157
e	.050 BSC		e	.050 BSC		e	.050 BSC		e	.050 BSC	
H	.2284	.2440	H	.2284	.2440	H	.2284	.2440	H	.2284	.2440
h	.0099	.0196	h	.0099	.0196	h	.0099	.0196	h	.0099	.0196
L	.016	.050	L	.016	.050	L	.016	.050	L	.016	.050
A	.060	.068	A	.060	.068	A	.060	.068	A	.060	.068
α	0°	8°	α	0°	8°	α	0°	8°	α	0°	8°
ZD	.021	REF	ZD	.021	REF	ZD	.020	REF	ZD	.020	REF
A2	.054	.062	A2	.054	.062	A2	.054	.062	A2	.054	.062
			D2	.118	.138						
			E2	.080	.098						

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
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6. REFERENCE TO JEDEC MS-012.

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020609PCB			TOLERANCES (INCH/MM)	FINISHING	ORIGINATOR						
J	—	DRAFT ANGLE 9±2° BOTTOM VDI #12~27	FRAC	DECIMALS	REQUESTOR				TITLE SOIC 8-14-16LD NARROW BODY PACKAGE OUTLINE		
I	—	ADD 8LD EP	±	X XX XXX XXXX	TOOLING DEPT MANAGER						
H	—	ADD PIN ONE AREA	ANGLE		ENGINEERING MANAGER				REF NO : CUSTOMER SPECIFICATION		
REV POS	DESCRIPTION	DATE BY APPD	±		QA DEPT MANAGER						
					CTC DESIGN DEPT MANAGER				SHEET NO : 3 OF 3		

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