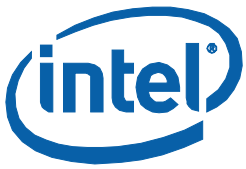

Intel® 4 Series Chipsets Chipset Family

Specification Update

For the Intel® 82Q45, 82Q43, 82B43, 82G45, 82G43, 82G41 Graphics and Memory Controller Hub (GMCH) and the Intel® 82P45, 82P43 Memory Controller Hub (MCH)

July 2010

Document Number: 319971-014

Contents

Revision History

Revision	Description	Date
-001	• Initial release	June 2008
-002	• Added Intel 4 Series Chipset 82G41 GMCH	September 2008
-003	• Added Intel 4 Series Chipset 82Q43 and 82Q45 GMCH	September 2008
-004	• Added Errata 1 – 3	October 2008
-005	• Added G45 component marking information	February 2009
-006	• Added QDF numbers for updated G43 and G41 production parts and added QDF for B43 in the Component Marking Information table • Updated Intel® 4 Series Chipset Family Sku Matrix table • Added Errata 4	May 2009
-007	• Added Component Identification for B43	June 2009
-008	• Added Errata 5 and 6	July 2009
-009	• Added Errata 7	August 2009
-010	• Added Errata 8 and 9	September 2009
-011	• Updated Specification Changes section to add min and max spec for CL_VREF	November 2009
-012	• Updated VCC and VCC_EXP requirements for B43 • Updated DIMM support for B43	March 2010
-013	• All changes in Rev012 of the Spec update incorporated into Intel® 4 Series Chipset Family Datasheet Rev 007 • Updated Intel® 4 Series Chipset Family Sku Matrix table	April 2010
-014	• Added Errata 10 and 11	July 2010

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number/Location
Intel® 4 Series Chipsets Chipset Family Datasheet	319970-006

Nomenclature

Errata are design defects or errors. Errata may cause the Intel 4 Series Chipset (G)MCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed (G)MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

NO.	A2	A3	PLANS	ERRATA
1	X	X	No Fix	Intel® Series 4 Express Chipsets' Integrated audio codec's subsystem ID (SSID) resets to the default value after warm reset
2	X	X	No Fix	C3/C4 Enabled Systems May Encounter Hang When Entering C3 from C2
3	X	X	No Fix	Intel® 4 Series (G)MCH DDR3 1N Mode CMD-to-CLK (tIS) Violation
4	X	X	No Fix	Intel®4 Series Express Chipset (Desktop) Erroneous Memory Read Request

NO.	A2	A3	PLANS	ERRATA
5	X	X	No Fix	Intel®4 Series Express Chipset (Desktop) AUX CH Low Differential Pk-Pk Voltage Swing
6	X	X	No Fix	Intel®4 Series Express Chipset (Desktop) Temporary display corruption during mode change in 1-lane and 2-lane configurations of Display Port interface
7	X	X	No Fix	Intel® 4 Series Express Chipset Self-Refresh Exit VIX Spec Violation
8	X	X	No Fix	Intel® 4 Series Express Chipsets Integrated Graphics Overlay Display Corruption Issue
9	X	X	No Fix	Intel® 4 Series Express Chipset C3/C4 Shutdown Issue
10	X	X	No Fix	Intel® 4 Series Express Chipset PCIe Root Port May Not Initiate Link Speed Change
11	X	X	No Fix	Intel® 4 Series Express Chipset DDR3 1066MHz 1N Mode Issue

NO.	SPECIFICATION CHANGES
	There are no Specification Changes in this revision of the specification update

NO.	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this revision of the specification update

NO.	DOCUMENTATION CHANGES
	There are no Documentation Changes in this revision of the specification update

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Identification Information

Component Identification via Programming Interface

The Intel 4 Series Chipset (G)MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]		Revision Number[3]
A2	8086h	82Q45/82Q43 GMCH	2E10h	02h
		82G45/82G43 GMCH	2E20h	
		82P45/82P43 MCH		
		82G41 GMCH	2E30h	
A2	8086h	82P45/82P43 MCH	2E20h	03h
A3	8086h	82Q45/82Q43 GMCH	2E10h	03h
		82G45/82G43 GMCH	2E20h	
		82G41 GMCH	2E30h	
		82B43 GMCH (Base)	2E40h	
		82B43 GMCH (Soft Sku)	2E90h	

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 4 Series Chipset (G)MCH may be identified by the following component markings:

Stepping	Product	S-Spec	Lead/PbFree	Top Marking	Notes
A2	GMCH	SLB7Z	PbFree	AC82P45	82P45 MCH
A2	GMCH	SLB83	PbFree	AC82P43	82P43 MCH
A3	GMCH	SLB84	PbFree	AC82G45	82G45 GMCH
A3	GMCH	SLB85	PbFree	AC82G43	82G43 GMCH
A3	GMCH	SLB8D	PbFree	AC82G41	82G41 GMCH
A3	GMCH	SLB8C	PbFree	AC82P45	82P45 MCH

Stepping	Product	S-Spec	Lead / PbFree	Top Marking	Notes
A3	GMCH	SLB89	PbFree	AC82P43	82P43 MCH
A3	GMCH	SLB8A	PbFree	AC82Q45	82Q45 GMCH
A3	GMCH	SLB88	PbFree	AC82Q43	82Q43 GMCH
A3	GMCH	SLB8G	PbFree	AC82G45	82G45 GMCH
A3	GMCH	SLGQ2	PbFree	AC82G43	82G43 GMCH - Support for 2 DIMMs/Channel
A3	GMCH	SLGQ3	PbFree	AC82G41	82G41 GMCH - Support for HDMI & ICH7R
A3	GMCH	SLGL7	PbFree	AC82B43	82B43 GMCH

Intel® 4 Series Chipset Family Sku Matrix

Feature			SKU							
			Q45	Q43	B43	G45	G43	G41	P45	P43
FSB Support	1333 MHz		•	•	•	•	•	•	•	•
	1067 MHz		•	•	•	•	•	•	•	•
	800 MHz		•	•	•	•	•	•	•	•
Memory Support	DIMMS Per Channel		2	2	2	2	1/2[1]	1	2	2
	DDR3	1067 MHz	•	•	•	•	•	•	•	•
		800 MHz	•	•	•	•	•	•	•	•
	DDR2	800 MHz	•	•	•	•	•	•	•	•
		667 MHz	•	•	•	•	•	•	•	•
ICH Support	Intel® ICH10DO		•							
	Intel ICH10D			•	•					
	Intel ICH10					•	•		•	•
	Intel ICH10R					•	•		•	•
	Intel ICH7							•		
	Intel ICH7R							•[2]		
Discrete GFX	PCIe* Gen 2 1x16		•	•	•	•	•		•	•
	PCIe Gen 2 2x8								•	
	PCIe Gen 1 1x16		•	•	•	•	•	•	•	•
	PCIe Gen 1 2x8								•	
Integrated GFX	5th Generation Core		•	•	•	•	•	•	NA	
	DirectX 10		•	•	•	•	•	•		
	OpenGL 2.0		•	•	•	•	•	•		
	Intel Clear Video Technology					•	•	•		
	Dual Independent Display		•	•	•	•	•	•		
	ADD2/MEC		•	•	•	•	•	•		
	HDMI* 1.3				Upgrade[3]	•	•	•[2]		
	DVI*		•	•	•	•	•	•		
	DisplayPort*		•	•	•	•	•	•		
	Integrated HDCP		•	•	•	•	•	•		
	PAVP		•	•	•	•	•	•		

Feature		SKU							
		Q45	Q43	B43	G45	G43	G41	P45	P43
	VGA*	•	•	•	•	•	•		
	Full HW decode acceleration of MPEG2, VC1 and AVC				•				
Platform Technologies	Intel® AMT	•							
	Intel® Upgrade Service			•					
	Standard Manageability		•	Upgrade[4]					
	Intel® Remote Wake Technology (Intel® RWT)				•	•		•	•
	ASF[5]	•	•	•	•	•		•	•
	Intel QST[5]	•	•	•	•	•		•	•
	Intel TPM 1.2	•	•						
	Intel VT-d	•							
	Intel TXT	•	•						

Note:

1. Support for DIMMs/Channel varies on G43 parts. Please refer to *Component Marking Information* table to identify feature support.
2. Support of ICH7R/HDMI varies on G41 parts. Please refer to *Component Marking Information* table to identify feature support.
3. Enabled via Intel® Upgrade Service.
4. Enabled via Intel® Upgrade Service offering a “down the wire” Manageability Upgrade consisting of Intel Standard Manageability + CIRA.
5. Intel® Quiet System Technology and ASF functionality requires a correctly configured system, including an appropriate (G)MCH with ME, ME firmware, and system BIOS support.

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Errata

1. Intel® Series 4 Express Chipsets' Integrated audio codec's subsystem ID (SSID) resets to the default value after warm reset

Problem: The integrated audio codec's subsystem ID register will reset to the default value of 80860101h after CF9 reset

Implication: All Intel Series 4 Express Chipsets' integrated HDMI audio codec will have the same SSID value of 80860101h after OS boot, regardless of values programmed by system BIOS

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum

Status: No Fix

2. C3/C4 Enabled Systems May Encounter Hang When Entering C3 from C2

Problem: In synthetic laboratory testing, systems with C3/C4 enabled Processors supporting C3/C4 power states may encounter a situation where snoopable upstream traffic on DMI is allowed to proceed after the system has transitioned into C3. Systems based on the Q45 sku with VT-d enabled exhibit the issue more commonly than systems without VT-d enabled

Implication: When the above situation occurs, the C3 state snooped transactions are not able to complete and system hangs will occur

Note – This issue has only been observed in laboratory testing with synthetic operating systems and focus testing. The MCH will not enter PCIe Gen2 compliance test mode

Workaround: None

Status: No Fix

3. Intel® 4 Series (G)MCH DDR3 1N Mode CMD-to-CLK (tIS) Violation

Problem: Intel® 4 Series (G) MCH may violate DDR3 JEDEC spec CMD-to-CLK setup time (tIS). The following speeds and configurations may be affected
- DDR3 1067 Single DIMM per/ch
- DDR3 800 Dual DIMM per/ch

Violation does not occur in any other frequency or DIMM configuration

Implication: Violating JEDEC spec may cause system to not boot or potentially experience anomalous behavior

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum

Status: No Fix

4. Intel® 4 Series Express Chipset (Desktop) Erroneous Memory Read Request

Problem: Under memory stress conditions, the logic block responsible for transitions from the Host Clock Domain to the Memory Clock Domain may generate an erroneous memory read request

Implication: The erroneous read request may result in indeterminate system behavior

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum

Status: No Fix

5. Intel® 4 Series Express Chipset (Desktop) AUX CH Low Differential Pk-Pk Voltage Swing

Problem: Intel® 4 Series Chipset AUX Channel Differential Pk-Pk voltage swing may not meet the DisplayPort Standard on digital port C
- Minimum V_{Diff} Pk-Pk expected at TP2 (Test Point 2 defined by the DisplayPort Standard) is 160 mV
- Digital port B is not affected

Implication: Low AUX CH differential Pk-Pk swing may result in DisplayPort device not detecting the Chipset

Note: Intel has not observed any functional failures with available DisplayPort devices during focused DisplayPort validation

Workaround: None

Status: No Fix

6. Intel® 4 Series Express Chipset (Desktop) Temporary display corruption during mode change in 1-lane and 2-lane configurations of Display Port interface

Problem: The Intel® 4 Series Express Chipset family transmits incorrect number of VB-IDs during idle pattern in 1-lane and 2-lane configurations. During idle pattern, VB-ID is transmitted once in 1-lane and twice in 2-lane configurations instead of 4 times. The DP specification 1.1a states that VB-ID should be sent 4 times irrespective of the lane count.

Implication: Temporary display corruption may occur during video mode change. Issue occurs when the transmitter sends idle pattern to a 1-lane or 2-lane DisplayPort receiver

Implication not present during active video in 1-lane, 2-lane, or 4-lane configurations.

Workaround: None
A BIOS code change and graphics driver update has been identified and may be implemented to mitigate this erratum

Status: No Fix

7. Intel® 4 Series Express Chipset Self-Refresh Exit VIX Spec Violation

Problem: The Intel® 4 Series Express Chipset family may not comply with the JEDEC* Spec for V_{IX} min voltage specified for clock signal (CK) when exiting DDR3 dynamic self-refresh (SRX)

Implication: This may result in indeterminate system behavior

- Intel has observed functional failures resulting from this issue only on systems using DDR3 memory in laboratory testing in synthetic test environments with focused test patterns

Workaround: None
A BIOS code change and graphics driver update has been identified and may be implemented to mitigate this erratum

Status: No Fix

8. Intel® 4 Series Express Chipsets Integrated Graphics Overlay Display Corruption Issue

Problem: The Intel® Q45/Q43/B43/G45/G43/G41 Express Chipsets may not be able to supply pixels to overlay on pipe A after overlay was previously enabled and then disabled on pipe B

Implication: Video overlay display corruption in Extended Desktop mode with Microsoft Windows Vista* or Windows 7* is possibly observed when video media

playback is moved between 2 display devices with video overlay scaling enabled

Systems using Microsoft Windows XP* are not affected

Workaround: A graphics driver update has been identified and may be implemented to mitigate this erratum

Status: No Fix

9. Intel® 4 Series Express Chipsets C3/C4 Shutdown Issue

Problem: The Intel® Q45/Q43/B43/G45/G43/P45/P43 Express Chipset platform may exhibit display corruption or system hang while exiting C3 or C4 state

Implication: This may result in indeterminate system behavior

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum

Status: No Fix

10. Intel® 4 Series Express Chipset PCIe* Root Port May Not Initiate Link Speed Change

Problem: PCIe specification rev 2.0 requires the upstream component to maintain the PCIe link at the target link speed or the highest speed supported by both components on the link, whichever is lower. PCIe root port will not initiate the link speed change without being triggered by the software. System BIOS will trigger the link speed change under normal boot scenarios. However, BIOS is not involved in some scenarios such as link disable/re-enable or secondary bus reset and therefore the speed change may not occur unless initiated by the downstream component. This erratum does not affect the ability of the downstream component to initiate a link speed change. All known 5.0Gb/s-capable PCIe downstream components have been observed to initiate the link speed change without relying on the root port to do so.

Implication: Due to this erratum, the PCIe root port may not initiate a link speed change during some hardware scenarios causing the PCIe link to operate at a lower than expected speed. Intel has not observed this erratum with any commercially available platform.

Workaround: None identified.

Status: No Fix.

11. Intel® 4 Series Express Chipsets DDR3 1066MHz 1N Mode Issue

Problem: The Intel® 4 Series Express Chipset platform may violate DDR3 JEDEC* Spec for CMD-to-CLK hold time (tIH) when running DDR3 1066MHz memory in 1N mode using 1DIMM/channel configuration.

Implication: This may result in boot failures or system hangs.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix.

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Specification Change

There are no specification changes in this Specification Update revision

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision

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