NCE N-Channel Enhancement Mode Power MOSFET

General Features

• $V_{DS} = 60V, I_D = 0.3A$

 $R_{DS(ON)} < 3\Omega$ @ $V_{GS}=5V$

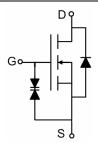
 $R_{DS(ON)}$ < 2Ω @ V_{GS} =10V

ESD Rating: HBM 2300V

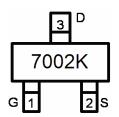
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

Application

- Direct logic-level interface: TTL/CMOS
- Drivers: relays, solenoids, lamps, hammers, display, memories, transistors, etc.
- Battery operated systems
- Solid-state relays



Schematic diagram



Marking and pin assignment



SOT-23 top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7002K	2N7002K	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _G s	±20	V	
Continuous Proin Current (T150°C)	T _A =25℃	1	0.3	Α	
Continuous Drain Current (T _J =150℃)	T _A =100°C	- I _D	0.19		
Drain Current-Pulsed (Note 1)		I _{DM}	0.8	Α	
Maximum Power Dissipation		P _D	0.35	W	
Operating Junction and Storage Temperature Range		T_{J}, T_{STG}	-55 To 150	$^{\circ}$ C	

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	350	°C/W
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Electrical Characteristics (TA=25 ℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics				•		
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	68	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μΑ
Cata Rady Lagkaga Current	1	V _{GS} =±10V,V _{DS} =0V	-	±100	±500	nA
Gate-Body Leakage Current	I_{GSS}	V _{GS} =±20V,V _{DS} =0V	-	±4	±10	uA
On Characteristics (Note 3)				•		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\mu A$	1	1.7	2.5	V
Drain-Source On-State Resistance	В	V _{GS} =5V, I _D =0.4A	-	1.3	3	Ω
Diali-Source Oil-State Resistance	$R_{DS(ON)}$	V _{GS} =10V, I _D =0.5A	-	1	2	Ω
Forward Transconductance	g FS	V _{DS} =10V,I _D =0.2A	0.1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{lss}	V_{DS} =25V, V_{GS} =0V,	-	21	50	PF
Output Capacitance	C _{oss}	V _{DS} -25V,V _{GS} -0V, F=1.0MHz	-	11	25	PF
Reverse Transfer Capacitance	C_{rss}	F = 1.0WH12	-	4.2	5	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}		-	10	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, I_{D} =0.2A	-	50	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{GEN} =10 Ω	-	17	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Cata Charge	_	V _{DS} =10V,I _D =0.3A,		1.7	3	nC
Total Gate Charge	Q_g	V _{GS} =4.5V		1.7	3	iiC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =0.2A	-	-	1.3	V
Diode Forward Current (Note 2)	Is		-	-	0.2	Α

Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production

Typical Electrical And Thermal Characteristics

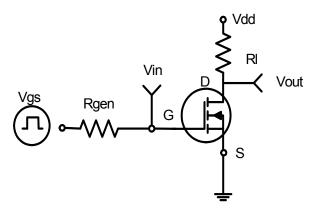


Figure 1:Switching Test Circuit

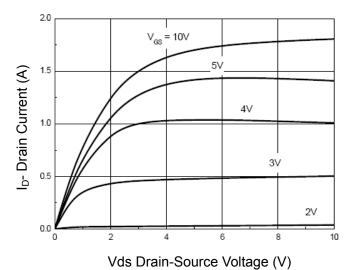


Figure 3 Output Characteristics

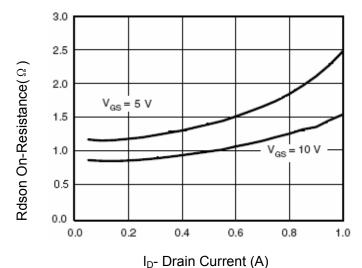


Figure 5 Drain-Source On-Resistance

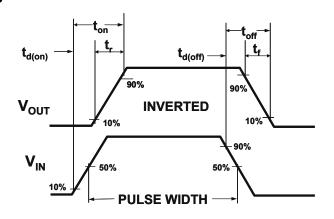


Figure 2:Switching Waveforms

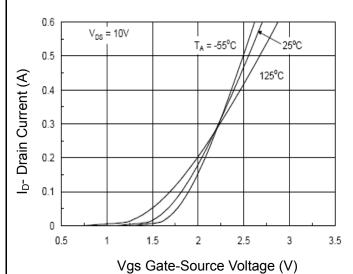
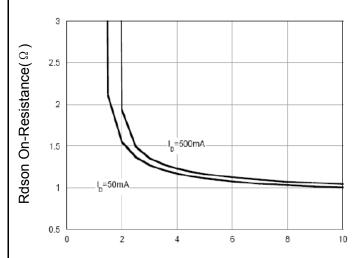
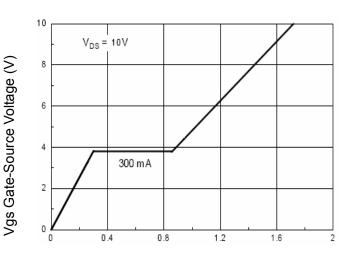


Figure 4 Transfer Characteristics



Vgs Gate-Source Voltage (V)
Figure 6 Rdson vs Vgs





Qg Gate Charge (nC) Figure 7 Gate Charge

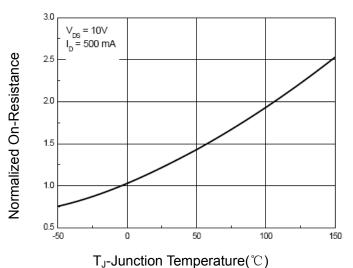


Figure 9 Drain-Source On-Resistance

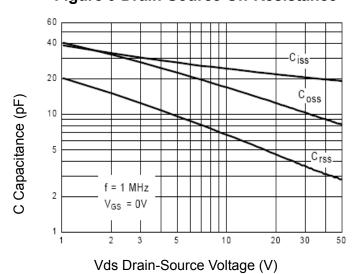
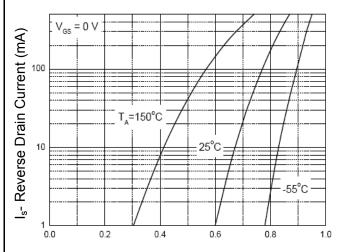
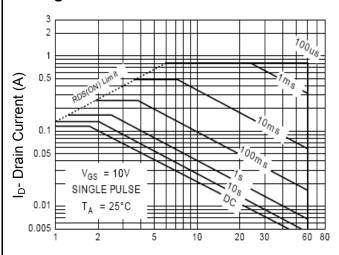


Figure 11 Capacitance vs Vds



Vsd Source-Drain Voltage (V)

Figure 8 Source-DrainDiode Forward



Vds Drain-Source Voltage (V)

Figure 10 Safe Operation Area



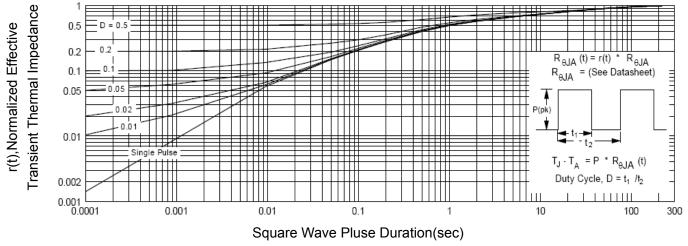
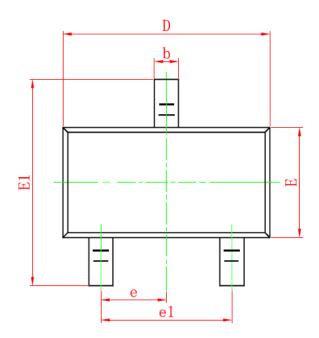
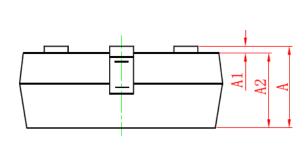
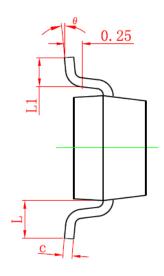


Figure 12 Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Information







Symbol	Dimensions in Millimeters			
	MIN.	MAX.		
Α	0.900	1.150		
A 1	0.000	0.100		
A2	0.900	1.050		
b	0.300	0.500		
С	0.080	0.150		
D	2.800	3.000		
E	1.200	1.400		
E1	2.250	2.550		
е	0.950TYP			
e1	1.800	2.000		
L	0.550REF			
L1	0.300	0.500		
θ	0°	8°		

Notes

- 1. All dimensions are in millimeters.
- 2. Tolerance ±0.10mm (4 mil) unless otherwise specified
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
- 4. Dimension L is measured in gauge plane.
- 5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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