I²C Bus Real-time Clock Module

Product Features

- RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year, with Leap Year Compensation Valid Up to 2100
- 31 Bytes of RAM for Scratchpad Data Storage
- Uses Standard 32.768kHz, 6pF or 12pF Load, Watch Crystal
- Programmable Time/Date, Open-Drain ALARM Output (Status Can also Be Polled)
- Oscillator Compensation on Chip
  -Digitally controlled trim capacitors in oscillator
  -Digitally frequency adjustment settings to ±190ppm
- OUT Pin for SRAM Power
- µP Reset Output
- Manual Reset Input with Push-Button Switch Debounce
- Independent Power-Fail and Reset Comparators
- 400kHz 2-Wire Interface
- Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock Registers or RAM
- Bus Timeout to Prevent Lockup of Malfunctioning Bus Interface
- Dual Power-Supply Pins for Primary and Backup Power
- Programmable Trickle Charger
- Uses Less than 1µA Timekeeping Current at 3.0V
- Operating voltages of 3V and 3.3V
- Lead free and Green Package: 16-pin TSSOP

Table 1 Function Comparison Table

Part No	Reset Threshold	Operation Voltage	Trickle Charger
PT7C4908R	2.63V	3.0V	Yes
PT7C4908S	2.93V	3.3V	Yes

Product Description

The PT7C4908R/S are I2C™-compatible real-time clocks (RTCs) with a microprocessor supervisor, optional trickle charger, backup power source, and NV RAM controller. The PT7C4908R/S provide a switchover to battery power, and time and date indication. The NV RAM is 31 bytes of static RAM that are available for scratchpad storage. The PT7C4908R/S are controlled through a 2-wire serial bus.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. A time/date-programmable ALARM output completes the features list for the real-time clock section of the PT7C4908. The alarm function can also be used in a polled mode by periodically reading the alarm out status bit in the minutes register.

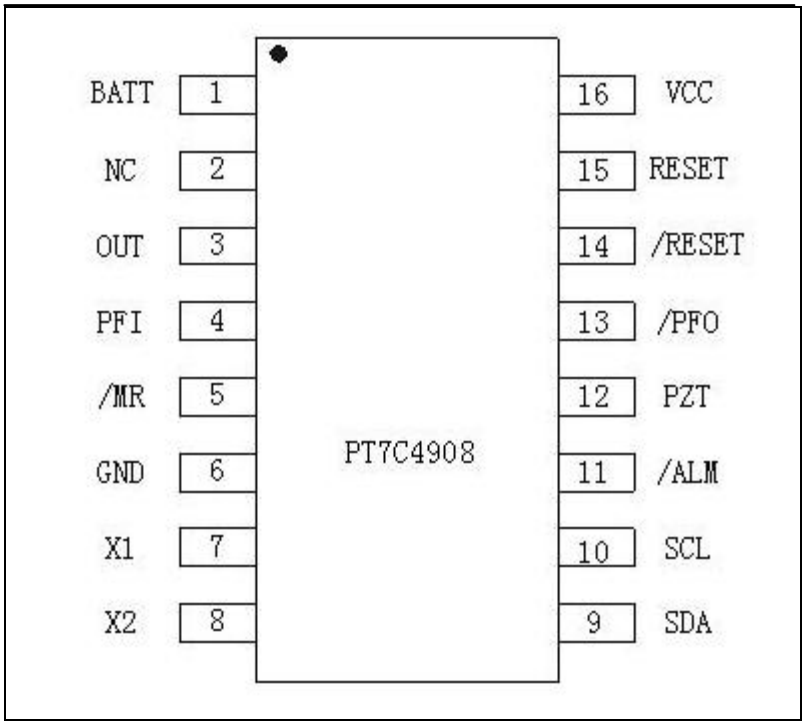
A built-in µP supervisor with an open-drain reset ensures the µP powers up in a known state. A reset threshold is available for 3V or 3.3V supplies. The piezo transducer output, PZT, is register selectable for one of four frequencies, can be turned on and off through a register bit, or selected to go on when the /ALM, alarm output, goes active.

The PT7C4908 are available in a 16-pin TSSOP package and operate over the -40℃ to +85℃ temperature range.

Application

- Point-of-Sale Equipment
- Programmable Logic Controller
- Handheld Instruments
- Medical Instrumentation

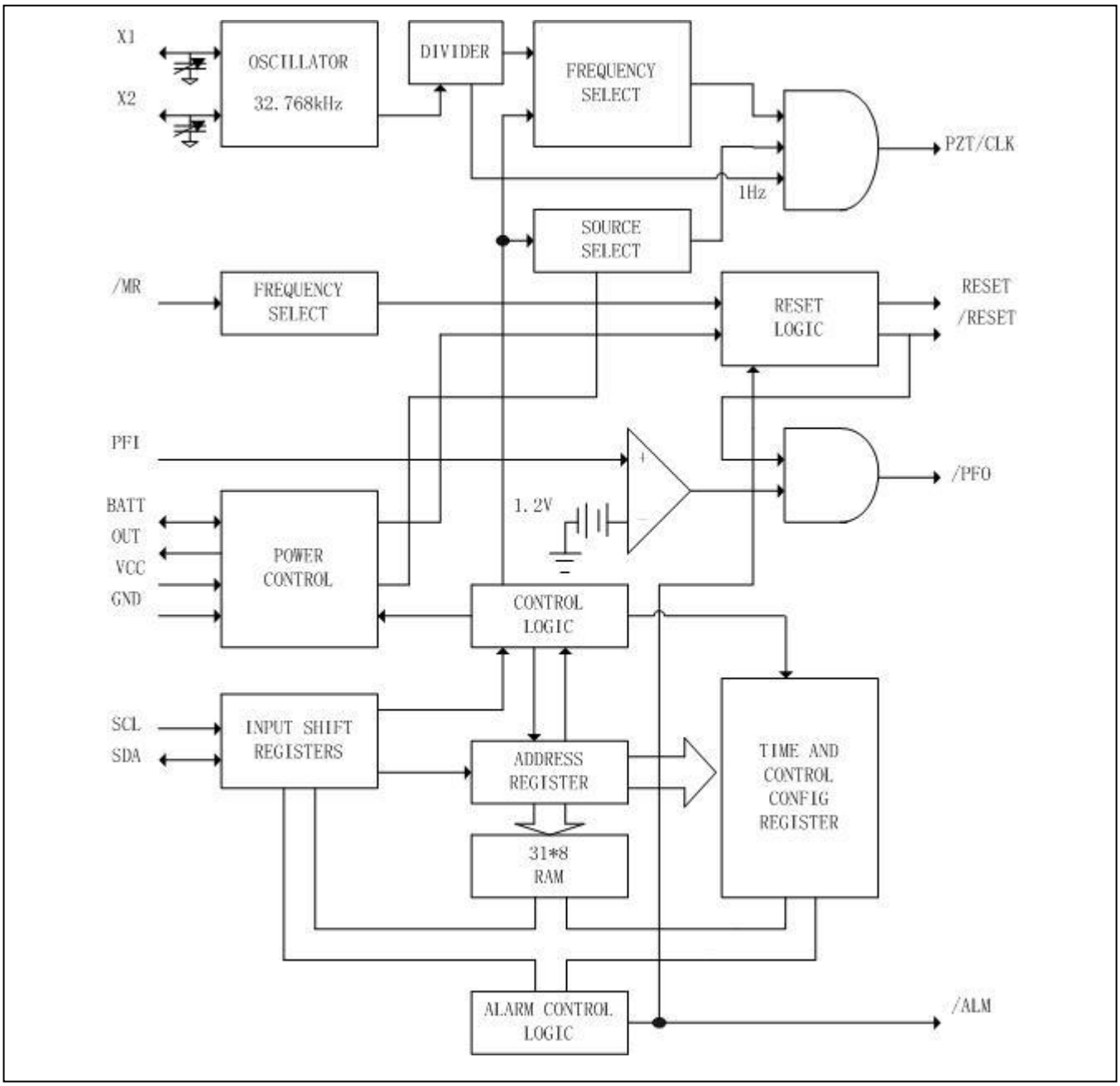
Pin Assignment



Pin Description

Pin no.	Pin	Type	Description
1	BATT	I	Backup Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, OUT connects to BATT. Connect BATT to GND if no backup battery supply is used.
2	NC	-	No connected.
3	OUT	O	Supply Output for CMOS RAM or Other ICs Requiring Use of Backup Battery Power. Bypass to GND with at least a 0.1μF capacitor.
4	PFI	I	Power-Fail Comparator Input. For monitoring external power supplies.
5	/MR	I	Manual Reset Input. The active-low input has an internal pullup resistor. Internal debouncing circuitry ensures noise immunity. Leave open if unused.
6	GND	-	Ground
7	X1	I	32.768kHz Crystal Pin; Oscillator Input
8	X2	O	32.768kHz Crystal Pin; Oscillator Output
9	SDA	I/O	Serial Data Line. Data input/output connection for the 2-wire serial interface.
10	SCL	I	Serial Clock Line. Clock input connection for the 2-wire serial interface.
11	/ALM	O	Alarm Output. Open drain, active low.
12	PZT	O	Piezo Transducer Output. Push-pull Piezo transducer output.
13	/PFO	O	Power-Fail Comparator Output. Push-pull active low.
14	/RESET	O	Open-Drain, Active-Low Reset Output
15	RESET	O	Push-Pull, Active-High Reset Output. Complement of /RESET.
16	VCC	I	Main Supply Input. Bypass to GND with at least a 0.01μF capacitor.

Function Block



Maximum Ratings

Storage Temperature……..- 65°C to +150°C
Ambient Temperature with Power Applied……-40 °C to +85 °C
BATT or Vcc……- 0.3 to +6.0V
OUT, ALM, SCL, SDA, PFO, RESET.…… - 0.3 to +6.0V
All other Pins…….……..- 0.3 to (V_{SUP} + 0.3V)
(Where V_{SUP} is greater of V_{BATT} or V_{CC})
Input Current Vcc……500mA
Input Current BATT……100mA
Input Current GND……20mA
Output Current OUT……450mA
Output Current(All other optputs)……20mA
Power Dissipation (TA = +70 ℃)…… 727mW
(QSOP-20 package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

T_A = -40 to +85 ℃, V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, unless otherwise noted. Typical values are at T_A = +25 ℃.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	PT7C4908R (Note 3)		2.7	-	3.3	V
		PT7C4908S (Note 3)		3.0	-	3.6	
Operating Voltage Range BATT	V_{BATT}	PT7C4908R (Note 4)		2.0	-	3.6	V
		PT7C4908S (Note 4)		2.0	-	3.6	
BATT Current (Note 5)	I_{BATT}	Crystal fail-circuit disabled	V_{BATT} = 2V, V_{CC} = 0V	-	0.30	0.75	µA
			V_{BATT} = 3V, V_{CC} = 0V	-	0.32	0.95	
			V_{BATT} = 3.6V, V_{CC} = 0V	-	0.34	1.1	
Timekeeping Current (Note 5)	I_{BATT}	Crystal fail-circuit enabled	V_{BATT} = 2V, V_{CC} = 0V	-	0.32	0.75	µA
			V_{BATT} = 3V, V_{CC} = 0V	-	0.34	0.95	
			V_{BATT} = 3.6V, V_{CC} = 0V	-	0.36	1.1	
Active Supply Current (Note 6)	I_{CCA}	PZT disabled, crystal-disabled	V_{CC} = 3.3V, V_{BATT} = 0V	-	20	140	µA
			V_{CC} = 3.6V, V_{BATT} = 0V	-	22	150	
Standby Current (Note 5)	I_{CCS}	PZT disabled, crystal-disabled	V_{CC} = 3.3V, V_{BATT} = 0V	-	7	9	µA
			V_{CC} = 3.6V, V_{BATT} = 0V	-	7	9	
Standby Current (Note 5)	I_{CCS}	Crystal fail-circuit enabled	V_{CC} = 3.3V, V_{BATT} = 0V	-	6	18	µA
			V_{CC} = 3.6V, V_{BATT} = 0V	-	6	25	
Trickle-Charge Diode Voltage Drop (Two Diodes)	-	-		-	1.2	-	V
Trickle Charge Resistors	R1	-		-	1.7	-	kΩ
	R2	-		-	2.8	-	
	R3	-		-	5.0	-	

To be continued.

Continued.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT							
OUT in Battery-Backup Mode (Note 4)	V_{OUT}	V_{BATT} = 3.0V, V_{CC} = 0V, I_{OUT} = 80mA		V_{BATT} -0.15	V_{BATT} - 0.1	-	V
		V_{BATT} = 2.0V, V_{CC} = 0V, I_{OUT} = 40mA		V_{BATT} -0.1	V_{BATT} - 0.05	-	
OUT in V_{CC} Mode (Note 4)	V_{OUT}	V_{CC} = 3.0V, V_{BATT} = 0V, I_{OUT} = 100mA		V_{CC} - 0.15	V_{CC} - 0.1	-	V
		V_{CC} = 2.7V, V_{BATT} = 0V, I_{OUT} = 50mA		V_{CC} – 0.1	V_{CC} - 0.05	-	
V_{BATT} to V_{CC} Switch over Threshold	V_{TRU}	Power-up (V_{CC} < V_{RST}) switch from V_{BATT} to V_{CC} (Note 7)		-	V_{BATT} + 0.05	-	V
V_{CC} to V_{BATT} Switchover Threshold	V_{TRD}	Power-down (V_{CC} < V_{RST}) switch from V_{CC} to V_{BATT} (Note 7)		-	V_{BATT} - 0.05	-	V
MANUAL RESET INPUT							
/MR Input Threshold	V_{IL}	-		-	-	0.3 ×V_{CC}	V
	V_{IH}	-		0.7 ×V_{CC}	-	-	
/MR Internal Pullup Resistance	-	-			50	-	kΩ
/MR Minimum Pulse Width	-	-		1	-	-	µs
/MR Glitch Immunity	-	(Note 8)		-	-	50	ns
/MR to Reset Delay	-	(Note 8)		-	200	350	ns
POWER-FAIL INPUT AND POWER-FAIL OUTPUT							
PFI Input Threshold	V_{PFT}	V_{CC} = $V_{CC(MIN)}$		1.19	1.27	1.31	V
PFI Input Current	-	-		-100	+2	+100	nA
PFI to PFO Delay	-	(Note 8)	PFI rising	0.06	0.2	2.2	µs
			PFI falling	2.4	5	12	
PFI Hysteresis	V_{PFH}	PFI rising		-	30	-	mV
/PFO Output Voltage High	V_{OH}	I_{SOURCE} = 200µA, PFI = V_{CC} = $V_{CC(MIN)}$		0.9 ×V_{CC}	-	-	V
/PFO Output Voltage Low	V_{OL}	I_{SINK}= 1.2mA, V_{BATT}= 2V, PFI = V_{CC} = 0V		-	-	0.2	V
PZT OUTPUT							
PZT Output Short-Circuit Current (V_{CC} Must Be > V_{RST} for PZT to Be Active)	I_{PZT}	PT7C4908R	Sink current	5	-	18	
			Source current	5	-	20	
		PT7C4908S	Sink current	6	-	20	
			Source current	6.5	-	25	
PZT Frequency 1	PZT_{f1}	-		-	1024	-	Hz
PZT Frequency 2	PZT_{f2}	-		-	2048	-	Hz
PZT Frequency 3	PZT_{f3}	-		-	4096	-	Hz
PZT Frequency 4	PZT_{f4}	-		-	8192	-	Hz
PZT Off-Leakage Current	I_{OLKG}	-		-1	-	+1	µA

To be continued.

Continued.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ALARM OUTPUT							
/ALM Output Low Voltage	V_{OL}	V_{BATT} = 2.0V, V_{CC} = 0V, I_{OL} = 3mA		-	-	0.2	V
		V_{CC} = 2.7V, I_{OL} = 5mA, V_{BATT} = 0V		-	-	0.25	
/ALM Off-Leakage Current	I_{OLKG}	-		-1	-	+1	µA
RESET FUNCTION							
Reset Threshold	V_{RST}	PT7C4909S/10S		2.80	2.93	3.00	V
		PT7C4909R/10R		2.50	2.63	2.70	
V_{RST} Hysteresis	V_{HYST}	-		-	10	-	mV
V_{CC} Falling Reset Delay		V_{CC} falling from $V_{RST(MAX)}$ to $V_{RST(MIN)}$ at 10V/ms, measured from the beginning of V_{CC} falling to RESET asserting high		-	10	50	µs
Reset Active Timeout Period	t_{RP}	-		140	200	280	ms
/RESET Output Low Voltage	V_{OL}	Reset asserted	I_{OL} = 1.6mA, V_{BATT} = 2.0V, V_{CC} = 0V	-	-	0.2	V
/RESET Off-Leakage Current	I_{LKG}	-		-1	-	+1	µA
RESET Output High Voltage	V_{OH}	Reset asserted	I_{OH} = 20µA, V_{CC} = 1.0V, V_{BATT} = 0V	0.8 ×V_{CC}	-	-	V
			I_{OH} = 1mA, V_{CC} = 2V, V_{BATT} = 0V	0.9 ×V_{CC}	-	-	
RESET Output Low Voltage	V_{OL}	V_{CC} = $V_{CC(MIN)}$, I_{OL} = 1.6mA		-	0.032	0.1	V
2-WIRE DIGITAL INPUTS (SCL, SDA) ($V_{CC(MIN)}$< V_{CC} < $V_{CC(MAX)}$)							
Input High Voltage	V_{IH}	-		0.7 ×V_{CC}	-	-	V
Input Low Voltage	V_{IL}	-		-	-	0.3 ×V_{CC}	V
Input Hysteresis	V_{HYS}	-		-	0.05 ×V_{CC}	-	V
Input Leakage Current		V_{IN}= GND or V_{CC}		-1	-	+1	µA
Input Capacitance		(Note 8)		-	-	10	pF
Output Low Voltage	V_{OL}	I_{OL} = 4mA, V_{CC} = $V_{CC(MIN)}$		-	-	0.4	V

AC Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40℃ to +85℃, unless otherwise noted.) (Notes 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE BUS TIMING						
SCL Clock Frequency	f_{SCL}	(Note 9)	0.32	-	400.00	kHz
Bus Timeout	$t_{TIMEOUT}$	-	1	-	2	s
Bus Free Time Between STOP and START Condition	t_{BUF}	-	1.3	-	-	µs
Hold Time After (Repeated) START Condition; After This Period, the First Clock Is Generated	$t_{HD:STA}$	-	0.6	-	-	µs
Repeated START Condition Setup Time	$t_{SU:STA}$	-	0.6	-	-	µs
STOP Condition Setup Time	$t_{SU:STO}$	-	0.6	-	-	µs
Data Hold Time	$t_{HD:DAT}$	(Notes 10, 11)	0	-	0.9	µs
Data Setup Time	$t_{SU:DAT}$	-	100	-	-	ns
SCL Low to Data Out Valid	$t_{VD:DAT}$	(Note 8)	50	-	-	ns
SCL Low Period	t_{LOW}	-	1.3	-	-	µs
SCL High Period	t_{HIGH}	-	0.6	-	-	µs
SCL/SDA Rise Time	t_R	(Note 12)	20 + 0.1*C_B	-	300	ns
SCL/SDA Fall Time (Receiving)	t_F	(Notes 12, 13)	20 + 0.1*C_B	-	300	ns
SCL/SDA Fall Time (Transmitting)	t_F	(Notes 12, 13)	20 + 0.1*C_B	-	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 8)	-	-	50	ns
Capacitive Load of Each Bus Line	C_B	-	-	-	400	pF

Note 1: V_{RST} is the reset threshold for V_{CC}.
Note 2: All parameters are 100% tested at T_A = +85℃. Limits over temperature are guaranteed by design and not production tested.
Note 3: 2-wire serial interface is operational for $V_{CC} > V_{RST}$.
Note 4: See the *Function Details* section (BATT function).
Note 5: I_{BATT} and I_{CCS} are specified with SDA and SCLK pulled high, OUT floating, and /CE_OUT floating.
Note 6: 2-wire serial interface operating at 400kHz, SDA pulled high.
Note 7: For OUT switch over to BATT, V_{CC} must fall below V_{RST} and V_{BATT}. For OUT switchover to V_{CC}, V_{CC} must be above V_{RST} or above V_{BATT}.
Note 8: Guaranteed by design. Not production tested.
Note 9: Due to the 2-wire bus timeout feature, there is a minimum specification on the SCL clock frequency based on a 31-byte burst-mode transaction to RAM. See the *Timeout Feature* section.
Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
Note 11: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 12: C_B = total capacitance of one bus line in pF.
Note 13: The maximum t_F for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_F is specified at 250ns. This allows series protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

Function Description

Overview of Functions

The PT7C4908R/S contain eight 8-bit timekeeping registers, two burst address registers, a trickle charge register, a control register, a configuration register, an alarm configuration register, and seven alarm threshold
registers, all controlled through a 2-wire serial interface. Refer to PT7C4908 block diagram.
The OUT pin supplies voltage for CMOS RAM or other ICs requiring the use of backup battery power. When V_{CC} rises above the reset threshold (V_{RST}) or above V_{BATT}, OUT is connected to V_{CC}. When V_{CC} falls below V_{RST} and V_{BATT}, BATT is connected to OUT. If enabled, an on-board trickle charger charges BATT from V_{CC}.
BATT can act as a backup supply from either a battery or SuperCap™.
There are two reset outputs, /RESET and RESET. They become active while V_{CC} is below the reset threshold(V_{RST}) or while manual reset (/MR) is held low, and for t_{RP} after /MR goes high, V_{CC} rises above the reset threshold. Reset thresholds are available for 3V and 3.3V applications. /MR is internally pulled high and contains debounce circuitry to accommodate a manual pushbutton reset switch.
A power-fail comparator is available to monitor other system voltages through PFI and report the status through /PFO. If the PT7C4909/PT7C4910 are in reset, /PFO is low; otherwise, it is high as long as PFI is greater than 1.27V (typ).
The piezo transducer drive output (PZT) has register selectable frequencies of 1.024kHz, 2.048kHz, 4.096kHz, or 8.192kHz. This output can be selected to become active when the alarm is triggered or can be independently controlled through the configuration register. When activated, the PZT outputs a frequency with an attention-getting 1Hz duty cycle of 50% on and 50% off.
An on-chip crystal oscillator maintaining circuit, for use with a 32.768kHz crystal, provides the clock for timekeeping functions.

Registers

1. Register Address Definition

REGISTER ADDRESS

FUNCTION	A7	A6	A5	A4	A3	A2	A1	A0
SEC	1	0	0	0	0	0	0	RD /W
MIN	1	0	0	0	0	0	1	RD /W
HR	1	0	0	0	0	1	0	RD /W
DATE	1	0	0	0	0	1	1	RD /W
MONTH	1	0	0	0	1	0	0	RD /W
DAY	1	0	0	0	1	0	1	RD /W
YEAR	1	0	0	0	1	1	0	RD /W
CONTROL	1	0	0	0	1	1	1	RD /W
TRICKLE CHARGER	1	0	0	1	0	0	0	RD /W
CENTURY	1	0	0	1	0	0	1	RD /W
ALARM CONFIG	1	0	0	1	0	1	0	RD /W
TEST CONFIG	1	0	0	1	0	1	1	RD
1Hz MODULATION ENABLE	1	0	1	1	0	0	0	/W
TEST REGISTER 2	1	0	1	1	0	0	1	/W
DIGITAL OFFSET ADJUST	1	0	1	1	1	0	0	RD /W
OSCILLATOR CAP ADJUST	1	0	1	1	1	1	0	RD /W

REGISTER DEFINITION

FUNCTION	VALUE	D7	D6	D5	D4	D3	D2	D1	D0
SEC	00-59	0	10 SEC			1 SEC			
	POR STATE	0	0	0	0	0	0	0	0
MIN	00-59	ALM OUT	10 MIN			1 MIN			
	POR STATE	0	0	0	0	0	0	0	0
HR	00-23	12/24	0	10 HR	10 HR	1 HR			
	01-12	1/0		A/P 0/1					
	POR STATE	0	0	0	0	0	0	0	0
DATE	01-28/29 01-30 01-31	0	0	10 DATE		1 DATE			
	POR STATE	0	0	0	0	0	0	0	1
MONTH	01-12	0	0	0	10 M	1 MONTH			
	POR STATE	0	0	0	0	0	0	0	1
DAY	01-07	0	0	0	0	0	WEEKDAY		
	POR STATE	0	0	0	0	0	0	0	1
YEAR	00-99	10 YEAR				1 YEAR			
	POR STATE	0	1	1	1	0	0	0	0
CONTROL		WP	0	0	0	0	0	0	0
	POR STATE	0	0	0	0	0	0	0	0
TRICKLE CHARGER		TCS	TCS	TCS	TCS	DS	DS	RS	RS
	POR STATE	0	0	0	0	0	0	0	0
CENTURY	00-99	1000 YEAR				100 YEAR			
	POR STATE	0	0	0	1	1	0	0	1
ALARM CONFIG		0	YEAR	DAY	MONTH	DATE	HOUR	MIN	SEC
	POR STATE	0	0	0	0	0	0	0	0
TEST CONFIG		0	0	0	0	0	1	1	1
	POR STATE	0	0	0	0	0	1	1	1
1Hz MODULATION ENABLE		0	0	0	0	0	0	0	EN_1Hz
	POR STATE	0	0	0	0	0	0	0	0
TEST REGISTER 2									
DIGITAL OFFSET ADJUST		D7	D6	D5	D4	D3	D2	D1	D0
	POR STATE	0	0	0	0	0	0	0	0
OSCILLATOR CAP ADJUST		D7	D6	D5	D4	D3	D2	D1	D0
	POR STATE	1	1	0	0	1	1	0	0

NOTE: POR STATE DEFINES POWER-ON RESET STATE OF REGISTER CONTENTS. THE TEST CONFIG REGISTER IS A READ-ONLY REGISTER.

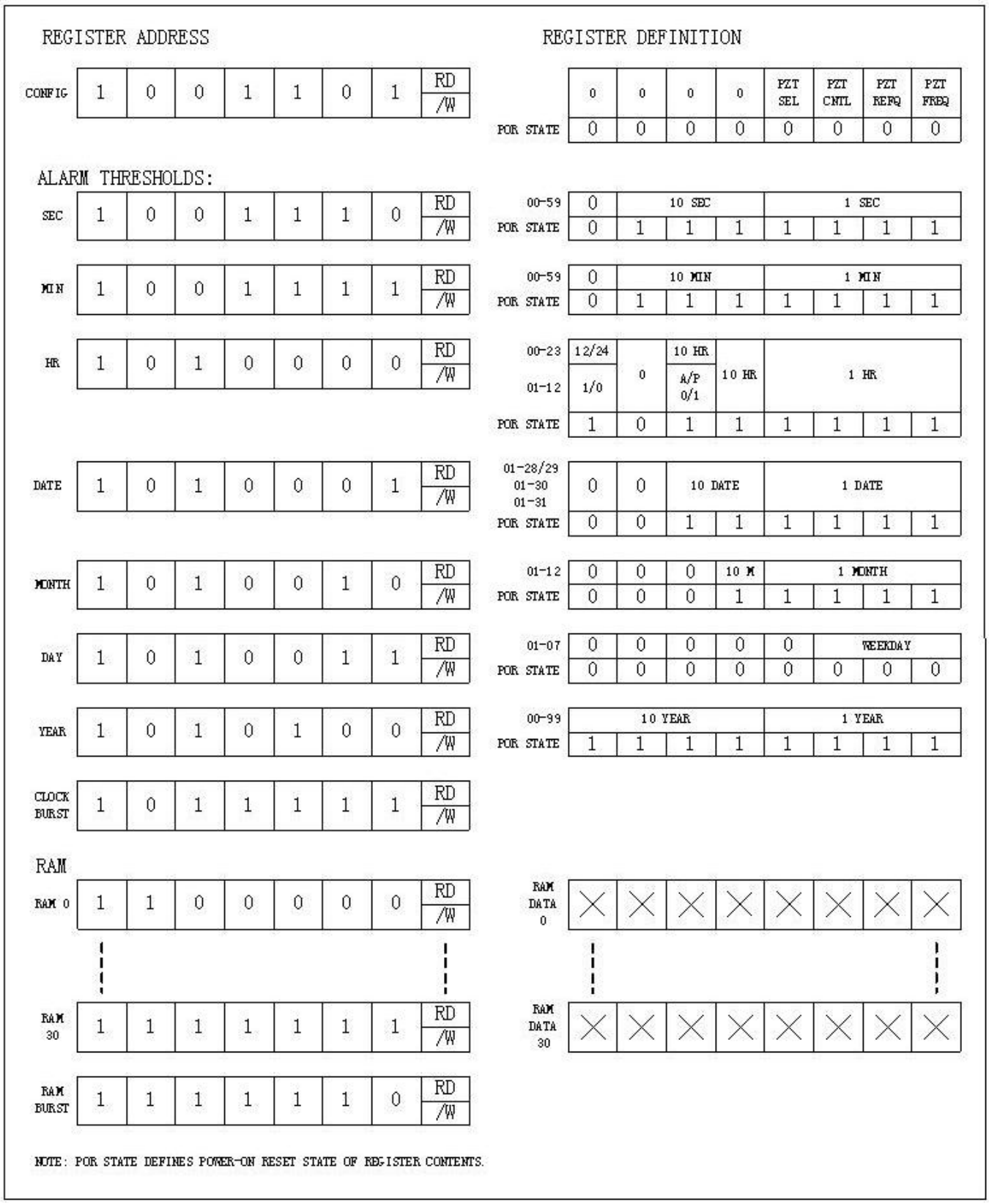


Figure 1 Register Address Definition

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2. Hex Register Address/Description

Table 2. Hex Register Address/Description

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)	POR CONTENTS (BCD)
80	81	Seconds	00	00
82	83	Minutes	00	00
84	85	Hours	00	00
86	87	Date	01	01
88	89	Month	01	01
8A	8B	Day	01	01
8C	8D	Year	70	70
8E	8F	Control	00	00
90	91	Trickle charger	00	00
92	93	Century	19	19
94	95	Alarm configuration	00	00
—	97	Test configuration*	07	07
9A	9B	Configuration	00	00
9C	9D	Seconds alarm threshold	7F	7F
9E	9F	Minutes alarm threshold	7F	7F
A0	A1	Hours alarm threshold	BF	BF
A2	A3	Date alarm threshold	3F	3F
A4	A5	Month alarm threshold	1F	1F
A6	A7	Day alarm threshold	00	00
A8	A9	Year alarm threshold	FF	FF
B0	--	Test register1(write-only)	N/A	N/A
B2	--	Test register2(write-only)	N/A	N/A
B8	B9	Digital offset adjust	00	00
BC	BD	Oscillator capacitor adjust	CC	CC
BE	BF	Clock burst	N/A	N/A
C0	C1	RAM 0	Indeterminate	Indeterminate
C2	C3	RAM 1	Indeterminate	Indeterminate
C4	C5	RAM 2	Indeterminate	Indeterminate
C6	C7	RAM 3	Indeterminate	Indeterminate
C8	C9	RAM 4	Indeterminate	Indeterminate
CA	CB	RAM 5	Indeterminate	Indeterminate
CC	CD	RAM 6	Indeterminate	Indeterminate
CE	CF	RAM 7	Indeterminate	Indeterminate
D0	D1	RAM 8	Indeterminate	Indeterminate
D2	D3	RAM 9	Indeterminate	Indeterminate
D4	D5	RAM 10	Indeterminate	Indeterminate
D6	D7	RAM 11	Indeterminate	Indeterminate
D8	D9	RAM 12	Indeterminate	Indeterminate
DA	DB	RAM 13	Indeterminate	Indeterminate
DC	DD	RAM 14	Indeterminate	Indeterminate

To be continued.

Continued.

WRITE (HEX)	READ (HEX)	DESCRIPTION	POR CONTENTS (HEX)	POR CONTENTS (BCD)
DE	DF	RAM 15	Indeterminate	Indeterminate
E0	E1	RAM 16	Indeterminate	Indeterminate
E2	E3	RAM 17	Indeterminate	Indeterminate
E4	E5	RAM 18	Indeterminate	Indeterminate
E6	E7	RAM 19	Indeterminate	Indeterminate
E8	E9	RAM 20	Indeterminate	Indeterminate
EA	EB	RAM 21	Indeterminate	Indeterminate
EC	ED	RAM 22	Indeterminate	Indeterminate
EE	EF	RAM 23	Indeterminate	Indeterminate
F0	F1	RAM 24	Indeterminate	Indeterminate
F2	F3	RAM 25	Indeterminate	Indeterminate
F4	F5	RAM 26	Indeterminate	Indeterminate
F6	F7	RAM 27	Indeterminate	Indeterminate
F8	F9	RAM 28	Indeterminate	Indeterminate
FA	FB	RAM 29	Indeterminate	Indeterminate
FC	FD	RAM 30	Indeterminate	Indeterminate
FE	FF	RAM Burst	N/A	N/A

Crystal Selection

A 32.768kHz crystal is connected to the PT7C4908 through pins 9 and 10 (X1 and X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF or 12pF where the capacitive load is included in the PT7C4908. When designing the PC board, keep the crystal as close to the X1 and X2 pins as possible. Keep the trace lengths short and small and place a guard ring around the crystal and connect the ring to GND to reduce capacitive loading and prevent unwanted noise pickup. Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling. Finally, an additional local ground plane on an adjacent PC board layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane should be isolated from the regular PC board ground plane, should be no larger than the perimeter of the guard ring, and connected to the GND pin of the PT7C4908. Ensure that this ground plane does not contribute to significant capacitance between signal line and ground on the connections that run from X1 and X2 to the crystal.
Some crystal manufacturers and part numbers for their SMT, 32.768kHz watch crystals that require 6pF or 12pF loads are listed in Table 3. In addition, these manufacturers offer other package options depending upon the specific application considerations.

Table 3 Crystal Manufacturers and Part Numbers

MANUFACTURER	PART	TEMP RANGE (℃)	CL (pF)		+25℃ FREQUENCY TOLERANCE (ppm)
Caliber Electronics	AWS2A-32.768KHz, AWS2B-32.768KHz	-20 to +70	12	6	±20
ECS INC International	ECS-.327-6.0-17	-10 to +60	12	6	±20
Fox Electronics	FSM327	-40 to +85	12	6	±20
M-tron	SX2010/ SX2020	-20 to +75	12	6	±20
Raltron	RSE-32.768-6-C-T	-10 to +60	12	6	±20

Timekeeping accuracy of the PT7C4908 is dependent on the frequency stability of the external crystal. To determine frequency stability, use the following equations:

$$\Delta f = f * k * (T_0 - T)^2$$

where:
Δf = change in frequency from +25 ℃ (Hz)
f = nominal crystal frequency (Hz)
k = parabolic curvature constant (-0.035 ±0.005ppm/ ℃^{2} for 32.768kHz watch crystals)
T_0 = turnover temperature (+25 ℃ ±5 ℃ for 32.768kHz watch crystals)
T = temperature of interest (℃)
For example: What is the worst-case change in oscillator frequency from +25 ℃ ambient to +45 ℃ ambient?
Δf_{drift} = 32.768Hz * (-0.04ppm/ ℃)^2 * (20 ℃ - 45 ℃)^2 = -0.8192Hz

What is the worst-case timekeeping error per second?
1) Error due to temperature drift:
Δt_{drift} = {[1 / [(f + Δf_{drift}) / 32,768]] - 1s}/1s = {[1 / [(32.768Hz - 0.8192Hz) / 32.768]] - 1s}/1s = 0.000025s/s
2) Error due to +25 ℃ initial crystal tolerance of ±20ppm:
$\Delta f_{initial}$ = 32.768Hz * (-20ppm) = -0.65536Hz
$\Delta t_{initial}$ = {[1 / [(f + $\Delta f_{initial}$) / 32.768]] - 1}/1s
$\Delta t_{initial}$ = {[1 / [(32.768 - 0.65536)/32.768]] - 1} /1s = 0.000020s/s
3) Total timekeeping error per second:
$\Delta t_{total} = \Delta t_{drift} + \Delta t_{initial}$
Δt_{total} = 0.000025s / s + 0.000020s / s = 0.000045s/s

After 1 month that translates to:
Δt = (31day) * (24hr/day) * (60min/hr) * (60s/min) * (0.000045s/s) = 120.158s
Total worst-case timekeeping error at the end of 1 month at +45 ℃ is approximately 120s or 2min (assumes negligible parasitic layout capacitance).

Table 4. Acceptable Quartz Crystal Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Frequency	f	-	32.768	-	kHz
Equivalent series resistance (ESR)	R_S	-	-	60	kΩ
Parallel load capacitance	C_L	-	6	-	pF
		-	12	-	
Q factor	Q	40,000	-	-	-

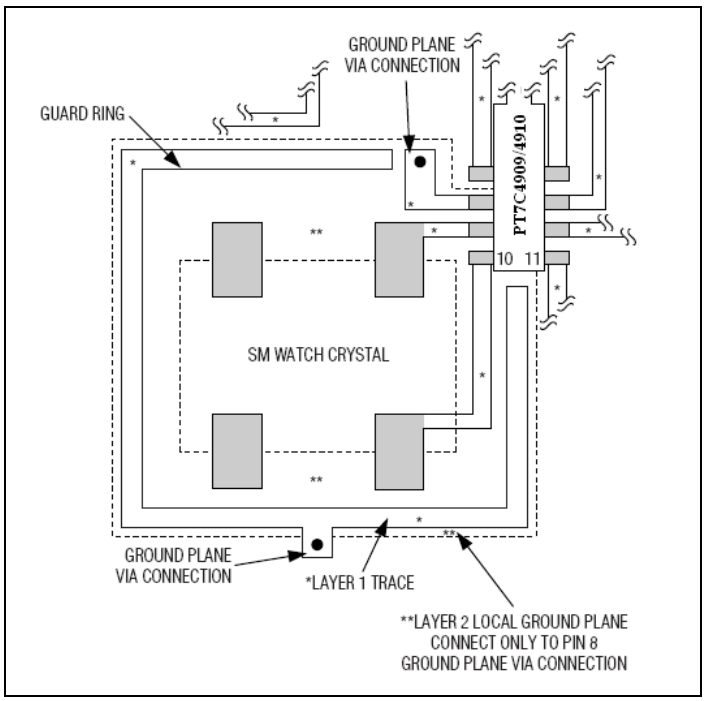


Figure 2 Recommended Layout for Crystal

Control Register (Write Protect Bit)

Bit 7 of the control register is the write protect bit. The lower 7 bits (bits 0–6) are forced to zero and always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

Hours Register (AM-PM/12-24 Mode)

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20h–23h).

Clock Burst

Addressing the clock burst register specifies burst mode operation. In this mode, the first seven clock/calendar registers and the control register can be consecutively read or written starting with bit 7 of address BEh for a write and BFh for a read. If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer occurs to any of the seven clock/calendar registers or the control register. When writing to the clock registers in the burst mode, all eight registers must be written in order for the data to be transferred. In addition, the WP bit in the control register must be set to zero prior to a clock burst write.

RAM

The static RAM is 31 bytes addressed consecutively in the RAM address space. Even address/commands (C0h–FCh) are used for writes, and odd address/commands (C1h–FDh) are used for reads. The contents of the RAM are static and remain valid for VOUT down to 1.5V (TYP).

RAM Burst

Addressing the RAM burst register specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written starting with bit 7 of address FEh for a write and FFh for a read. When writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to is transferred to RAM regardless of whether all 31 bytes are written.

Trickle Charger Register

The trickle charge register controls the trickle charger characteristics of the PT7C4908. The trickle charger functional schematic (Figure 3) shows the basic components of the trickle charger. Table 6 details the bit settings for trickle charger control. Trickle charge selection (TCS) bits D7–D4 control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns disable the trickle charger. The PT7C4908 powers up with the trickle charger disabled. The diode select (DS) bits (D3–D2) select whether two diodes or no diodes are connected between VCC and BATT. If DS is 10, no diode is selected; if DS is 01, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independent of the state of the TCS bits. The RS bits (D1–D0) select the resistor that is connected between VCC and BATT. If both RS bits are set to zero, the trickle charger is disabled, regardless of any other bit states in the trickle charger register. RS bits set to 10 select a 1.7K, 01 selects 2.9K, and 11 select 5K.
Diode and resistor selection is determined by the user, according to the maximum current desired for the battery or Super Cap charging. The maximum charging current can be calculated as shown in the following example. Assume that a system power supply of 3V is applied to VCC and a SuperCap is connected to BATT. Also assume that the trickle charger has been enabled with no diode and resistor R1 between VCC and BATT. The maximum current IMAX would therefore be calculated as follows:

$IMAX = 3.0V/R1 \approx 3.0V/1.7k\Omega \approx 1.76mA$

As the Super Cap charges, the voltage difference between VCC and VBATT decreases, and therefore the charge current decreases.

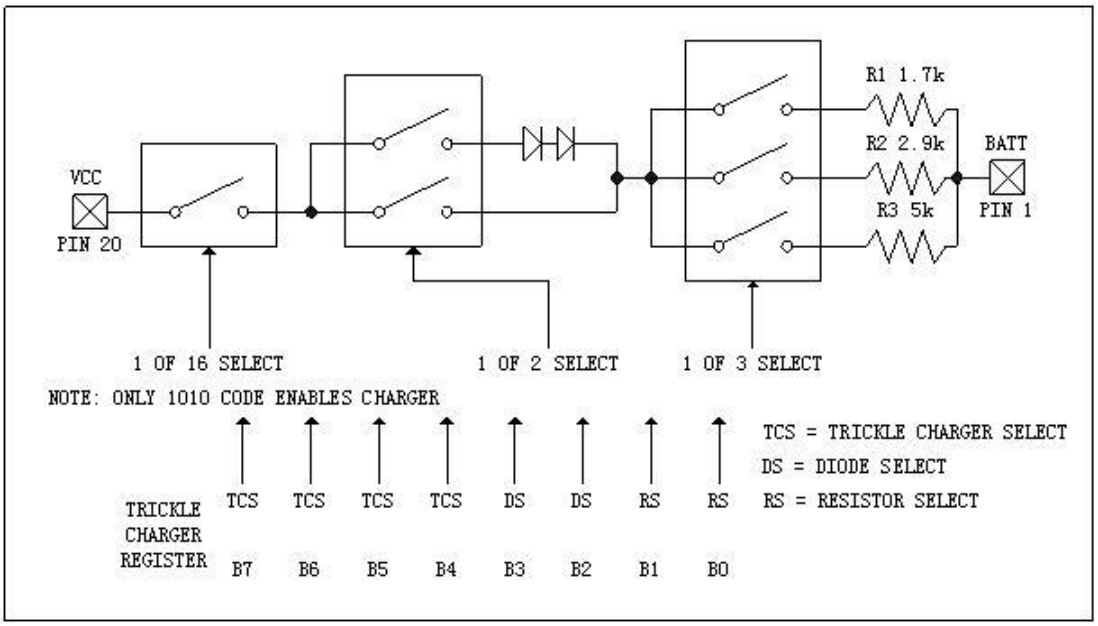


Figure 3 Trickle charger functional schematic

Table 5 Trickle Charger Register Control

D7	D6	D5	D4	D3	D2	D1	D0	ACTION
TCS	TCS	TCS	TCS	DS	DS	RS	RS	
×	×	×	×	0	0	×	×	Trickle charger disabled
×	×	×	×	1	1	×	×	Trickle charger disabled
×	×	×	×	×	×	0	0	Trickle charger disabled
1	0	1	0	1	0	1	0	No diode selected, 1.7k selected
1	0	1	0	1	0	0	1	No diode selected, 2.9k selected
1	0	1	0	1	0	1	1	No diode selected, 5k selected
1	0	1	0	0	1	1	0	Two diode selected, 1.7k selected
1	0	1	0	0	1	0	1	Two diode selected, 2.9k selected
1	0	1	0	0	1	1	1	Two diode selected, 5k selected

OUT Function

OUT is an output supply voltage for external devices. When V_{CC} rises above the reset threshold or is greater than V_{BATT}, OUT connects to V_{CC}. When V_{CC} falls below V_{RST} and V_{BATT}, OUT connects to BATT. There is a typical V_{TRU} - V_{TRD} hysteresis associated with the switching between V_{CC} and BATT if BATT < V_{RST} and typically V_{HYST} of hysteresis if BATT > V_{RST}. Connect at least a 0.1µF capacitor from OUT to ground (GND). Switching from V_{CC} to BATT uses a break-before-make switch; a capacitor from OUT to GND prevents loss of power needed for clock data and RAM during switchover.

Oscillator Start Time

The PT7C4909/4910 oscillator typically takes 300ms to settle to its optimum operating power level after startup. To ensure the oscillator is operating, the system software should validate this by reading the seconds register. Any reading with more than 0s, from the POR value of 0s, is a validation that the oscillator is operating.

Power-On Reset (POR)

The PT7C4908 contain an integral POR circuit that ensures all registers are reset to a known state on power-up. On initial power-up, once VOUT rises above 0.75V (typ), the POR circuit releases the registers for normal operation. Should VOUT dip to less than 1.5V (typ), the contents of the PT7C4908 registers can no longer be guaranteed.

Table 6 I/O and IC sections powered from V_{CC} and BATT

DESCRIPTION	PIN NAME	POWER=V_{CC}	V_{CC}<V_{RST}	V_{CC}<V_{RST} COMMENTS	COMMENTS
Crystal Oscillator I/O	X1	Enabled	Enabled	-	-
Crystal Oscillator I/O	X2	Enabled	Enabled	-	-
Backup Power-Supply Input	BATT	N/A	N/A	-	Power pin
OUT (> of V_{CC} or BATT if V_{CC}< V_{RESET})	OUT	N/A	N/A	-	Power output pin
Manual Reset Input	/MR	Enabled	Disabled	Input ignored	-
Power-Fail Input	PFI	Enabled	Disabled	Input ignored	-
Ground	GND	N/A	N/A	-	Power pin
Active Low, Open-Drain Reset Output (-OD)	/RESET	Enabled	Enabled	Pulled low	-
Active High, Push/Pull Reset Output	RESET	Enabled	Enabled	Pulled to VCC	-
Power-Fail Output	/PFO	Enabled	Enabled	Pulled low	-
Alarm Output	/ALM	Enabled	Enabled		-
Piezo Output	PZT	Enabled	Disabled	High impedance	-
2-Wire Bus Data I/O	SDA	Enabled	Disabled	-	-
2-Wire Bus Clock	SCL	Enabled	Disabled	-	-
Main Power-Supply Input	V_{CC}	N/A	N/A	-	Power pin
Trickle Charge	-	Enabled	Disabled	-	-
FEATURES					
Crystal Oscillator	-	Enabled	Enabled	-	Supply = OUT
RAM	-	Enabled	Enabled	-	Supply = OUT
Timekeeping Registers	-	Enabled	Enabled	-	Supply = OUT
Control Registers	-	Enabled	Enabled	-	Supply = OUT
Alarm Registers	-	Enabled	Enabled	-	Supply = OUT
Power-Fail Comparator	-	Enabled	Enabled	Disabled in BATT	Supply = OUT
RESET Comparator	-	Enabled	Enabled	-	Supply = VCC
Internal Reference	-	Enabled	Enabled	-	Supply = VCC
Power Switchover	-	Enabled	Enabled	-	Supply = VCC
Piezo Dividers/Select Register	-	Enabled	Enabled	-	Supply = OUT
Trickle Charge	-	Enabled	Disabled	-	Supply = OUT

Alarm Generation Registers

The alarm function generates an ALARM when the contents of the SEC, MIN, HR, DATE, MONTH, DAY, or YEAR registers match the respective alarm threshold registers. Also, the generation of the ALARM is programmable through the alarm configuration register. The alarm configuration register can be written to with an address of 94H or it can be read with an address of 95H. The alarm configuration register definition is shown in Figure 1 (register address definition). Placing a 1 in the appropriate bit enables the /ALM and the alarm out status bit when the selected alarm threshold register contents match the respective timekeeping register contents. For example, writing 0000 0001 to the alarm configuration register causes the alarm pin to get triggered every minute (each time the contents of the seconds timekeeping register match the contents of the seconds alarm threshold register). Writing 0000 0010 causes the alarm to go on every hour (each time the contents of the minutes timekeeping register match the contents of the minutes alarm threshold register). Writing a 0100 1111 to the alarm configuration register, therefore, causes the alarm to be triggered on a specific second, of a specific minute, of a specific hour, of a specific date, of a specific year. The alarm output stays low until it is “cleared” by reading or writing to the alarm configuration register or by reading or writing to any of the alarm threshold registers.

Minutes Register (Alarm Out Status)

An alarm out status bit is available if it is desired to use the alarm function as a polled alarm instead of connecting directly to the /ALM output pin. Bit D7 in the minutes timekeeping register contains the status of the /ALM output with a 1 indicating the alarm function has triggered and zero indicating no triggered alarm.

Manual Reset Input

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. With the PT7C4908, a logic low on /MR asserts reset. Reset remains asserted while /MR is low, and for t_{RP} (Figure 4) after it returns high. /MR has an internal pull-up resistor of typically 50kΩ, so it can be left open if it is not used. Internal debounce circuitry requires a minimum low time on the /MR input of 1µs with 100ns (typ) minimum glitch immunity.

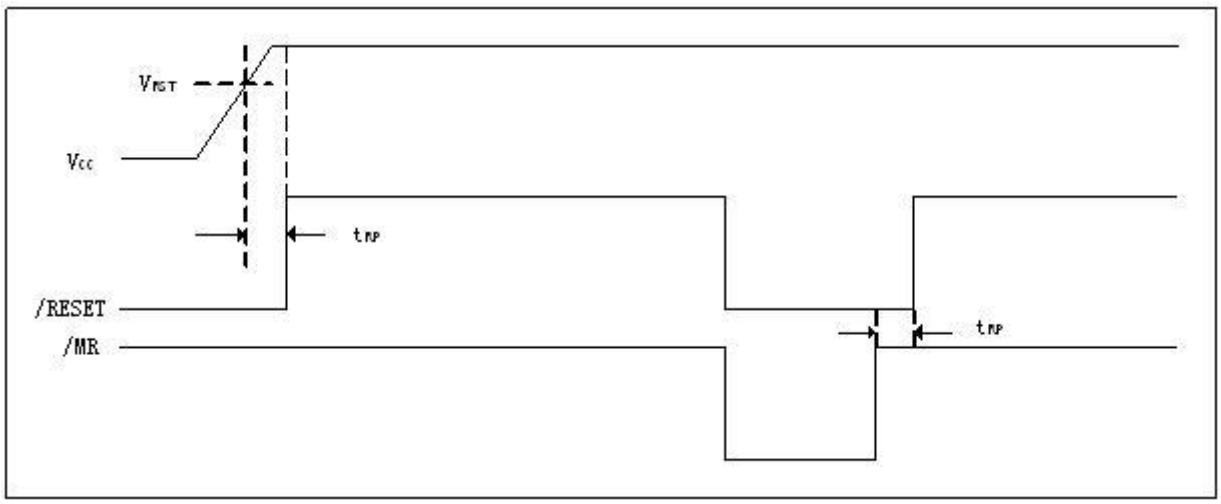


Figure 4 Manual Reset Timing

Reset Outputs

A µP's reset input starts the µP in a known state. When /RESET and RESET are active, all control inputs (/MR, /CE_IN, and the 2-wire interface) are disabled. The PT7C4908 µP supervisory circuit asserts a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. /RESET, opendrain active low, and RESET (push-pull active high) are guaranteed to be active for $0V < V_{CC} < V_{RST}$, provided V_{OUT} is greater than 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps /RESET and RESET active for the reset timeout period (t_{RP}); after this interval, /RESET becomes inactive (high) and RESET becomes inactive (low). If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET and /RESET become active. Each time RESET and /RESET are asserted, they are held active for the reset timeout period.

The PT7C4908R is optimized to monitor 3.0V ±10% power supplies. Except when /MR is asserted, reset does not occur until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the power supply falls below +2.5V.

The PT7C4908S is optimized to monitor 3.3V ±10% power supplies. Except when /MR is asserted, reset does not occur until V_{CC} falls below 3.0V (3.0V is just above 3.3V - 10%), but is guaranteed to occur before the power supply falls below 2.8V.

Negative-Going VCC Transients

The PT7C4909/4910 are relatively immune to short duration negative transients (glitches) while issuing resets to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not recommended.

Maximum transient duration vs. reset comparator overdrive shows the maximum pulse period that can occur on V_{CC} for which reset pulses are NOT generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.6V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the typical maximum pulse width a negative-going V_{CC} transient can have without causing a reset. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 60mV below the reset threshold and lasts for 60µs or less does not cause a reset pulse to be issued. A capacitor of at least 0.1µF mounted close to the V_{CC} pin provides additional transient immunity.

Interfacing to Microprocessors with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the PT7C4909/4910 /RESET or RESET outputs. If, for example, the RESET output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O. Buffer the RESET output to other system components. The positive voltage supply for the RESET pin is V_{CC}. If V_{CC} drops, then so does the V_{OH} of this pin.

Power-Fail Comparator

The PT7C4908 PFI is compared to an internal reference. If the PFI voltage is less than the power-fail threshold(V_{PFT}), /PFO goes low. The power-fail comparator is intended for use as an under voltage detector to signal a failing power supply and can monitor either positive or negative supplies using a voltage-divider to PFI. However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.
Any time $V_{CC} < V_{RST}$, /PFO is forced low, regardless of the state of PFI. Any time $V_{CC} > V_{RST}$ and /RESET is active low (during the reset timeout period), /PFO is forced high, regardless of the state of PFI. If the comparator is unused, connect PFI to V_{CC} and leave /PFO floating. Figure 5 shows PFI and /PFO timing.

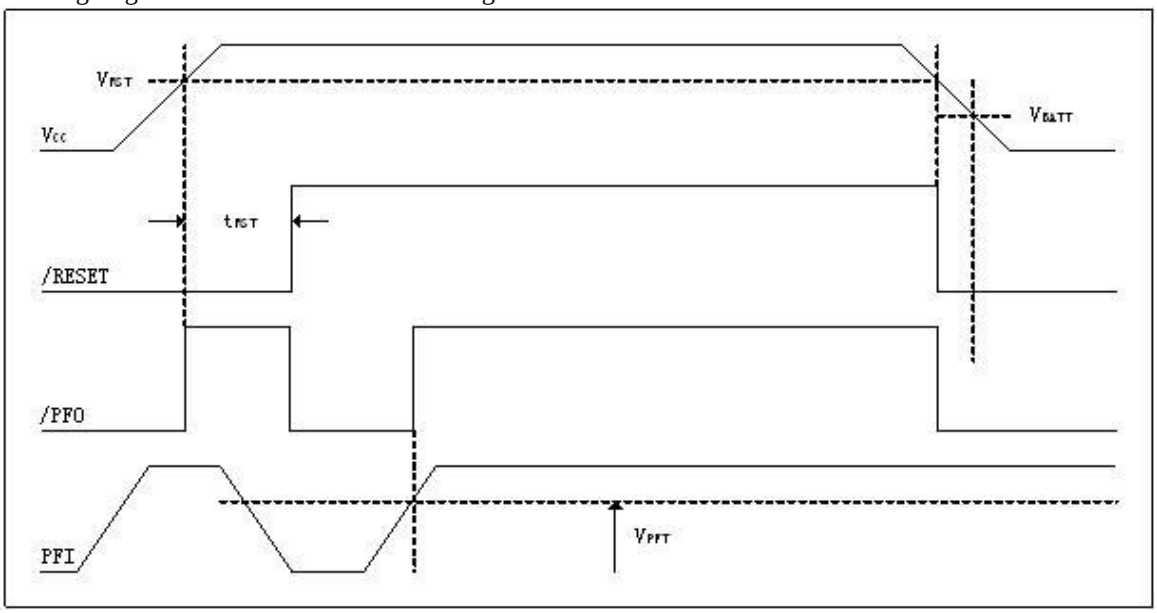


Figure 5 PFI and /PFO Timing

Piezo Transducer Output Drive

The push-pull, piezo transducer drive output, PZT, is selectable through the configuration register for frequencies of 1.024kHz, 2.048kHz, 4.096kHz, or 8.192kHz (Table 6). Bits D0 and D1 control which frequency outputs to PZT. If in battery backup mode (when V_{CC} falls below the reset threshold and below V_{BATT}), the PZT output is disabled to high impedance to prevent battery drain from the backup battery on the BATT pin.
Table 7 lists the piezo transducer control bits.
Bit D3, the PZT SEL bit, selects whether the /ALM, alarm output, controls when the selected PZT frequency is gated to PZT or whether control is given to the PZT CNTL bit, bit D2. If D3 = 1, then the /ALM controls gating of the selected PZT frequency to PZT. When the alarm is triggered, the selected frequency stays on PZT until the alarm is cleared by writing to or reading from the alarm configuration register. If D3 = 0, then the PZT CNTL bit, D2, determines when and for how long the selected frequency appears at PZT. Bit D2, the PZT CNTL bit, controls whether the selected frequency is gated to PZT, provided D3 = 0. D2 = 1 gates the selected frequency to PZT and D2 = 0 inhibits the selected frequency (PZT remains low).
Anytime a frequency is selected to be gated through to the PZT output, it is modulated by a 1Hz square wave. The PZT output then turns on for 0.5s and off for 0.5s. Since the human ear is particularly sensitive to changes in condition, switching a sound on and off makes it more noticeable than a continuous sound of the same frequency.
The PZT output swings between V_{CC} and GND through the output stage's on-resistance, R_{OUT_PZT}. To allow flexibility of the PZT output to work with many different types of piezo buzzers, R_{OUT_PZT} is designed to be as low as practical. To minimize peak currents into the piezo buzzer, an external current-limiting resistor Rs may be required. Ipeak is now equal to V_{CC} / (Rs + R_{OUT_PZT}). Rs can be adjusted to reduce the sound amplitude from the external piezo buzzer. The value of Rs varies for each application and should be chosen at the prototype design stage with the piezo buzzer installed in a cavity approximating its final housing. The typical value of R_{OUT_PZT} is calculated from V_{OUT} / I_{PZT}, where I_{PZT} is the average of the sink and source currents. Figure 6 is the piezo transducer functional diagram.

Table 7 Piezo Transducer Selectable Frequencies

D1(PZT FREQ)	D0(PZT FREQ)	PZT TYPICAL FREQUENCY (kHz)
0	0	1.024
0	1	2.048
1	0	32.768
1	1	8.192

Table 8 1Hz MODULATION ENABLE

EN_1Hz	Square wave output at PZT
0(Default)	PZT output square wave with 1Hz modulation
1	PZT output square wave without 1Hz modulation

Table 9 Piezo Transducer Control Bits

D3(PZT SEL)	D2(PZT CNTL)	CONDITION	PZT
0	0	PZT CNTL bit, D2, has control	Low
0	1	PZT CNTL bit, D2, has control	Selected frequency
1	0	/ALM has control, D2 is ignored; assume alarm triggered	Selected frequency
1	1	/ALM has control, D2 is ignored; assume alarm cleared by reading the alarm configuration register	Low

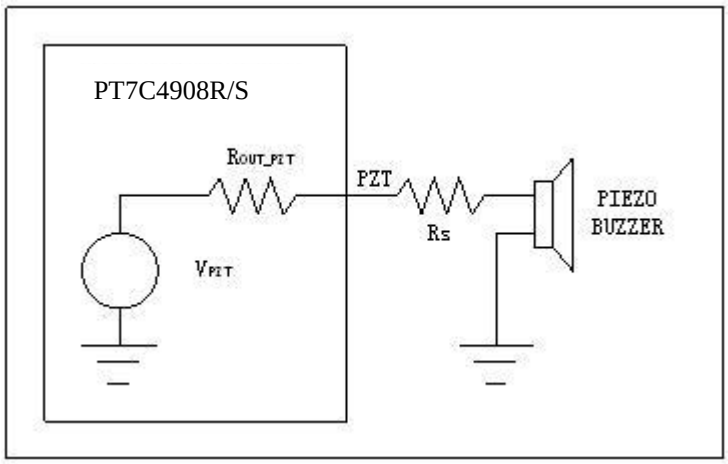


Figure 6 Piezo Transducer Functional Diagram

Test Configuration Register

This is a read-only register.

Test Register

The block implements an I²C interface controller, which can operate at a maximum frequency of 400KHz. It fully supports the four types of I²C transfer (single write, single read, burst write and burst read) as defined in the spec. Besides, this block also incorporates a test block, which implements four test modes that can be entered by first writing 0xFF to TEST REG1(address 0xB0) and then writing a specific value to TEST REG2(address 0xB2) through I²C interface.

Table 10 The four test modes and their entries by i2c write transfers list:

Test mode	Purpose of the test mode	TEST REG 1	TEST REG 2
Test reset 1	Reset all the RTC relevant registers and all the DFFs in the digital clock division chain	0XFF	0XB0
Test clock 1	Generate a test clock to replace the 16kHz clock input of the digital clock division chain	0XFF	0XA1
Test clock 2	Generate a test clock to replace the 128Hz pulse generated in the middle of the digital clock division chain	0XFF	0XA2
Test clock 3	Generate a test clock for all the timekeeping registers	0XFF	0XA3
Test clock 4	Generate a test clock to replace the 1Hz pulse generated by the digital clock division chain	0XFF	0XA4

Offset Adjust

1. Digital adjust

This block incorporates a digital clock division chain and a clock precision adjustment function. The digital clock division chain receives the 16KHz clock from the oscillator as input, and, through a series of DFFs, generates a 1Hz-periodic pulse to update the second counter in timekeeping registers. In order to speed up the clock division cycle during test, the input 16KHz clock and the 128Hz pulse in the middle of the clock division chain can be replaced by test_clock1 and test_clock2 generated by the test block in i2c control block (see the above table).

The precision of the clock generated by the division chain can be set ahead or behind through the clock precision adjustment function, if a proper adjustment data is set in register DOFFSET (0xB8). The binary encoded settings in the seven bits from F6 to F0 are used to set the precision of the clock generated from the 32768Hz oscillator up to ±189.1×10-6 in the forward (ahead) or reverse(behind) direction, in units of ±3.05×10-6. The adjustment happens once every 20 seconds (at "00","20" and "40" seconds). The adjustment amount and adjustment value are listed in the table below:

Adjustment amount	Adjustment data		bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(ppm)	Decimal	Hexadecimal	F6	F5	F4	F3	F2	F1	F0
-189.10	+63	3F h	0	1	1	1	1	1	1
-186.05	+62	3E h	0	1	1	1	1	1	0
-183.00	+61	3D h	0	1	1	1	1	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
-9.15	+4	04 h	0	0	0	0	1	0	0
-6.10	+3	03 h	0	0	0	0	0	1	1
-3.05	+2	02 h	0	0	0	0	0	1	0
OFF	+1	01 h	0	0	0	0	0	0	1
OFF	0	00 h	0	0	0	0	0	0	0
+3.05	-1	7F h	1	1	1	1	1	1	1
+6.10	-2	7E h	1	1	1	1	1	1	0
+9.15	-3	7D h	1	1	1	1	1	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
+183.00	-60	44 h	1	0	0	0	1	0	0
+186.05	-61	43 h	1	0	0	0	0	1	1
+189.10	-62	42 h	1	0	0	0	0	1	0
OFF	-63	41 h	1	0	0	0	0	0	1
OFF	-64	40 h	1	0	0	0	0	0	0

The adjustment is carried out in this way: Assume DOFFSET is set to 02h, then every 20 seconds an additional cycle of 16KHz will be added to all the clock signals in the division chain. If 03h is set, two additional cycles of 16KHz will be added every 20 seconds, etc. Assume DOFFSET is set to 7Fh, then every 20 seconds a cycle of 16KHz will be removed from all the clock signals in the division chain. If 7Eh is set, then two cycles of 16KHz will be removed every 20 seconds, etc.

2. Analogy adjust

The crystal load capacitance (C_L) include in IC can be configured by the OSCILLATOR CAP ADJUST register, the register address is 1011, 1100. The default value is 1100, 1100. The D7~D4 bit 1100H correspond 12pF C_{X1} paralleled connected to X1, and D3~D0 bit 1100H correspond 12pF C_{X2} paralleled connected to X2, and the total C_L is 6pF.

Details are listed in the below table:

Total C_L	Adjustment data		bit 7	Bit6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	C_{X1}	C_{X2}								
0pF	0	0	0	0	0	0	0	0	0	0
0.5pF	1	1	0	0	0	1	0	0	0	1
1pF	2	2	0	0	1	0	0	0	1	0
	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮
6pF (Default)	12	12	1	1	0	0	1	1	0	0
6.5pF	13	13	1	1	0	1	1	1	0	1
7pF	14	14	1	1	1	0	1	1	1	0
7.5pF	15	15	1	1	1	1	1	1	1	1

Reading / Writing Data via the I²C Bus Interface

1. 2-wire Interface

The PT7C4908 uses a bidirectional 2-wire serial interface. The two lines are SDA and SCL. Both lines must be connected to a positive supply through individual pull up resistors. Data transfers can only be initiated when the bus is not busy (both SDA and SCL are high). When V_{CC} is less than V_{RST}, communication with the serial bus is terminated and inactive to prevent erroneous communication from the microprocessor. Figure 7 is the 2-wire bus timing diagram.

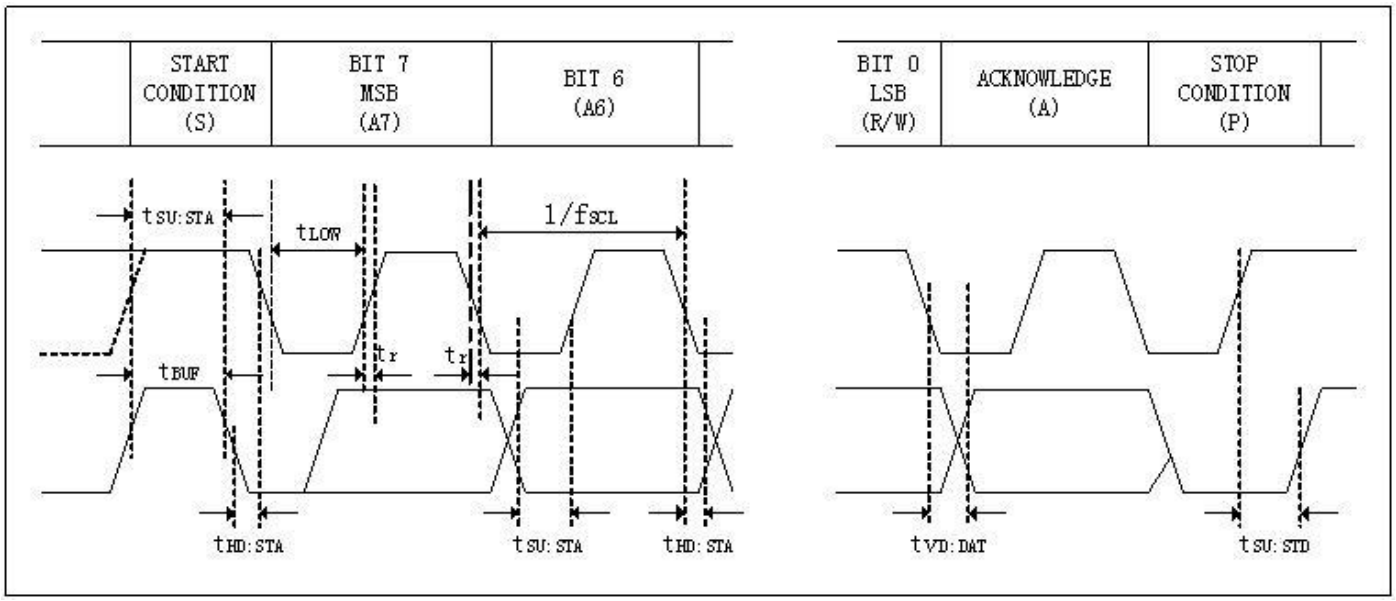


Figure 7 2 Wire Bus Timing Diagram

2. Timeout Feature

The purpose of the bus timeout is to reset the serial bus interface and change the SDA line from an output to an input, which releases the SDA line from being held low. This is necessary when the PT7C4908 is transmitting data and become stuck at logic low. If the SDA line is stuck low, any other device on the bus is not able to communicate. The logic above, shown in Figure 8, is intended to illustrate the timeout feature. If an I²C transaction takes more than 1s (minimum timout period), a timeout condition occurs. When a timeout condition is observed, the I²C interface resets to the IDLE state and waits for a new I²C transaction. In order to complete the 31-byte burst read/write from the RAM before an I²C timeout, the minimum SCL frequency must be 0.32kHz. A valid start condition sets Time_Out_CLR = 1 and the counting begins. A valid stop condition returns Time_Out_CLR = 0 and disables the up/down counter.

Figure 9 shows the normal 2-wire bus operation.

Figure 10 illustrates what happens when the SDA line is stuck low for two clock cycles of 1Hz_CLK during a valid bus transaction. Depending on when the actual valid bus transaction begins relative to the 1Hz CLK, the timeout period is either t1 = 2s or t2 = 1s.

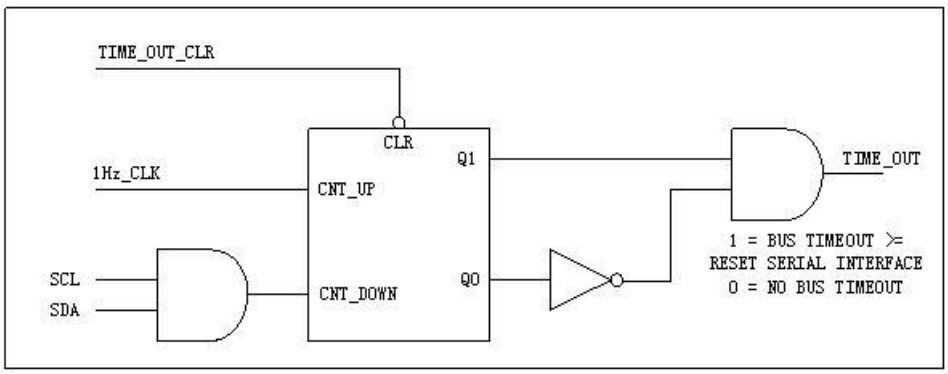


Figure 8 Timeout Simplified Functional Diagram

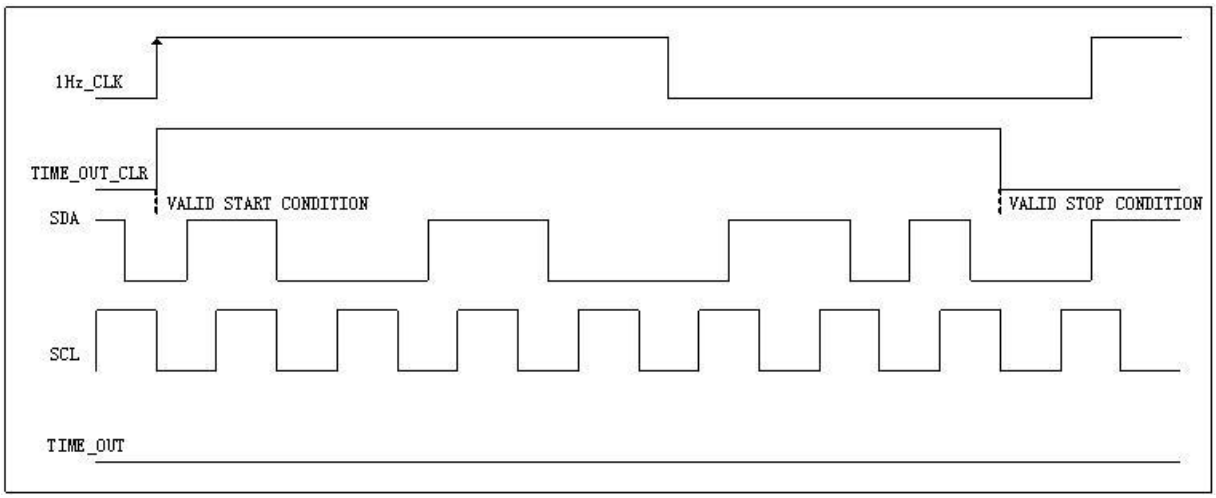


Figure 9 Normal 2-Wire Bus Operation

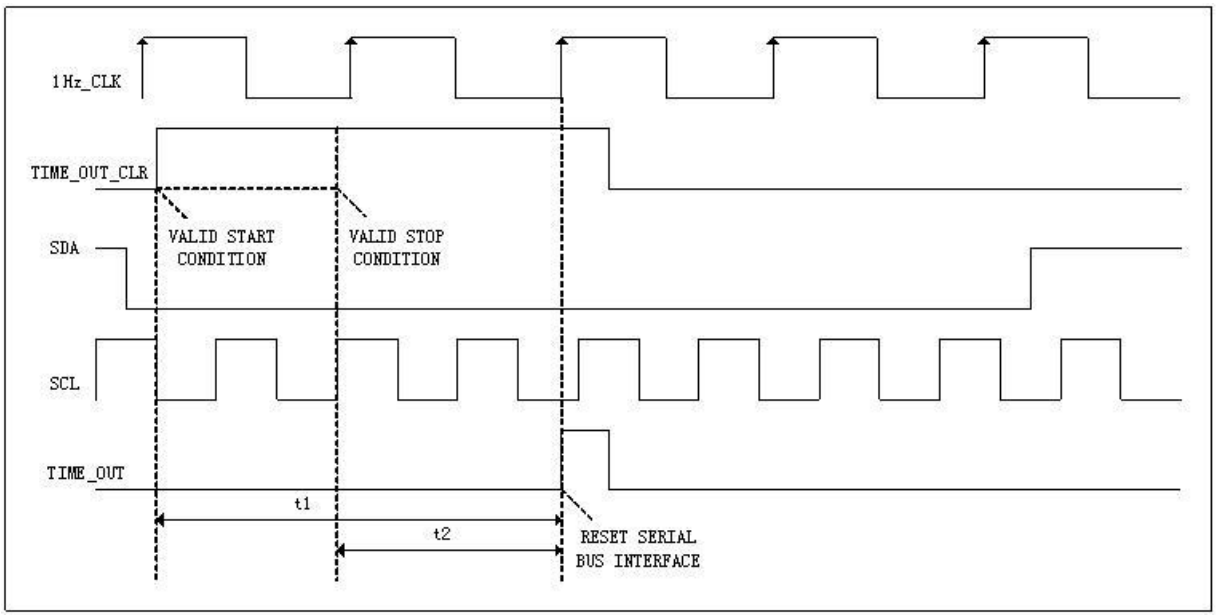


Figure 10 Timeout 2-Wire Bus Operation

3. BIT Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as control signals (Figure 11).

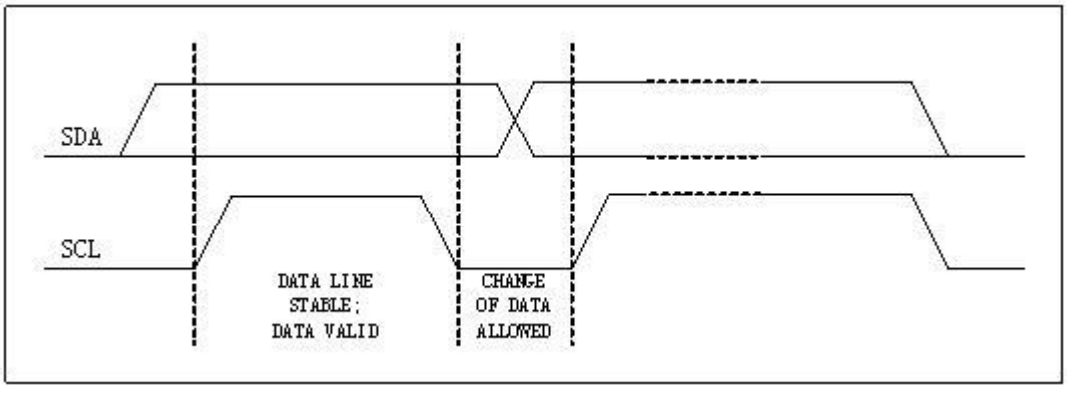


Figure 11 Bit Transfer

4. Starting and Stopping Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA, while SCL is high, is defined as the START (S) condition. A low-to-high transition of the data line while SCL is high is defined as the STOP (P) condition (Figure 12).

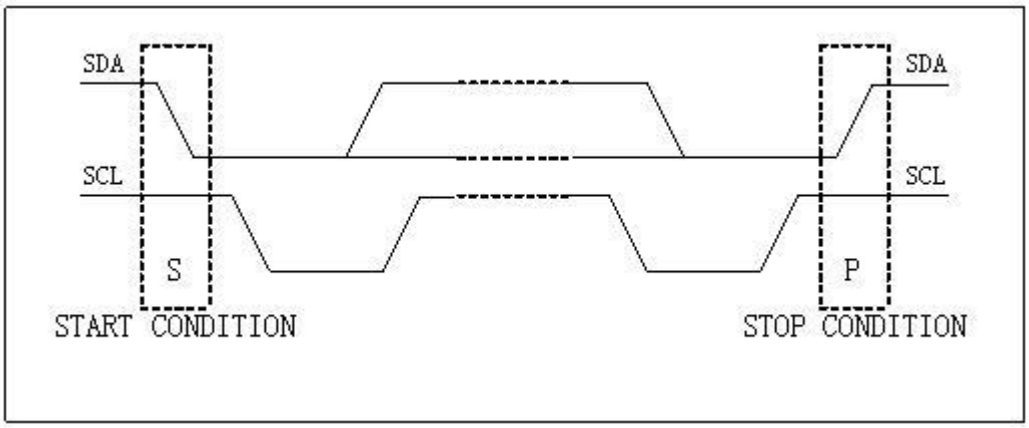


Figure 12 Start and Stop Conditions

5. Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter, during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of the data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

6. Slave Address Byte

Before any data is transmitted on the bus, the device that should respond is addressed first. The first byte sent after the start (S) procedure is the address byte. The PT7C4908 acts as a slave transmitter/receiver. Therefore, SCL is only an input clock signal and SDA is a bidirectional data line. The slave address for the PT7C4908 is shown in Figure 13.

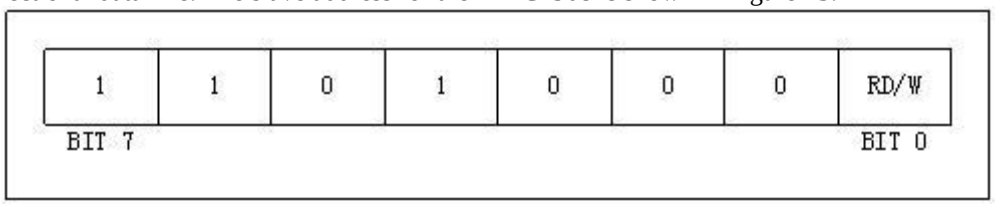


Figure 13 2-Wire Slave Address Byte

7. Address/Command Byte

The command byte is shown in Figure 14. The MSB (bit 7) must be a logic 1. If it is zero, writes to the PT7C4909/ 4910 are disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or a read operation (output) if logic 1. The command byte is always input starting with the MSB (bit 7).

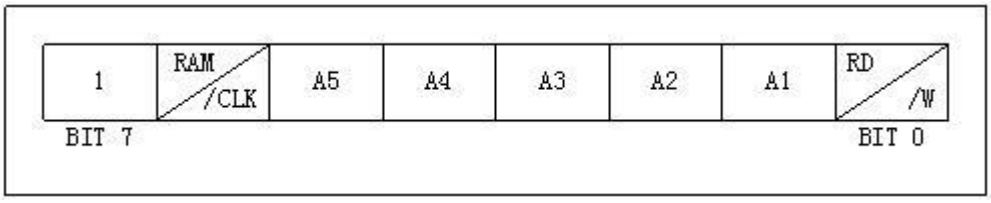


Figure 14 Address/Command Byte

8. Reading from the Timekeeping Registers

The timekeeping registers (seconds, minutes, hours, date, month, day, and year) can be read either with a single read or a burst read. The century register can only be read with a single read. Since the real-time clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock counters could change during a read operation, thereby reporting inaccurate timekeeping data. In the PT7C4908, each clock register's data is buffered by a latch. Clock register data is latched by the 2-wire bus read command (on the falling edge of SCL when the slave acknowledge bit is sent after the address/command byte has been sent by the master to read a timekeeping register). Collision-detection circuitry ensures that this does not happen coincident with a seconds counter update to ensure accurate time data is being read. This avoids time data changes during a read operation. The clock counters continue to count and keep accurate time during the read operation.

If single reads are to be used to read each of the timekeeping registers individually, then it is necessary to do some error checking on the receiving end. The potential for error is the case when the seconds counter increments before all the other registers are read out. For example, suppose a carry of 13:59:59 to 14:00:00 occurs during single read operations of the timekeeping registers. Then, the net data could become 14:59:59, which is erroneous real-time data. To prevent this with single-read operations, read the seconds register first (initial seconds) and store this value for future comparison. When the remaining timekeeping registers have been read out, read the seconds register again (final seconds). If the initial seconds value is 59, check that the final seconds value is still 59; if not, repeat the entire single-read process for the timekeeping registers. A comparison of the initial seconds value with the final seconds value can indicate if there was a bus delay problem in reading the timekeeping data (difference should always be 1s or less). Using a 100kHz bus speed, sequential single reads would take under 2.5ms to read all seven of the timekeeping registers, plus a second read of the seconds register.

The most accurate way to read the timekeeping registers is to do a burst read. In the burst read, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are read sequentially, in the order listed with the seconds register first. They must be all read out as a group of eight registers, with 8 bits each, for proper execution of the burst read function. All seven timekeeping registers are latched upon the receipt of the burst read command. Worst-case errors that can occur between the actual time and the read time is 1s, assuming the entire burst
read is done in less than 1s.

9. Reading from the Timekeeping Registers

The time and date can be set by writing to the timekeeping registers (seconds, minutes, hours, date, month, day, year, and century). To avoid changing the current time by an incomplete write operation, the current time value is buffered from being written directly to the timekeeping registers. The timekeeping registers continue to count, and on the next rising edge of the 1Hz seconds clock, the new data is loaded into the timekeeping registers. The new value will be incremented on the next rising of the 1Hz seconds clock. Collision-detection circuitry ensures that this does not happen coincident with a seconds register update to ensure accurate time data is being written. This avoids time data changes during a write operation. An incomplete write operation aborts the time update procedure and the contents of the input buffer are discarded.

If single write operations are to be used to write to each of the timekeeping registers, then error checking is needed. If the seconds register is to be updated, update it first and then read it back and store its value as the initial seconds. Update the remaining timekeeping registers and then read the seconds register again (final seconds). If initial seconds were 59, ensure they are still 59. If initial seconds were not 59, ensure that final seconds are within 1s of initial seconds. If the seconds register is not to be written to, then read the seconds register first and save it as initial seconds. Write to the required timekeeping registers and then read the seconds register again (final seconds). If initial seconds were 59, ensure they are still 59. If initial seconds were not 59, ensure that final seconds are within 1s of initial seconds.

Although both single writes and burst writes are possible, the most accurate way to write to the timekeeping registers is to do a burst write. In the burst write, the main timekeeping registers (seconds, minutes, hours, date, month, day, year) and the control register are written to sequentially. They must be all written to as a group of eight registers, with 8 bytes each, for proper execution of the burst write function. All seven timekeeping registers are simultaneously loaded into the input buffer at the end of the 2-wire bus write operation. The worst-case error that can occur between the actual time and the write time update is 1s. Figure 15 shows PT7C4908 data transfer.

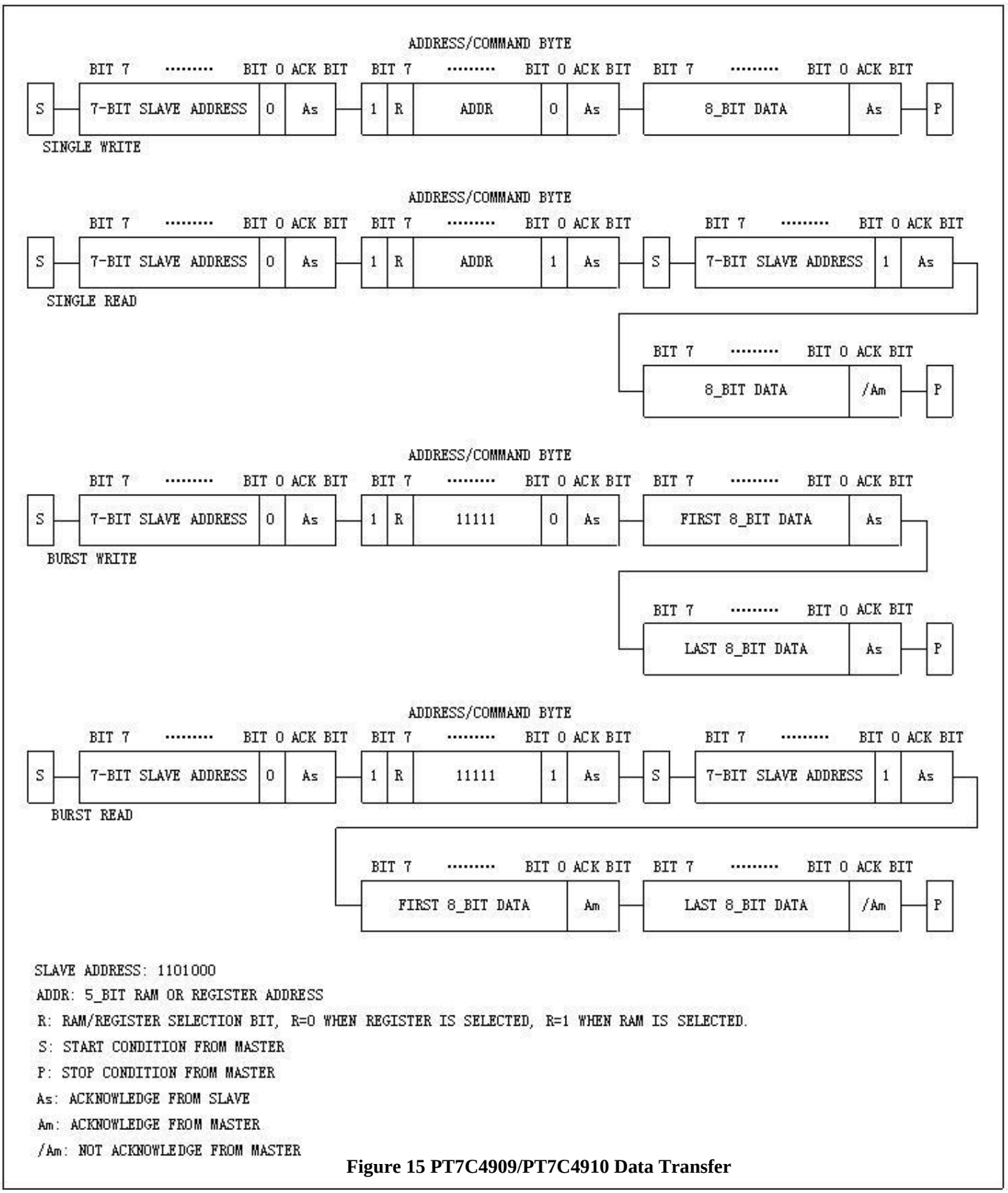
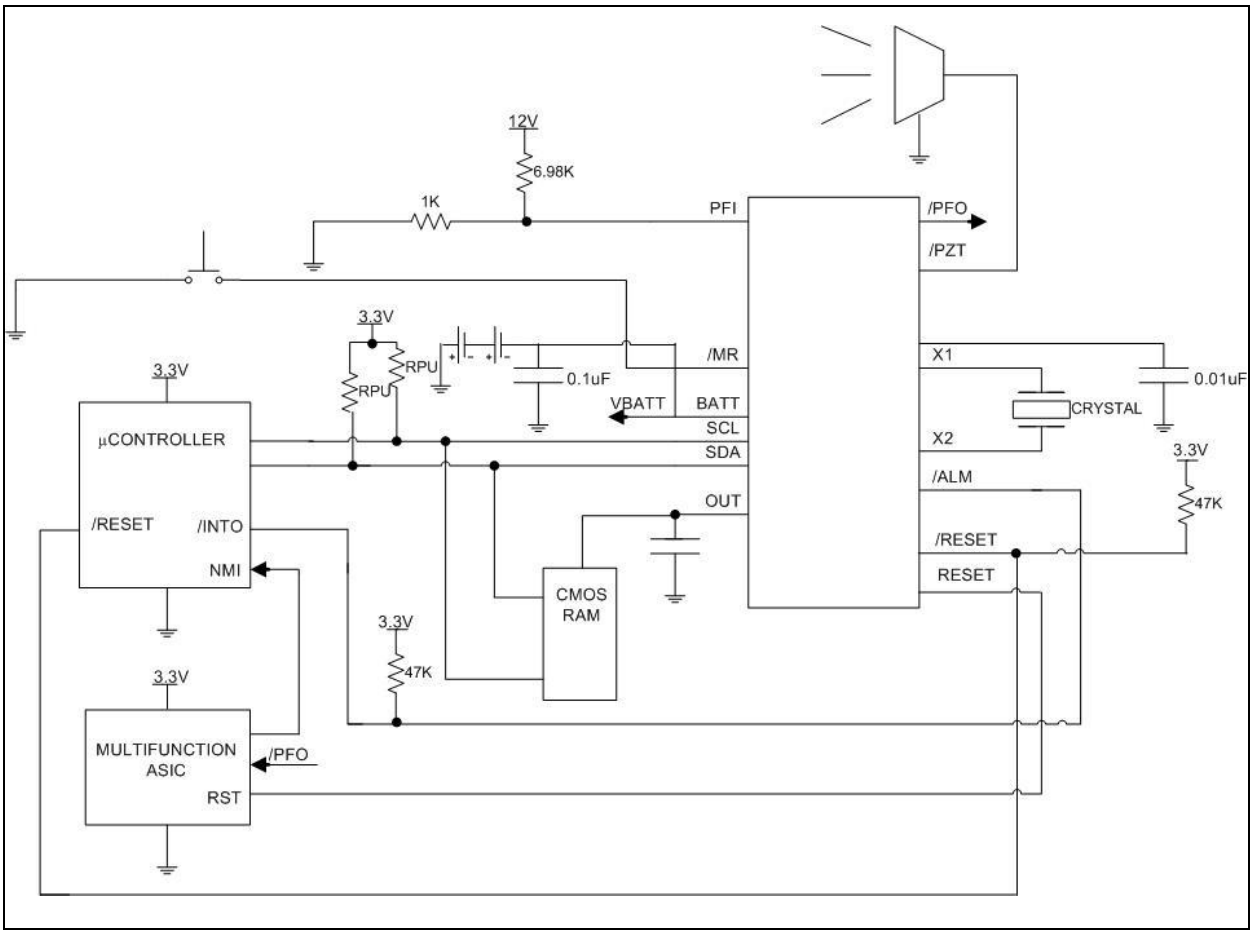


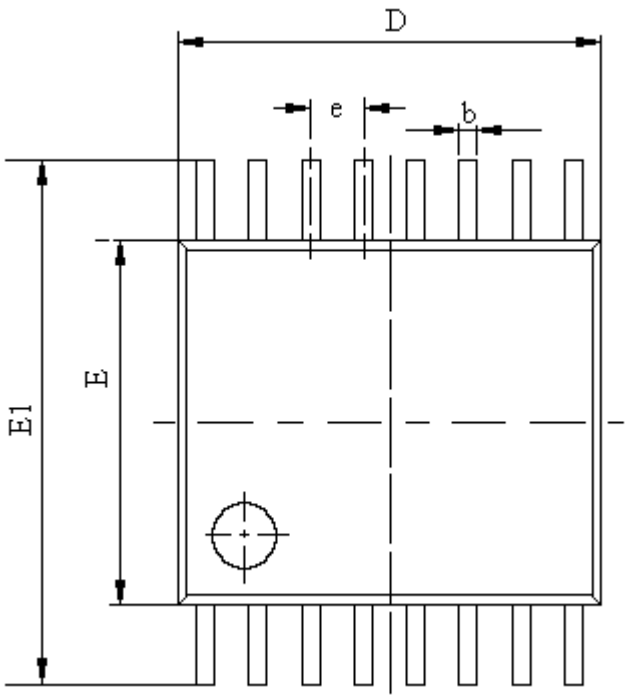
Figure 15 PT7C4909/PT7C4910 Data Transfer

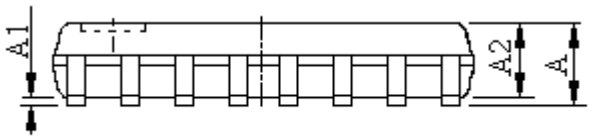
Application Circuit



Mechanical Information

LE(Lead free and Green TSSOP-16)





Note:
1) Ref: JEDEC MO-153F/AD

PKG. DIMENSIONS(MM)		
SYMBOL	MIN	MAX
A		1.10
A1	0.02	0.15
A2	0.80	1.00
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	4.30	4.50
E1	6.25	6.55
e	0.65 BSC	
L	0.50	0.70
θ	1°	7°

Ordering Information

Part Number	Package Code	Package
PT7C4908RLE	L	Lead free and Green 16-Pin TSSOP
PT7C4908SLE	L	Lead free and Green 16-Pin TSSOP

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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