Data Sheet May 1999 File Number 2485.7

Numerically Controlled Oscillator/Modulator

The Intersil HSP45116 combines a high performance quadrature Numerically Controlled Oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the Block Diagram, the HSP45116 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/ Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32 bits, which results in frequency resolution better than 0.008Hz at 33MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be down converted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

Features

- NCO and CMAC on One Chip
- 15MHz, 25.6MHz, 33MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.008Hz Tuning Resolution at 33MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

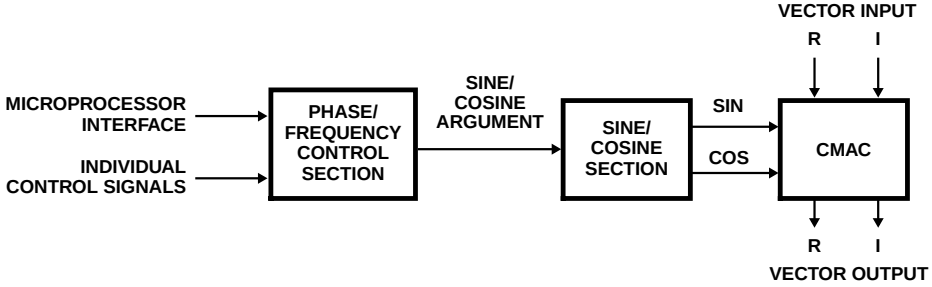
- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45116VC-15	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116VC-25	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116GC-15	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-25	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-33	0 to 70	145 Ld CPGA	G145.A
HSP45116GI-15	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-25	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-33	-40 to 85	145 Ld CPGA	G145.A
HSP45116GM-15/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116GM-25/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116AVC-52	0 to 70	160 Ld MQFP	Q160.28x28

†This part has its own data sheet under HSP45116A, AnswerFAX document no. 4156.

Block Diagram



Pinouts

145 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	V_{CC}	IMIN 4	IMIN 8	IMIN 9	IMIN 11	IMIN 15	IMIN 16	GND	V_{CC}	IO 18	IO 15	IO 12	IO 10	GND	V_{CC}	A
B	GND	IMIN 1	IMIN 5	IMIN 7	IMIN 10	IMIN 13	IMIN 14	IO 19	IO 16	IO 14	IO 11	IO 8	IO 7	IO 5	IO 2	B
C	RIN 15	RIN 18	IMIN 2	IMIN 3	IMIN 6	IMIN 12	IMIN 17	IMIN 18	IO 17	IO 13	IO 9	IO 6	IO 4	IO 1	RO 18	C
D	RIN 13	RIN 17	IMIN 0	INDEX									IO 3	RO 19	RO 17	D
E	RIN 10	RIN 14	RIN 16										IO 0	RO 16	RO 15	E
F	RIN 7	RIN 11	RIN 12										RO 14	RO 13	RO 11	F
G	V_{CC}	RIN 9	RIN 8										RO 9	RO 12	RO 10	G
H	GND	RIN 6	RIN 5										RO 8	RO 7	GND	H
J	RIN 3	RIN 1	RIN 4										RO 5	RO 4	V_{CC}	J
K	RIN 2	RIN 0	SH 1										RO 1	RO 2	RO 6	K
L	SH 0	ACC	$\overline{RBYTILD}$										$\overline{PACO}$	DET 1	RO 3	L
M	$\overline{ENPH}$ $\overline{REG}$	$\overline{PEAK}$	MOD 1										$\overline{OEREXT}$	$\overline{OEI}$	RO 0	M
N	$\overline{ENOF}$ $\overline{REG}$	$\overline{BINFMT}$	MOD 0	$\overline{LOAD}$	$\overline{ENCF}$ $\overline{REG}$	$\overline{MODPI}$ /2PI	AD 0	C 14	C 13	C 8	C 2	OUT-MUX 1	OUT-MUX 0	$\overline{OEIEXT}$	DET 0	N
P	$\overline{TICO}$	$\overline{PACI}$	PMSEL	$\overline{CLROFR}$	$\overline{ENTIREG}$	$\overline{CS}$	AD 1	C 15	C 10	C 9	C 6	C 3	C 1	$\overline{OER}$	GND	P
Q	V_{CC}	GND	$\overline{ENPHAC}$	$\overline{ENI}$	CLK	$\overline{WR}$	V_{CC}	GND	C 12	C 11	C 7	C 5	C 4	C 0	V_{CC}	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

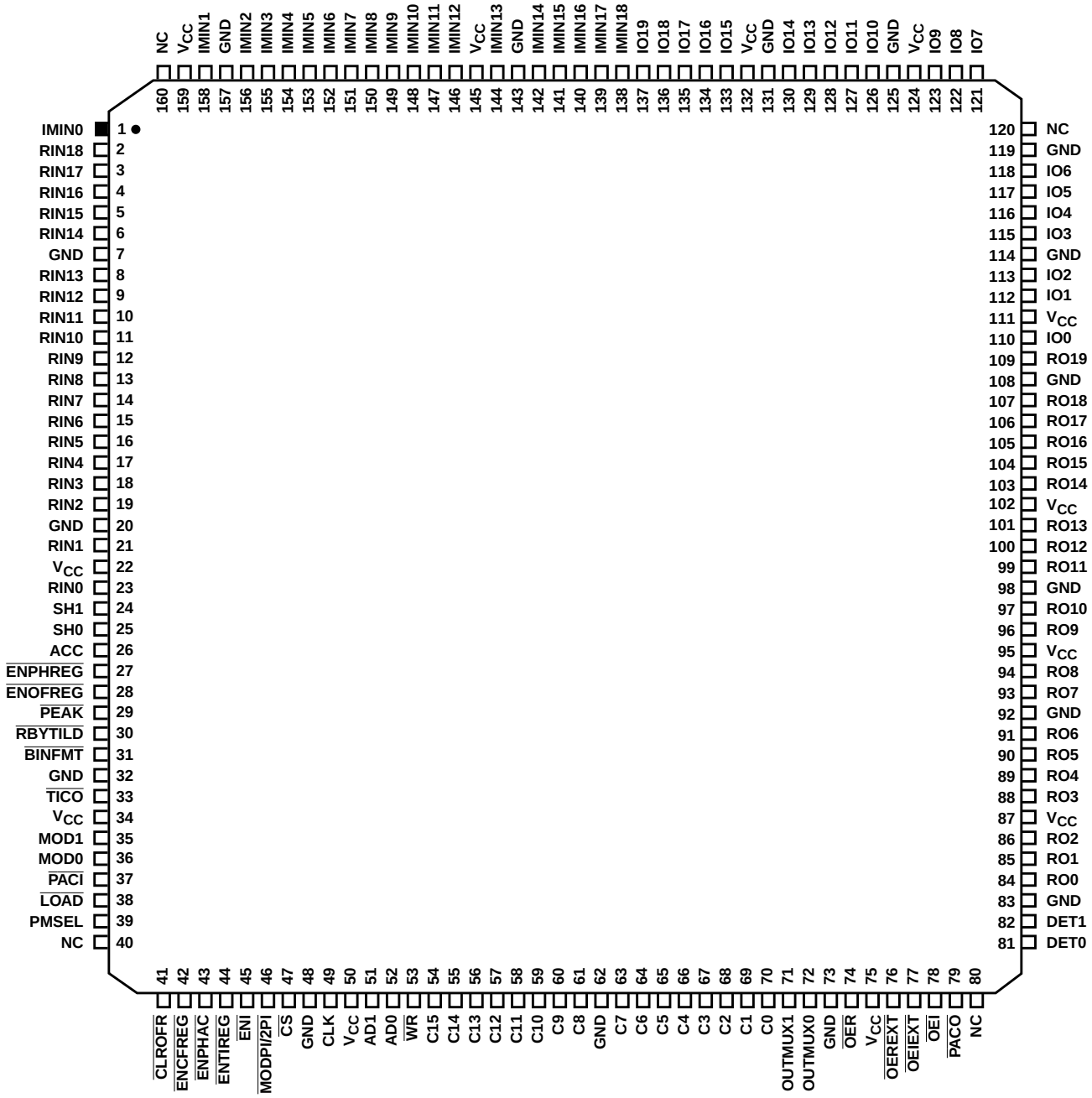
Pinouts (Continued)

145 PIN PGA
BOTTOM VIEW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	V_{CC}	GND	IO 10	IO 12	IO 15	IO 18	V_{CC}	GND	IMIN 16	IMIN 15	IMIN 11	IMIN 9	IMIN 8	IMIN 4	V_{CC}	A
B	IO 2	IO 5	IO 7	IO 8	IO 11	IO 14	IO 16	IO 19	IMIN 14	IMIN 13	IMIN 10	IMIN 7	IMIN 5	IMIN 1	GND	B
C	RO 18	IO 1	IO 4	IO 6	IO 9	IO 13	IO 17	IMIN 18	IMIN 17	IMIN 12	IMIN 6	IMIN 3	IMIN 2	RIN 18	RIN 15	C
D	RO 17	RO 19	IO 3									INDEX	IMIN 0	RIN 17	RIN 13	D
E	RO 15	RO 16	IO 0										RIN 16	RIN 14	RIN 10	E
F	RO 11	RO 13	RO 14										RIN 12	RIN 11	RIN 7	F
G	RO 10	RO 12	RO 9										RIN 8	RIN 9	V_{CC}	G
H	GND	RO 7	RO 8										RIN 5	RIN 6	GND	H
J	V_{CC}	RO 4	RO 5										RIN 4	RIN 1	RIN 3	J
K	RO 6	RO 2	RO 1										SH 1	RIN 0	RIN 2	K
L	RO 3	DET 1	$\overline{PACO}$										$\overline{RBYTILD}$	ACC	SH 0	L
M	RO 0	$\overline{OEI}$	$\overline{OEREXT}$										MOD 1	$\overline{PEAK}$	$\overline{ENPH}$ $\overline{REG}$	M
N	DET 0	$\overline{OEIEXT}$	OUT-MUX 0	OUT-MUX 1	C 2	C 8	C 13	C 14	AD 0	$\overline{MODPI}$ /2PI	$\overline{ENCF}$ $\overline{REG}$	$\overline{LOAD}$	MOD 0	$\overline{BINFMT}$	$\overline{ENOF}$ $\overline{REG}$	N
P	GND	$\overline{OER}$	C 1	C 3	C 6	C 9	C 10	C 15	AD 1	$\overline{CS}$	$\overline{ENTIREG}$	$\overline{CLROFR}$	PMSEL	$\overline{PACI}$	$\overline{TICO}$	P
Q	V_{CC}	C 0	C 4	C 5	C 7	C 11	C 12	GND	V_{CC}	$\overline{WR}$	CLK	$\overline{ENI}$	$\overline{ENPHAC}$	GND	V_{CC}	Q
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Pinouts (Continued)

160LEAD MQFP
TOP VIEW



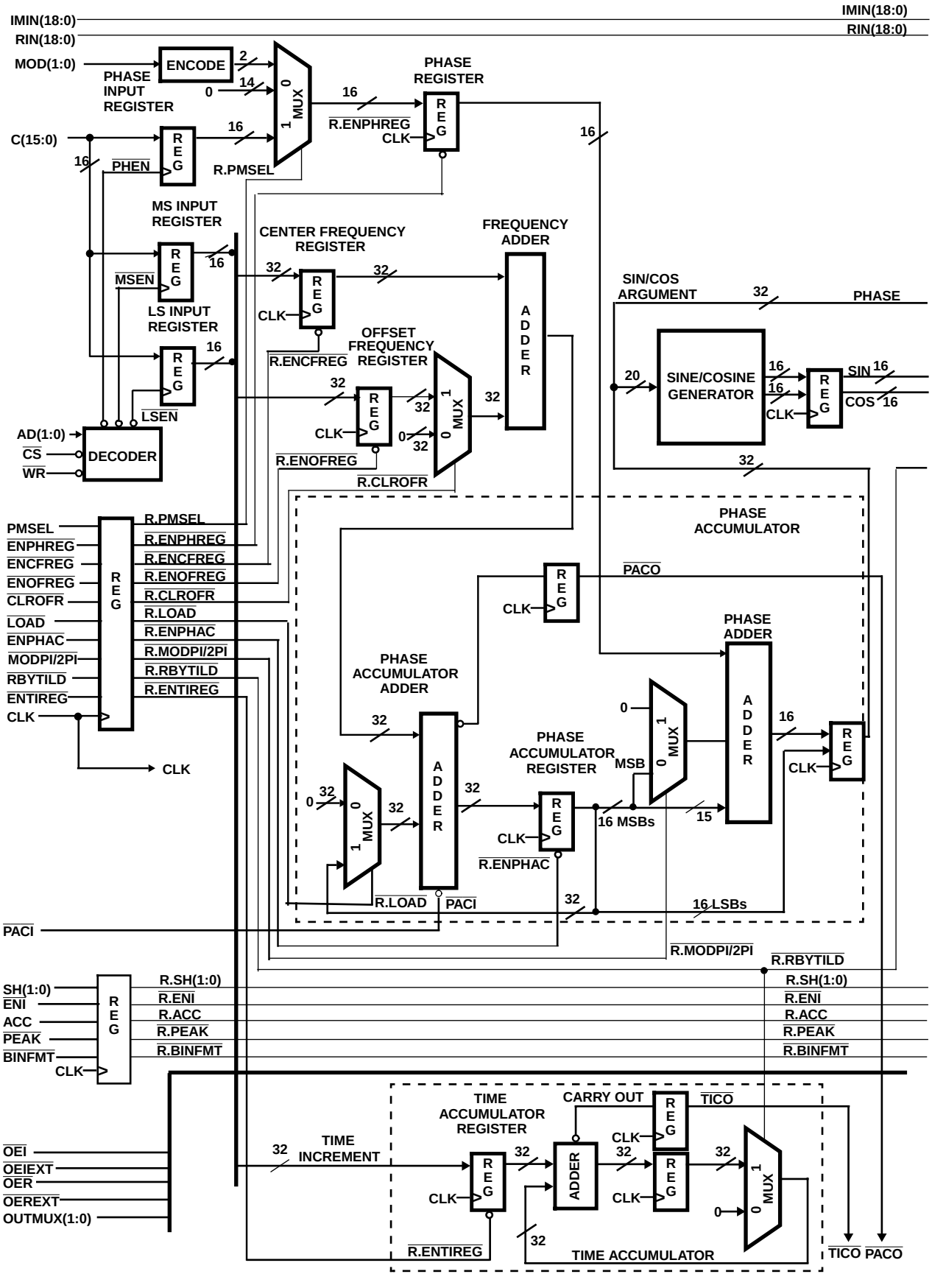
Pin Description

NAME	NUMBER	TYPE	DESCRIPTION
V_{CC}	A1, A9, A15, G1, J15, Q1, Q7, Q15	-	+5V Power supply input.
GND	A8, A14, B1, H1, H15, P15, Q2, Q8	-	Power supply ground input.
C0-15	N8-11, P8-13, Q9-14	I	Control input bus for loading phase and frequency data into the PFCS. C15 is the MSB.
AD0-1	N7, P7	I	Address pins for selecting destination of C0-15 data.
$\overline{CS}$	P6	I	Chip Select (active low).
$\overline{WR}$	Q6	I	Write Enable. Data is clocked into the register selected by AD0-1 on the rising edge of $\overline{WR}$ when the $\overline{CS}$ line is low.
CLK	Q5	I	Clock. All registers, except the control registers clocked with $\overline{WR}$, are clocked (when enabled) by the rising edge of CLK.
$\overline{ENPHREG}$	M1	I	Phase Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENPHREG}$ enables the clocking of data into the phase register.
$\overline{ENOFREG}$	N1	I	Frequency Offset Register Enable (active Low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENOFREG}$ enables clocking of data into the frequency offset register.
$\overline{ENCFREG}$	N5	I	Center Frequency Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENCFREG}$ enables clocking of data into the center frequency register.
$\overline{ENPHAC}$	Q3	I	Phase Accumulator Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENPHAC}$ enables clocking of the phase accumulator register.
$\overline{ENTIREG}$	P5	I	Time Interval Control Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENTIREG}$ enables clocking of data into the time accumulator register.
$\overline{ENI}$	Q4	I	Real and Imaginary Data Input Register (RIR, IIR) Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENI}$ enables clocking of data into the real and imaginary input data register.
$\overline{MODPI/2PI}$	N6	I	Modulo $\pi/2\pi$ Select. When low, the Sine and Cosine ROMs are addressed modulo 2π (360 degrees). When high, the most significant address bit is held low so that the ROMs are addressed modulo π (180 degrees). This input is registered on chip by clock.
$\overline{CLROFR}$	P4	I	Frequency Offset Register Output Zero (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{CLROFR}$ zeros the data path from the frequency offset register to the frequency adder. New data can still be clocked into the frequency offset register; $\overline{CLROFR}$ does not affect the contents of the register.
$\overline{LOAD}$	N4	I	Phase Accumulator Load Control (active low). Registered on chip by CLK. Zeroes feedback path in the phase accumulator without clearing the phase accumulator register.
MOD0-1	M3, N3	I	External Modulation Control Bits. When selected with the PMSEL line, these bits add a 0, 90, 180, or 270 degree offset to the current phase in the phase accumulator. The lower 14 bits of the phase control path are set to zero. These bits are loaded into the phase register when $\overline{ENPHREG}$ is low.
PMSEL	P3	I	Phase Modulation Select Line. This line determines the source of the data clocked into the phase register. When high, the phase control register is selected. When low, the external modulation pins (MOD0-1) are selected for the most significant two bits and the least significant two bits and the least significant 14 bits are set to zero. This control is registered by CLK.
$\overline{RBYTILD}$	L3	I	ROM Bypass, Timer Load. Active low, registered by CLK. This input bypasses the sine/ cosine ROM so that the 16-bit phase adder output and lower 16 bits of the phase accumulator go directly to the CMAC's sine and cosine inputs, respectively. It also enables loading of the timer accumulator register by zeroing the feedback in the accumulator.
$\overline{PACI}$	P2	I	Phase Accumulator Carry Input (active low). A low on this pin causes the phase accumulator to increment by one, in addition to the values in the phase accumulator register and frequency adder.

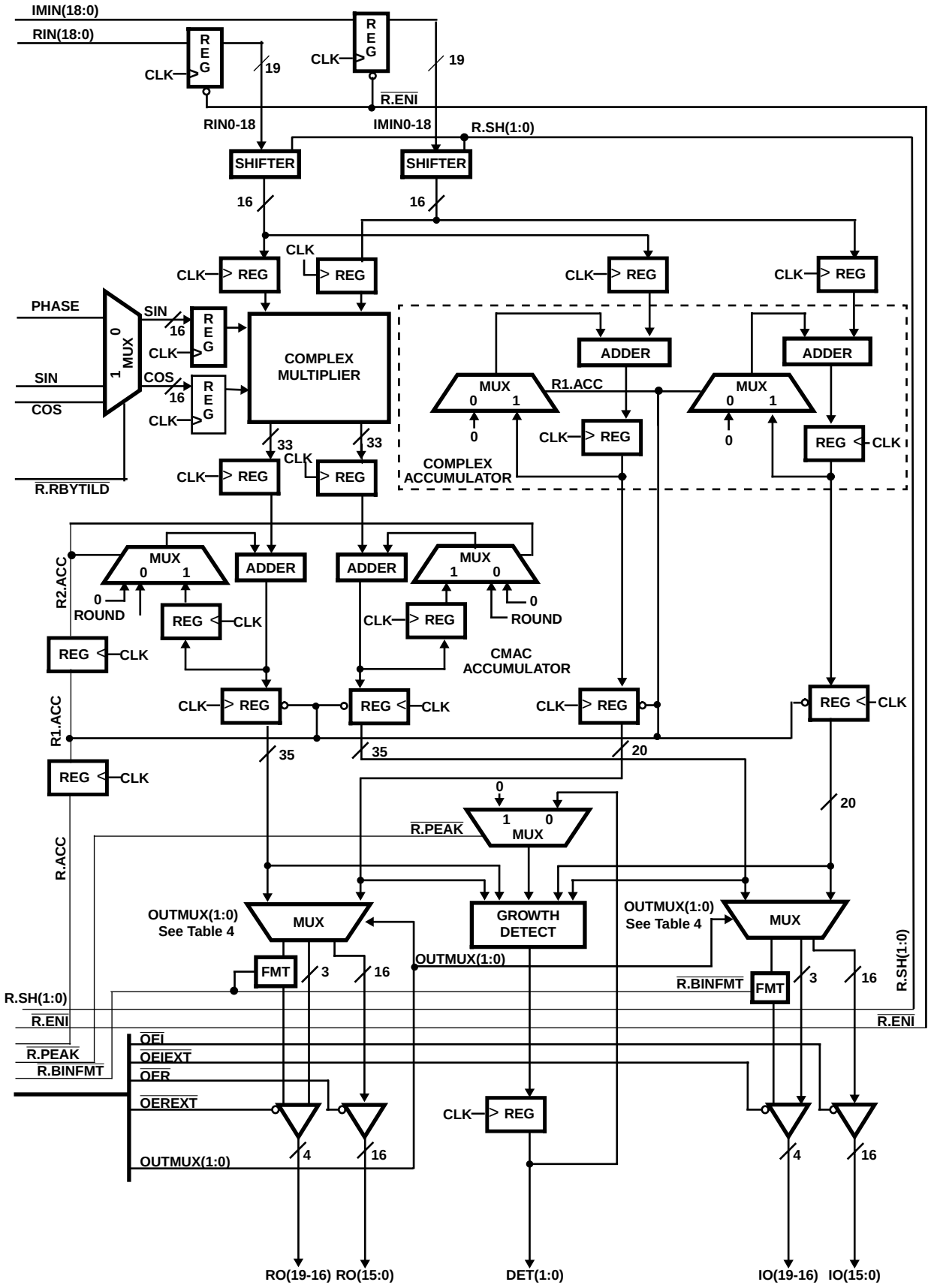
Pin Description (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
$\overline{\text{PACO}}$	L13	O	Phase Accumulator Carry Output. Active low and registered by CLK. A low on this output indicates that the phase accumulator has overflowed, i.e., the end of one sine/cosine cycle has been reached.
$\overline{\text{TICO}}$	P1	O	Time Interval Accumulator Carry Output. Active low, registered by CLK. This output goes low when a carry is generated by the time interval accumulator. This function is provided to time out control events such as synchronizing register clocking to data timing.
RIN0-18	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	I	Real Input Data Bus. This is the external real component into the complex multiplier. The bus is clocked into the real input data register by CLK when $\overline{\text{ENI}}$ is asserted; two's complement.
IMIN0-18	A2-7, B2-7, C3-8, D3	I	Imaginary Input Data Bus. This is the external imaginary component into the complex multiplier. The bus is clocked into the real input data register by CLK when $\overline{\text{ENI}}$ is asserted; two's complement.
SH0-1	K3, L1	I	Shift Control Inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	I	Accumulate/Dump Control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
$\overline{\text{BINFMT}}$	N2	I	This input is used to convert the two's complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two's complement representation. This input is registered by CLK.
$\overline{\text{PEAK}}$	M2	I	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DET0-1 pins. When the $\overline{\text{PEAK}}$ input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that $\overline{\text{PEAK}}$ is activated.
OUTMUX0-1	N12, N13	I	These inputs select the data to be output on RO0-19 and IO0-19.
RO0-19	C15, D14, D15, E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15	O	Real Output Data Bus. These Three-state outputs are controlled by $\overline{\text{OER}}$ and $\overline{\text{OEREXT}}$. OUTMUX0-1 select the data output on the bus.
IO0-19	A10-13, B8-15, C9-14, D13, E13	O	Imaginary Output Data Bus. These Three-state outputs are controlled by $\overline{\text{OEI}}$ and $\overline{\text{OEIEXT}}$. OUTMUX0-1 select the data output on the bus.
DET0-1	N15, L14	O	These output pins indicate the number of bits of growth in the accumulators. While $\overline{\text{PEAK}}$ is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
$\overline{\text{OER}}$	P14	I	Three-state control for bits RO0-15. Outputs are enabled when the line is low.
$\overline{\text{OEREXT}}$	M13	I	Three-state control for bits RO16-19. Outputs are enabled when the line is low.
$\overline{\text{OEI}}$	M14	I	Three-state control for bits IO0-15. Outputs are enabled when the line is low.
$\overline{\text{OEIEXT}}$	N14	I	Three-state control for bits IO16-19. Outputs are enabled when the line is low.

Functional Block Diagram



Functional Block Diagram (Continued)



Functional Description

The Numerically Controlled Oscillator/Modulator (NCOM) produces a digital complex sinusoid waveform whose amplitude, phase and frequency are controlled by a set of input command words. When used as a Numerically Controlled Oscillator (NCO), it generates 16-bit sine and cosine vectors at a maximum sample rate of 33MHz. The NCOM can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. The Complex Multiplier/ Accumulator (CMAC) can be used to multiply this waveform by an input signal for AM and QAM signals. By stepping the phase input, the output of the ROM becomes an FFT twiddle factor; when data is input to the Vector Inputs (see Block Diagram), the NCOM calculates an FFT butterfly.

As shown in the Block Diagram, the NCOM consists of three parts: Phase and Frequency Control Section (PFCS), Sine/Cosine Generator, and CMAC. The PFCS stores the phase and frequency inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Generator performs a lookup on this phase and outputs the appropriate values for the sine and cosine. The sine and cosine form one set of inputs to the CMAC, which multiplies them by the input vector to form the modulated output.

Phase and Frequency Control Section

The phase and frequency of the internally generated sine and cosine are controlled by the PFCS (Block Diagram). The PFCS generates a 32-bit word that represents the current phase of the sine and cosine waves being generated; the Sine/ Cosine Argument. Stepping this phase angle from 0 through full scale (2^{32} - 1) corresponds to the phase angle of a sinusoid starting at 0^{o} and advancing around the unit circle counterclockwise. The PFCS automatically increments the phase by a preprogrammed amount on every rising edge of the external clock. The value of the phase step (which is the sum of the Center and Offset Frequency Registers) is:

$$\text{Phase Step} = \frac{\text{Signal Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

The PFCS is divided into two sections: the Phase Accumulator uses the data on C0-15 to compute the phase angle that is the input to the Sine/Cosine Section (Sine/Cosine Argument); the Time Accumulator supplies a pulse to mark the passage of a preprogrammed period of time.

The Phase Accumulator and Time Accumulator work on the same principle: a 32-bit word is added to the contents of a 32-bit accumulator register every clock cycle; when the sum causes the adder to overflow, the accumulation continues with the 32 bits of the adder going into the accumulator register. The overflow bit is used as an output to indicate the timing of the accumulation overflows. In the Time Accumulator, the overflow bit generates $\overline{\text{TICO}}$, the Time Accumulator carry out (which is the only output of the Time Accumulator). In the Phase Accumulator, the overflow is inverted to generate the Phase Accumulator Carry Out, $\overline{\text{PACO}}$.

The output of the Phase Accumulator goes to the Phase Adder, which adds an offset to the top 16 bits of the phase. This 32-bit number forms the argument of the sine and cosine, which is passed to the Sine/Cosine Generator.

Both accumulators are loaded 16 bits at a time over the C0-15 bus. Data on C0-15 is loaded into one of the three input registers when $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are low. The data in the Most Significant Input Register and Least Significant Input Register forms a 32-bit word that is the input to the Center Frequency Register, Offset Frequency Register and Time Accumulator. These registers are loaded by enabling the proper register enable signal; for example, to load the Center Frequency Register, the data is loaded into the LS and MS Input Registers, and $\overline{\text{ENCFREG}}$ is set to zero; the next rising edge of CLK will pass the registered version of $\overline{\text{ENCFREG}}$, $\overline{\text{R.ENCFREG}}$, to the clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the Input Registers will be continuously loaded into the Center Frequency Register as long as $\overline{\text{R.ENCFREG}}$ is low.

The Phase Register is loaded in a similar manner. Assuming PMSEL is high, the contents of the Phase Input Register is loaded into the Phase Register on every rising clock edge that R.ENPHREG is low. If PMSEL is low, MOD0-1 supply the two most significant bits into the Phase Register (MOD1 is the MSB) and the least significant 14 bits are loaded with 0. MOD0-1 are used to generate a Quad Phase Shift Keying (QPSK) signal (Table 2).

TABLE 1. AD0-1 DECODING

AD1	AD0	$\overline{\text{CS}}$	$\overline{\text{WR}}$	FUNCTION
0	0	0	↑	Load least significant bits of frequency input.
0	1	0	↑	Load most significant bits of frequency input.
1	0	0	↑	Load phase register.
1	1	X	X	Reserved.
X	X	1	X	No Operation.

The Phase Accumulator consists of registers and adders that compute the value of the current phase at every clock. It has three inputs: Center Frequency, which corresponds to the carrier frequency of a signal; Offset Frequency, which is the deviation from the Center Frequency; and Phase, which is a 16-bit number that is added to the current phase for PSK

modulation schemes. These three values are used by the Phase Accumulator and Phase Adder to form the phase of the internally generated sine and cosine.

The sum of the values in Center and Offset Frequency Registers corresponds to the desired phase increment (modulo 2^{32}) from one clock to the next. For example, loading both registers with zero will cause the Phase Accumulator to add zero to its current output; the output of the PFCS will remain at its current value; i.e., the output of the NCOM will be a DC signal. If a hexadecimal 00000001 is loaded into the Center Frequency Control Register, the output of the PFCS will increment by one after every clock. This will step through every location in the Sine/Cosine Generator, so that the output will be the lowest frequency above DC that can be generated by the NCOM, i.e., the clock frequency divided by 2^{32}. If the input to the Center Frequency Control Register is hex 80000000, the PFCS will step through the Generator with half of the maximum step size, so that frequency of the output waveform will be half of the sample rate.

The operation of the Offset Frequency Control Register is identical to that of the Center Frequency Control Register; having two separate registers allows the user to generate an FM signal by loading the carrier frequency in the Center Frequency Control Register and updating the Offset Frequency Control Register with the value of the frequency offset - the difference between the carrier frequency and the frequency of the output signal. A logic low on $\overline{\text{CLROFR}}$ disables the output of the Offset Frequency Register without clearing the contents of the register.

TABLE 2. MOD0-1 DECODE

MOD1	MOD0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

Initializing the Phase Accumulator Register is done by putting a low on the $\overline{\text{LOAD}}$ line. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the phase increment summer on the next clock.

The final phase value going to the Generator can be adjusted using $\overline{\text{MODPI/2PI}}$ to force the range of the phase to be 0^0 to 180^0 (modulo π) or 0^0 to 360^0 (modulo 2π). Modulo 2π is the mode used for modulation, demodulation, direct digital synthesis, etc. Modulo π is used to calculate FFTs. This is explained in greater detail in the Applications Section.

The Phase Register adds an offset to the output of the Phase Accumulator. Since the Phase Register is only 16 bits, it is added to the top 16 bits of the Phase Accumulator.

The Time Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Input Registers and is latched into the Time Accumulator Register on rising edges of CLK while $\overline{\text{ENTIREG}}$ is low. The output of the Time Accumulator is the accumulator carry out, $\overline{\text{TICO}}$. $\overline{\text{TICO}}$ can be used as a timer to enable the periodic sampling of the output of the NCOM. The number programmed into this register equals 2^{32} x CLK period/desired time interval. $\overline{\text{TICO}}$ is disabled and its phase is initialized by zeroing the feedback path of the accumulator with $\overline{\text{RBYTILD}}$.

Sine/Cosine Section

The Sine/Cosine Section (Figure 1) converts the output of the PFCS into the appropriate values for the sine and cosine. It takes the most significant 20 bits of the PFCS output and passes them through a look up table to form the 16-bit sine and cosine inputs to the CMAC.

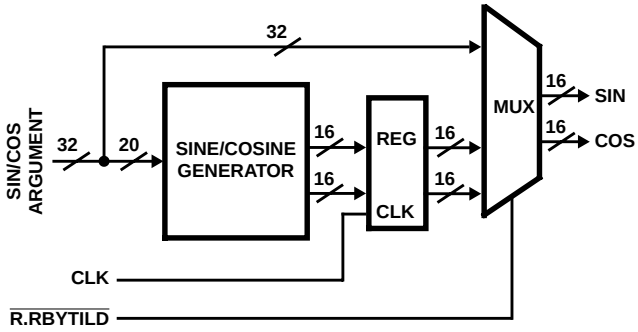


FIGURE 1. SINE/COSINE SECTION

The 20-bit word maps into 2π radians so that the angular resolution is $2\pi/2^{20}$. An address of zero corresponds to 0 radians and an address of hex FFFFF corresponds to 2π- ($2\pi/2^{20}$) radians. The outputs of the Generator Section are 2's complement sine and cosine values. The sine and cosine outputs range from hexadecimal 8001, which represents negative full scale, to 7FFF, which represents positive full scale. Note that the normal range for two's complement numbers is 8000 to 7FFF; the output range of the SIN/COS generator is scaled by one so that it is symmetric about 0.

The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better.

If $\overline{\text{RBYTILD}}$ is low, the output of the PFCS goes directly to the inputs of the CMAC. If the real and imaginary inputs of the CMAC are programmed to hex 7FFF and 0 respectively, then the output of the PFCS will appear on output bits 0 through 15 of the NCOM with the output multiplexers set to bring out the most significant bits of the CMAC output (OUTMUX = 00). The most significant 16 bits out of the PFCS appears on IOUT0-15 and the least significant bits come out on ROUT0-15.

Complex Multiplier/Accumulator

The CMAC (Figure 2) performs two types of functions: complex multiplication/accumulation for modulation and demodulation of digital signals, and the operations necessary to implement an FFT butterfly. Modulation and demodulation are implemented using the complex multiplier and its associated accumulator; the rest of the circuitry in this section, i.e., the complex accumulator, input shifters and growth detect logic are used along with the complex multiplier/accumulator for FFTs. The complex multiplier performs the complex vector multiplication on the output of the Sine/Cosine Section and the vector represented by the real and imaginary inputs RIN and IIN. The two vectors are combined in the following manner:

ROUT = COS x RIN - SIN x IIN

IOUT = COS x IIN + SIN x RIN

RIN and IIN are latched into the input registers and passed through the shift stages. Clocking of the input registers is enabled with a low on $\overline{ENI}$. The amount of shift on the latched data is programmed with SH0-1 (Table 3). The output of the shifters is sent to the CMAC and the auxiliary accumulators.

TABLE 3. INPUT SHIFT SELECTION

SH1	SH0	SELECTED BITS
0	0	RIN0-15, IMIN0-15
0	1	RIN1-16, IMIN1-16
1	0	RIN2-17, IMIN2-17
1	1	RIN3-18, IMIN3-18

The 33-bit real and imaginary outputs of the Complex Multiplier are latched in the Multiplier Registers and then go through the Accumulator Section of the CMAC. If the ACC line is high, the feedback to the accumulators is enabled; a low on ACC zeroes the feedback path, so that the next set of real and imaginary data out of the complex multiplier is stored in the CMAC Output Registers.

The data in the CMAC Output Registers goes to the Multiplexer, the output of which is determined by the OUTMUX0-1 lines (Table 4). $\overline{BINFMT}$ controls whether the output of the Multiplexer is presented in two's complement or unsigned format; $\overline{BINFMT}$ = 0 inverts ROUT19 and IOUT19 for unsigned output, while $\overline{BINFMT}$ = 1 selects two's complement.

TABLE 4. OUTPUT MULTIPLEXER SELECTION

OUT MUX 1	OUT MUX 0	RO16-19	RO0-15	IO16-19	IO0-15
0	0	Real CMAC 31-34	Real CMAC 15-30	Imag CMAC 31-34	Imag CMAC 15-30
0	1	Real CMAC 31-34	0, Real CMAC 0-14	Imag CMAC 31-34	0, Imag CMAC 0-14
1	0	Real ACC 16-19	Real ACC 0-15	Imag ACC 16-19	Imag ACC 0-15
1	1	Reserved	Reserved	Reserved	Reserved

The Complex Accumulator duplicates the accumulator in the CMAC. The input comes from the data shifters, and its 20-bit complex output goes to the Multiplexer. ACC controls whether the accumulator is enabled or not. OUTMUX0-1 determines whether the accumulator output appears on ROUT and IOUT.

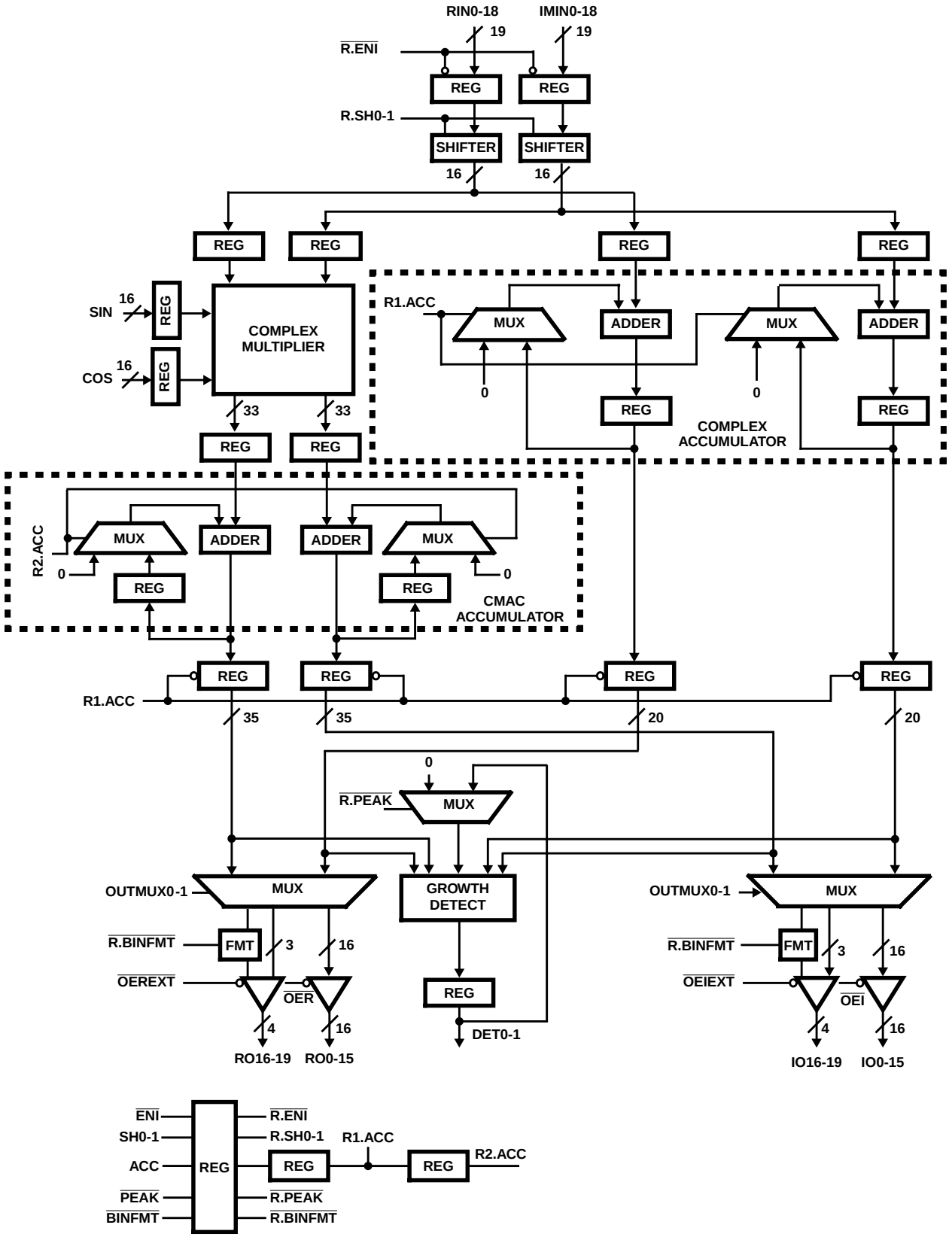


FIGURE 2. COMPLEX MULTIPLIER/ACCUMULATOR; ALL REGISTERS CLOCKED BY CLK

The Growth Detect circuitry outputs a two bit value that signifies the amount of growth on the data in the CMAC and Complex Accumulator. Its output, DET0-1, is encoded as shown in Table 5. If $\overline{PEAK}$ is low, the highest value of DET0-1 is latched in the Growth Detect Output Register.

The relative weighting of the bits at the inputs and outputs of the CMAC is shown in Figure 3. Note that the binary point of the sine, cosine, RIN and IIN is to the right of the most significant bit, while the binary point of RO and IO is to the right of the fifth most significant bit. These CMAC external input and output busses are aligned with each other to facilitate cascading NCOMs for FFT applications.

TABLE 5. GROWTH ENCODING

DET 1	DET 0	NUMBER OF BITS OF GROWTH ABOVE 2^0
0	0	0
0	1	1
1	0	2
1	1	3

SIN/COS INPUT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	. 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

↑ Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR INPUT (RIN, IIN)
SH = 00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	. 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

↑ Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 00

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	-2^0	. 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

↑ Radix Point

COMPLEX MULTIPLIER/ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 01

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	0

COMPLEX ACCUMULATOR OUTPUT (RO, IO)
OUTMUX = 10

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^4	2^3	2^2	2^1	-2^0	. 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

↑ Radix Point

FIGURE 3. BIT WEIGHTING

Applications

The NCOM can be used for Amplitude, Phase and Frequency modulation, as well as in variations and combinations of these techniques, such as QAM. It is most effective in applications requiring multiplication of a rotating complex sinusoid by an external vector. These include AM and QAM modulators and digital receivers. The NCOM implements AM and QAM modulation on a single chip, and is a element in demodulation, where it performs complex down conversion. It can be combined with the Intersil HSP43220 Decimating Digital Filter to form the front end of a digital receiver.

Modulation/Demodulation

Figure 4 shows a block diagram of an AM modulator. In this example, the phase increment for the carrier frequency is loaded into the center frequency register, and the modulating input is clocked into the real input of the CMAC, with the imaginary input set to 0. The modulated output is obtained at the real output of the CMAC. With a sixteen bit, two's complement signal input, the output will be a 16-bit real number, on ROUT0-15 (with OUTMUX = 00).

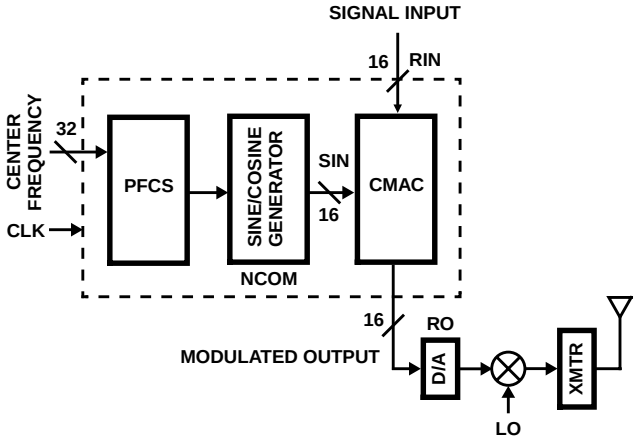


FIGURE 4. AMPLITUDE MODULATION

By replacing the real input with a complex vector, a similar setup can generate QAM signals (Figure 5). In this case, the carrier frequency is loaded into the center frequency register as before, but the modulating vector now carries both amplitude and phase information. Since the input vector and the internally generated sine and cosine waves are both 16 bits, the number of states is only limited by the characteristics of the transmission medium and by the analog electronics in the transmitter and receiver.

The phase and amplitude resolution for the Sine/Cosine section (16-bit output), delivers a spectral purity of greater than 90dBc. This means that the unwanted spectral components due to phase uncertainty (phase noise) will be greater than 90dB below the desired output (dBc, decibels below the carrier). With a 32-bit phase accumulator in the Phase/Frequency Control Section, the frequency tuning resolution equals the clock frequency divided by 2^{32}. For example, a 25MHz clock gives a tuning resolution of 0.006Hz.

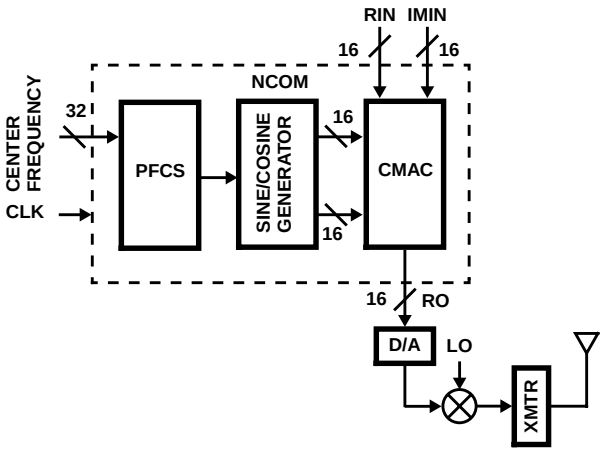


FIGURE 5. QUADRATURE AMPLITUDE MODULATION (QAM)

The NCOM also works with the HSP43220 Decimating Digital Filter to implement down conversion and low pass filtering in a digital receiver (Figure 6). The NCOM performs complex down conversion on the wideband input signal by multiplying the input vector and the internally generated complex sinusoid. The resulting signal has components at twice the center frequency and at DC. Two HSP43220s, one each on the real and imaginary outputs of the HSP45116, perform low pass filtering and decimation on the down converted data, resulting in a complex baseband signal.

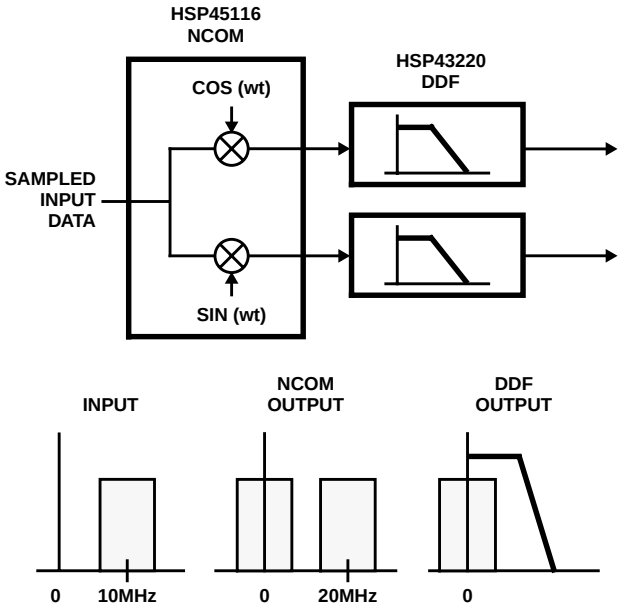


FIGURE 6. CHANNELIZED RECEIVER CHIP SET

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
MQFP Package	22.0	N/A
PGA Package	23.1	3

Maximum Junction Temperature
MQFP Package . . . . . 150^oC
PGA Package . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

Die Characteristics

Component Count . . . . . 103,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
High Level Clock Input	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Low Level Clock Input	V_{ILC}	V_{CC} = 4.75V	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400mA, V_{CC} = 4.75V	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = 2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 4	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 15MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Notes 2 and 4	-	182	mA

Capacitance $T_A = 25^oC$, Note 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Capacitance	C_{IN}	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground	-	15	pF
Output Capacitance	C_O		-	15	pF

NOTES:

2. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 10mA/MHz.
3. Not tested, but characterized at initial design and at major process/design changes.
4. Output load per test load circuit with switch open and C_L = 40pF.

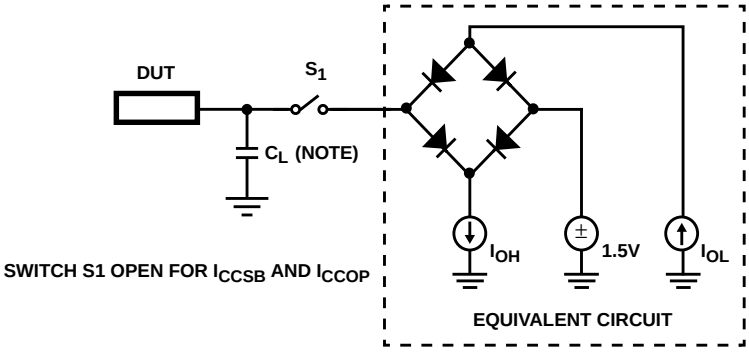
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (Note 5)

PARAMETER	SYMBOL	NOTES	-15 (15MHz)		-25 (25.6MHz)		-33 (33MHz)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		66	-	39	-	30	-	ns
CLK High	t_{CH}		26	-	15	-	12	-	ns
CLK Low	t_{CL}		26	-	15	-	12	-	ns
$\overline{WR}$ Low	t_{WL}		26	-	15	-	12	-	ns
$\overline{WR}$ High	t_{WH}		26	-	15	-	12	-	ns
Setup Time; AD0-1, $\overline{CS}$ to $\overline{WR}$ Going High	t_{AWS}		18	-	13	-	13	-	ns
Hold Time; AD0, AD1, $\overline{CS}$ from $\overline{WR}$ Going High	t_{AWH}		0	-	0	-	0	-	ns
Setup Time C0-15 from $\overline{WR}$ Going High	t_{CWS}		20	-	15	-	15	-	ns
Hold Time C0-15 from $\overline{WR}$ Going High	t_{CWH}		0	-	0	-	0	-	ns
Setup time $\overline{WR}$ High to CLK High	t_{WC}	7	20	-	16	-	12	-	ns
Setup Time MOD0-1 to CLK Going High	t_{MCS}		20	-	15	-	15	-	ns
Hold Time MOD0-1 from CLK Going High	t_{MCH}		0	-	0	-	0	-	ns
Setup Time $\overline{PACI}$ to CLK Going High	t_{PCS}		25	-	15	-	11	-	ns
Hold Time $\overline{PACI}$ from CLK Going High	t_{PCH}		0	-	0	-	0	-	ns
Setup $\overline{ENPHREG}$, $\overline{ENCFREG}$, $\overline{ENOFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{CLROFR}$, PMSEL, $\overline{LOAD}$, $\overline{ENI}$, ACC, $\overline{BINFMT}$, $\overline{PEAK}$, $\overline{MODPI/2PI}$, SH0-1, $\overline{RBYTILD}$ from CLK Going High	t_{ECS}		18	-	12	-	12	-	ns
Hold Time $\overline{ENPHREG}$, $\overline{ENCFREG}$, $\overline{ENOFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{CLROFR}$, PMSEL, $\overline{LOAD}$, $\overline{ENI}$, ACC, $\overline{BINFMT}$, $\overline{PEAK}$, $\overline{MODPI/2PI}$, SH0-1, $\overline{RBYTILD}$ from CLK Going High	t_{ECH}		0	-	0	-	0	-	ns
Setup Time RIN0-18, IMIN0-18 to CLK Going High	t_{DS}		18	-	12	-	12	-	ns
Hold Time RIN0-18, IMIN0-18 from CLK Going High	t_{DH}		0	-	0	-	0	-	ns
CLK to Output Delay RO0-19, IO0-19	t_{DO}		-	40	-	24	-	19	ns
CLK to Output Delay DET0-1	t_{DEO}		-	40	-	27	-	20	ns
CLK to Output Delay $\overline{PACO}$	t_{PO}		-	30	-	20	-	12	ns
CLK to Output Delay $\overline{TICO}$	t_{TO}		-	30	-	20	-	12	ns
Output Enable Time $\overline{OER}$, $\overline{OEI}$, $\overline{OEREXT}$, $\overline{OEIEXT}$	t_{OE}		-	25	-	20	-	20	ns
OUTMUX0-1 to Output Delay	t_{MD}		-	40	-	28	-	26	ns
Output Disable Time	t_{OD}	6	-	20	-	15	-	15	ns
Output Rise, Fall Time	t_{RF}	6	-	8	-	8	-	6	ns

NOTES:

5. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; input levels (all other inputs) 0V and 3.0V; timing reference levels (CLK) 2.0V; all others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.
6. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
7. Applicable only when outputs are being monitored and $\overline{ENCFREG}$, $\overline{ENPHREG}$, or $\overline{ENTIREG}$ is active.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

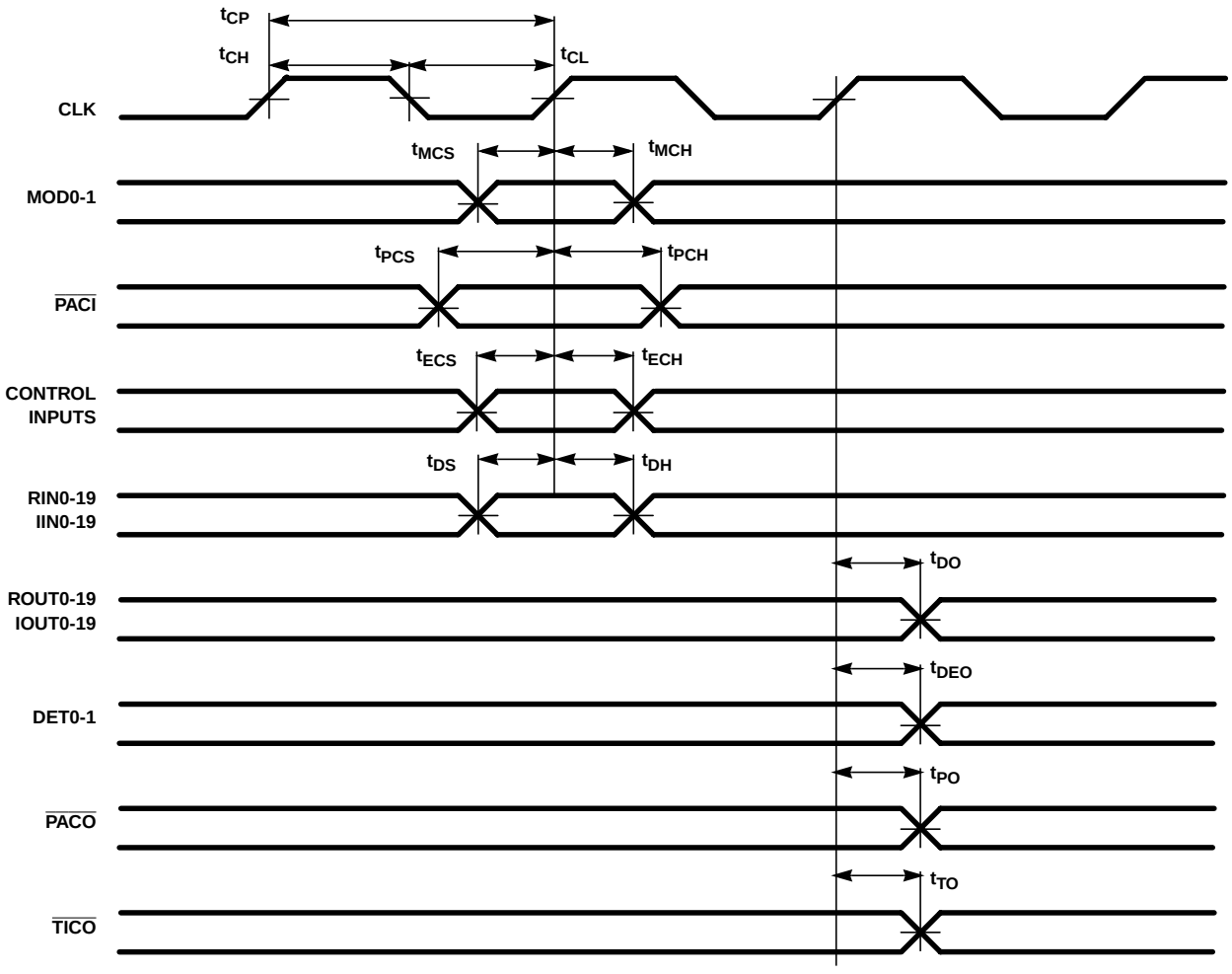


FIGURE 7. INPUT AND OUTPUT TIMING

Waveforms (Continued)

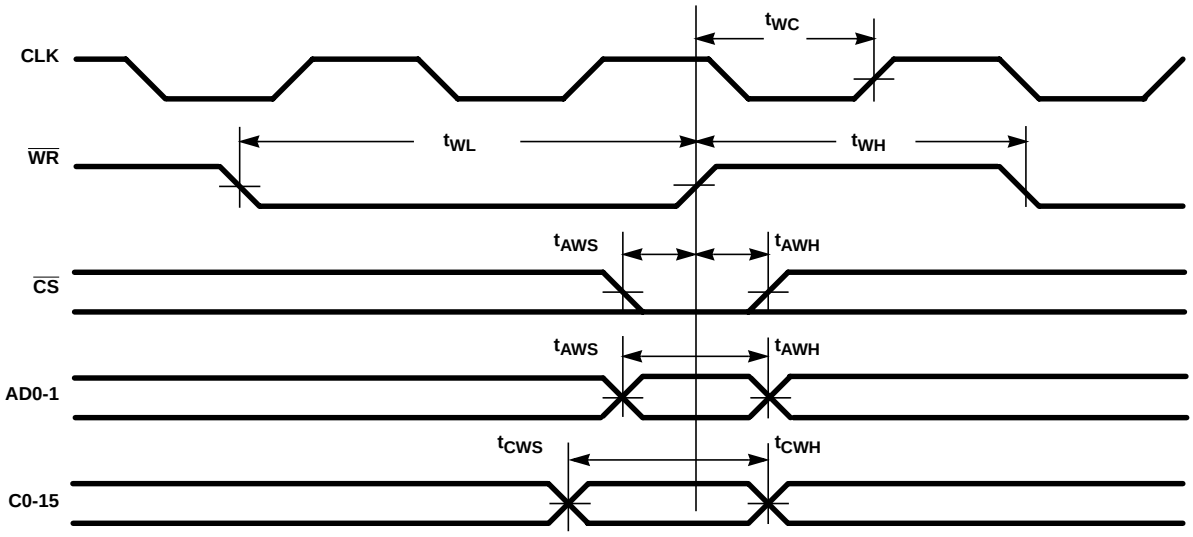


FIGURE 8. CONTROL BUS TIMING

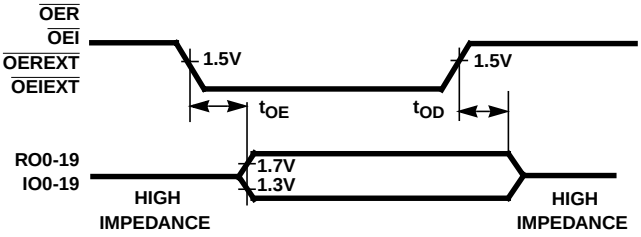


FIGURE 9. OUTPUT ENABLE, DISABLE TIMING

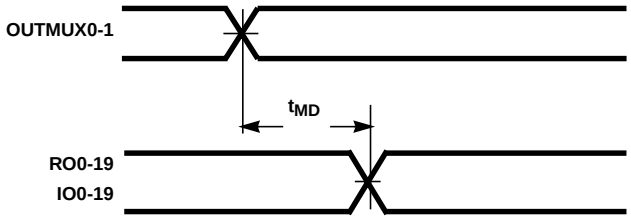


FIGURE 10. MULTIPLEXER TIMING

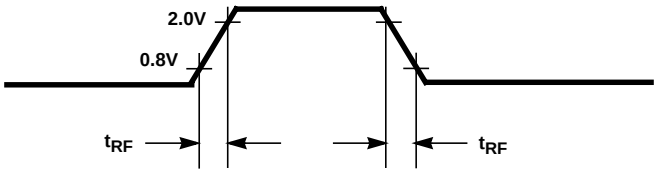


FIGURE 11. OUTPUT RISE AND FALL TIMES

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