



RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 50 W RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1995 MHz.

1800 MHz

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQ} = 1800$ mA, $P_{out} = 50$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

| Frequency | G_{ps} (dB) | η_D (%) | Output PAR (dB) | ACPR (dBc) | IRL (dB) |
|-----------|---------------|--------------|-----------------|------------|----------|
| 1805 MHz | 18.4 | 27.2 | 7.1 | -35.2 | -11 |
| 1840 MHz | 19.3 | 28.0 | 7.1 | -35.0 | -24 |
| 1880 MHz | 19.6 | 29.3 | 7.0 | -34.0 | -14 |

1900 MHz

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQ} = 1800$ mA, $P_{out} = 50$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

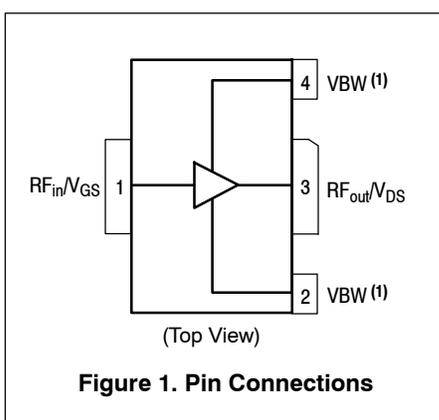
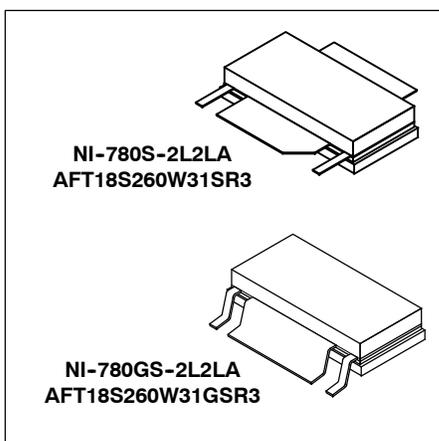
| Frequency | G_{ps} (dB) | η_D (%) | Output PAR (dB) | ACPR (dBc) | IRL (dB) |
|-----------|---------------|--------------|-----------------|------------|----------|
| 1930 MHz | 19.0 | 25.1 | 6.8 | -34.2 | -20 |
| 1960 MHz | 19.3 | 25.6 | 6.9 | -34.5 | -18 |
| 1995 MHz | 19.6 | 26.6 | 6.8 | -33.9 | -12 |

Features

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications

AFT18S260W31SR3
AFT18S260W31GSR3

1805–1995 MHz, 50 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS



1. Device can operate with the V_{DD} current supplied through pin 2 or pin 4 alone.

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|----------------------------------------------------------------------------|-----------|-------------|-----------|
| Drain-Source Voltage | V_{DSS} | -0.5, +65 | Vdc |
| Gate-Source Voltage | V_{GS} | -6.0, +10 | Vdc |
| Operating Voltage | V_{DD} | 32, +0 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Case Operating Temperature Range | T_C | -40 to +125 | °C |
| Operating Junction Temperature Range (1,2) | T_J | -40 to +225 | °C |
| CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | CW | 168 1.1 | W W/°C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------------|------|
| Thermal Resistance, Junction to Case Case Temperature 91°C , 50 W CW, 28 Vdc, $I_{DQ} = 1800\text{ mA}$, 1840 MHz | $R_{\theta JC}$ | 0.32 | °C/W |

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|-------|
| Human Body Model (per JESD22-A114) | 2 |
| Machine Model (per EIA/JESD22-A115) | B |
| Charge Device Model (per JESD22-C101) | IV |

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics

| | | | | | |
|---------------------------------------------------------------------------------------------------|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 5 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μAdc |

On Characteristics

| | | | | | |
|----------------------------------------------------------------------------------------------------------------|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 360\ \mu\text{Adc}$) | $V_{GS(th)}$ | 0.8 | 1.2 | 1.6 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1800\text{ mAdc}$, Measured in Functional Test) | $V_{GS(Q)}$ | 1.4 | 1.8 | 2.2 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.6\text{ Adc}$) | $V_{DS(on)}$ | 0.1 | 0.15 | 0.3 | Vdc |

Functional Tests (4,5) (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1800\text{ mA}$, $P_{out} = 50\text{ W Avg.}$, $f = 1880\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

| | | | | | |
|----------------------------------------------------------|----------|------|-------|-------|-----|
| Power Gain | G_{ps} | 18.5 | 19.6 | 21.0 | dB |
| Drain Efficiency | η_D | 26.0 | 29.3 | — | % |
| Output Peak-to-Average Ratio @ 0.01% Probability on CCDF | PAR | 6.3 | 7.0 | — | dB |
| Adjacent Channel Power Ratio | ACPR | — | -34.0 | -30.0 | dBc |
| Input Return Loss | IRL | — | -14 | -6 | dB |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to [AN1955](#), *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Part internally matched both on input and output.
5. Measurements made with device in straight lead configuration, before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

(continued)

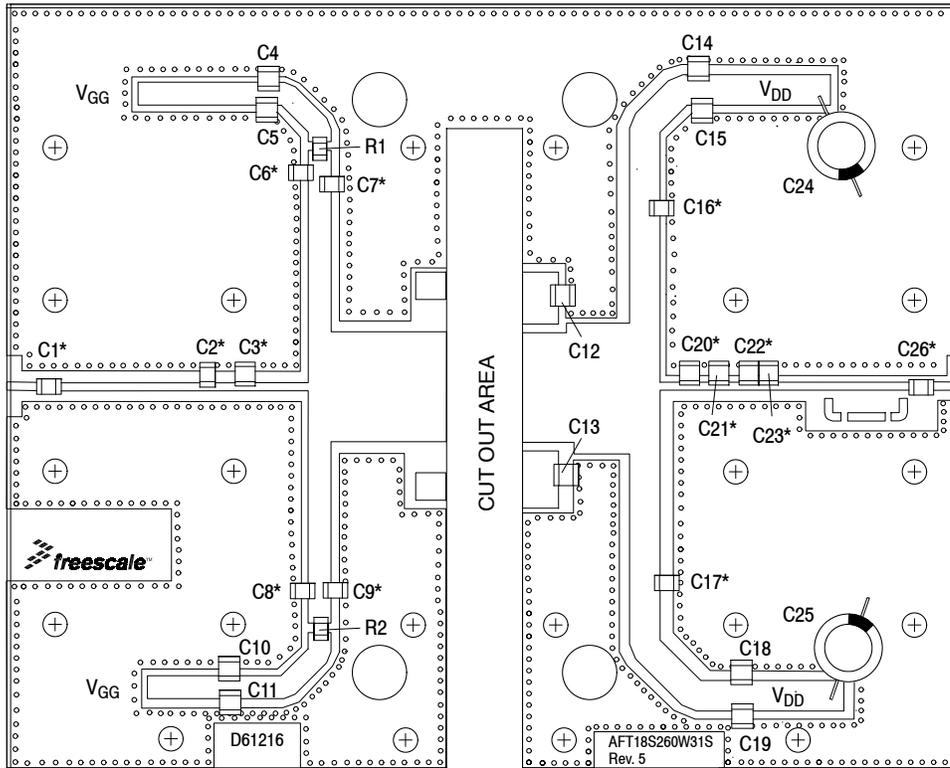
Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|--------------------|-----|-------|
| Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 1800\text{ mA}$, $f = 1840\text{ MHz}$ | | | | | |
| VSWR 10:1 at 32 Vdc, 269 W CW ⁽¹⁾ Output Power (3 dB Input Overdrive from 229 W CW ⁽¹⁾ Rated Power) | No Device Degradation | | | | |
| Typical Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1800\text{ mA}$, 1805–1880 MHz Bandwidth | | | | | |
| P_{out} @ 1 dB Compression Point, CW | P1dB | — | 229 ⁽¹⁾ | — | W |
| AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.) | Φ | — | -13 | — | ° |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | VBW _{res} | — | 85 | — | MHz |
| Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 50\text{ W Avg.}$ | G _F | — | 1.2 | — | dB |
| Gain Variation over Temperature (-30°C to +85°C) | ΔG | — | 0.001 | — | dB/°C |
| Output Power Variation over Temperature (-30°C to +85°C) ⁽¹⁾ | $\Delta P1dB$ | — | 0.011 | — | dB/°C |

Table 5. Ordering Information

| Device | Tape and Reel Information | Package |
|------------------|-------------------------------------------------------|----------------|
| AFT18S260W31SR3 | R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel | NI-780S-2L2LA |
| AFT18S260W31GSR3 | | NI-780GS-2L2LA |

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C1, C2, C3, C6, C7, C8, C9, C16, C17, C20, C21, C22, C23, and C26 are mounted vertically.

Figure 2. AFT18S260W31SR3 Test Circuit Component Layout

Table 6. AFT18S260W31SR3 Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|------------------------------------------------|---------------------------------------------|----------------------|--------------|
| C1, C6, C7, C9, C10, C17, C18, C19, C20, C26 | 8.2 pF Chip Capacitors | ATC100B8R2CT500XT | ATC |
| C2 | 1.0 pF Chip Capacitor | ATC100B1R0BT500XT | ATC |
| C3 | 0.3 pF Chip Capacitor | ATC100B0R3BT500XT | ATC |
| C4, C5, C11, C12, C13, C14, C15, C16, C21, C22 | 10 μ F Chip Capacitors | GRM32ER61H106KA12L | Murata |
| C8 | 0.5 pF Chip Capacitor | ATC100B0R5BT500XT | ATC |
| C23 | 2.0 pF Chip Capacitor | ATC100B2R0BT500XT | ATC |
| C24, C25 | 470 μ F, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| R1, R2 | 2.37 Ω , 1/4 W Chip Resistors | CRCW12062R37FNEA | Vishay |
| PCB | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D61216 | MTL |

TYPICAL CHARACTERISTICS — 1805–1880 MHz

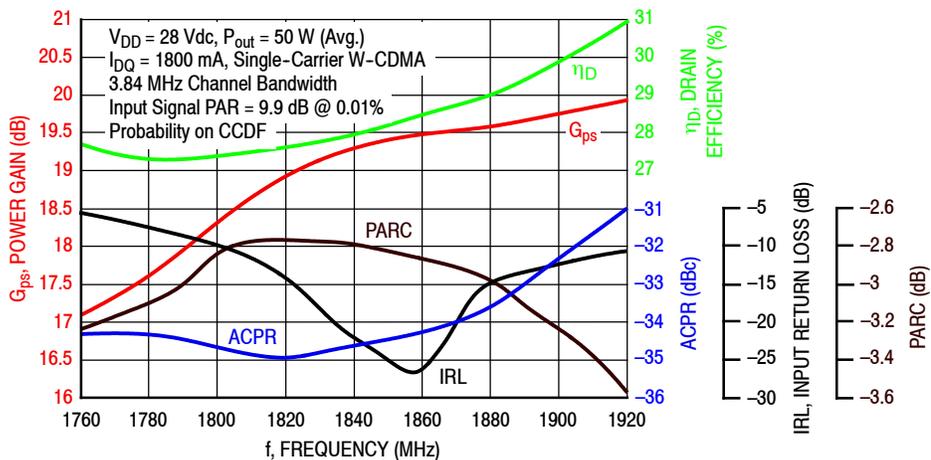


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 50$ Watts Avg.

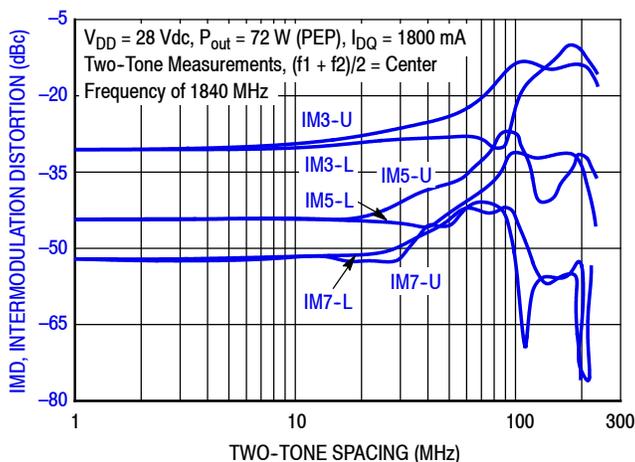


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

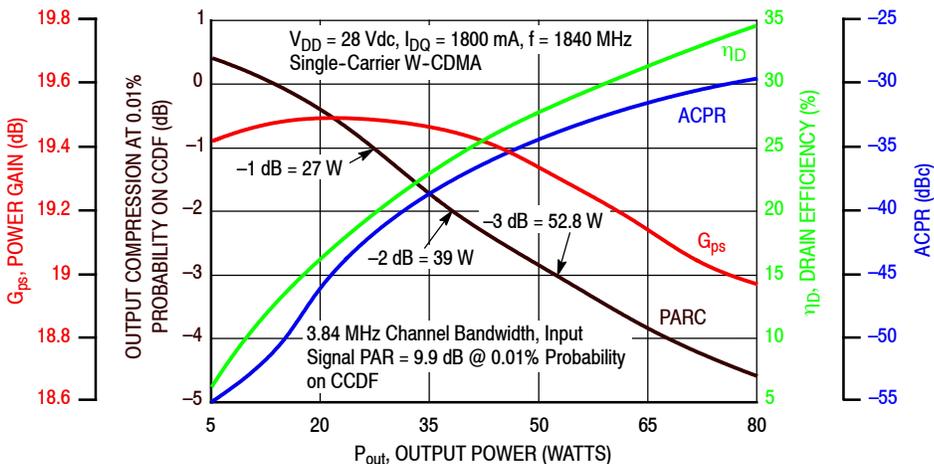


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

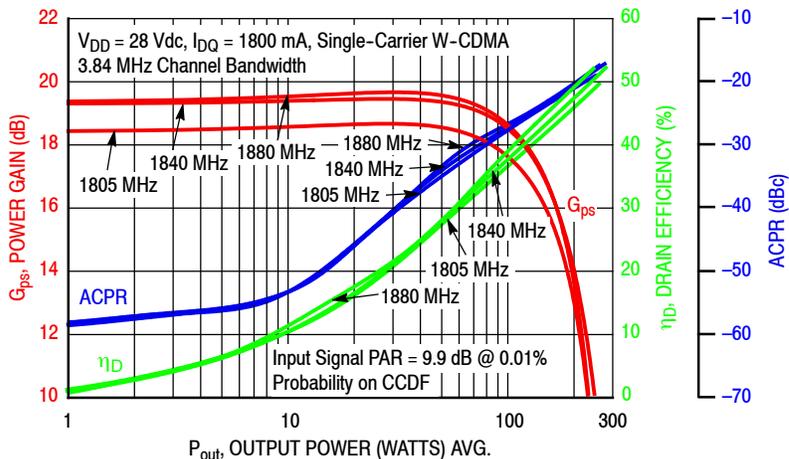


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

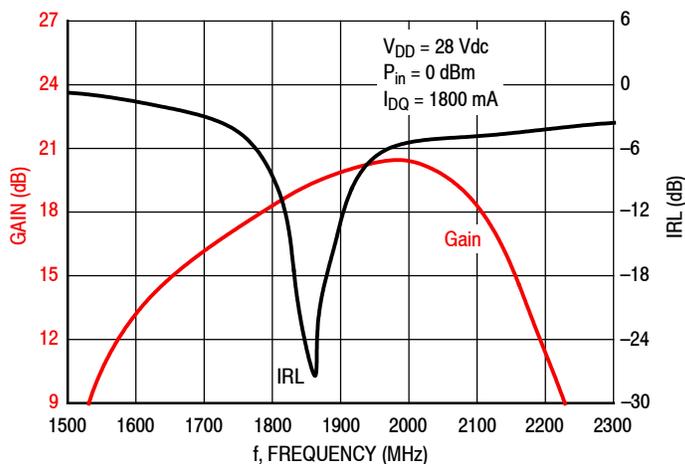


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 2110 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(ON)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1805 | $0.90 - j2.84$ | $0.93 + j2.68$ | $1.10 - j3.64$ | 18.1 | 55.0 | 313 | 52.8 | -10 |
| 1840 | $0.88 - j2.79$ | $1.07 + j2.71$ | $1.06 - j3.72$ | 18.1 | 54.9 | 307 | 51.2 | -10 |
| 1880 | $1.12 - j2.86$ | $1.35 + j2.80$ | $1.06 - j3.80$ | 18.2 | 54.5 | 284 | 50.8 | -10 |

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1805 | $0.90 - j2.84$ | $0.90 + j2.82$ | $1.10 - j3.82$ | 15.9 | 55.7 | 373 | 53.1 | -15 |
| 1840 | $0.88 - j2.79$ | $1.06 + j2.85$ | $1.11 - j3.88$ | 16.0 | 55.6 | 366 | 52.5 | -16 |
| 1880 | $1.12 - j2.86$ | $1.37 + j2.97$ | $1.06 - j3.92$ | 16.0 | 55.4 | 344 | 51.6 | -15 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 2110 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(ON)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1805 | $0.90 - j2.84$ | $0.87 + j2.65$ | $1.70 - j2.31$ | 20.9 | 52.9 | 195 | 63.1 | -17 |
| 1840 | $0.88 - j2.79$ | $1.02 + j2.70$ | $1.59 - j2.46$ | 20.9 | 53.0 | 200 | 62.1 | -17 |
| 1880 | $1.12 - j2.86$ | $1.32 + j2.81$ | $1.48 - j2.63$ | 20.8 | 52.8 | 190 | 60.3 | -16 |

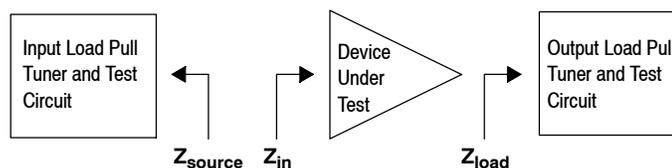
| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1805 | $0.90 - j2.84$ | $0.85 + j2.75$ | $1.55 - j2.50$ | 18.5 | 54.0 | 251 | 64.1 | -25 |
| 1840 | $0.88 - j2.79$ | $1.02 + j2.84$ | $1.50 - j2.56$ | 18.7 | 53.9 | 245 | 63.2 | -25 |
| 1880 | $1.12 - j2.86$ | $1.34 + j2.97$ | $1.47 - j2.79$ | 18.6 | 53.8 | 240 | 61.0 | -24 |

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

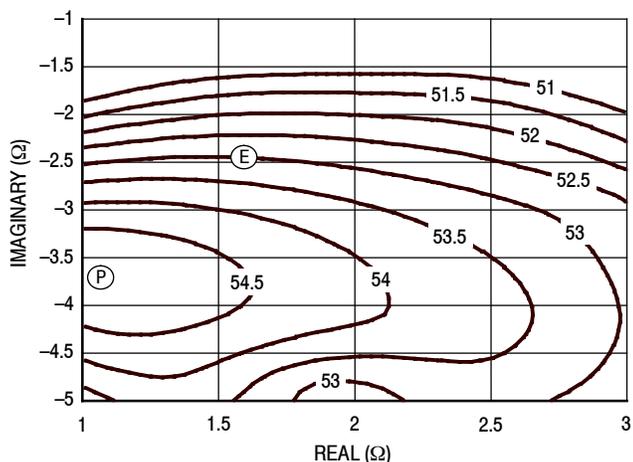


Figure 8. P1dB Load Pull Output Power Contours (dBm)

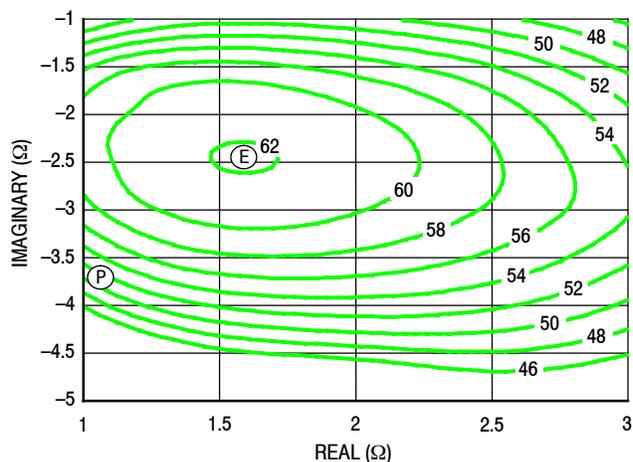


Figure 9. P1dB Load Pull Efficiency Contours (%)

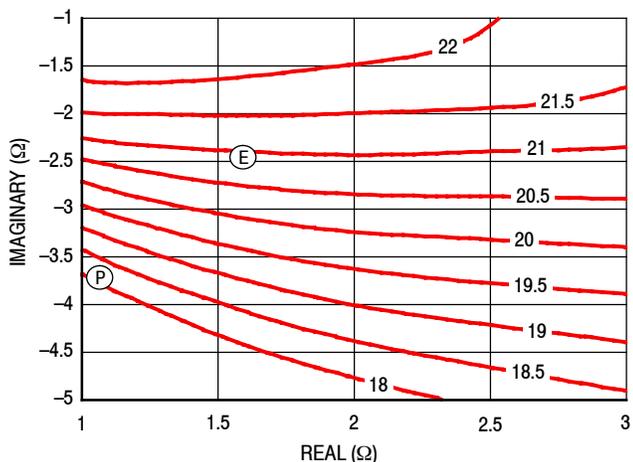


Figure 10. P1dB Load Pull Gain Contours (dB)

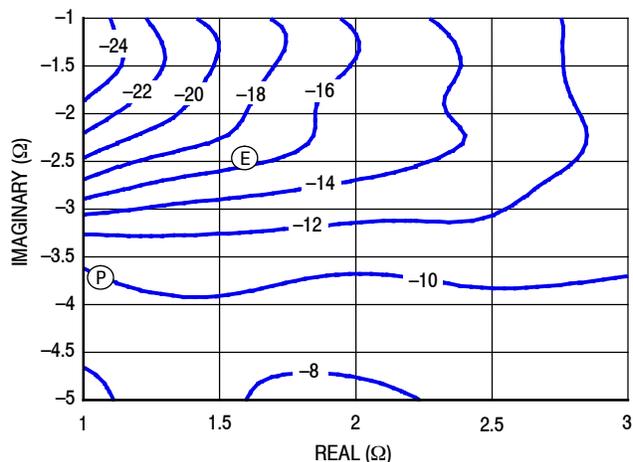


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

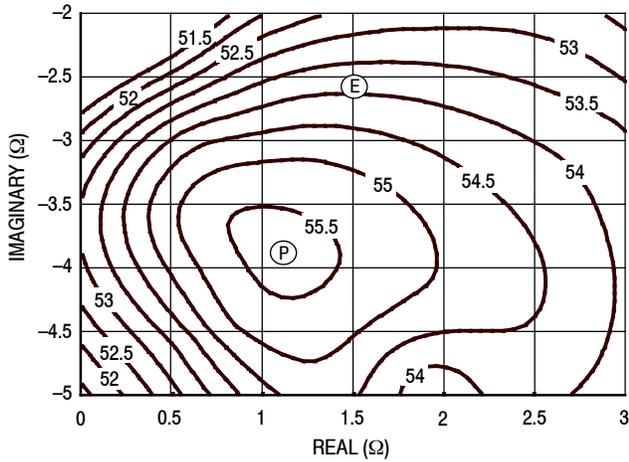


Figure 12. P3dB Load Pull Output Power Contours (dBm)

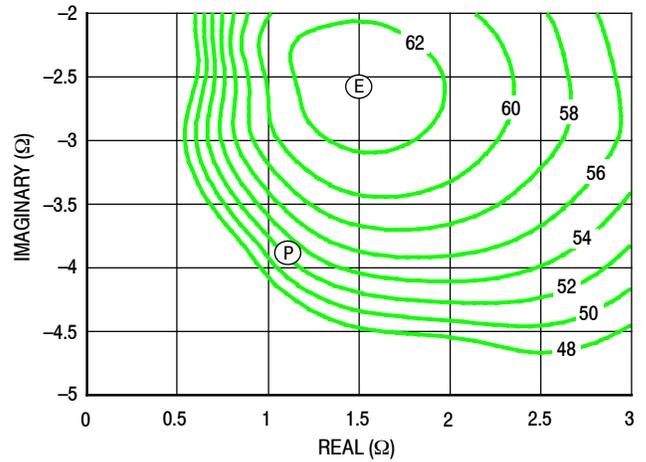


Figure 13. P3dB Load Pull Efficiency Contours (%)

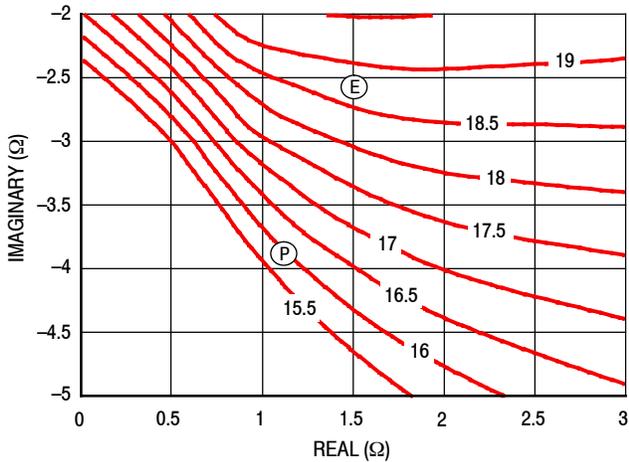


Figure 14. P3dB Load Pull Gain Contours (dB)

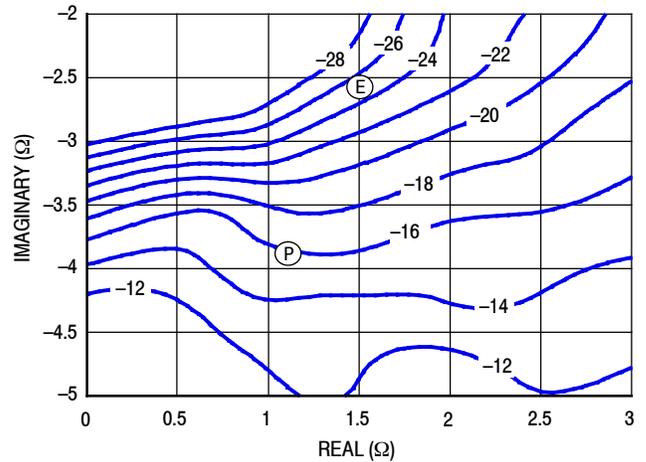
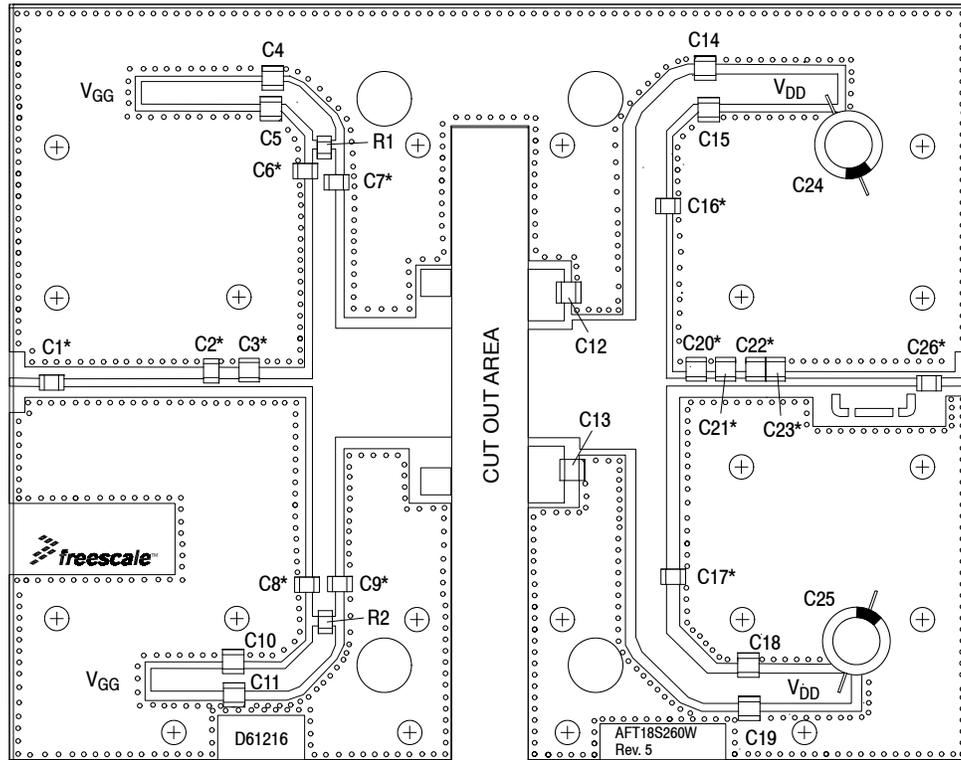


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power



*C1, C2, C3, C6, C7, C8, C9, C16, C17, C20, C21, C22, C23, and C26 are mounted vertically.

Figure 16. AFT18S260W31SR3 Test Circuit Component Layout — 1930–1995 MHz

Table 9. AFT18S260W31SR3 Test Circuit Component Designations and Values — 1930–1995 MHz

| Part | Description | Part Number | Manufacturer |
|------------------------------------------------|---------------------------------------------|----------------------|--------------|
| C1, C26 | 10 pF Chip Capacitors | ATC100B100JT500XT | ATC |
| C2, C3 | 1.2 pF Chip Capacitors | ATC100B1R2BT500XT | ATC |
| C4, C5, C10, C11, C12, C13, C14, C15, C18, C19 | 10 μ F, Chip Capacitors | GRM32ER61H106KA12L | Murata |
| C6, C7, C8, C9 | 7.5 pF Chip Capacitors | ATC100B7R5CT500XT | ATC |
| C16, C17 | 8.2 pF Chip Capacitors | ATC100B8R2CT500XT | ATC |
| C20, C23 | 0.5 pF Chip Capacitors | ATC100B0R5BT500XT | ATC |
| C21 | 2.2 pF Chip Capacitor | ATC100B2R2JT500XT | ATC |
| C22 | 0.3 pF Chip Capacitor | ATC100B0R3BT500XT | ATC |
| C24, C25 | 470 μ F, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| R1, R2 | 2.37 Ω , 1/4 W Chip Resistors | CRCW12062R37FNEA | Vishay |
| PCB | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D61216 | MTL |

TYPICAL CHARACTERISTICS — 1930–1995 MHz

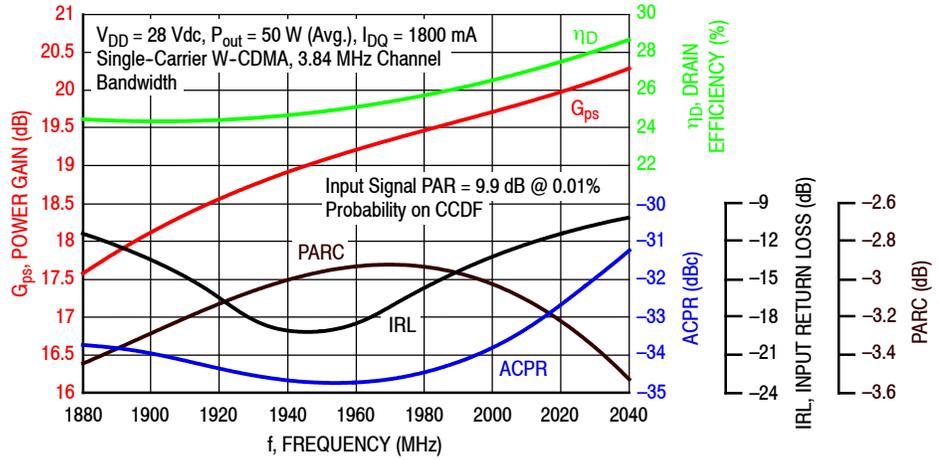


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 50$ Watts Avg.

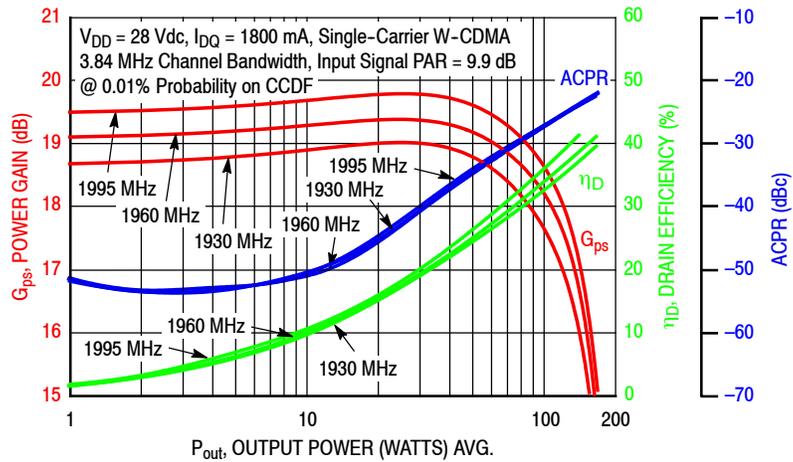


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

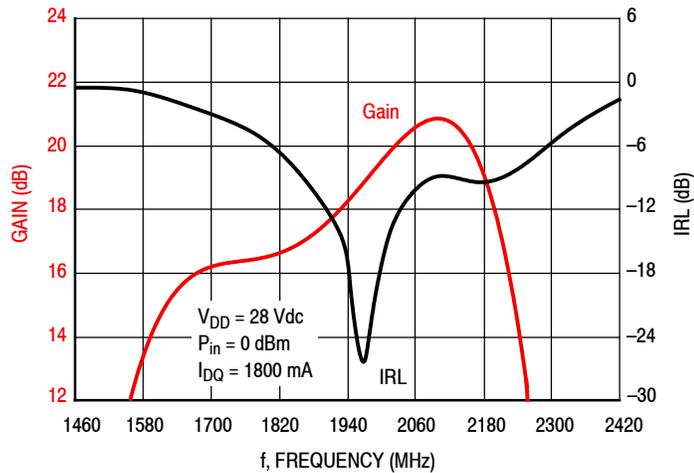


Figure 19. Broadband Frequency Response

Table 10. Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 2107 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(ON)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1930 | $1.49 - j3.03$ | $1.79 + j2.85$ | $1.11 - j4.04$ | 18.6 | 54.5 | 284 | 50.7 | -10 |
| 1960 | $1.62 - j3.06$ | $2.11 + j2.78$ | $1.12 - j4.30$ | 18.5 | 54.5 | 282 | 49.5 | -11 |
| 1995 | $1.98 - j2.99$ | $2.53 + j2.49$ | $1.21 - j4.65$ | 18.5 | 54.3 | 270 | 47.1 | -10 |

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Output Power | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1930 | $1.49 - j3.03$ | $1.88 + j3.04$ | $1.11 - j4.22$ | 16.2 | 55.3 | 342 | 50.4 | -16 |
| 1960 | $1.62 - j3.06$ | $2.26 + j2.97$ | $1.16 - j4.40$ | 16.4 | 55.3 | 340 | 50.9 | -16 |
| 1995 | $1.98 - j2.99$ | $2.76 + j2.61$ | $1.26 - j4.71$ | 16.5 | 55.2 | 329 | 49.2 | -16 |

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 11. Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 2107 \text{ mA}$, Pulsed CW, $10 \mu\text{sec(ON)}$, 10% Duty Cycle

| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P1dB | | | | | |
| | | | $Z_{\text{load}}^{(1)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1930 | $1.49 - j3.03$ | $1.73 + j2.80$ | $1.33 - j2.89$ | 21.2 | 52.8 | 193 | 60.7 | -18 |
| 1960 | $1.62 - j3.06$ | $2.00 + j2.70$ | $1.39 - j3.00$ | 21.3 | 52.7 | 186 | 59.9 | -17 |
| 1995 | $1.98 - j2.99$ | $2.36 + j2.41$ | $1.43 - j3.39$ | 21.1 | 52.8 | 189 | 56.7 | -15 |

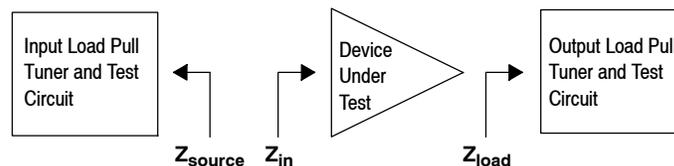
| f (MHz) | $Z_{\text{source}} (\Omega)$ | $Z_{\text{in}} (\Omega)$ | Max Drain Efficiency | | | | | |
|---------|------------------------------|--------------------------|----------------------------------|-----------|-------|-----|--------------|-----------|
| | | | P3dB | | | | | |
| | | | $Z_{\text{load}}^{(2)} (\Omega)$ | Gain (dB) | (dBm) | (W) | η_D (%) | AM/PM (°) |
| 1930 | $1.49 - j3.03$ | $1.84 + j3.00$ | $1.33 - j3.00$ | 19.1 | 53.7 | 237 | 61.6 | -26 |
| 1960 | $1.62 - j3.06$ | $2.20 + j2.87$ | $1.39 - j3.09$ | 19.1 | 53.6 | 230 | 61.1 | -25 |
| 1995 | $1.98 - j2.99$ | $2.64 + j2.48$ | $1.38 - j3.43$ | 19.1 | 53.7 | 235 | 58.5 | -22 |

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


P1dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

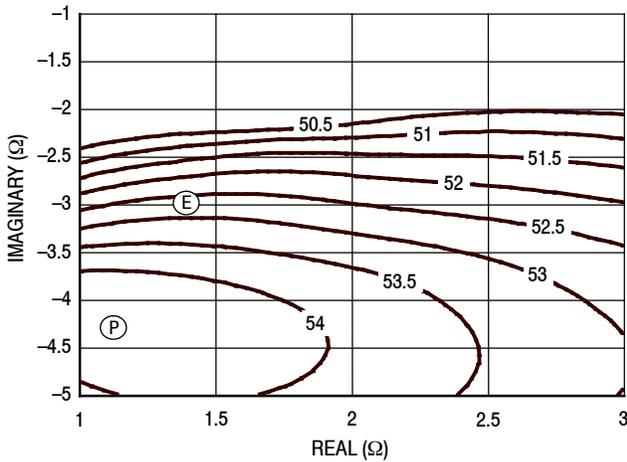


Figure 20. P1dB Load Pull Output Power Contours (dBm)

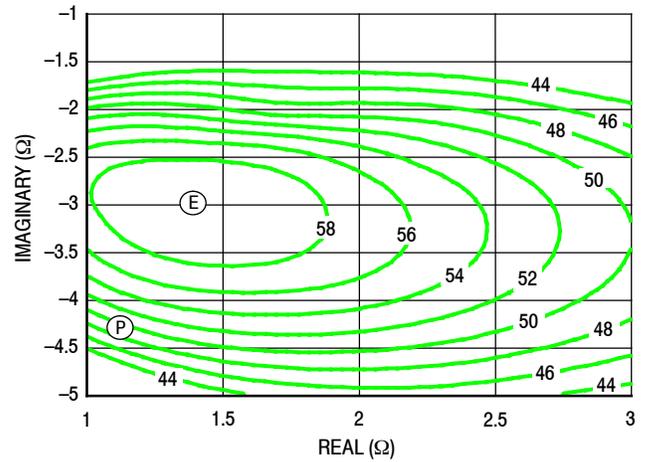


Figure 21. P1dB Load Pull Efficiency Contours (%)

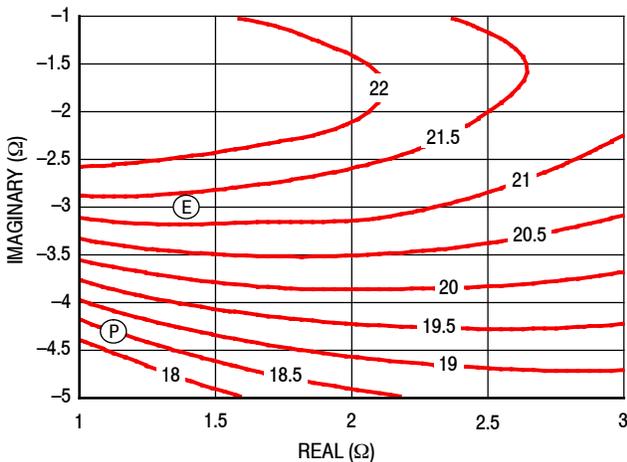


Figure 22. P1dB Load Pull Gain Contours (dB)

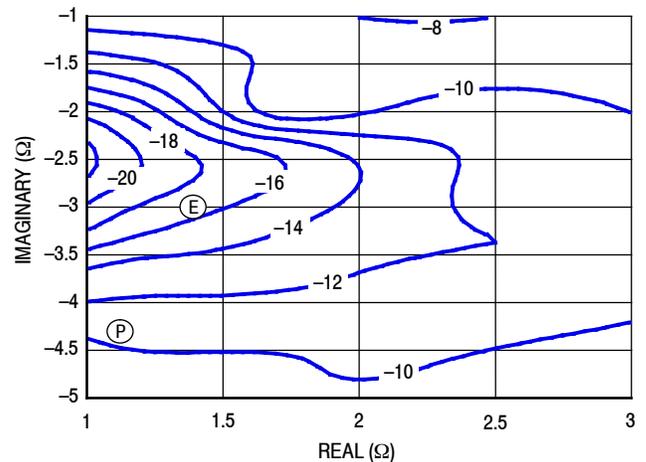


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

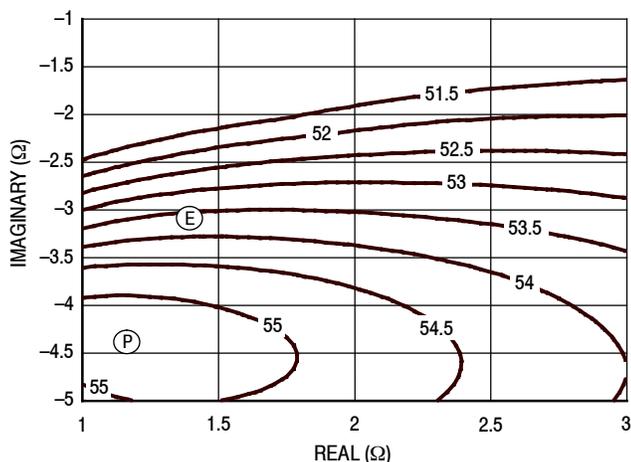


Figure 24. P3dB Load Pull Output Power Contours (dBm)

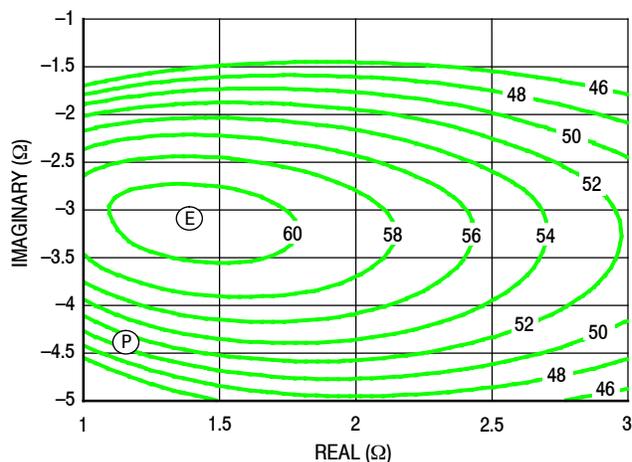


Figure 25. P3dB Load Pull Efficiency Contours (%)

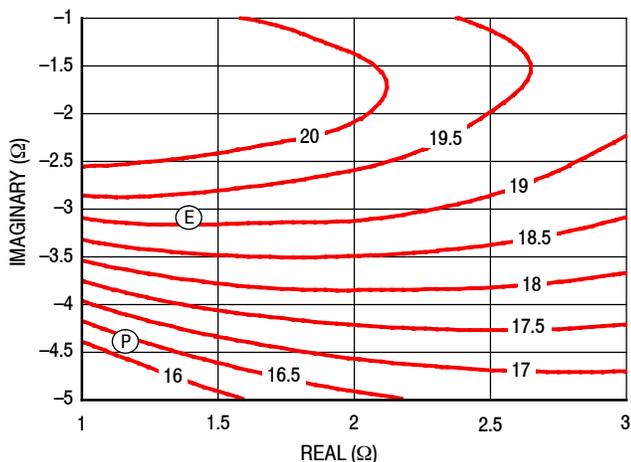


Figure 26. P3dB Load Pull Gain Contours (dB)

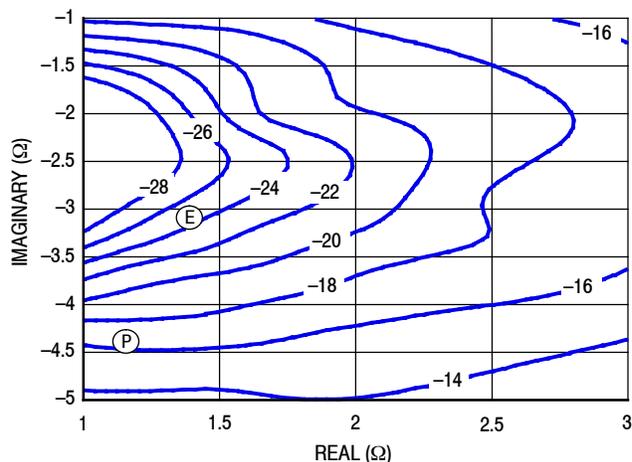
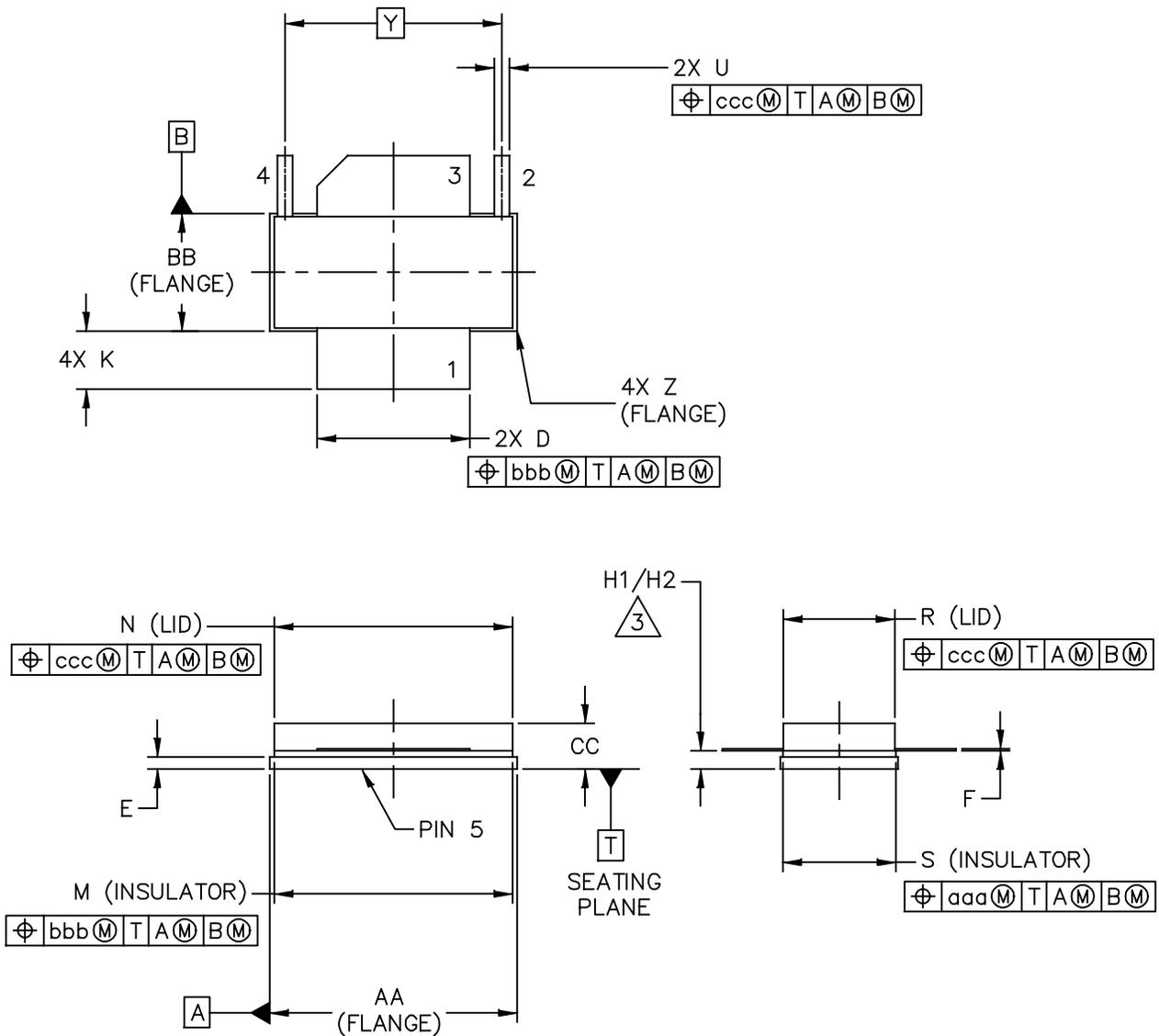


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



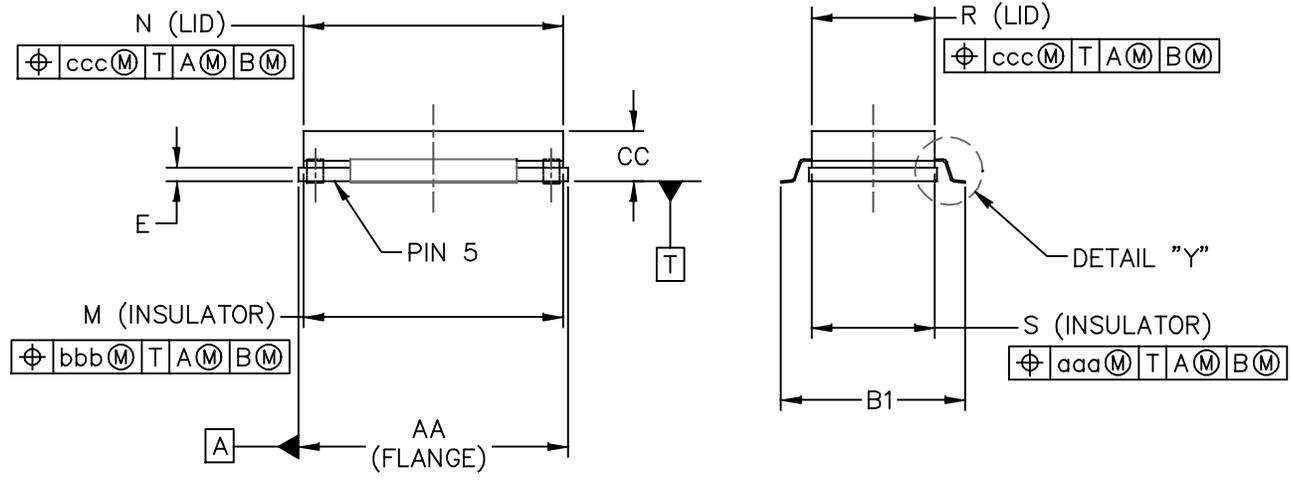
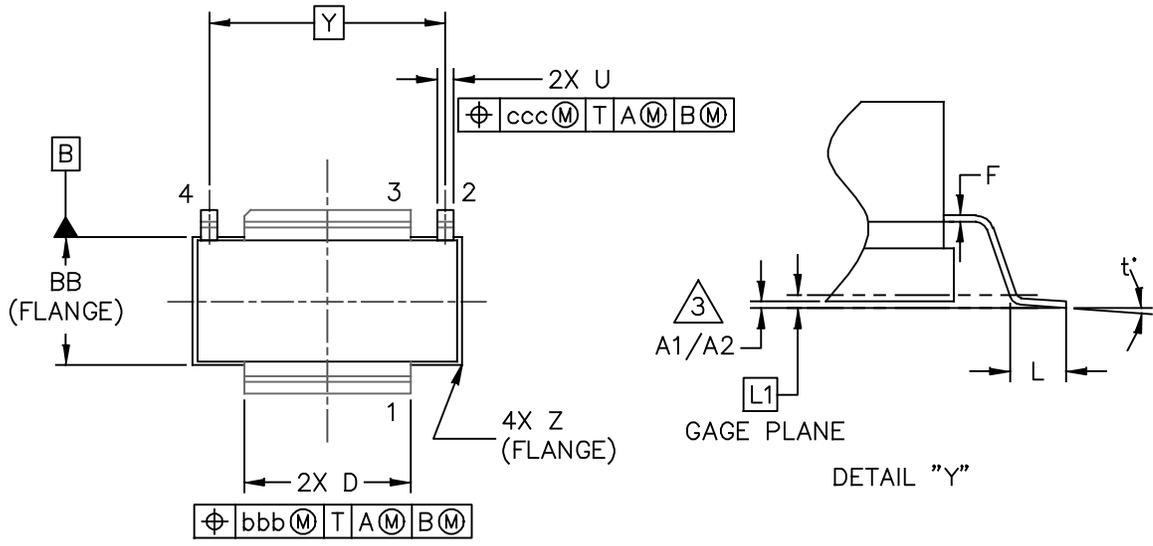
| | | |
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| | STANDARD: NON-JEDEC | |
| | 05 DEC 2014 | |

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM THE FLANGE TO CLEAR THE EPOXY FLOW OUT REGION PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|---------------------------------------------------------|------|------|--------------------|-------|--------------------------------------|----------------------------|-------|------------|-------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| AA | .805 | .815 | 20.45 | 20.70 | R | .365 | .375 | 9.27 | 9.53 |
| BB | .380 | .390 | 9.65 | 9.91 | S | .365 | .375 | 9.27 | 9.53 |
| CC | .125 | .170 | 3.18 | 4.32 | U | .045 | .055 | 1.14 | 1.40 |
| D | .495 | .505 | 12.57 | 12.83 | Y | .710 BSC | | 18.03 BSC | |
| E | .035 | .045 | 0.89 | 1.14 | Z | R.000 | R.040 | R0.00 | R1.02 |
| F | .003 | .007 | 0.08 | 0.18 | aaa | .005 | | 0.13 | |
| H1 | .057 | .067 | 1.45 | 1.70 | bbb | .010 | | 0.25 | |
| H2 | .054 | .070 | 1.37 | 1.78 | ccc | .015 | | 0.38 | |
| K | .170 | .210 | 4.32 | 5.33 | | | | | |
| M | .774 | .786 | 19.66 | 19.96 | | | | | |
| N | .772 | .788 | 19.61 | 20.02 | | | | | |
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| | | | | | 05 DEC 2014 | | | | |



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NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSION A1/A2 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM. A1 APPLIES TO PINS 1 AND 3. A2 APPLIES TO PINS 2 AND 4.

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|---------------------------------------------------------|----------|------|--------------------|-------|--------------------------------------|----------------------------|-------|------------|-------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| AA | .805 | .815 | 20.45 | 20.70 | R | .365 | .375 | 9.27 | 9.53 |
| A1 | .002 | .008 | 0.05 | 0.20 | S | .365 | .375 | 9.27 | 9.53 |
| A2 | .002 | .008 | 0.05 | 0.20 | U | .045 | .055 | 1.14 | 1.40 |
| BB | .380 | .390 | 9.65 | 9.91 | Y | .710 BSC | | 18.03 BSC | |
| B1 | .546 | .562 | 13.87 | 14.27 | Z | R.000 | R.040 | R0.00 | R1.02 |
| CC | .125 | .170 | 3.18 | 4.32 | t' | 0' | 8' | 0' | 8' |
| D | .495 | .505 | 12.57 | 12.83 | aaa | .005 | | 0.13 | |
| E | .035 | .045 | 0.89 | 1.14 | bbb | .010 | | 0.25 | |
| F | .003 | .007 | 0.08 | 0.18 | ccc | .015 | | 0.38 | |
| L | .038 | .046 | 0.97 | 1.17 | | | | | |
| L1 | .010 BSC | | 0.25 BSC | | | | | | |
| M | .774 | .786 | 19.66 | 19.96 | | | | | |
| N | .772 | .788 | 19.61 | 20.02 | | | | | |
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| TITLE: NI-780GS-2L2LA | | | | | DOCUMENT NO: 98ASA00624D REV: 0 | | | | |
| | | | | | STANDARD: NON-JEDEC | | | | |
| | | | | | 05 DEC 2014 | | | | |

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|---------------------------------|
| 0 | Apr. 2015 | • Initial Release of Data Sheet |

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