Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 256K (32K x 9-BIT) SRAM

ADVANCE INFORMATION
IDT10596RR
IDT100596RR
IDT101596RR

FEATURES:

- 32,768-words x 9-bit organization
- Self-Timed Write, with registers on inputs and outputs
- Balanced Read/Write cycle time: 10/12/15 ns
- Wide word for reduced address loading
- Differential clock input
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard pinouts

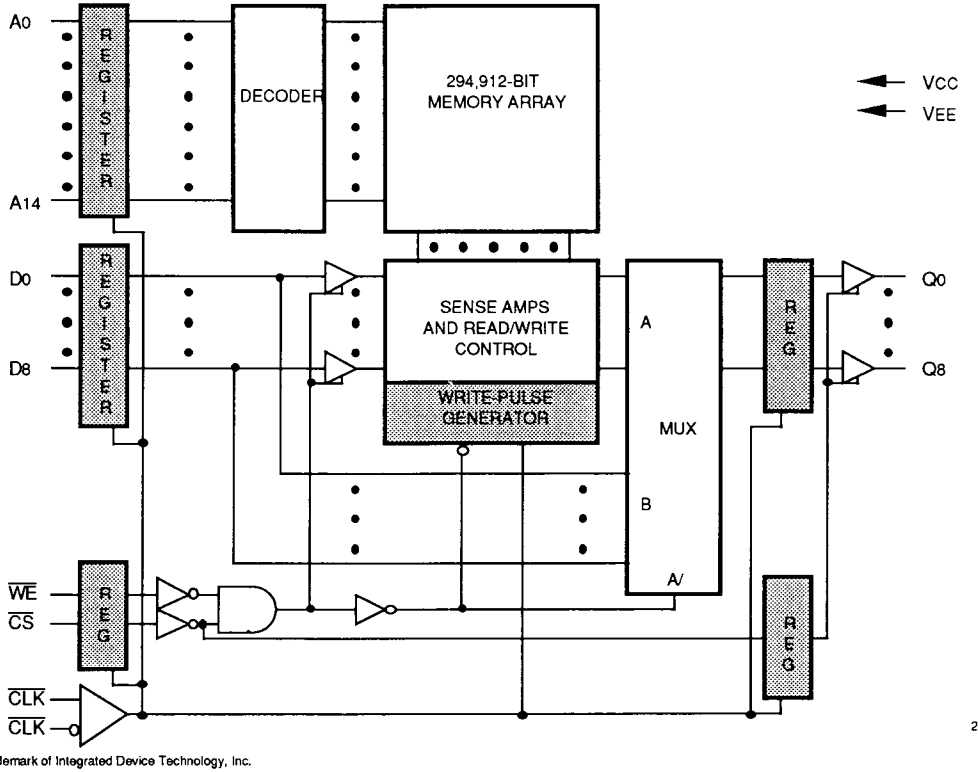
DESCRIPTION:

The IDT10596RR, IDT100596RR, and IDT101596RR are 294,912-bit high-speed BiCEMOS™ ECL self-timed static random access memories (STRAM) organized as 32Kx9, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

These devices are part of a family of nine-bit-wide ECL SRAMs. The devices have been configured to follow the proposed ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is similar to CMOS devices of equivalent density. Inputs are captured and outputs gated by the rising edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



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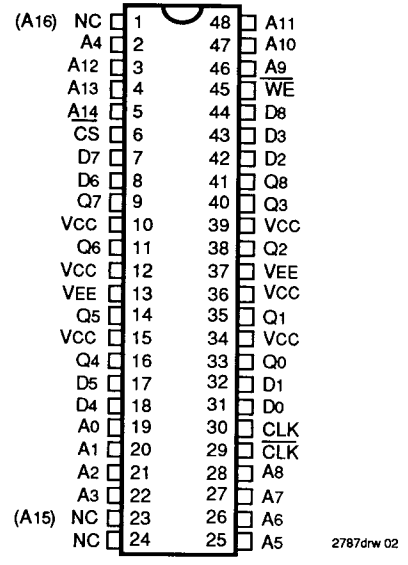
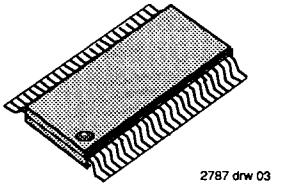
PIN CONFIGURATION

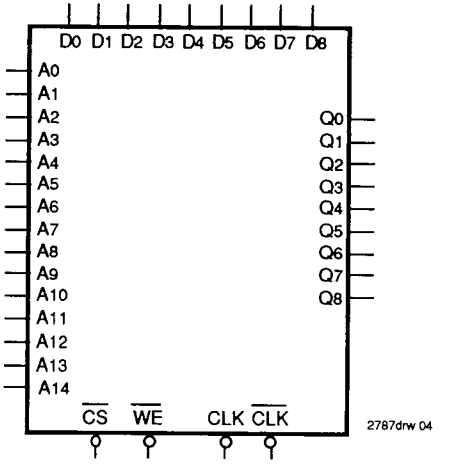


TOP VIEW



300-Mil-Wide
Plastic SSOP Package
48

LOGIC SYMBOL



32Kx9
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A14	Address Inputs
D0 through D8	Data Inputs
Q0 through Q8	Data Outputs
$\overline{CS}$	Chip Select Input (Internal pull down)
$\overline{WE}$	Write Enable Input
CLK, $\overline{CLK}$	Differential Clock Imputs
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
VCCA	Less Negative Supply Voltage for Output
NC	No Connect (Not internally bonded)

2787 tbl 01

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

NOTE:
1. Referenced to VCC

2787 tbl 02

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DATAOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

NOTES:
1. H=High, L=Low, X=Don't Care.
2. DATAOUT initiated by next rising CLK.

2787 tbl 04

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	SSOP Typ.	SSOP Max.	Unit
CIN	Input Capacitance	TBD	–	pF
COUT	Output Capacitance	TBD	–	pF

2787tbl 03

B

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2787 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA	–

2787 tbl 06

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +85	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150	°C
PT	Power Dissipation		2.0	W
IOUT	DC Output Current (Output High)		-50	mA

2787 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(VEE = -4.5V, RL = 50Ω to -2.0V, TA = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
VOH	Output HIGH Voltage	VIN = VIHA or VILB		-1025	-955	-880	mV
VOL	Output LOW Voltage	VIN = VIHA or VILB		-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	VIN = VIHB or VILA		-1035	–	–	mV
VOLC	Output Threshold LOW Voltage	VIN = VIHB or VILA		–	–	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I IH	Input HIGH Current	VIN = VIHA	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I IL	Input LOW Current	VIN = VILB	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
IEE	Supply Current	All Inputs and Outputs Open		-260	-200	–	mA

2787 tbl 08

NOTE:

1. Typical parameters are specified at VEE = -4.5V, TA = +25°C and maximum loading.

B

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2787 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

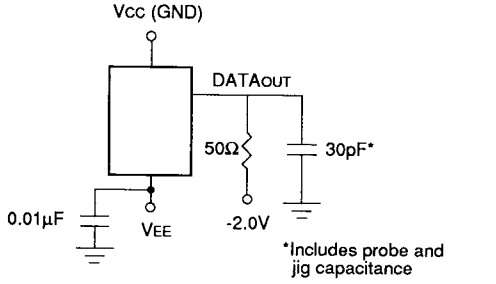
Symbol	Parameter	Test Condition		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-280	-220	–	mA

2787 tbl 10

NOTE:

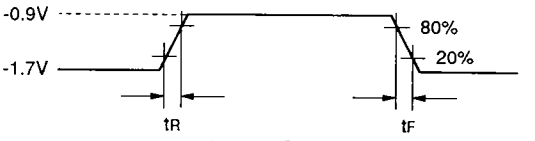
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2787 drw 05

AC TEST INPUT PULSE



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2787 drw 06

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2787 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10596RR, IDT100596RR, and IDT101596RR Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance.

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of $\overline{CLK}$). In the case of a write cycle, the memory cell is written by an internal timer initiated by the rising edge of CLK, and write data conducted to the outputs. Output data is clocked out the output register and is held through the next cycle.

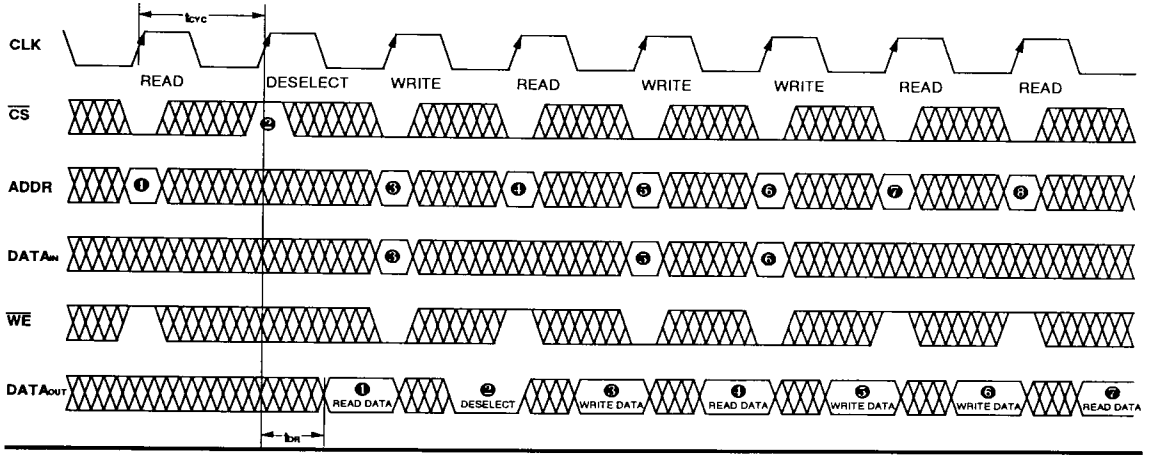
READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, after access occurs internally, the read data for the read address clocked in at ❶ is clocked through the output register to the output pins by the next rising edge of clock (for this example, at ❷). There is a short delay from rising clock to output ready, called tDR (see Read Cycle Timing).

The output register takes some time to change state for the next output, but this time is very short. Therefore, data hold time from clock high (tDH) is specified as zero minimum hold time.

B

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



DESELECT TIMING

Because the outputs are registered, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) after the next rising clock edge. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses an internal timer as the write pulse, and thus only one edge of clock need be determined (de-skewed) exactly.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after the next clock high edge). This function is sometimes called "Transparent Write," and is useful for write-through cache applications. Thus the input data sampled at ❸ is available on the output in the next cycle.

There are no restrictions on the order of read cycles and write cycles.

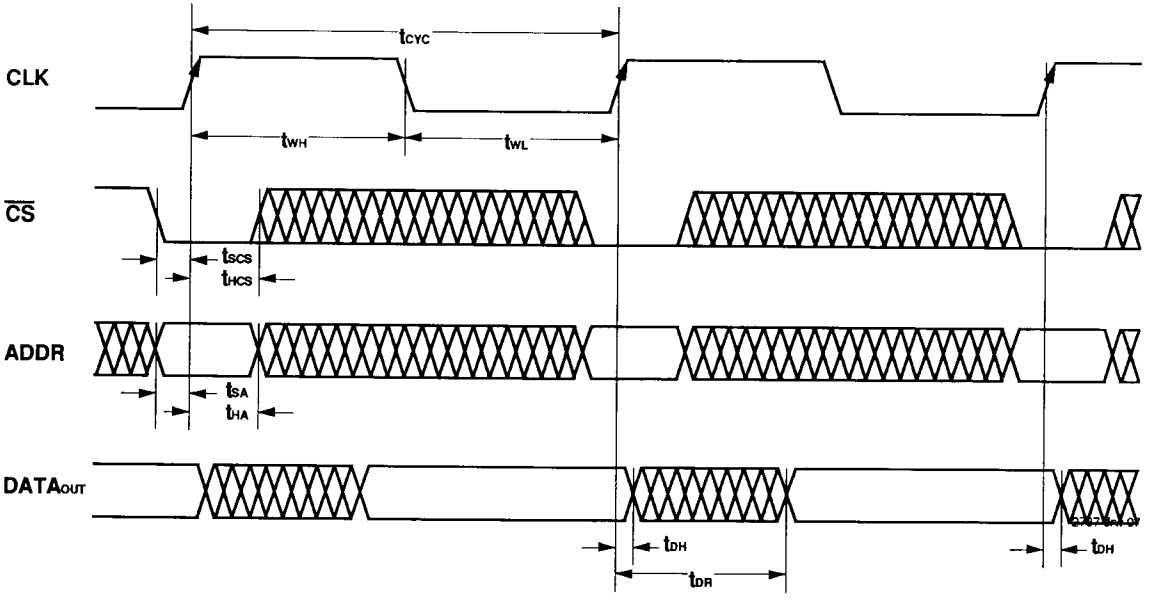
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10596RR10 100596RR10 101596RR10		10596RR12 100596RR12 101596RR12		10596RR15 100596RR15 101596RR15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
tCYC	Cycle Time	—	10	—	12	—	15	—	ns
tWL	Clock Low Pulse Width	—	4	—	5	—	6	—	ns
tWH	Clock High Pulse Width	—	4	—	5	—	6	—	ns
tSCS	Setup Time for Chip Select	—	1	—	1	—	1	—	ns
tSA	Setup Time for Address	—	1	—	1	—	1	—	ns
tHCS	Hold Time for Chip Select	—	2	—	2	—	2	—	ns
tHA	Hold Time for Address	—	2	—	2	—	2	—	ns
tDH	Data Hold from Clock High	—	0	—	0	—	0	—	ns
tDR	Data Ready from Clock High	—	0	4	0	4	0	4	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

2787 tbl 12

READ CYCLE TIMING DIAGRAM



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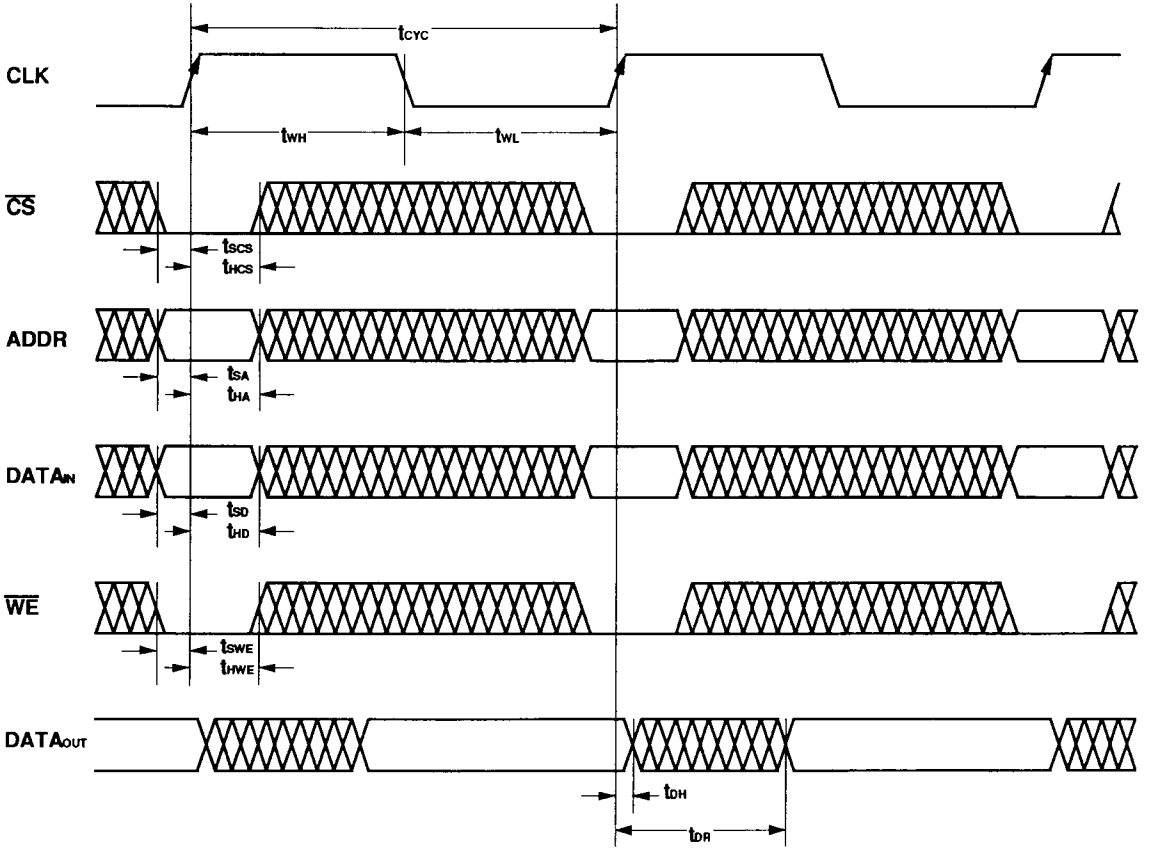
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10596RR10 100596RR10 101596RR10		10596RR12 100596RR12 101596RR12		10596RR15 100596RR15 101596RR15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE									
tSWE	Setup Time for Write Enable	—	1	—	1	—	1	—	ns
tSD	Setup Time for Data In	—	1	—	1	—	1	—	ns
tHWE	Hold Time for Write Enable	—	2	—	2	—	2	—	ns
tHD	Hold Time for Data In	—	2	—	2	—	2	—	ns

NOTES:
2787 tbl 12

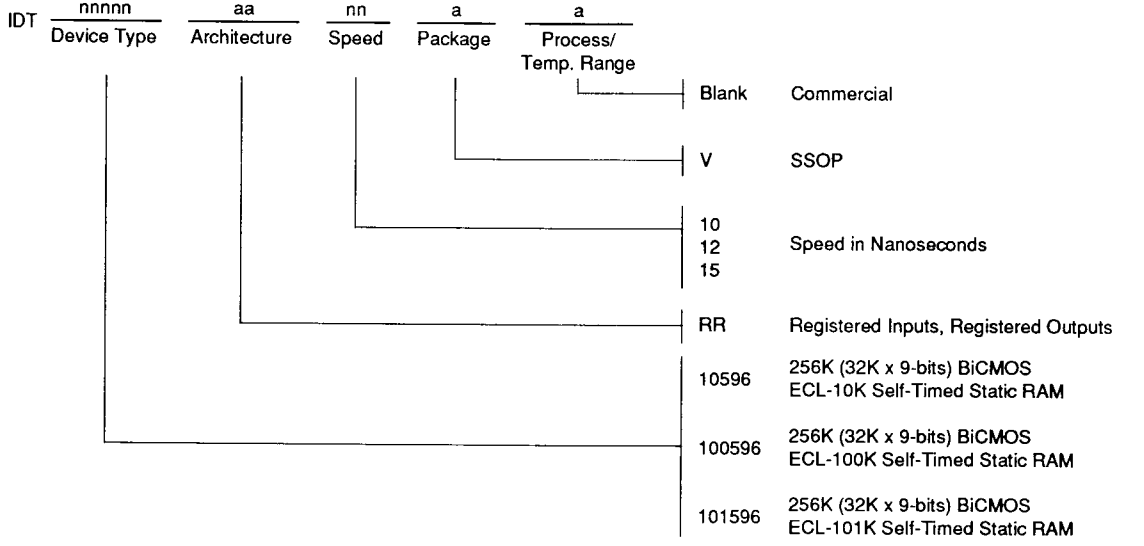
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and access timing is the same as the Read Cycle with the addition of the above requirements. Write Data appears on the output pins after the next rising edge of CLK.

WRITE CYCLE TIMING DIAGRAM



2787 drw 08

ORDERING INFORMATION



2787 drw 09

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