N-channel 80 V, 35 m $\Omega$  logic level MOSFET in LFPAK33 19 September 2016 Product data sheet

#### 1. **General description**

Logic level N-channel MOSFET in an LFPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### 2. **Features and benefits**

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

#### Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	80	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	26	Α	
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	62	W	
Static characte	Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	28	35	mΩ	
Dynamic characteristics								
$Q_{GD}$	gate-drain charge	$I_D = 10 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	4.9	-	nC	





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# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source		D
2	S	Source		
3	S	Source		G T T
4	G	Gate		mbb076 S
mb	D	Mounting base; connected to drain	LFPAK33 (SOT1210)	

# 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9M35-80E	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210		

# 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M35-80E	93580E

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS}$ = 20 k $\Omega$		-	80	V
$V_{GS}$	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	10	V
		Pulsed; T <sub>j</sub> ≤ 175 °C	[1][2]	-15	15	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	62	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	26	Α
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	19	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3		-	106	Α

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#### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain	diode					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	26	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	106	Α
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 26 A; $V_{sup}$ ≤ 80 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3][4]	-	32.3	mJ

- 1] Accumulated pulse duration up to 50 hours delivers zero defect ppm.
- [2] Significantly longer life times are achieved by lowering T<sub>i</sub> and or V<sub>GS</sub>
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

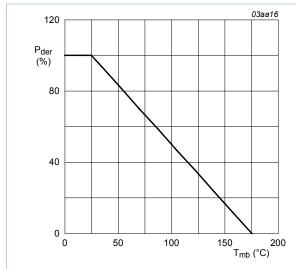


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

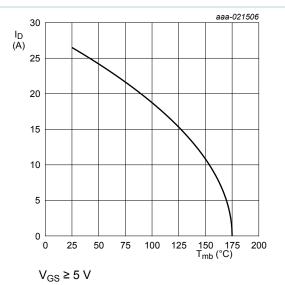
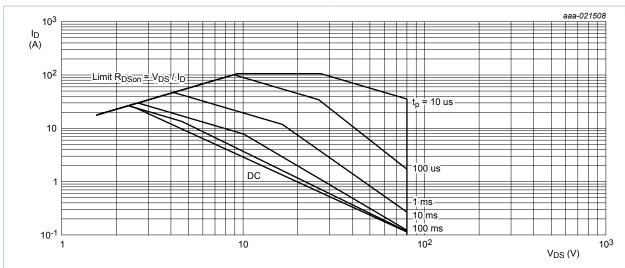


Fig. 2. Continuous drain current as a function of mounting base temperature

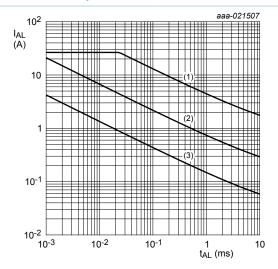
$$I_D = 26A \times \sqrt{\frac{175^{\circ}C - T_{mb}}{150^{\circ}C}}$$
 for  $T_{mb} \ge 25^{\circ}C$ 

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 $T_{mb}$  = 25 °C;  $I_{DM}$  is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1)  $T_{j \text{ (init)}}$  = 25 °C; (2)  $T_{j \text{ (init)}}$  = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

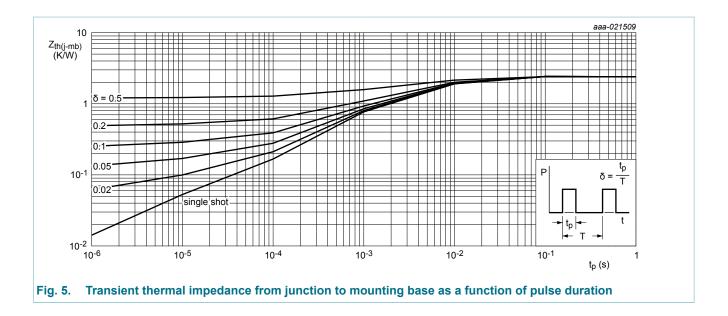
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	2.01	2.43	K/W

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#### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33



### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			_
V <sub>(BR)DSS</sub>		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ} C$	72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10	-	-	2.45	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; Fig. 10	0.5	-	-	V
I <sub>DSS</sub> c	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.01	1	μA
		V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
$I_{GSS}$	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	28	35	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	25	31	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 175 °C; <u>Fig. 12</u>	-	-	88	mΩ
Dynamic ch	naracteristics		,			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V;	-	13.5	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	3.3	-	nC
$Q_{GD}$	gate-drain charge		-	4.9	-	nC

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### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C <sub>iss</sub>	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; Fig. 15$	-	1356	1804	pF
C <sub>oss</sub>	output capacitance		-	106	127	pF
C <sub>rss</sub>	reverse transfer capacitance		-	52	71	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 60 V; $R_{L}$ = 5 $\Omega$ ; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 $\Omega$ ; $T_{j}$ = 25 °C	-	8.8	-	ns
t <sub>r</sub>	rise time		-	14	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	19.5	-	ns
t <sub>f</sub>	fall time		-	12	-	ns
Source-dra	nin diode	1				-
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}; Fig. 16$	-	0.78	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S$ = 10 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; $T_j$ = 25 °C	-	21	-	ns
Q <sub>r</sub>	recovered charge		-	21.6	-	nC

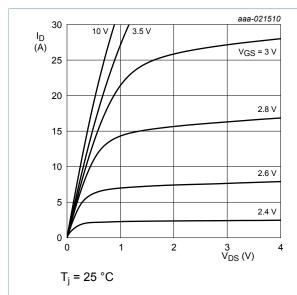


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

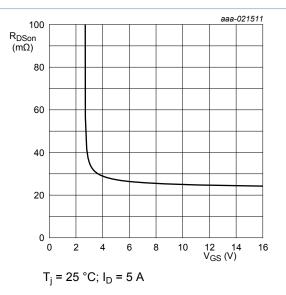


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

#### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33

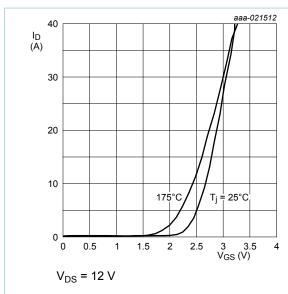


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

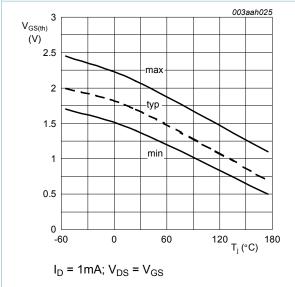
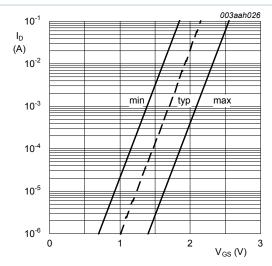


Fig. 10. Gate-source threshold voltage as a function of junction temperature



 $T_i = 25 \,^{\circ}C; V_{DS} = 5 \,^{\circ}V$ 

Fig. 9. Sub-threshold drain current as a function of gate-source voltage

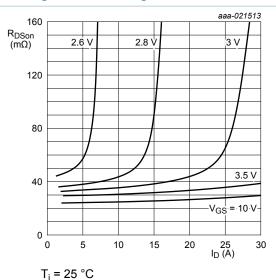


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

#### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33

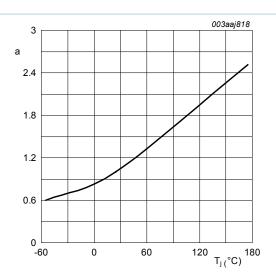


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

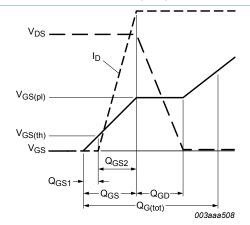


Fig. 14. Gate charge waveform definitions

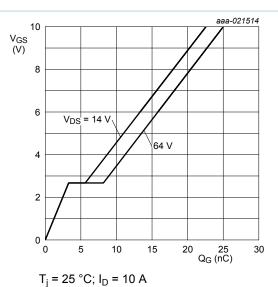


Fig. 13. Gate-source voltage as a function of gate charge; typical values

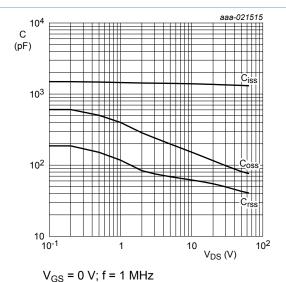
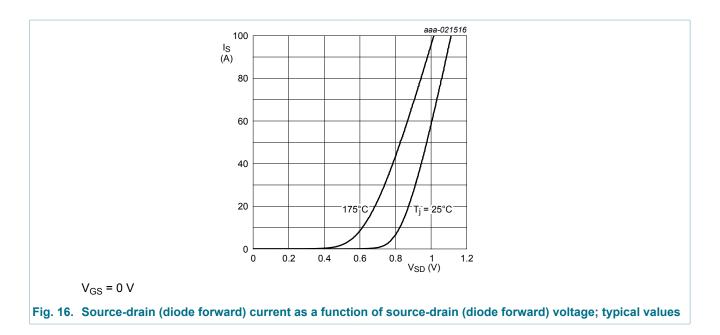


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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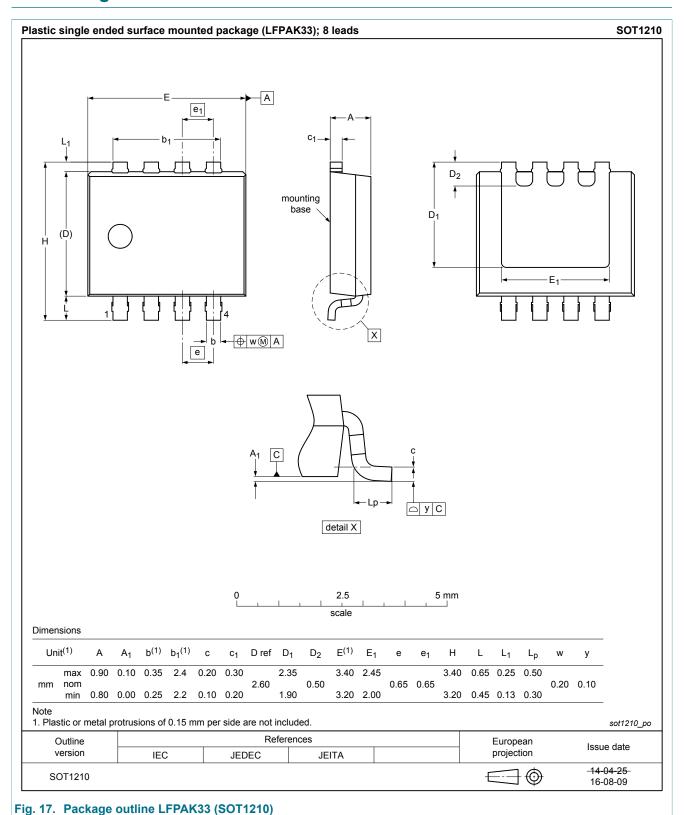


# 11. Application information

For guidance on how to use and understand this datasheet, please refer to application note <u>AN11158</u> "Understanding power MOSFET datasheet parameters".

#### N-channel 80 V, 35 m $\Omega$ logic level MOSFET in LFPAK33

## 12. Package outline



#### N-channel 80 V, 35 mΩ logic level MOSFET in LFPAK33

### 13. Legal information

#### 13.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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