

CCLD-912 Model
9×14 mm SMD, 3.3V, LVDS



Model CCLD-912 is a 77.760MHz to 161.000MHz LVDS Clock Oscillator operating at 3.3Volts. The oscillator utilizes a High Q Third Overtone crystal design providing very low Jitter and Phase Noise. No Sub-Harmonics are present in the Output Signal.



9×14mm SMD

Applications:

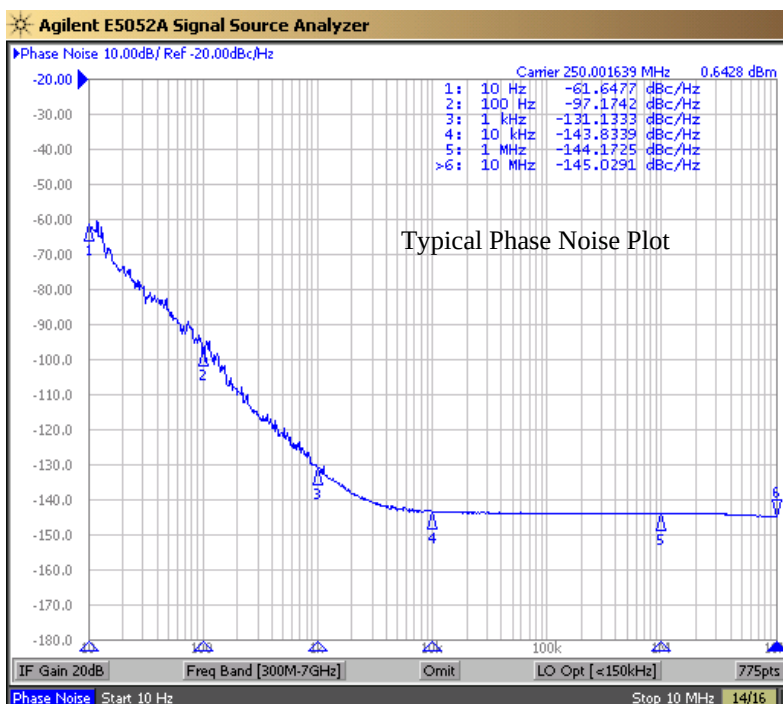
Digital Video
SONET/SDH/DWDM
Storage Area Networks
Broadband Access
Ethernet, Gigabit Ethernet

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Frequency Range:	77.760MHz to 161.000MHz
Frequency Stability Options(ppm):	±25, ±50, ±100
Temperature Range:	(standard) 0°C to +70°C
(Option M)	-20°C to +70°C
(Option X)	-40°C to +85°C
Storage:	-45°C to 90°C
Input Voltage:	3.3V ± 0.3V
Input Current:	45mA Typ., 66mA Max
Output:	Differential LVDS
Symmetry:	45/55% Max @ 50% Vdd
Rise/Fall Time:	1nsec Max @ 20% to 80% Vdd
Load:	100 Ohms Connected between OUT and COUT
Logic:	
Output Voltage Levels	"0"=0.90 Min., 1.10 Typ. "1"=1.43 Typ., 1.60 Max
Differential Output Voltage:	247mV Min., 454mV Max
Disable Time:	200nSec Max
Enable Time:	2mSec Max
Phase Jitter: 12kHz~80MHz	0.5psec Typ., 1psec RMS Max
Phase Noise: (See Plot Below)	
Sub-harmonics:	None
Aging:	<3ppm 1st/yr, <1ppm every year thereafter



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Crystek Part Number Guide

CCLD - 912 X - 50 - 155.520

#1 #2 #3 #4 #5

#1 Crystek LVDS Osc.
#2 Model 912
#3 Temp Range: Blank = 0/70°C, M = -20/70°C, X = -40/85°C
#4 Stability: (see Table 1)
#5 Frequency in MHz: 3 or 6 decimal places

Stability Indicator

Blank	± 100ppm
50	± 50ppm
25	± 25ppm

Table 1

Example:
CCLD-912X-50-155.520
3.3V, -40/85°C, ±50ppm, 155.520 MHz

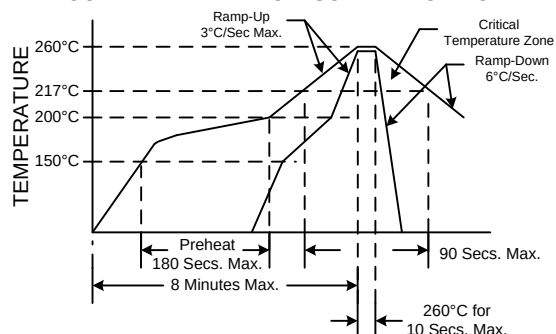
Mechanical:

Shock: MIL-STD-883, Method 2002, Condition B
Solderability: MIL-STD-883, Method 2003
Vibration: MIL-STD-883, Method 2007, Condition A
Solvent Resistance: MIL-STD-202, Method 215
Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J

Environmental:

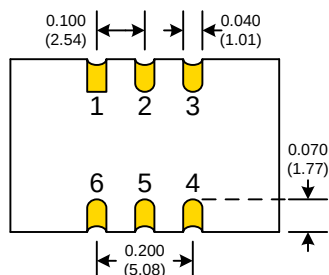
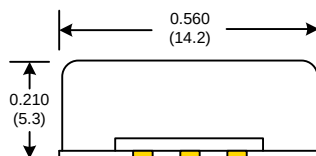
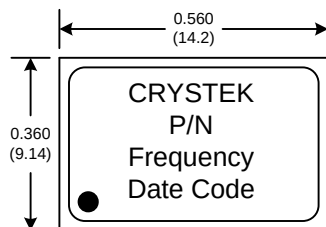
Thermal Shock: MIL-STD-883, Method 1011, Condition A
Moisture Resistance: MIL-STD-883, Method 1004

RECOMMENDED REFLOW SOLDERING PROFILE

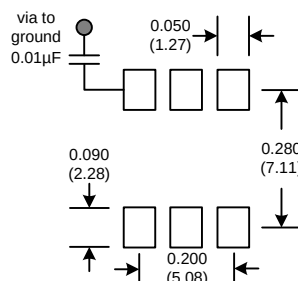


NOTE: Reflow Profile with 240°C peak also acceptable.

Dimensions inches (mm)
All dimensions are Max unless otherwise specified.



SUGGESTED PAD LAYOUT



Tristate Function

Function pin 1	Output pin
Open or N/C	Active
"1" level 0.7×Vdd Min	Active
"0" level 0.3×Vdd Max	High Z

PIN	Connection
1	Enable/Disable
2	N/C
3	GND
4	Output
5	Comp Output
6	Vcc

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