

BUK7210-55B

N-channel TrenchMOS standard level FET

Rev. 01 — 11 December 2008

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- 185 °C rated
- Q101 compliant
- Standard level compatible
- Very low on-state resistance

1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

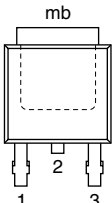
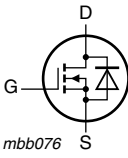
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 185\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3 ;	[1]	-	75	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 10 ; see Figure 9	-	8.5	10	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped inductive load	-	-	173	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT428 (SC-63; DPAK)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7210-55B	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

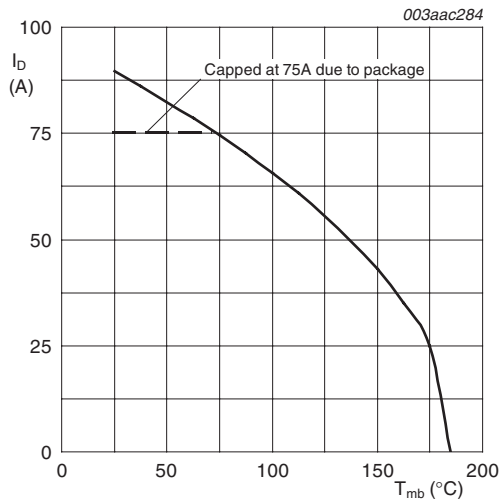
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 185 °C	-	55	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ; 25 °C ≤ T _j ≤ 185 °C	-	55	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ; see Figure 3 ;	[1]	-	89.6	A
		T _{mb} = 100 °C; V _{GS} = 10 V; see Figure 1	-	65.5	A	
		T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ; see Figure 3 ;	[2]	-	75	A
I _{DM}	peak drain current	T _{mb} = 25 °C; t _p ≤ 10 μs; pulsed	-	335	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	167	W	
T _{stg}	storage temperature		-55	185	°C	
T _j	junction temperature		-55	185	°C	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C;	[2]	-	75	A
		T _{mb} = 25 °C;	[3]	-	89.6	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	335	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 75 A; V _{sup} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped inductive load	-	173	mJ	

[1] Current is limited by power dissipation chip rating.

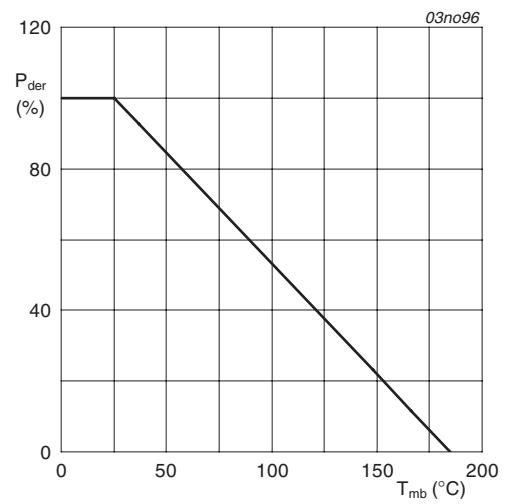
[2] Continuous current is limited by package.

[3] Current is limited by power dissipation chip rating.



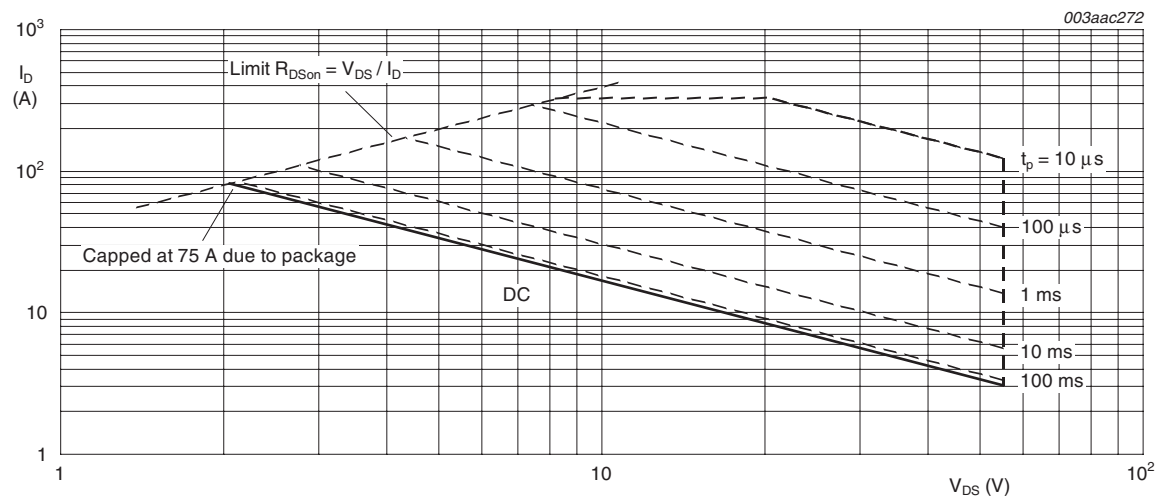
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on a printed circuit board; vertical in still air.; minimum footprint	-	75	-	K/W

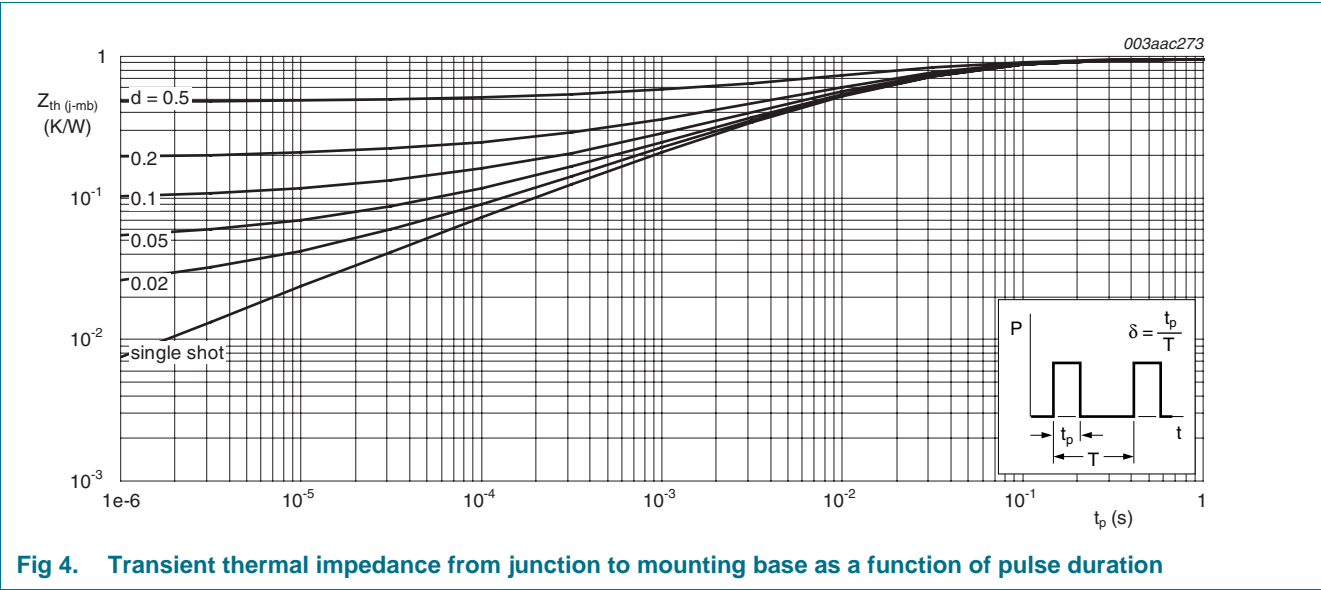


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	55	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; see Figure 7	-	1.75	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; see Figure 7 ; see Figure 8	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 185 °C; see Figure 7	0.9	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -40 °C; see Figure 7	-	2.8	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; see Figure 7	-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _J = 175 °C	-	1.5	500	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 125 °C	-	0.1	90	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 25 °C	-	0.02	1	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _J = 185 °C	-	3	800	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 20 V; T _J = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -20 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 185 °C; see Figure 9	-	-	20.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; see Figure 10 ; see Figure 9	-	8.5	10	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 10 V; T _J = 25 °C; see Figure 12 ; see Figure 13	-	35	-	nC
Q _{GS}	gate-source charge		-	9	-	nC
Q _{GD}	gate-drain charge		-	12	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _J = 25 °C; see Figure 14	-	1840	2453	pF
C _{oss}	output capacitance		-	379	455	pF
C _{rss}	reverse transfer capacitance		-	165	226	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _J = 25 °C	-	18	-	ns
t _r	rise time		-	91	-	ns
t _{d(off)}	turn-off delay time		-	48	-	ns
t _f	fall time		-	45	-	ns
L _D	internal drain inductance	measured from drain to center of die; T _J = 25 °C	-	2.5	-	nH
L _S	internal source inductance	measured from source lead to source bond pad; T _J = 25 °C	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 18 A; V _{GS} = 0 V; T _j = 150 °C	-	0.76	-	V
		I _S = 18 A; V _{GS} = 0 V; T _j = 175 °C	-	0.74	-	V
		I _S = 18 A; V _{GS} = 0 V; T _j = 100 °C	-	0.8	-	V
		I _S = 18 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 11	-	0.85	1.2	V
		I _S = 18 A; V _{GS} = 0 V; T _j = 125 °C	-	0.78	-	V
		I _S = 18 A; V _{GS} = 0 V; T _j = 185 °C; see Figure 11	-	0.73	-	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V;	-	67	-	ns
Q _r	recovered charge	V _{DS} = 30 V; T _j = 25 °C	-	65	-	nC

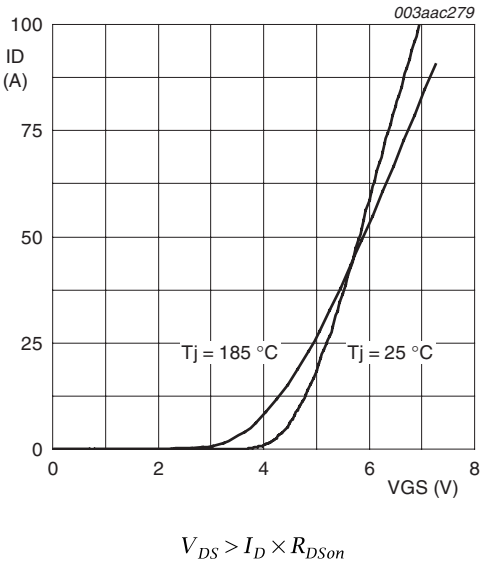


Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values

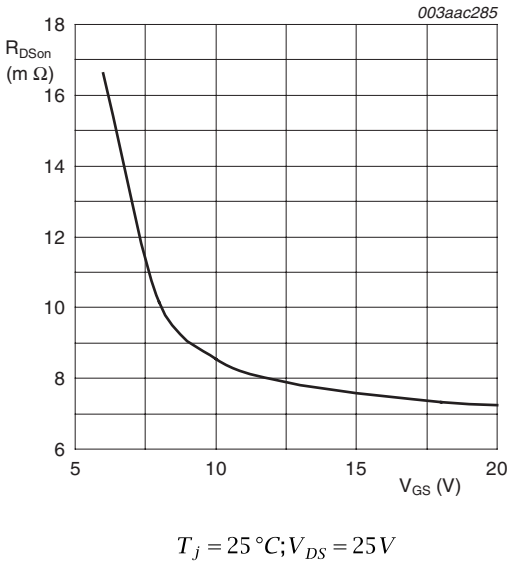
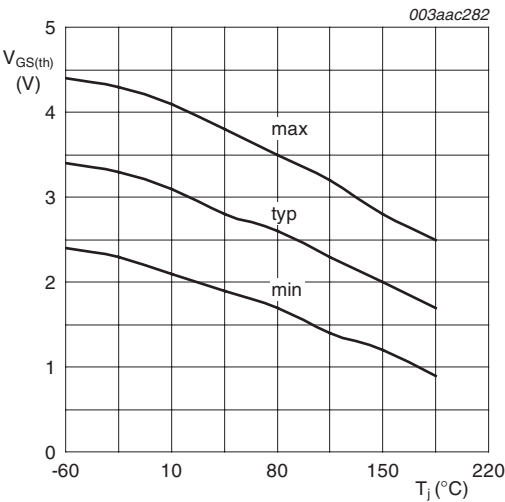
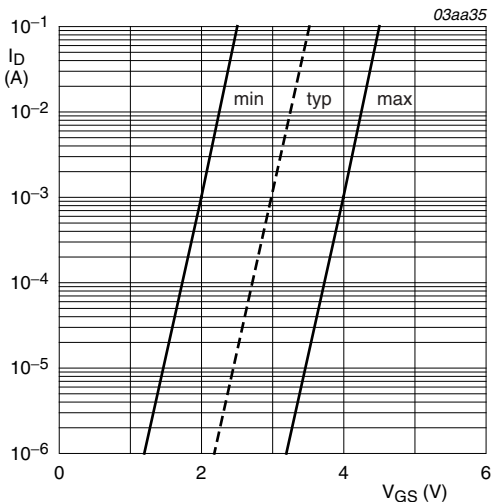


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



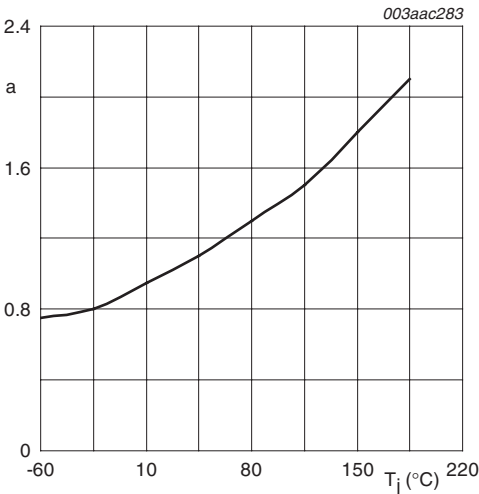
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



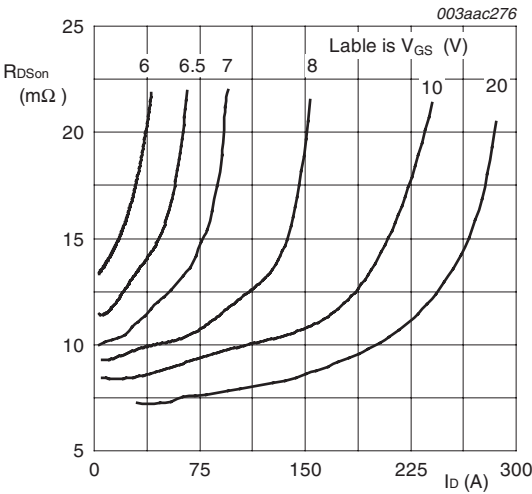
$$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25\text{ }^{\circ}\text{C}$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

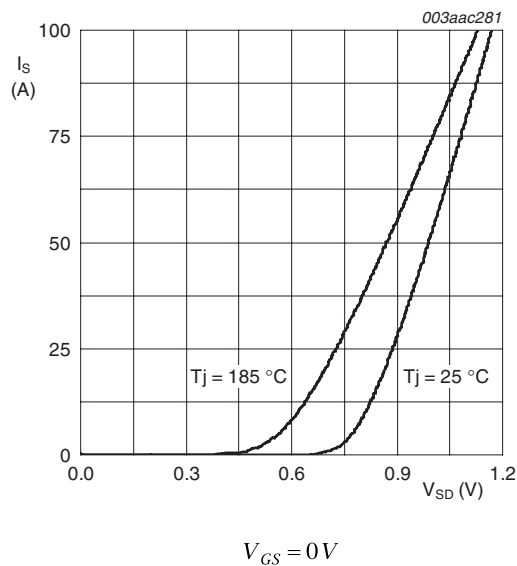


Fig 11. Source current as a function of source-drain voltage; typical values

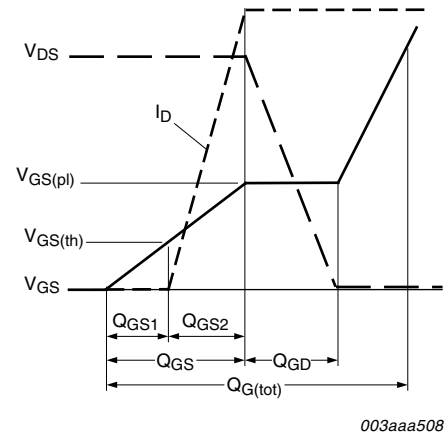


Fig 12. Gate charge waveform definitions

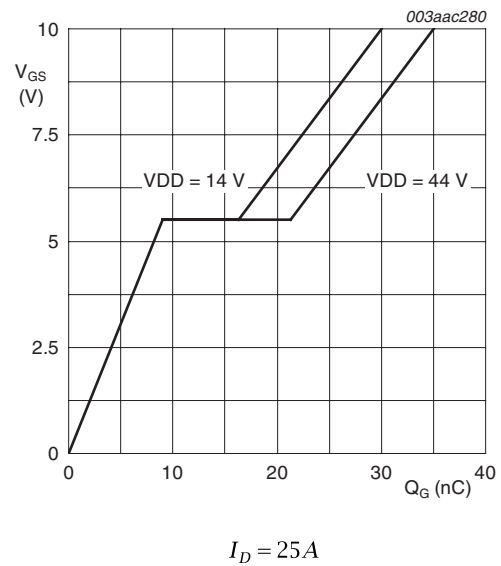


Fig 13. Gate-source voltage as a function of gate charge; typical values

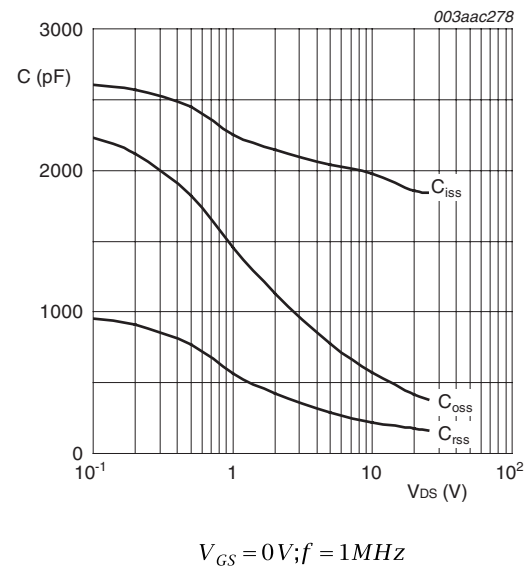
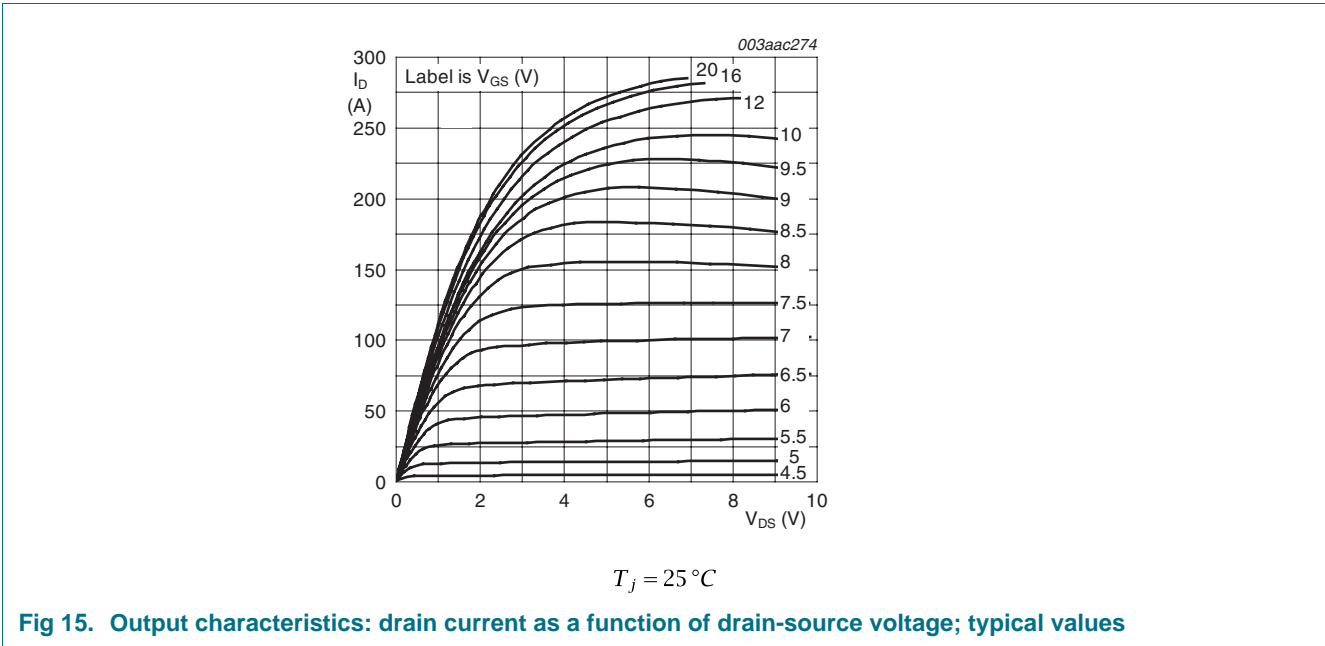


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

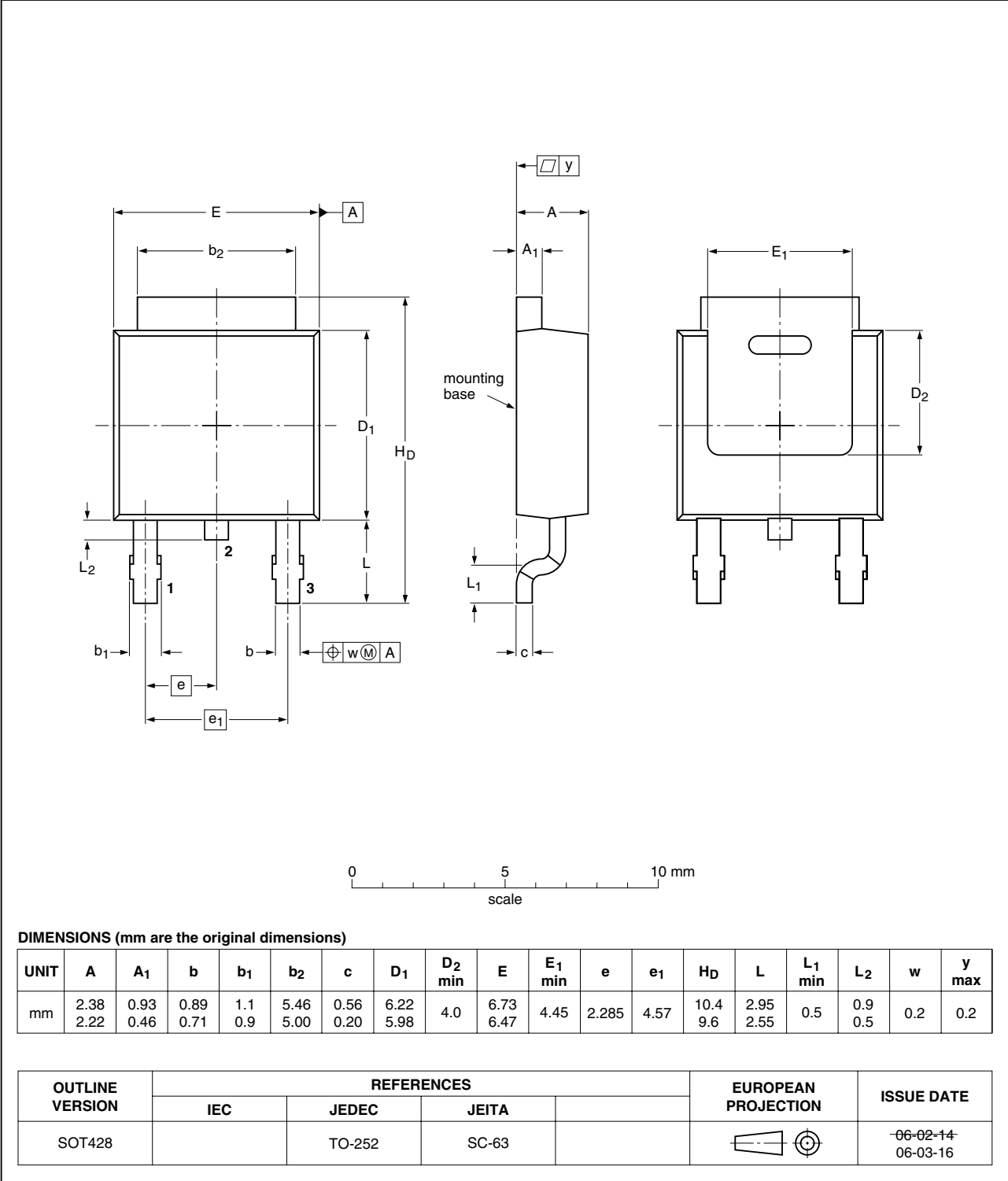


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7210-55B_1	20081211	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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