nexperia

**Important notice**

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

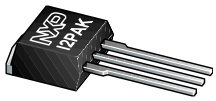
Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia




# BUK9E1R9-40E

## N-channel 40 V, 1.9 mΩ logic level MOSFET in I²PAK

5 June 2013 — Product data sheet

## 1. General description

Logic level N-channel MOSFET in a $I^2$PAK package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Power Steering
- Fan Control
- Ultra high performance power switching

## 4. Quick reference data

**Table 1. Quick reference data**

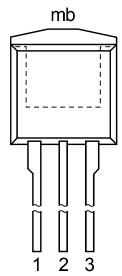
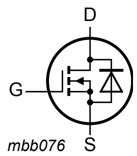
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j$ ≥ 25 °C; $T_j$ ≤ 175 °C | | - | - | 40 | V |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C; Fig. 1 | [1] | - | - | 120 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 349 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 1.6 | 1.93 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 5 V; $I_D$ = 25 A; $V_{DS}$ = 32 V; Fig. 13; Fig. 14 | | - | 40.9 | - | nC |

[1] Continuous current is limited by package.

Scan or click this QR code to view the latest information for this product

# 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |   I2PAK (SOT226) |   |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK9E1R9-40E | I2PAK | plastic single-ended package (I2PAK); TO-262 | SOT226 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| BUK9E1R9-40E | BUK9E1R9-40E |

# 8. Limiting values

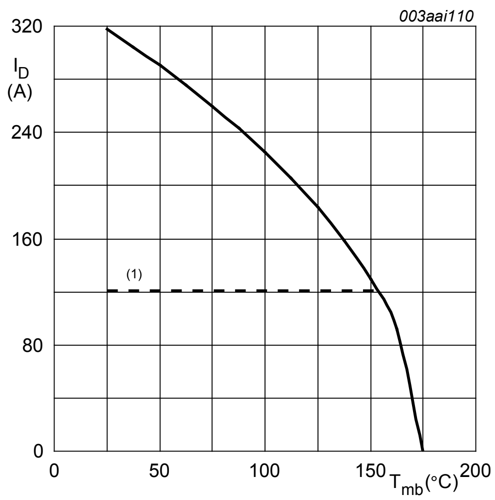
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j$ ≥ 25 °C; $T_j$ ≤ 175 °C | | - | 40 | V |
| $V_{DGR}$ | drain-gate voltage | $R_{GS}$ = 20 kΩ | | - | 40 | V |
| $V_{GS}$ | gate-source voltage | $T_j$ ≤ 175 °C; Pulsed | [1][2] | -15 | 15 | V |
| | | $T_j$ ≤ 175 °C; DC | | -10 | 10 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; Fig. 1 | [3] | - | 120 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 5 V; Fig. 1 | [3] | - | 120 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Fig. 4 | | - | 1228 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 2 | | - | 349 | W |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [3] | - | 120 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 1228 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 120 A; $V_{sup}$ ≤ 40 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3 | [4][5] | - | 1008 | mJ |

[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
[2] Significantly longer life times are achieved by lowering $T_j$ and or $V_{GS}$
[3] Continuous current is limited by package.
[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[5] Refer to application note AN10273 for further information.




(1) Capped at 120A due to package

**Fig. 1. Continuous drain current as a function of mounting base temperature**

$V_{GS} \geq 5V$

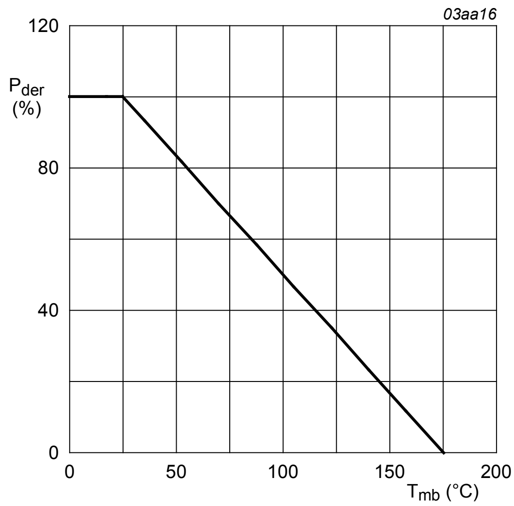



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

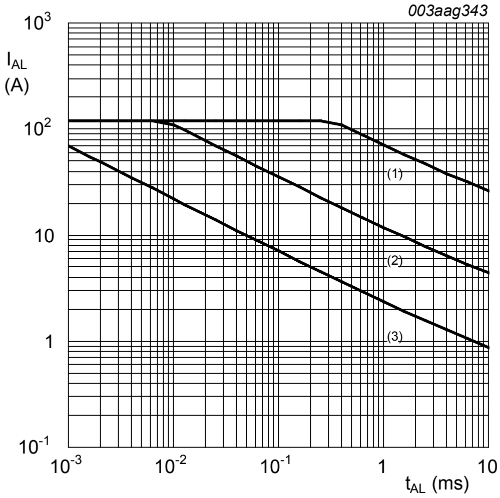



**Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 150°C$; (3) Repetitive Avalanche

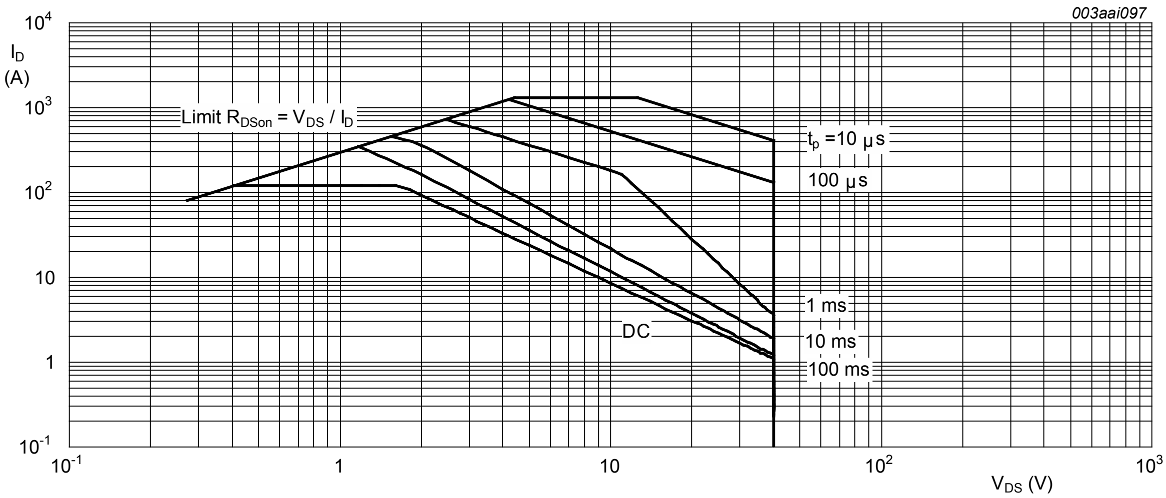



**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25°C$; $I_{DM}$ is a single pulse

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | - | 0.43 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | vertical in still air | | - | 65 | - | K/W |

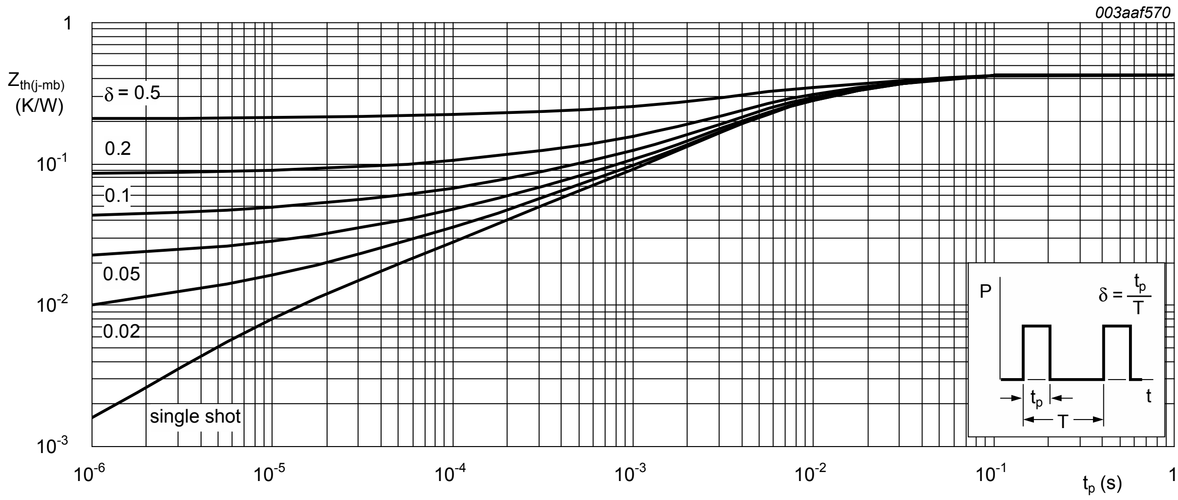


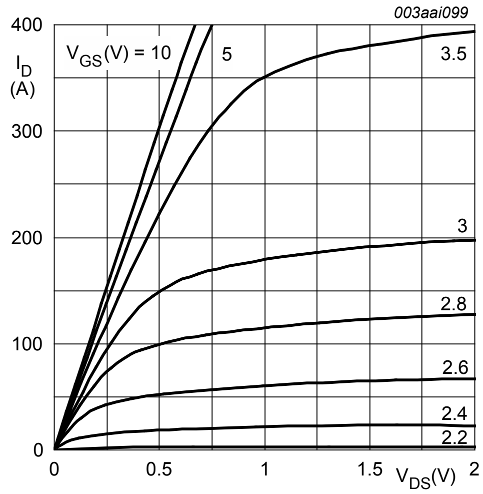

**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 40 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 1.4 | 1.7 | 2.1 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; Fig. 9 | | - | - | 2.45 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; Fig. 9 | | 0.5 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.13 | 1 | µA |
| | | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 1.6 | 1.93 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 1.4 | 1.7 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 175 °C; Fig. 12; Fig. 11 | | - | - | 3.7 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 32 V; $V_{GS}$ = 5 V; Fig. 13; Fig. 14 | | - | 120 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 26.9 | - | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GD}$ | gate-drain charge | | | - | 40.9 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | - | 12300 | 16400 | pF |
| $C_{oss}$ | output capacitance | | | - | 1530 | 1840 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 740 | 1020 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 Ω | | - | 95 | - | ns |
| $t_r$ | rise time | | | - | 118 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 195 | - | ns |
| $t_f$ | fall time | | | - | 119 | - | ns |
| $L_D$ | internal drain inductance | from upper edge of drain mounting base to center of die | | - | 2.5 | - | nH |
| | | from drain lead 6mm from package to centre of die | | - | 4.5 | - | nH |
| $L_S$ | internal source inductance | from source lead to source bonding pad | | - | 7.5 | - | nH |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.77 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V | | - | 57 | - | ns |
| $Q_r$ | recovered charge | | | - | 97 | - | nC |




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

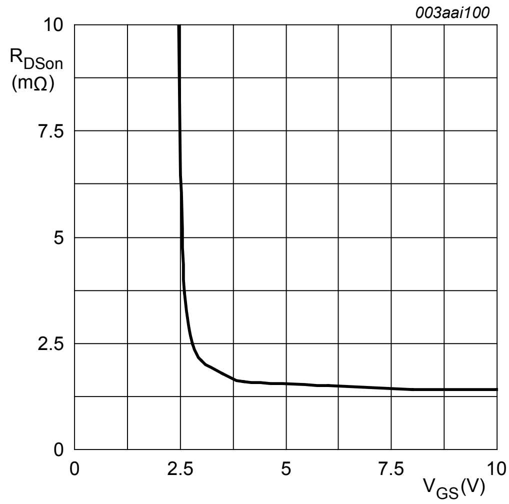



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25°C;\ I_D = 25A$

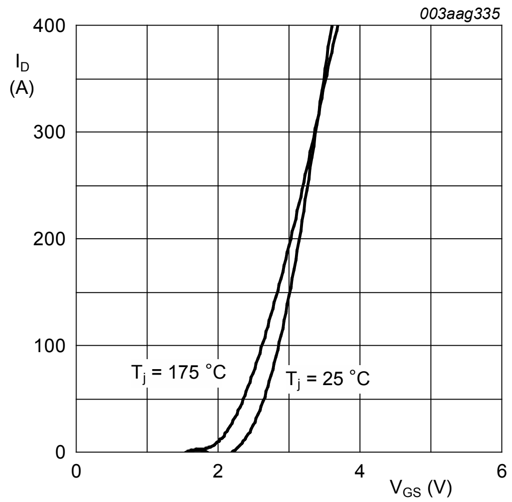



**Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$V_{DS} = 12\,V$

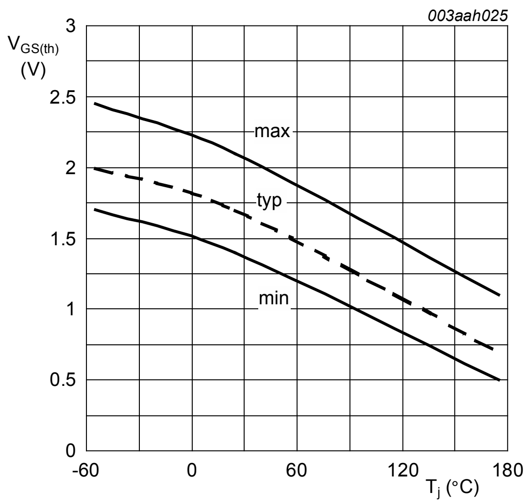



**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1$ mA; $V_{DS} = V_{GS}$

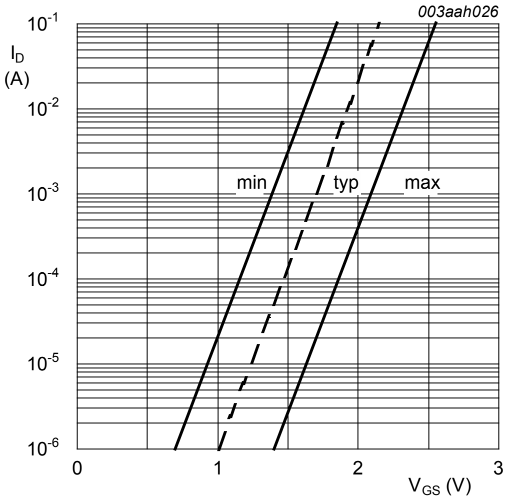
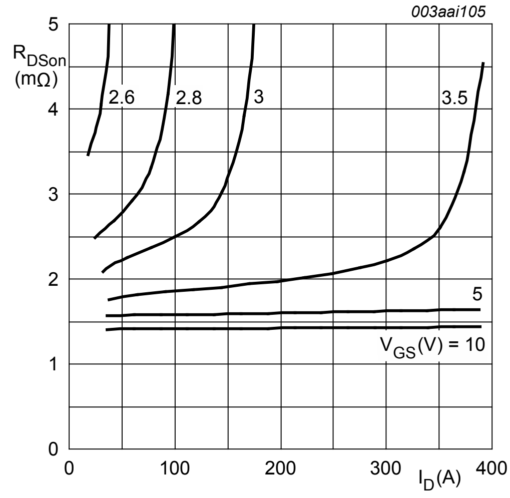



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25°C$; $V_{DS} = 5V$




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

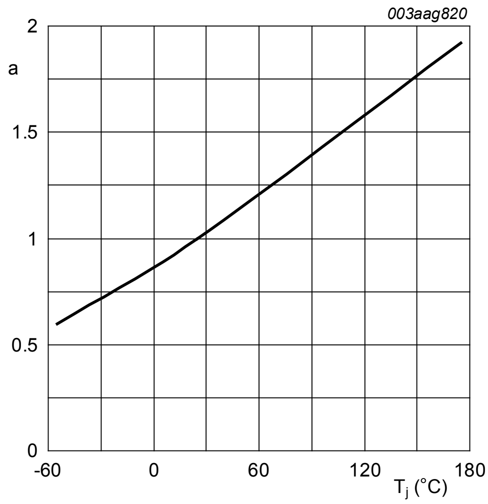



Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

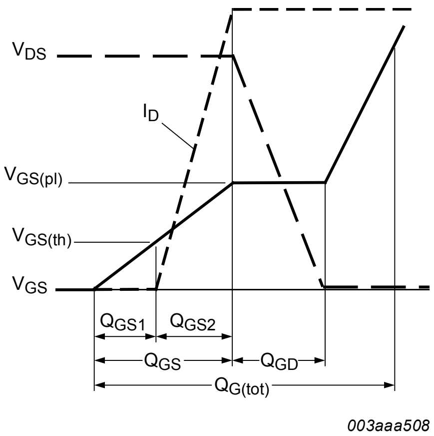
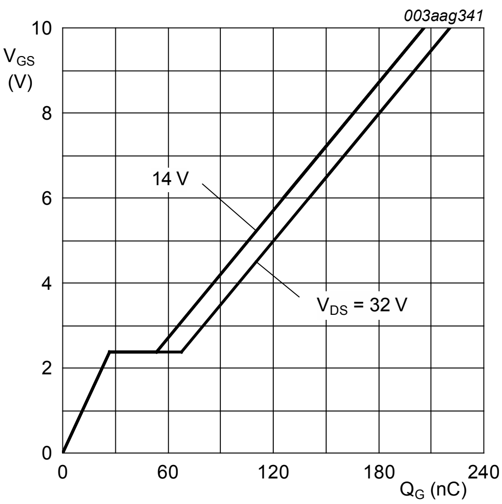
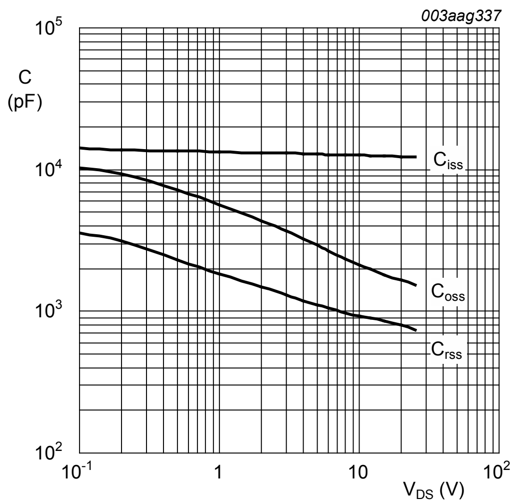



Fig. 13. Gate charge waveform definitions



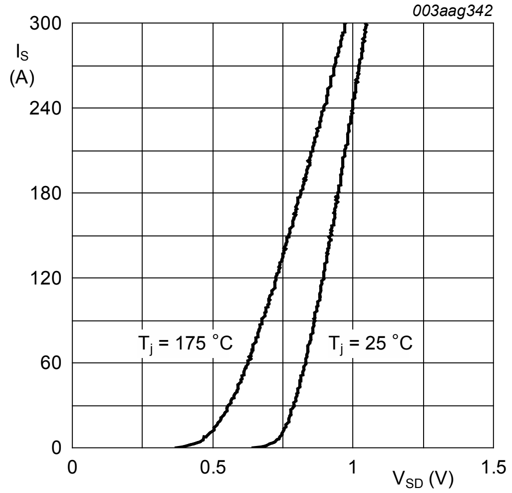

$T_j$ = 25 °C; $I_D$ = 25 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values




$V_{GS}$ = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

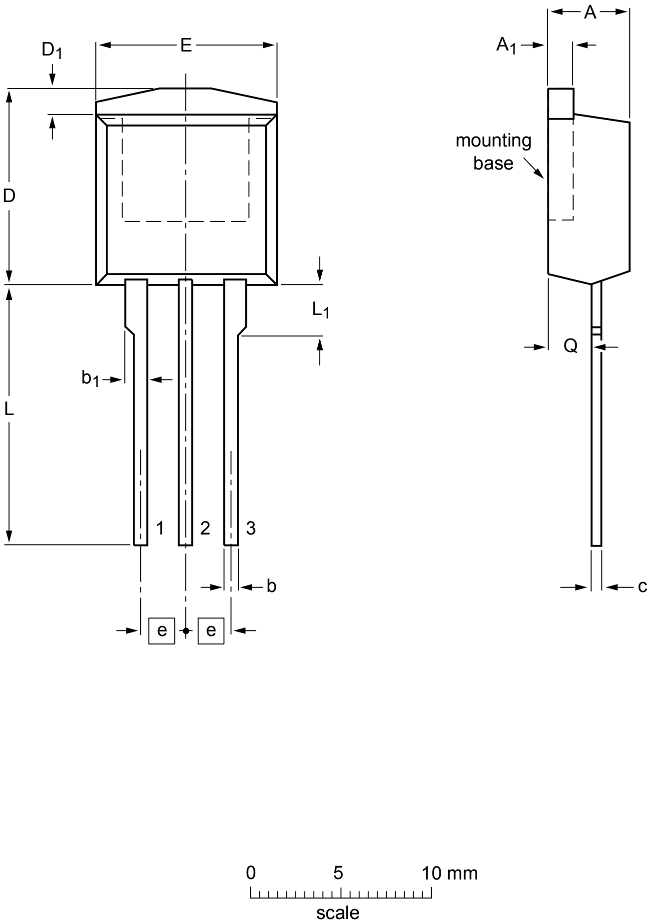



$V_{GS}$ = 0 V

**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

# 11. Package outline

**Plastic single-ended package (I2PAK); low-profile 3-lead TO-262** **SOT226**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | c | D max | $D_1$ | E | e | L | $L_1$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.5<br>4.1 | 1.40<br>1.27 | 0.85<br>0.60 | 1.3<br>1.0 | 0.7<br>0.4 | 11 | 1.6<br>1.2 | 10.3<br>9.7 | 2.54 | 15.0<br>13.5 | 3.30<br>2.79 | 2.6<br>2.2 |

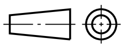
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT226 | | TO-262 | | |  | ~~06-02-14~~<br>09-08-25 |

Fig. 17. Package outline I2PAK (SOT226)

# 12. Legal information

## 12.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 12.2 Definitions

**Preview** — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 12.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**Adelante**, **Bitport**, **Bitsound**, **CoolFlux**, **CoReUse**, **DESFire**, **EZ-HV**, **FabKey**, **GreenChip**, **HiPerSmart**, **HITAG**, **I²C-bus** logo, **ICODE**, **I-CODE**, **ITEC**, **Labelution**, **MIFARE**, **MIFARE Plus**, **MIFARE Ultralight**, **MoReUse**, **QLPAK**, **Silicon Tuner**, **SiliconMAX**, **SmartXA**, **STARplug**, **TOPFET**, **TrenchMOS**, **TriMedia** and **UCODE** — are trademarks of NXP B.V.

**HD Radio** and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

## 13. Contents