

Field Programmable Blank Oscillator

Series **CPPL**

- Programmed with the PG-2000P, PG-3000 field oscillator programming instrument within seconds
- Can be programmed twice
- Provides a sealed finished custom oscillator
- Standard Package Options
- Ultra low jitter @ 1 million samples
- Power down and Tri-State options



Part Numbering Example: CPPL C 1 L Z - A5 B6 - XX.XXXX TS

CPPL	C	1	L	Z	A5	B6	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPL	C = CMOS T = TTL	1 = Full Size 4 = Half Size 5 = 3.2X5 Ceramic 7 = 5X7 Ceramic 8 = PLASTIC SMD 8B = PLASTIC SMD	Blank = 5V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.000~133.000 MHz	TS = Tri-State PD=PowerDwn

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.000		133.000	MHz
Available Stability Options:	-100 -50 -25		100 50 25	ppm ppm ppm
Programmable Input Voltage: (1-133 MHz) (1-100 MHz)	4.5 3.0	5.0 3.3	5.5 3.6	V V
Operating Temperature Range Options:	0 -20 -40		+70 +70 +85	°C °C °C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25°C, Vdd=5/3.3V			±5	
Programmable Output Level: TTL/CMOS				
Packaging: Tape and Reel (1K per Reel) Tube Bulk Shipping				

Operating Load Conditions:

Description	Min	Max	Unit
Vdd Supply Voltage	3.0	5.5	V
C _{TTL} Max Capacitive Load on outputs for TTL levels 4.5V-5.5V Vdd ≤ 40 MHz 4.5V-5.5V Vdd > 40-133 MHz		50 25	pF pF
C _{CMOS} Max Capacitive Load on outputs for CMOS levels 4.5V-5.5V Vdd, ≤ 66 MHz 4.5V-5.5V Vdd, >66-133 MHz 3.0V-3.6V Vdd, ≤ 40 MHz 3.0V-3.6V Vdd, >40-100 MHz		50 25 30 15	pF pF pF pF

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Electrical Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V _{IL} , Low-Level Input Voltage TO TRI-STATE OR POWER DOWN	4.5–5.5V V _{dd} 3.0–3.6V V _{dd}			0.8 0.2V _{dd}	V V
V _{IH} , High-Level Input Voltage TO ENABLE OUTPUT OR open	4.5–5.5V V _{dd} 3.0–3.6V V _{dd}	2.0 0.7			V V _{dd}
I _{IL} , Input Low Current I _{IH} , Input High Current	V _{IN} = 0V V _{IN} = V _{dd}			10 5	μA μA
Output Characteristics:					
V _{OL} , Low-Level Output Voltage	4.5V–5.5V V _{dd} , 16 mA I _{OL} 3.0V–3.6V V _{dd} , 8 mA I _{OL}			0.4 0.4	V V
V _{OHTTL} , High-level Output Voltage TTL	4.5V–5.5V V _{dd} , -16 mA I _{OL}	2.4			V
V _{OHCMOS} , High-level CMOS Voltage	4.5V–5.5V V _{dd} , -16 mA I _{OL} 3.0V–3.6V V _{dd} , -8 mA I _{OL}	V _{dd} -0.4 V _{dd} -0.4			V V
Power Supply Current: (unloaded)	4.5–5.5 V _{dd} , OUTPUT FREQ ≤ 133 MHz 3.0–3.6 V _{dd} , OUTPUT FREQ ≤ 100 MHz			45 25	mA mA
Standby Current:			10	50	μA
Tristate pull up	4.5–5.5 V _{dd} , V _{IN} = 0V 4.5–5.5 V _{dd} , V _{IN} = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
Tri-State Leakage Current	5.0 V _{dd}		20		μA
Output Enable Mode:	Output is Tri-Stated				
Power Down Mode:	Output is Tri-Stated.				

"Tristate internal pull up. Output active when high"



