



High-Speed Quad Monolithic SPST CMOS Analog Switch

FEATURES

- Fast Switching t_{ON} : 55 ns
- Low Charge Injection: 5 pC
- Low $r_{DS(on)}$: 32 Ω
- TTL/CMOS Compatible
- Low Leakage: 50 pA

BENEFITS

- Fast Settling Times
- Reduced Switching Glitches
- High Precision

APPLICATIONS

- High-Speed Switching
- Sample/Hold
- Digital Filters
- Op Amp Gain Switching
- Flight Control Systems
- Automatic Test Equipment
- Choppers
- Communication Systems

DESCRIPTION

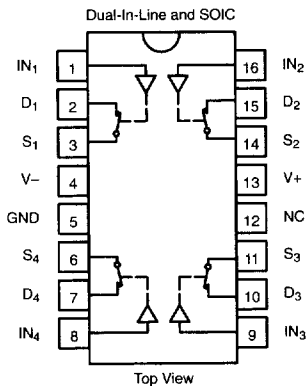
The DG271B high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

Built on the Vishay Siliconix' proprietary high voltage silicon gate process to achieve superior on/off performance, each

switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latchup.

The DG271B has a redesign internal regulator which improves start-up over the DG271.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG271BCJ
-40 to 85°C	16-Pin Narrow SOIC	DG271BDY



ABSOLUTE MAXIMUM RATINGS

V+ to V−	44 V
GND to V−	25 V
Digital Inputs ^a V _S , V _D	(V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first
Current, Any Terminal	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (DY Suffix)	−65 to 150°C
(CJ Suffix)	−65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic DIP ^c	470 mW
16-Pin Plastic Narrow SOIC ^d	600 mW

Notes:

- Signals on S_X, D_X, or I_{NX} exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C

SPECIFICATIONS^a

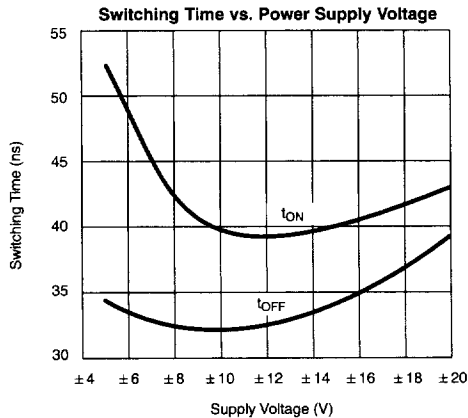
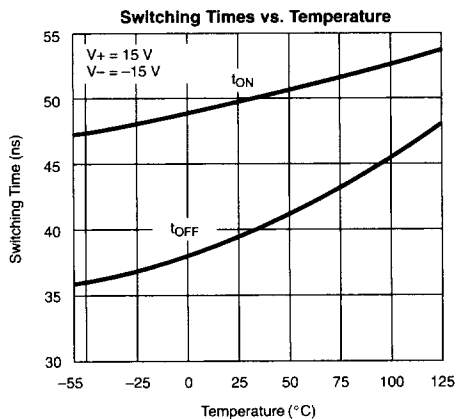
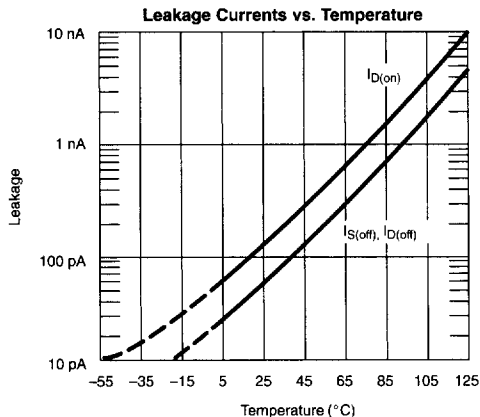
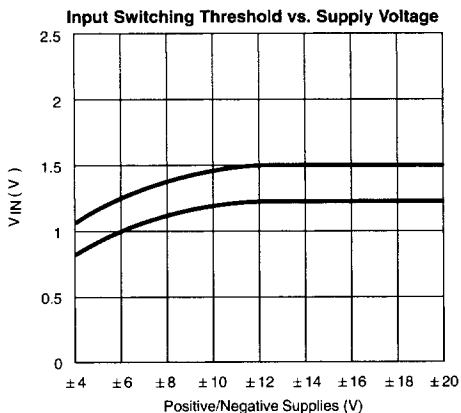
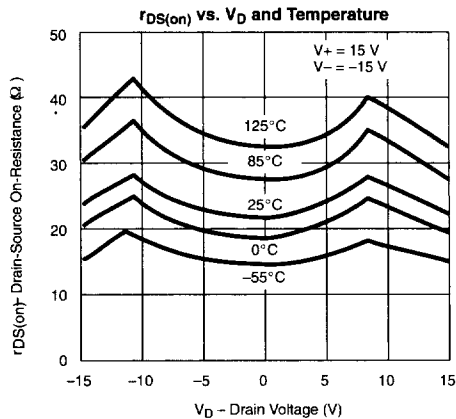
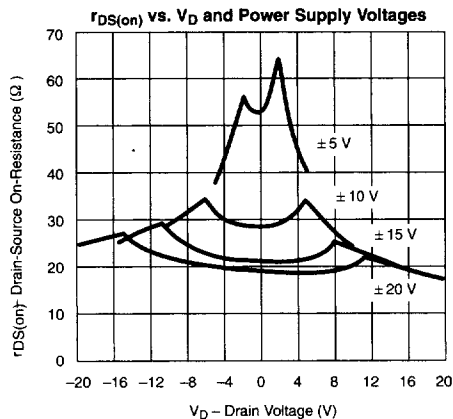
Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V− = −15 V VIN = 2.4 V, 0.8 V ^f	Temp ^b	C, D Suffix 0 to 70°C −40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	VANALOG		Full	−15		15	V
Drain-Source On-Resistance	rDS(on)	IS = 1 mA, VD = ± 10 V	Room Full		32	50 75	Ω
Switch Off Leakage Current	IS(off)	VD = ± 14 V, VS = ∓ 14 V	Room Full	−1 −20	± 0.05	1 20	nA
	ID(off)		Room Full	−1 −20	± 0.05	1 20	
Channel On Leakage Current	ID(on) + IS(on)	VS = VD = ± 14 V	Room Full	−1 −20	± 0.05	1 20	
Digital Control							
Input Current with Voltage High	IINH	VIN = 2 V	Full	−1	0.010	1	μA
		VIN = 15 V	Full	−1	0.010	1	
Input Current with Voltage Low	IINL	VIN = 0 V	Full	−1	0.010	1	
Dynamic Characteristics							
Turn-On Time	tON	VS = ± 10 V See Figure 3	Room Full		55	65 80	ns
Turn-Off Time	tOFF		Room Full		50	65 80	
Charge Injection	Q	CL = 1 nF, VS = 0 V Vgen = 0 V, Rgen = 0 Ω See Figure 3	Room		−5		pC
Source Off Capacitance	CS(off)	VS = 0 V, VIN = 5 V f = 1 MHz	Room		8		pF
Drain Off Capacitance	CD(off)		Room		8		
Channel On Capacitance	CD(on)	VD = VS = 0 V, VIN = 0 V	Room		30		
Off Isolation	OIRR	CL = 10 pF, RL = 1 kΩ f = 100 kHz See Figures 4 and 5	Room		85		dB
Crosstalk	XTALK		Room		100		
Supply							
Positive Supply Current	I+	All Channels On or Off VIN = 5 V or 0 V	Room Full		5.5	7.5 9	mA
Negative Supply Current	I−		Room Full	−6 −8	−3.4		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

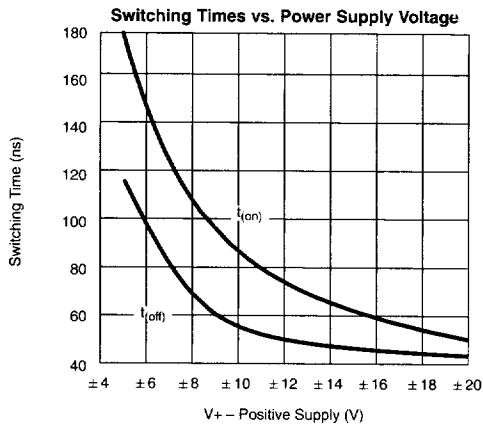
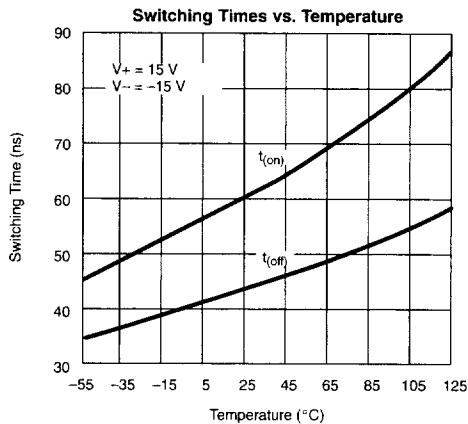


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

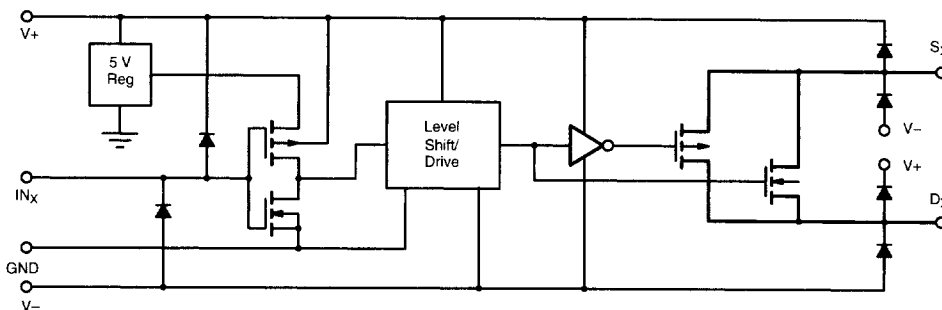


FIGURE 1.

TEST CIRCUITS

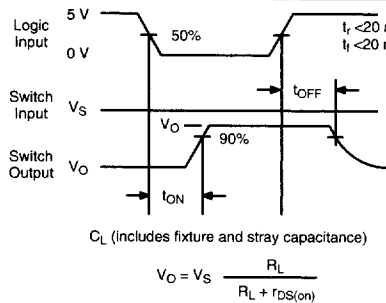
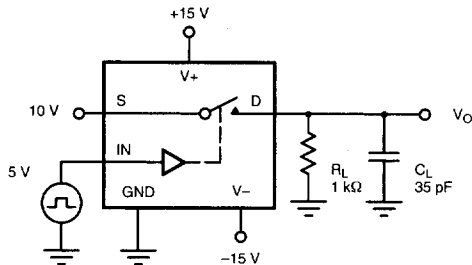


FIGURE 2. Switching Time