ASSP
Sigma delta Fractional-N PLL Frequency Synthesizer (3.5GHz single PLL)

MB15E64UV

➢DESCRIPTION

The Fujitsu MB15E64UV includes a serial input Sigma delta Fractional Phase Locked Loop (PLL) frequency synthesizer with fast lock up function. The PLL consists of 3.5GHz sigma delta Fractional-N PLL.

The new package (BCC18) decreases a mount area of MB15E64UV about 50% comparing with the latest package, BCC20.

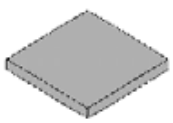
MB15E64UV is ideally suitable for digital mobile communications, such as CDMA.

➢FEATURE

-Operating frequency : 100MHz – 3500MHz
-Fractional-N PLL : modulo 262144(2^{18}) or 32768(2^{15})
Fast lock up and low noise.
-Power supply voltage :Vcc=2.7V to 3.3V
-Low current consumption : Icc (typ)=4.9mA(Vcc=Vp=3.0V, Ta=25°C)
-Direct power saving function : Power supply current in power saving mode
Typ. 0.1 uA (Vcc=3.0V, Ta=25°C), Max. 10 uA (Vcc=3.0V)
-Integrate the automatic selector circuit for the switching the loop filter (Possible to change the switching time)
-Switching charge pump current by a serial data.
Stable mode: 94uA / Fast lock mode: 4.5mA
-Integrate the open drain switch for the loop filter.
-2-modulus prescaler 16/17
-Serial input programmable reference divider : Binary 6bit R=1 to 63
-Serial input programmable divider consisting of
Binary 4 bit swallow counter : 0 to 15
Binary 8 bit programmable counter : 9 to 255
-Digital lock detector
-On-chip phase control for the phase comparator
-Operating temperature: Ta=-40 to +85 °C

➢PACKAGE

18-pad Plastic BCC



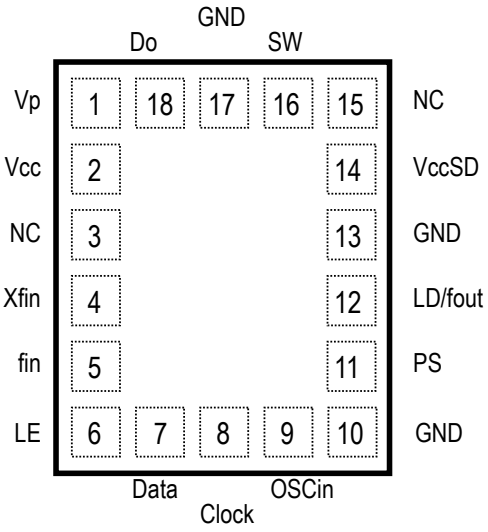
LCC-18P-M05

MB15E64UV

➢PIN ASSIGNMENT

BCC-18

TOP VIEW



LCC-18P-M05

➢PIN DESCRIPTIONS

Pin No	Pin name	I/O	Descriptions
1	Vp	–	Power supply voltage input pin for the Charge Pump circuit.
2	Vcc	–	Power supply voltage input pin. Except for CP circuit.
3	NC	–	No connection
4	Xfin	I	Prescaler complimentary input. This pin should be grounded via a capacitor.
5	fin	I	Prescaler input pin. Connection to an external VCO should be via AC coupling.
6	LE	I	Load Enable signal input. When LE is “H”, data in the shift register is transferred to the corresponding latch according to the control bits in the serial programming data.
7	Data	I	Serial data input. Data is transferred to the corresponding latch ref counter or program counter according to the control bits setting in the serial programming data.
8	CLK	I	Clock input for the 24 or 29 bit shift register. One bit data is shifted into the shift register on a rising edge of the clock.
9	OSCin	I	The programmable reference divider input. External TCXO reference oscillator input or connection to crystal. TCXO should be connected with via AC coupling.
10	GND	–	Ground
11	PS	I	Power saving mode control pin. This pin must be set at “L” when the power supply is started up. (Open is prohibited) PS=”H”: Normal mode (according to serial data) PS=”L”: Power saving mode
12	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout). The output signal is selected by the LD1, LD2 and LD3 bits in the serial data. Lock detector (LD) output has two mode, Buffer output or Open drain output. The LD signal is outputted by VDIG (3V system) in the Buffer mode. When Open drain mode is selected, the LD/fout pin should be connected to the outside power supply via pulled-up resistor. When the resistor is 50ohm, the leakage current of low state is about 50uA and the constant value is 4usec. (Recommendation value)
13	GND	–	Ground
14	VccSD	–	Power supply voltage input pin for the sigma delta modulation section. Except for CP.
15	NC	–	No connection
16	SW	O	Open drain switch for the high speed up mode
17	GND	–	Ground
18	Do	O	Charge Pump output.

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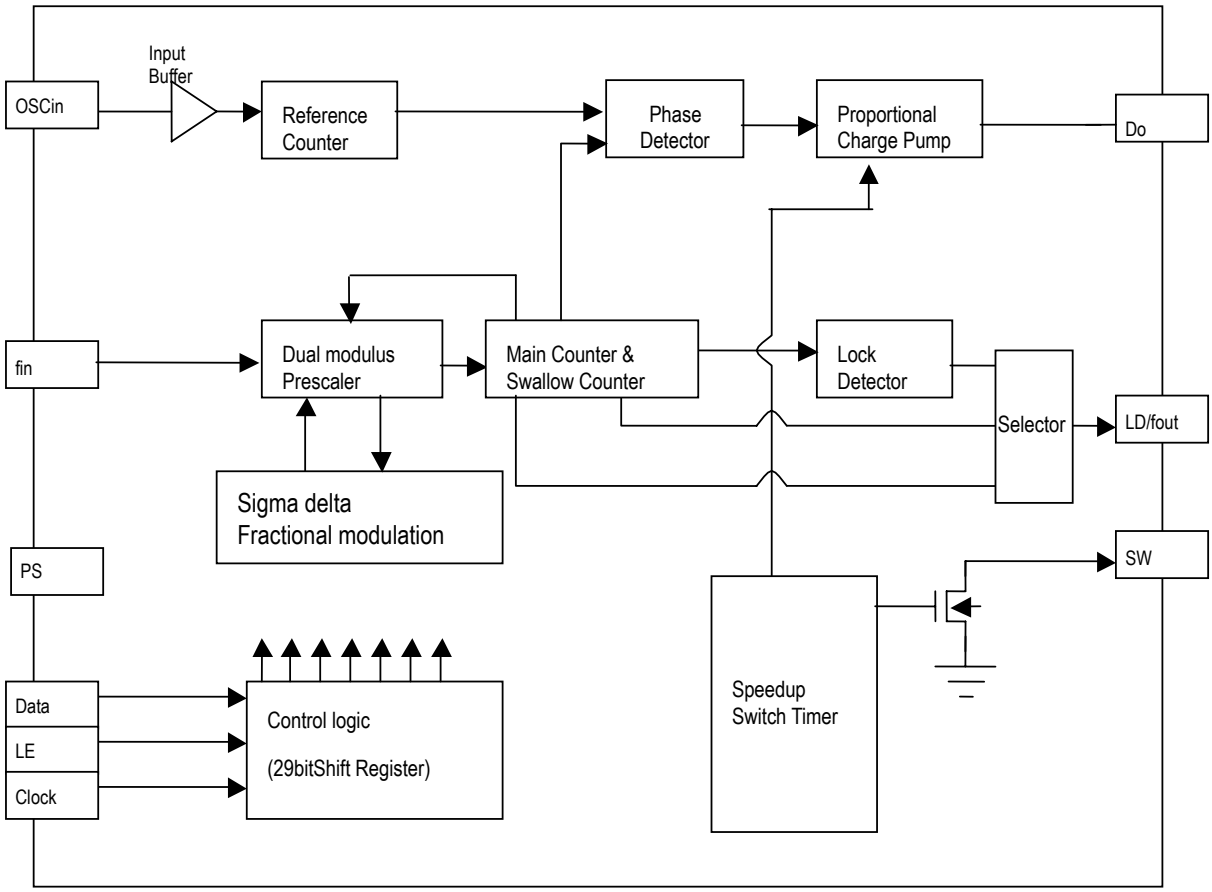
➢BLOCK DIAGRAM



➢ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	Vcc	-0.5 to 3.6	V	Vcc=VccSD
	Vp	Vcc to 3.6	V	
Input voltage	Vi	-0.5 to Vcc+0.5	V	
RF Input power AC Input voltage	P_I	max. +8	dBm	
	V_{IRF}	max. Vcc	V	
Output voltage	Vo	GND to Vcc	V	LD/fout
	V_{DO}	GND to Vp	V	Do
Input current	I_{MAX}	-10 to +10	mA	
Storage temperature	T_{STG}	-55 to +125	°C	

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

➢RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	Vcc	2.7	3.0	3.3	V	Vcc=VccSD
	Vp	Vcc	-	3.3	V	
Input voltage	Vi	GND	-	Vcc	V	
Operating temperature	Ta	-40	-	+85	°C	

Note: Vcc must supply equal voltage.

Handling Precautions

-This device should be transported and stored in anti-static containers.

-This is a static-sensitive device ; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.

-Always turn the power supply off before inserting or removing the device from its socket.

-Protect leads with a conductive sheet when handling or transporting PC boards with devices

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➢ELECTRICAL CHARACTERISITCS

(Vcc=2.7V to 3.3V, Ta=-40 to +85°C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
Power supply current		Icc*1	Vcc=Vp=3.0V		–	4.9	6.5	mA
Power saving current		Ips	Vcc current at PS="L		–	0.1*2	10	uA
Operating frequency		fin*3	AC coupling.		100	–	3500	MHz
		fosc	min. 500mVpp	R=1	5	–	20	MHz
				2 ≤ R ≤ 63	5	–	40	
Input sensitivity		PfinRF	50Ω termination		-10	–	+2	dBm
		Vosc			0.5	1.0	1.5	Vp-p
Phase Detector Operating Frequency		fMAIN_PD			0.4	–	20	MHz
Input voltage	Data, Clock LE	VIH	With Schmitt trigger circuit		0.7Vcc+0	–	–	V
		VIL	With Schmitt trigger circuit		–	–	0.3Vcc-0.	V
	PS	VIH			0.7Vcc	–	–	V
		VIL			–	–	0.3Vcc	V
Input current	Data Clock LE	IIH*4			-1.0	–	+1.0	uA
		IIL*4			-1.0	–	+1.0	uA
Output voltage	LD/fout	VOH	Vcc=3.0V, IOH=-1mA		Vcc-0.4	–	–	V
		VOL	Vcc=3.0V, IOL=1mA		–	–	0.4	V
	Do	VOH	Vcc=Vp=3.0V, IOH=-0.01mA		Vp-0.4	–	–	V
		VOL	Vcc=Vp=3.0V, IOH=0.01mA		–	–	0.4	V
High impedance cutoff current	Do	IOFF	Vcc=3.0V, VOFF=0.5V to Vcc-0.5V		–	–	2.5	nA
Hi-Speed mode output Resistance	SW	ZSSH	Normal mode (Switch at OFF)		100	–	–	kΩ
			Hi speed mode(Switch at ON)		–	35	70	Ω

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➢ELECTRICAL CHARACTERISITCS (Continued)

Parameter			Symbol	Condition	Value			Unit
					MIN	TYP	MAX	
Output current		LD/fout	I_{OH}*5	Vcc=3.0V	–	–	-1.0	mA
			I_{OL}	Vcc=3.0V	+1.0	–	–	mA
		Do	I_{DOH}*4	Vcc=Vp=3.0V,V_{DOH}=Vp/2 Ta=25°C, TMC=CS="L"	-0.16	-0.094	-0.04	uA
			I_{DOL}		+0.04	+0.094	+0.16	uA
			I_{DOH}*4	Vcc=Vp=3.0V,V_{DOH}=Vp/2 Ta=25°C, TMC="L",CS="H"	-6.1	-4.5	-2.4	mA
			I_{DOL}		+2.4	+4.5	+6.1	mA
CP current ratio	RF	I_{DOL}/I_{DOH}	I_{DOMT}*5	V_{DO}=Vp/2,Ta=25°C	–	8	15	%

∗1:Conditions: Vcc=VccSD=Vp=3.0V,Ta=25°C, fvco=3300MHz,fosc=19.2MHz(-2dBm), fr=3.84MHz in locking state

∗2:Conditions: Vcc=VccSD=Vp=3.0V, Ta=25°C, fosc=19.2MHz(-2dBm),CLK,Data,LE:VIL=GND, VIH=Vcc

∗3:AC coupling. The minimum frequency is specified with a connecting coupling capacitor of 1000pF.

∗4: The minus "-" means the direction of current flow.

∗5:Conditions: Vcc=Vp=3.0V, Ta=25°C (| | I_{DOL} | - | I_{DOH} | |)/ [(| I_{DOL} | + | I_{DOH}|)/2] × 100%

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➢ FUNCTIONAL DESCRIPTION

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Serial data of binary data is entered through Data pin. On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch them depending upon the control bit data setting.

Control bit (CN1, CN2 and CN3) and shift resistor format are as follows.
According to "LEN" bit, the serial data length can be changed. At that time, the order of the bits is also changed.
When "LEN" bit is "0", the format of first byte can be changed according to MODE bit.
*The 3rd Line with Mode bit should be inputted at first. If the 3rd Line is inputted finally after Power-ON, the 1st Line will be invalid.

Table1. Shift Register Configuration at "LEN" bit=1

LSB **Data Flow** → **MSB**

Line	CN1	CN2	CN3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
1st	1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	A1	A2	A3	A4	N1	N2	N3	N4	TMU1	TMU2
2nd	0	1	0	R1	R2	R3	R4	R5	R6	TM1	TM2	TM3	TM4	TM5	TM6	TM7	X	X	X	X	N5	N6	N7	N8	X	X	X	X	X
3rd	0	0	0	LD1	LD2	LD3	DET	FC	X	X	X	X	X	CS	ODSW	SC	X	MODE	TMC	X	X	X	PWDN	LEN	X	X	X	X	X

Table2. Shift Register Configuration at "LEN" bit=0 and "MODE" bit=0

LSB **Data Flow** → **MSB**

CN1	CN2	CN3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	A1	A2	A3	A4	N1
0	1	0	R1	R2	R3	R4	R5	R6	TM1	TM2	TM3	TM4	TM5	TM6	TM7	X	N2	N3	N4	N5	N6	N7	N8
0	0	0	LD1	LD2	LD3	DET	FC	X	X	X	X	X	CS	ODSW	SC	X	MODE	TMC	X	TMU1	TMU2	PWDN	LEN

Table3. Shift Register Configuration at "LEN"bit=0 and "MODE" bit=1

LSB **Data Flow** → **MSB**

CN1	CN2	CN3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	A1	A2	A3	A4	N1	N2	N3	N4
0	1	0	R1	R2	R3	R4	R5	R6	TM1	TM2	TM3	TM4	TM5	TM6	TM7	X	X	X	X	N5	N6	N7	N8
0	0	0	LD1	LD2	LD3	DET	FC	X	X	X	X	X	CS	ODSW	SC	X	MODE	TMC	X	TMU1	TMU2	PWDN	LEN

Note: Data input with MSB first.

Description for the serial data

F1 to F18	: Fractional-N increment setting bit for the fractional accumulator
(F1 to F15)	At MODE bit=0 (MODE1): 0 to 262143.
	At MODE bit=1 (MODE2): 0 to 32767 (F<Q)
A1 to A4	: Divide ratio setting bits for the swallow counter. (0 to 15)
N1 to N8	: Divide ratio setting bits for the programmable counter. (9 to 255)
R1 to R6	: Divide ratio setting bits for the reference counter. (1 to 63)
TMC	: Timer circuit switch bit. (TMC=1:Enable, TMC=0:Disable)
TM1 to TM7	: Delay time setting bits for timer at speed up mode.
TMU1, TMU2	: Compensate time setting bits at speed up. (The range is 0D to 15D, TM+TMU)
	At LEN bit=1:Set it on 1st Line.
	At LEN bit=0:Set it on 3rd Line.
LD1 to LD3	: Select bit for the lock detect output or a monitoring the counter output.
DET	: Select bit for the lock detect output. *1
	DET bit="0": Buffer output mode
	DET bit="1": Open drain mode
FC	:Phase control bit for the phase detector.
CS	:Charge pump current setting bit for speed up timer
	CS bit="0": Change charge pump current. The switching time depends on setting time of TM bit.(Icp is 4.5mA to 0.1mA).
	CS bit="1": Fix charge pump current (Icp=4.5mA)
ODSW	:Open drain (NMOS-Tr) switch control bit for the speed up mode.
	ODSW bit="0": Active. The period of ON/OFF depends on setting time of TM bit.
	ODSW bit="1": OFF
SC	: Order of sigma delta setting bit
	SC bit="0" : 2nd order
	SC bit="1" : 3rd order
MODE	: Modulo setting bit and data format of 1st Line setting bit.
	MODE bit="0": MODE1 Modulo=262144=(2^{18})
	MODE bit="1": MODE2 Modulo=32768=(2^{15})
PWDN	: Power saving setting bit. Control the power saving mode by the relation of the PWDN bit and PS pin
LEN	: Data length setting bit
	LEN bit="0": 24bit
	LEN bit="1": 29bit
X	:Dummy bit(Set "0")

Note : Data input with MSB first

*1: Lock detector (LD) output has two mode, Buffer output or Open drain output.
The LD signal is outputted by Vcc (3V system) in the Buffer mode. When Open drain mode is selected, the LD/fout pin should be connected to the outside power supply via pulled-up resistor. When the resistor is 50kohm, the leakage current of low state is about 50uA and the time constant value is 4usec. (Recommended value)

Synthesizer data setting (Fractional-N)

Fractional-N PLL divide ratio can be calculated using the following equation:

$$fvco = N_{TOTAL} \times fosc / R$$

$$N_{TOTAL} = 2 \times (P \times N + A + 3 + F/Q)$$

fvco : Output frequency of external voltage controlled oscillator (VCO)
NTOTAL: Total divide ratio
fosc : Reference oscillation frequency
R : Preset divide ratio of binary 6-bit reference counter (1 to 63)
P : Preset divide ratio of 2- modulus prescaler (16)
N : Preset divide ratio of binary 8-bit programmable counter (9 to 255)
A : Preset divide ratio of binary 4-bit swallow counter (0 to15)
F : A numerator of Fractional-N (MODE1:0 to 262143 or MODE2:0 to 32767)
Q : A denominator of Fractional-N (MODE1:2^18 or MODE2:2^15)

When F value is an even number, the value is added +1 at MODE1, and the value is added +1/8 at MODE2.

EX) fosc=19.8MHz, fvco=3500MHz and R=6
fr=19.8MHz/6=3.3MHz
NTOTAL/2=(3500MHz/3.3MHz)/2=530.3030303
Integer part: 530=PxN+A+3
At P=16 ∴N=32, A=15
Fraction part: F/Q=((3500MHz/3.3MHz)/2)-530
At Q=262144, F=79437.57496
Select Cut off the decimal. ∴F=79437
At that time, the frequency gap is for F=0.57496
∴fgap=0.57496/262144x(19.8MHz/6)/2=14Hz

Table4. Fractional-N increment of the fractional accumulator Data setting (F1 toF18)

Divide ratio (F)	F 18	F 17	F 16	F 15	F 14	F 13	F 12	F 11	F 10	F 9	F 8	F 7	F 6	F 5	F 4	F 3	F 2	F 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
262143	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: When the Modulo (Q) is 2^18, F1 to F=15 are available. F=0 to 32767
When the Modulo (Q) is 2^15, F1 to F=18 are available. F=0 to 262143

Table.5 Binary 8 bit Programmable counter data setting (N1 to N8)

Divide ratio (N)	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

Note: Divide ratio less than 9 is prohibited.

Table.6 Binary 4 bit swallow counter data setting (A1 to A4)

Divide ratio (A)	A 4	A 3	A 2	A 1
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

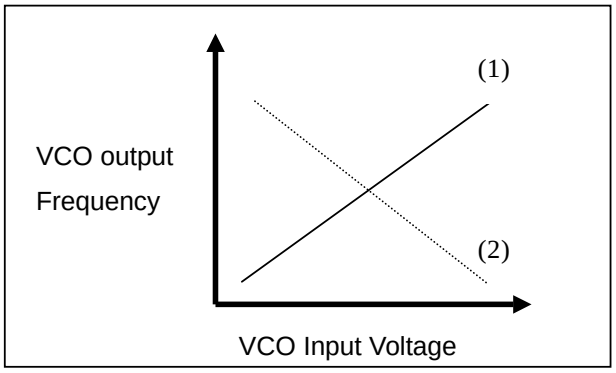
Note: Divide ratio (A) range=0 to 15, A<N

Table.7 Binary 6 bit programmable reference counter data setting (R1 to R6)

Divide ratio (R)	R 6	R 5	R 4	R 3	R 2	R 1
1	0	0	0	0	0	1
2	0	0	0	0	1	0
•	•	•	•	•	•	•
63	1	1	1	1	1	1

Table.8 Phase comparator phase switching data setting (FC)

	FC="1"	FC="0"
	Do	
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO polarity	(1)	(2)



NOTE: Z= High impedance

When the LPF and VCO characteristics are similar to (1), set FC bit high

When the VCO characteristics are similar to (2), set FC bit low.

Timer circuit

Fast lock up time can be achieved by using the timer circuit for speed up mode.
The timer circuit for speed up mode controls the time to switch the charge pump current, or internal open drain output or serial switch according to setting time automatically. The time set by TM bits. The variable charge pump current can be set by CS bit. Also the switching time of the open drain can be controlled by ODSW bit.

Table 9. Switching time setting bit (TM1 to TM7)

Value for the switching time(TM)	TM7	TM6	TM5	TM4	TM3	TM2	TM1	Ex. fosc=19.2MHz
1	0	0	0	0	0	0	1	3.3us
-	-	-	-	-	-	-	-	-
126	0	1	1	1	1	1	0	420us
127	1	1	1	1	1	1	1	423.3us

The switching time depends on oscillator frequency (fosc).

Switching time = 64 / fosc x TM

Table.10 Compensate time setting bits at speed up (TMU1 to TMU2)

Compensate value (TMU)	TMU2	TMU1
0	0	0
5	0	1
10	1	0
15	1	1

*Total value for the switching time of speed up is calculated by the following
Switching time =64/foscx(TM+TMU), TM+TMU=1 to 142

Table.11 High-speed mode function setting (ODSW)

	ODSW
1	OFF
0	Active

Table.12 Charge pump current setting bits (CS)

Charge pump current	CS	TMC bit (Timer circuit)
+/-0.094mA(fixed)	0	0
+/-4.5mA(fixed)	1	0
+/-4.5mA to +/-0.094mA	0	1
+/-4.5mA(fixed)	1	1

Table.13 LD/fout output setting bit(LD1 to LD3)

LD/fout output		LD3	LD2	LD1
LD		-	-	0
fout	fr	0	1	1
	fp	1	1	1
	Prohibit	-	0	1

When Lock detector output is selected, there are two outputs mode, Buffer output or Open drain.
In case of Buffer output, the output is digital output at 3V system.
In case of Open drain output, should pull up to the external voltage via resistor. When the resistor is 50kohm, the time constant is at 4usec, and then the leak current is about 50uA.

- Power saving mode

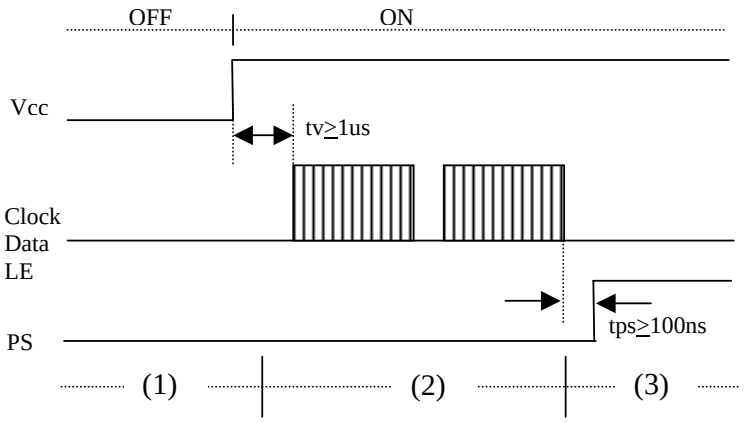
Table.14 Power saving mode setting

PLL State	PS pin	PWDN bit
Normal	H	1
Power saving	L	1
	H	0
	L	0

The intermittent mode control circuit reduces the PLL power consumption.
The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation.
When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Operation mode
The set section and reference oscillation circuit are operated. It is normal operation.

Power save mode
The power supply current in power save mode is at 0.1uA(typ). Max.10uA.
The phase detector output, Do, becomes high impedance.
The lock detector, LD, remains high, indicating a locked condition.



(1) Set PS="L" (power saving mode) at Power-ON.
(2) Set serial data 1us later after power supply remains stable (Vcc≥2.2V).
(3) Release power saving mode (PS : "L" → "H") at least 100ns after setting serial data.

➢ Serial data input timing

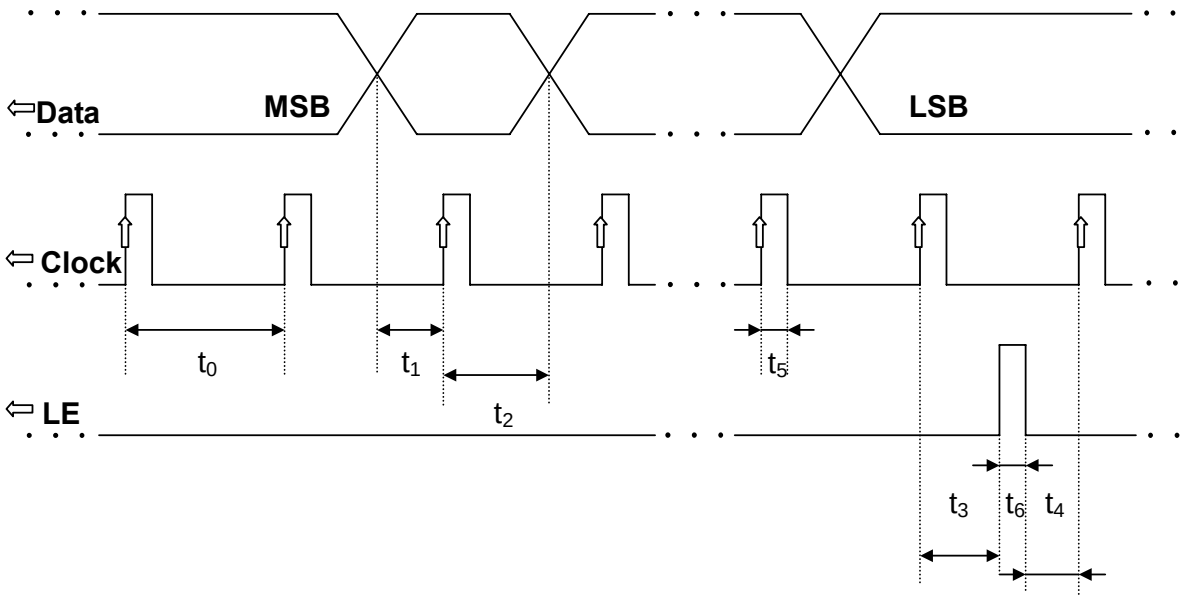


Table15.Timing parameters

Parameter	MIN.	TYP.	MAX.	Unit	Note
t0	100	–	–	ns	CK Rate
t1	20	–	–	ns	tsu CK→Data
t2	20	–	–	ns	th CK→ Data
t3	30	–	–	ns	tsu LE
t4	20	–	–	ns	tsu inactive
t5	30	–	–	ns	tw CK
t6	100	–	–	ns	tw LE

Note: LE should be “L” when the data is transferred into the shift register.

➢Setting method

Example: In case that the serial data length of 1st Line is 29bit..

1.Power-ON

Supply the voltage on all Vcc pins at the same time. If the voltage for Vcc is supplied at the different timing, the leak current is caused.

PS pin should be low at Power-ON.

2.Initial setting (PS pin is low)

LSB Data Flow → MSB

Line	CN1	CN2	CN3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
3rd	0	0	0	LD1	LD2	LD3	DET	FC	X	X	X	X	X	CS	OD SW	X	X	MO DE	TMC	X	X	X	PW DN	LE N	X	X	X	X	X
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1st	1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	A1	A2	A3	A4	N1	N2	N3	N4	TM U1	TM U2
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	0	0	0	0
2nd	0	1	0	R1	R2	R3	R4	R5	R6	TM 1	TM 2	TM 3	TM 4	TM 5	TM 6	TM 7	X	X	X	X	N5	N6	N7	N8	X	X	X	X	X
	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

(1) Input the binary data from 3rd Line first as the above table.

(2) Set each value in F bits, A bits, N bits and R bits of the initial operating frequency.

(3) 2nd and 3rd Lines are almost used at fixed status, so it is not necessary to reload the Lines after initial setting.
(It is necessary to write the 2nd Line according to the frequency setting after initial setting.)
In case that 1st Line is with 29bit length, you should only write the 1st Line when the frequency is changed.

(4) Monitor the state of LD/fout pin after data setting. When LD/fout is at “High”, the state of PLL is power saving and the operation is normal.

(5) Dummy bit, “x” should be set at “0”.

3.Release the power saving

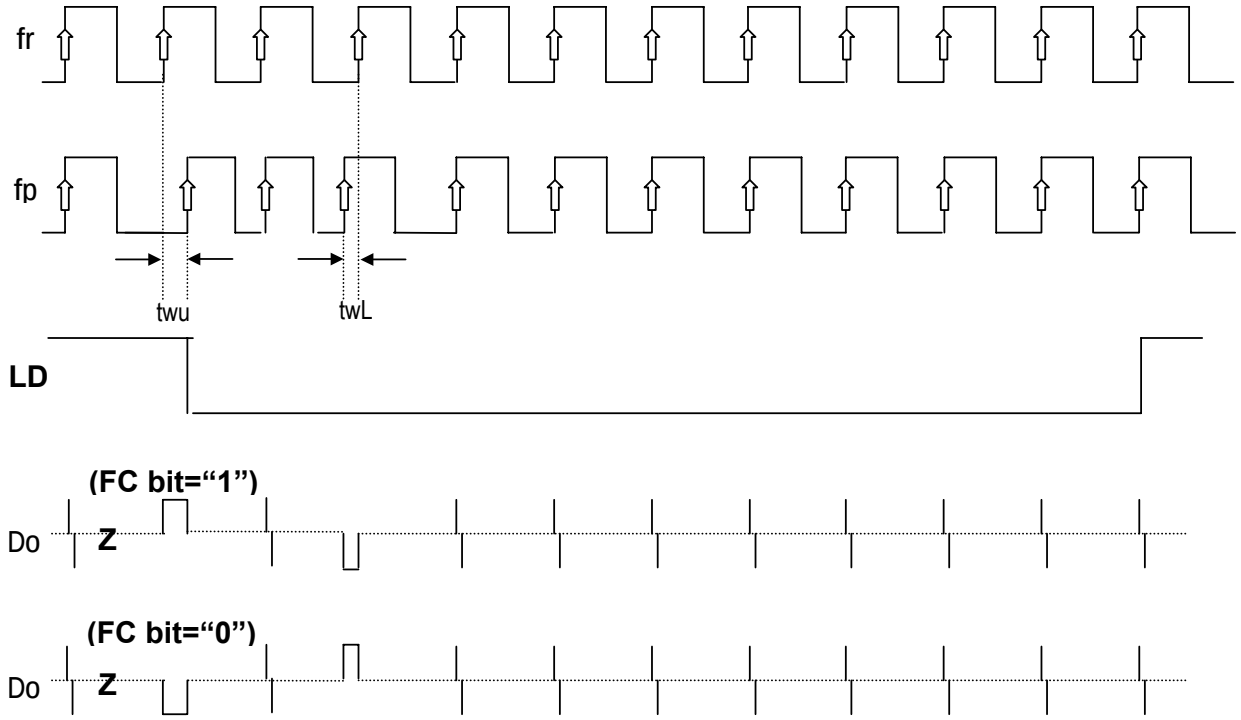
(1) PS pin change to “High”, and then PLL should be locked. When LD/fout is at “High”, PLL is locked.
*Turn on a VCO or a reference oscillator as TCXO before PS pin change to “High”.

4.Change the frequency

(1) Write 1st Line only according to frequency setting.
(If the N5 to N8 bit in 2nd Line need to be changed for setting frequency, it is necessary to write the 2nd Line.)

Line	CN1	CN2	CN3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
1st	1	F1	F2	F3	F4	F5	F6	F7	F8	F9	F 10	F 11	F 12	F 13	F 14	F 15	F 16	F 17	F 18	A1	A2	A3	A4	N1	N2	N3	N4	TM U1	TM U2
	1	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up	up

➢ Phase detector output waveform

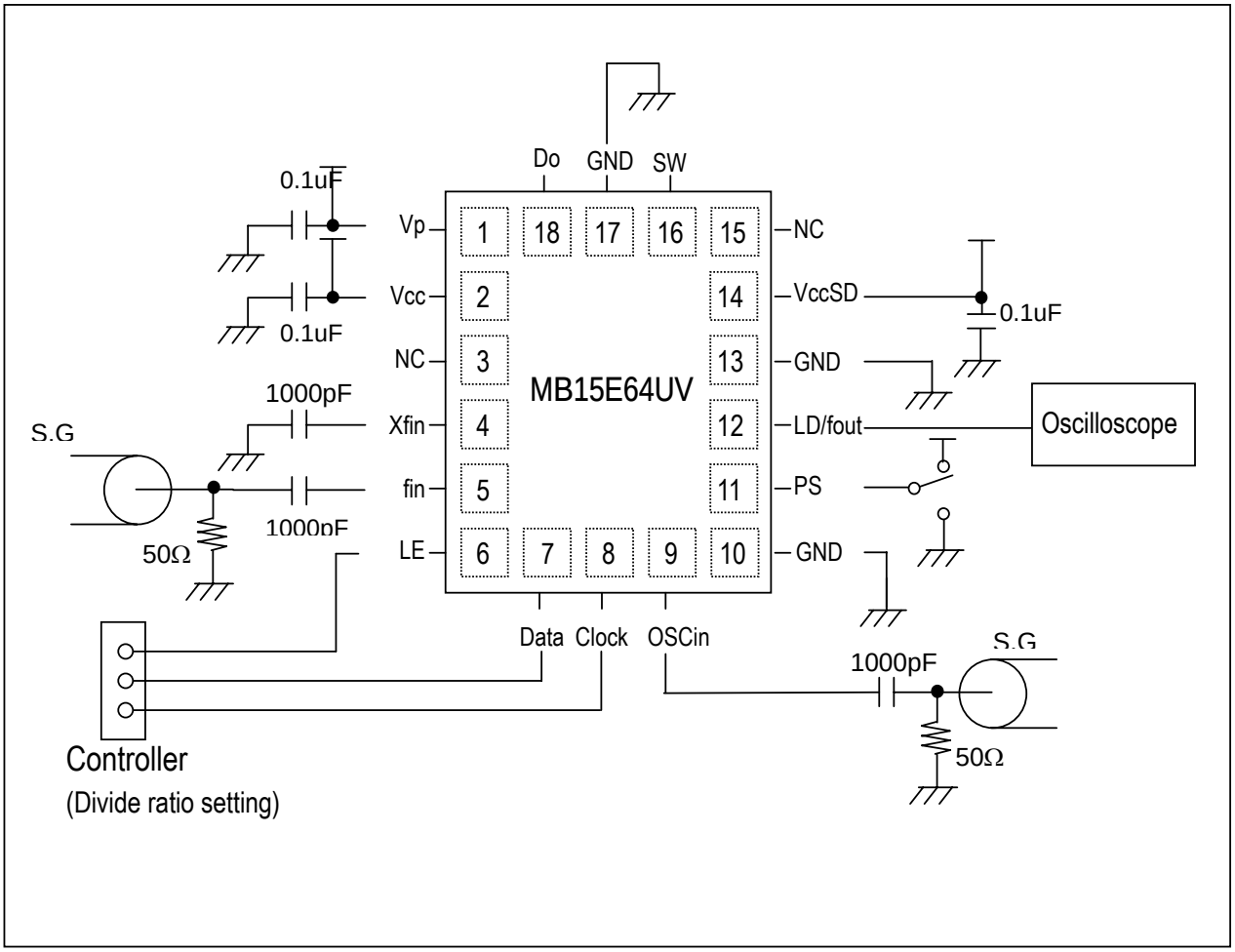


LD output logic table

PLL state	LD output
Locking state/Power save state	H
Unlocking state	L

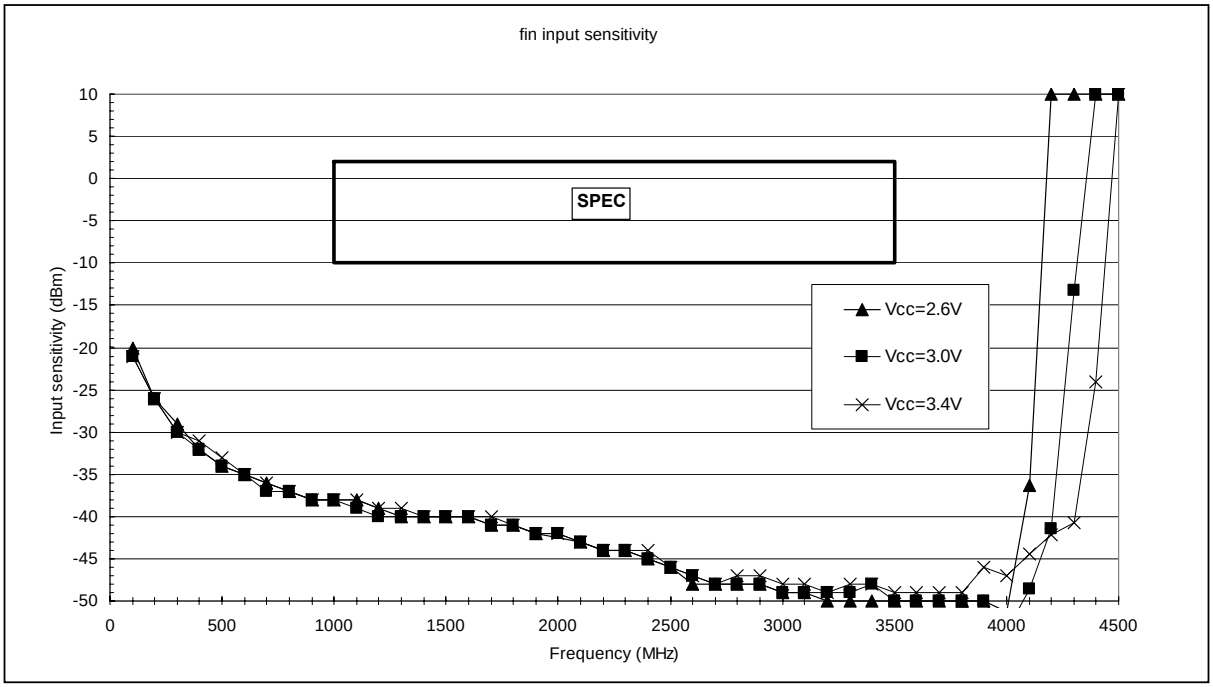
Note: 1.Phase error detection range = -2π to +2π
2.Pulses on Do signal during locked state are output to prevent dead zone.
3.LD output becomes low when phase error is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for eight cycles or more.
4. t_{WU} and t_{WL} depend on fin input frequency.
$t_{WU} \geq 1/(fin/16)/2$ (s) (e.g. $t_{WU} \geq$ 15.14ns, fin=2113.6MHz)
$t_{WL} \leq 2/(fin/16)/2$ (s) (e.g. $t_{WL} \leq$ 30.29ns, fin=2113.6MHz)

➢ Measurement circuit (for measuring input sensitivity of fin and OSCin)

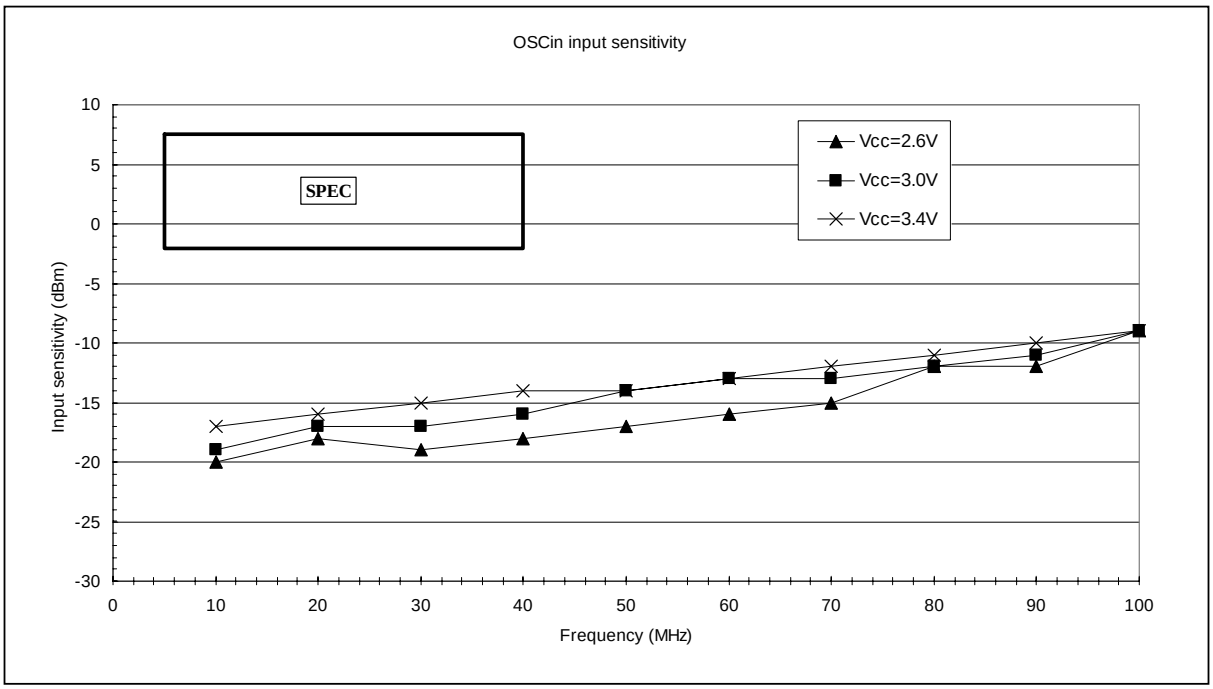


➢ TYPCAL CHARACTERISTICS

1.fin input sensetivity

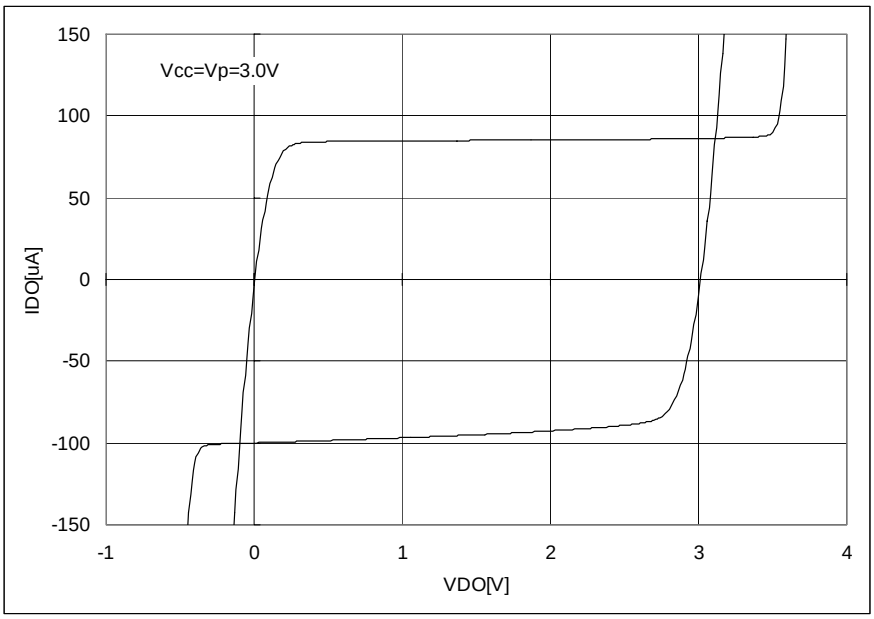


2.OSCin input sensetivity

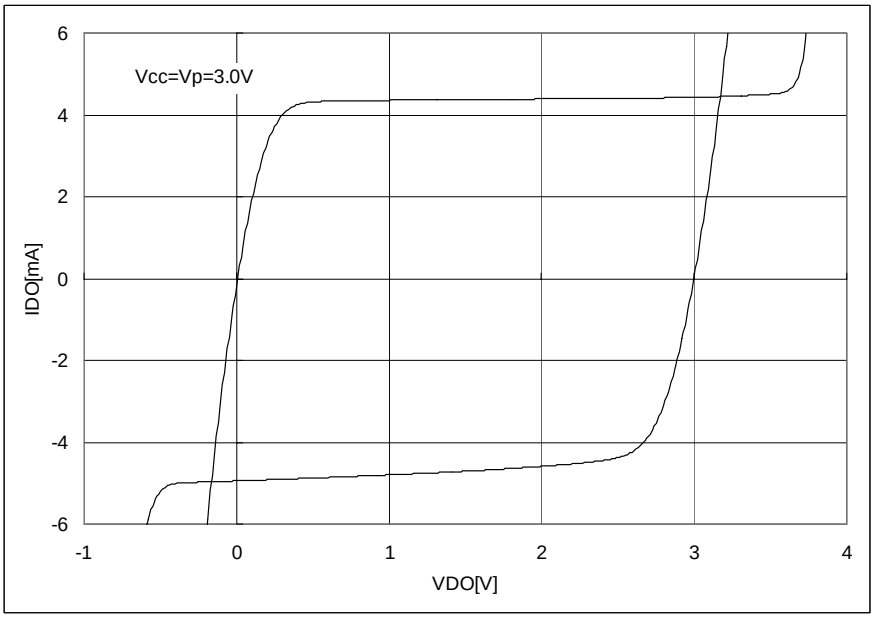


3.Do output current

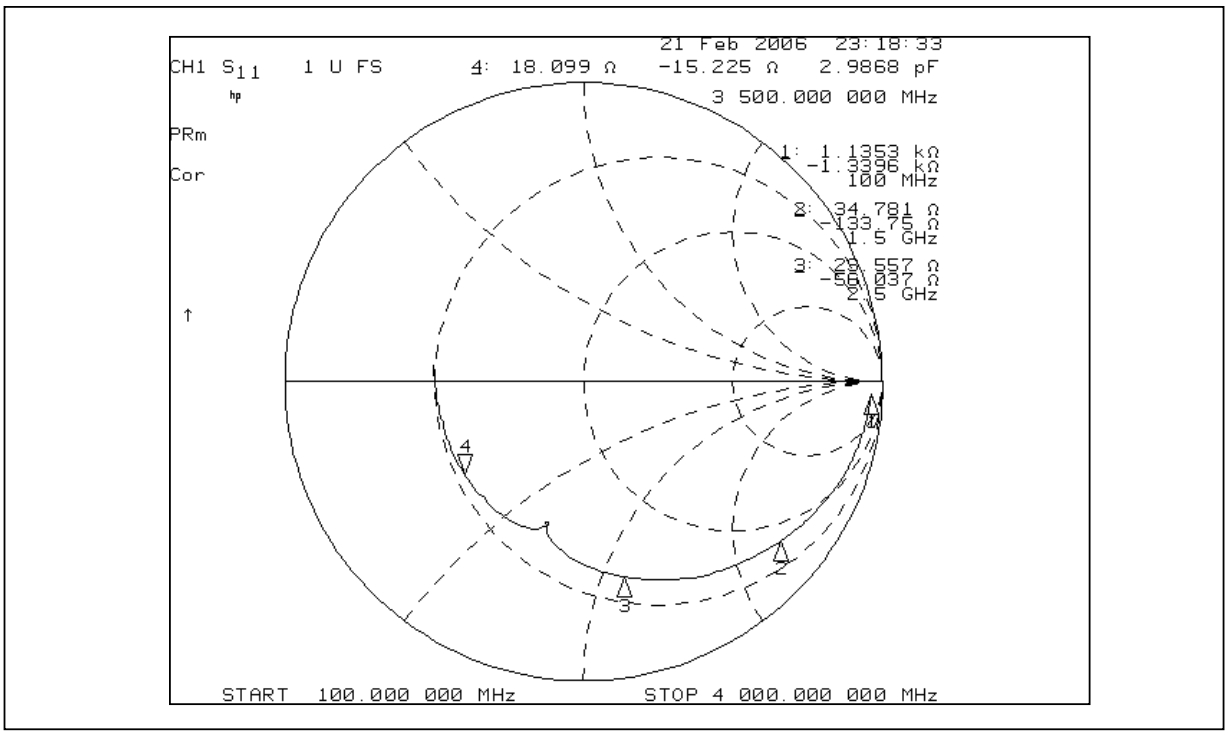
CP=94uA



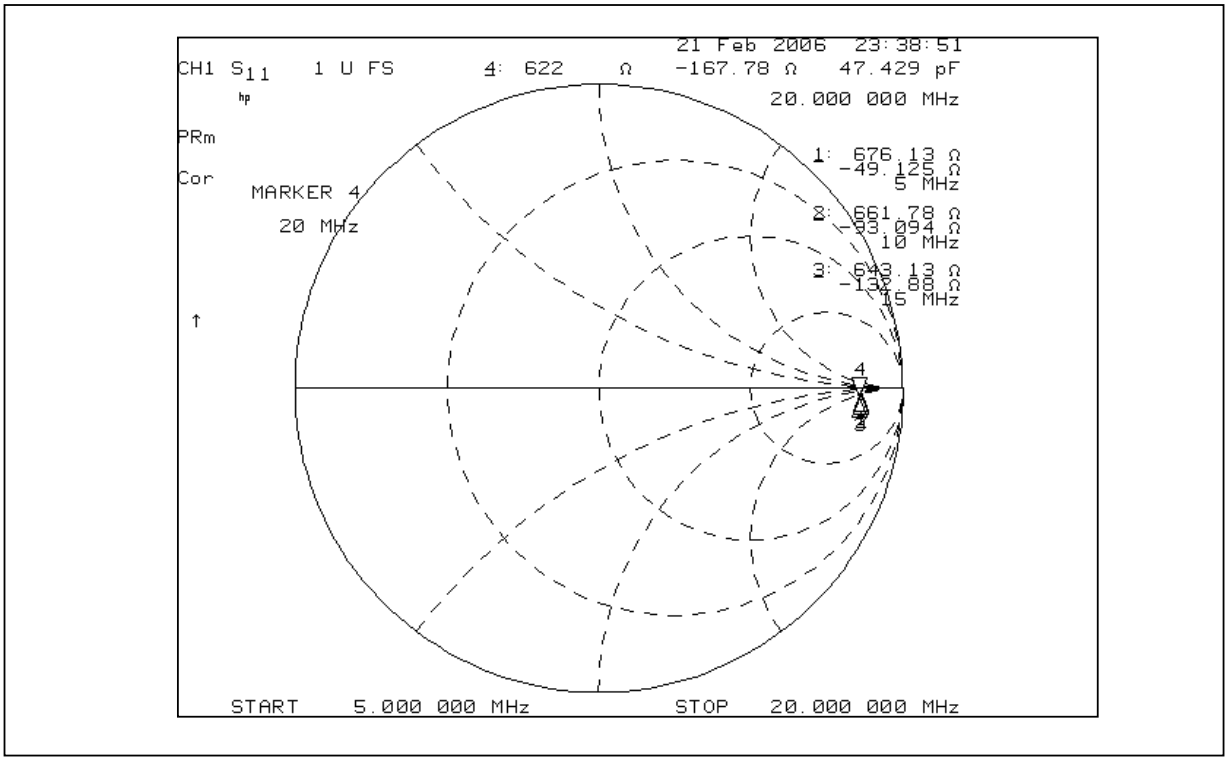
CP=4.5mA



4.fin input impedance

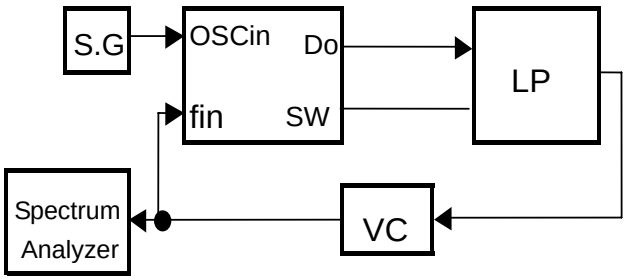


5.OSCin input impedance



MB15E64UV

➢ LOOP CHARACTERISTICS



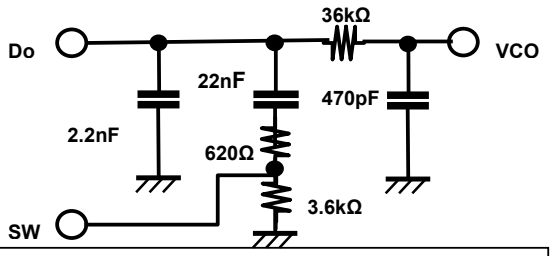
fvco=2113.6MHz Vcc=Vp=3.0V

Kv=55MHz/V Vvco=3.0V

fr=4.8MHz(R=4) Ta=25°C

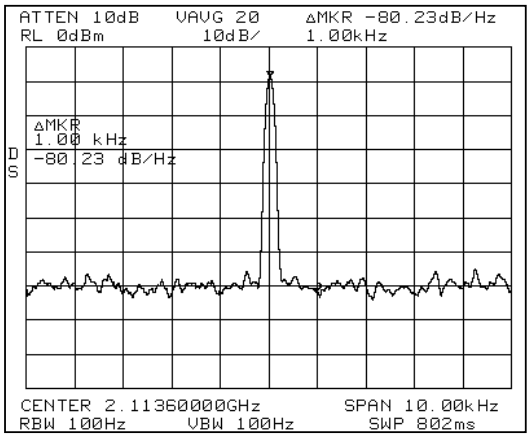
fosc=19.2MHz TMC="1",TM="10"

CS="0",ODSW="0",SC="1",MODE="0"

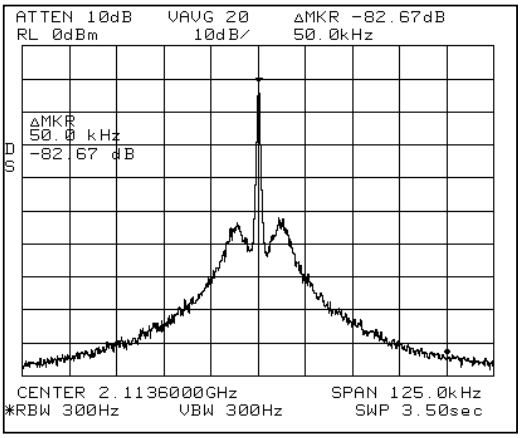


PLL Phase Noise & Spurious Noise

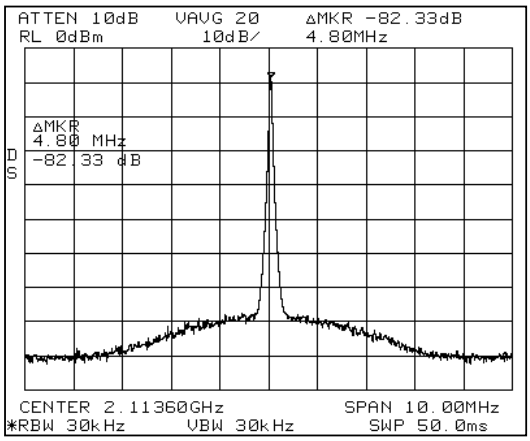
C/N 1kHz Offset



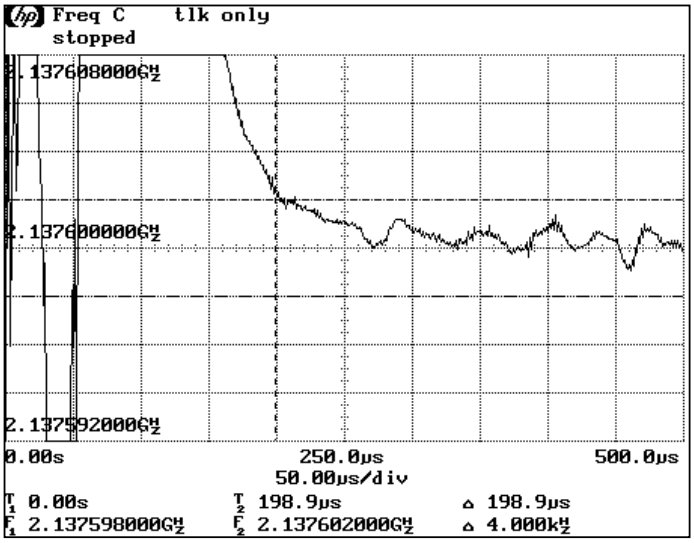
C/N 50kHz Offset



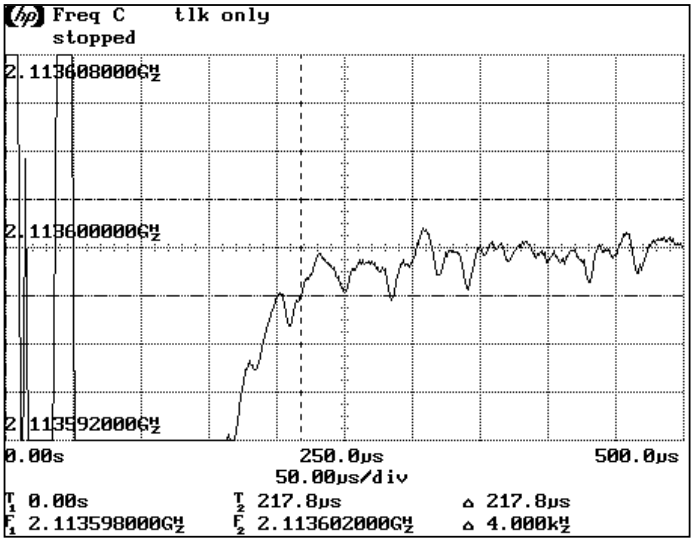
Ref.Leakage 4.8MHz Offset



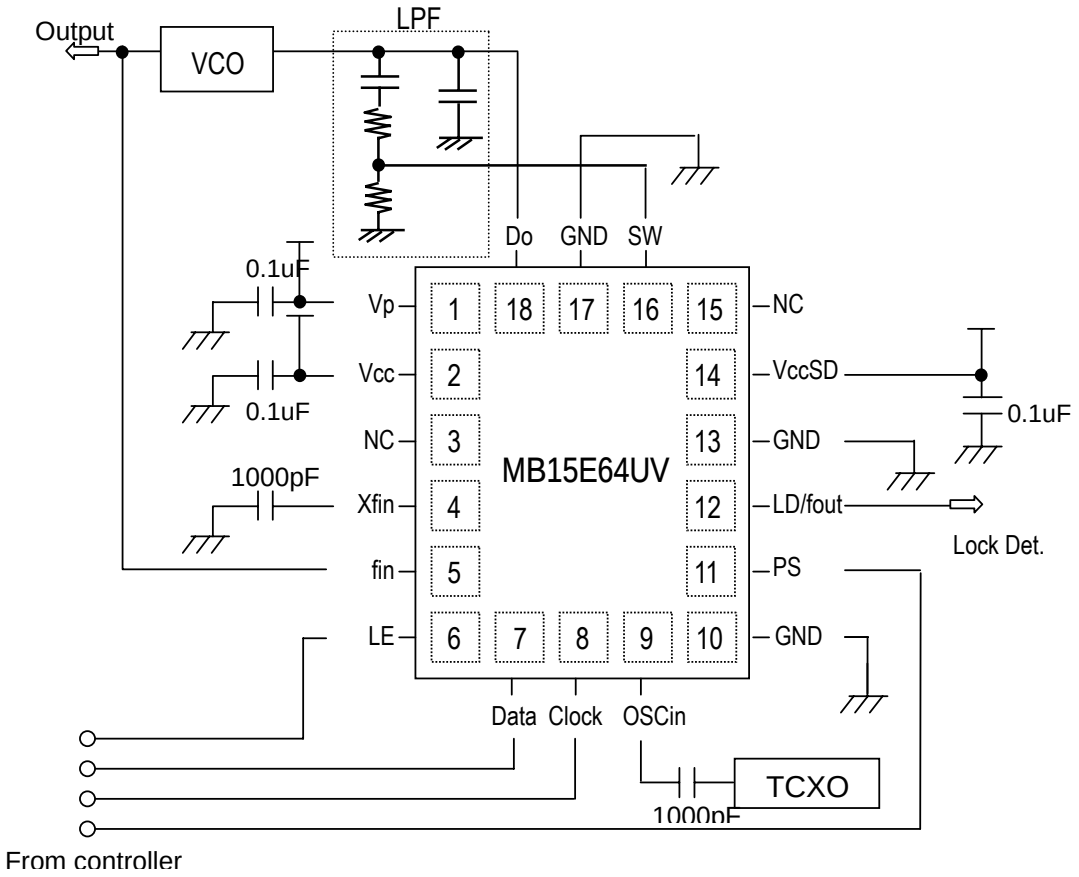
PLL Lock Up time
L:2113.6MHz -> H:2137.6MHz ±1kHz
Lch -> Hch 199us



PLL Lock Up time
H:2137.6MHz -> L:2113.6MHz ±1kHz
Hch -> Lch 218us



➢ Application example



Clock, Data, LE: Schmitt trigger circuit provided (Insert a pull-down or pull-up resister as needed to prevent oscillation when the terminals are left open)

➢SIGMA DELTA FRACTIONAL-N FUNCTION

Fractional-N type PLL uses the sigma delta modulation method, and has the following features.
(1) Integer operation at F=0
In F=0, the sigma delta circuit block is completely stopped, and RF PLL operates same as Integer-N PLL. Therefore, it is the best of the noise characteristic.

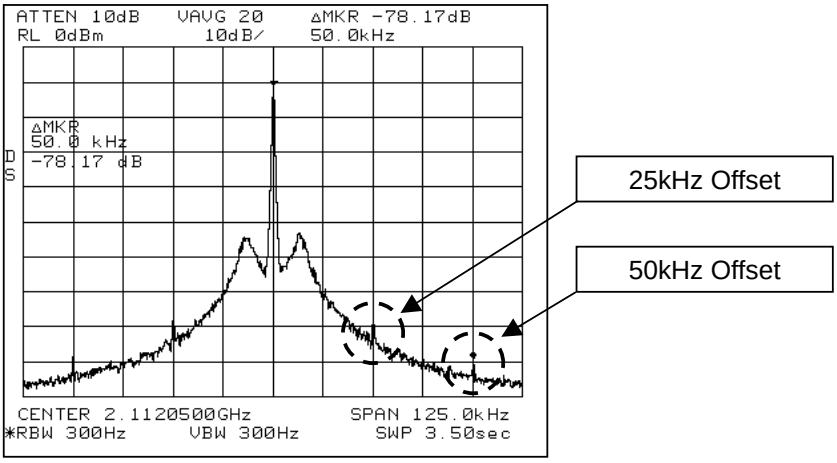
(2) Spurious characteristics
Spurious is generated in the offset part of fp, which is the comparison frequency. (It corresponds to reference Leak in the Integer-N PLL.)

(Ex.)
Ntotal becomes 440 in the use condition of fvco=2112.0MHz, fosc=19.2MHz, and R=4, and F becomes 0(Integer mode). At this time, spurious generation in the fp/R=19.2MHz/4=4.8MHz offset. (Reference Leak) (Spurious becomes a waveforms like RefLeakage of P22, and can improve by the filter design)

Spurious is generated in F/Q×fp or (Q-F)/Q×fp offset by the sigma delta circuit operation.

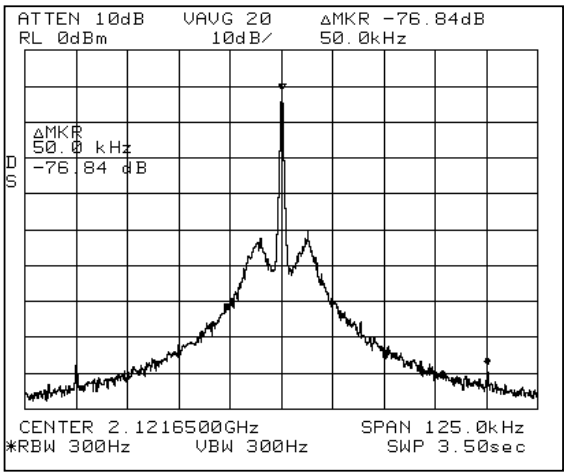
(Ex.)
Ntotal is 440.0104167, and F becoming 1365, and the spurious generation in the F/Q x 2 x fp=50kHz offset at fosc=19.2MHz, R=4, and fvco=2112.05MHz. Moreover, spurious generation in F/Q x fp=25khz offset

50kHz Offset

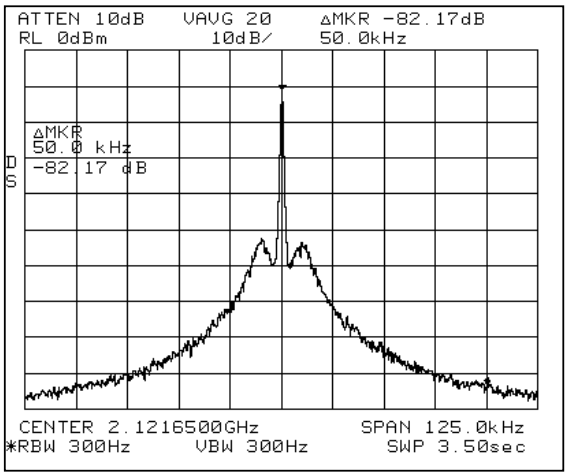


It is possible to adjust the filter as a method of decreasing this spurious. Moreover, spurious can be lost by changing R value, and changing fr.
For instance, F value becomes 1365 by Ntotal=442.0104167, and spurious is generated in F/Q x 2 x fp=50kHz and 50kHz offset in fvco=2121.65MHz at fosc=19.2MHz and R=4. However, F value becomes 67242 by Ntotal=552.5130208 when changing to R=5. Spurious is attenuated by LPF and disappears though generates spurious in the F/Q x 2 x fp=1.970MHz offset.
There is a possibility to which CN is deteriorated because the comparison frequency changes. Therefore, the characteristic confirmation by the use condition is necessary. The example of the waveforms in that case is appended to the next page.

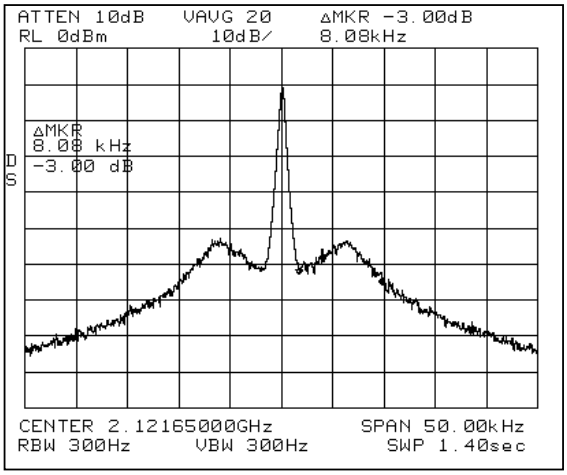
R=4 (50kHz offset)



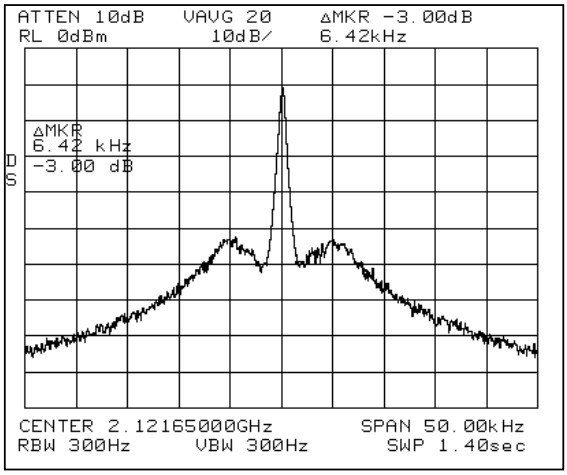
R=5 (50kHz offset)



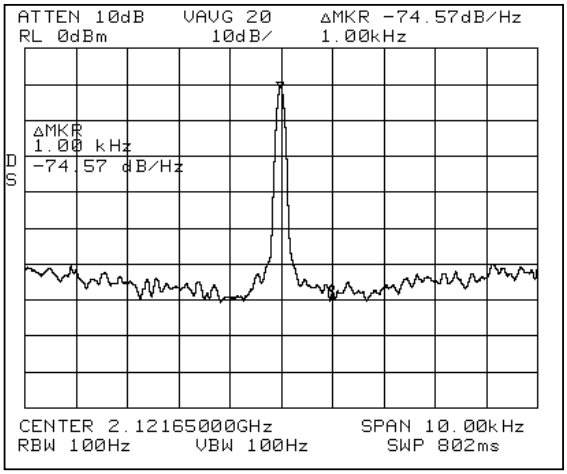
R=4 (In band waveform)



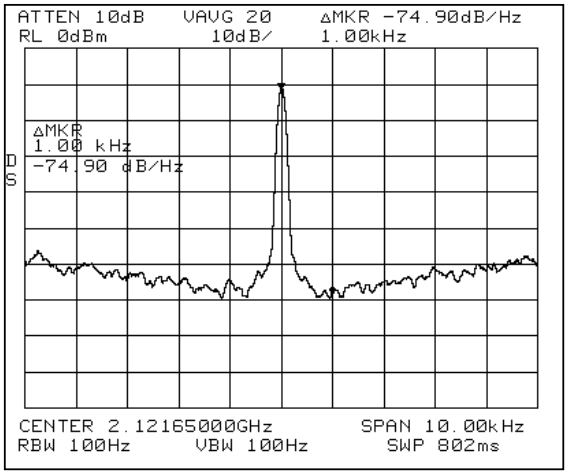
R=5 (In band waveform)



R=4 (1kHz offset)

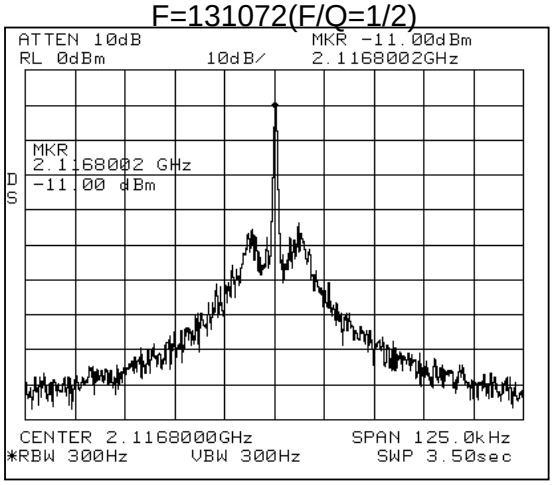


R=5 (1kHz offset)

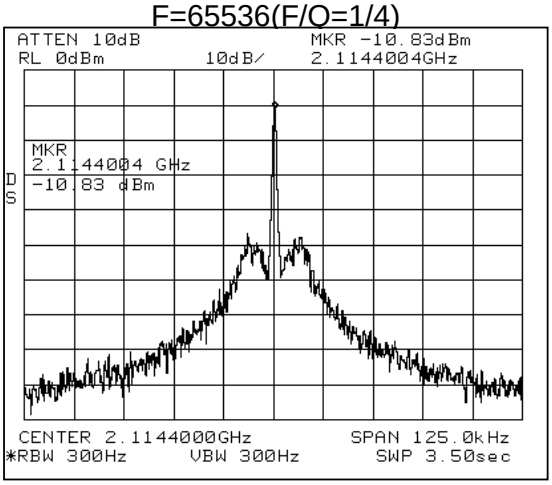


F/Q=1/2, 1/4, and 1/8 ··· When the binary dividing frequency is set, spurious is generated. When the decrease of spurious is difficult, spurious can be decreased by moving F value to the range of the allowance of the frequency gap.
(Ex.)
Spurious noise generation on the entire floor when F=131072(F/Q=1/2) is set.
Spurious noise generation on the floor when F=65536(F/Q=1/4) is set.
The example of the generation at that time in the following of the spurious waveform is shown. Moreover, the example of the waveform in case of F value +5 and F value +10 is shown.

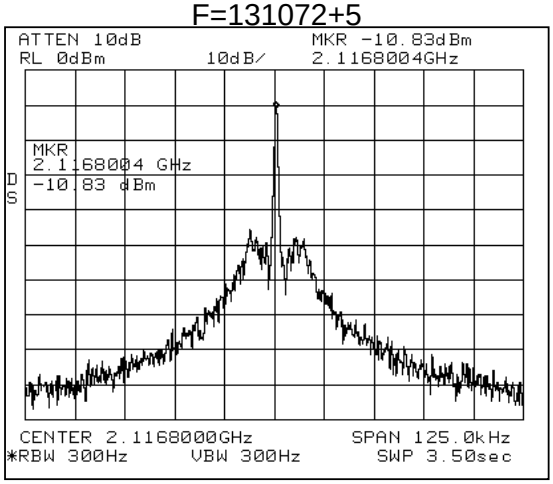
F=131072(F/Q=1/2)



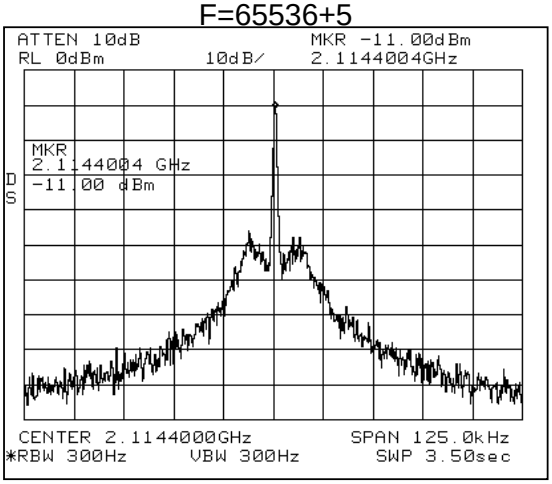
F=65536(F/Q=1/4)



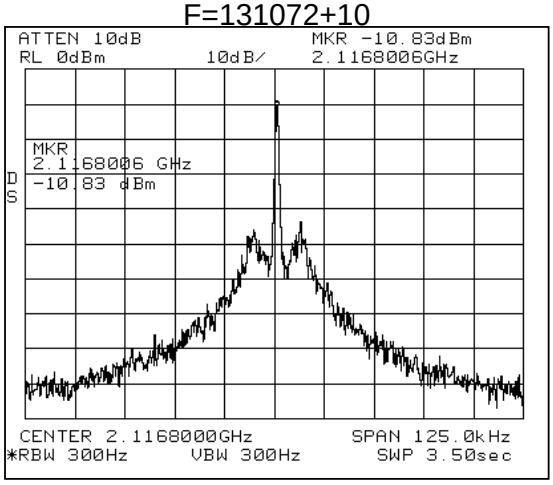
F=131072+5



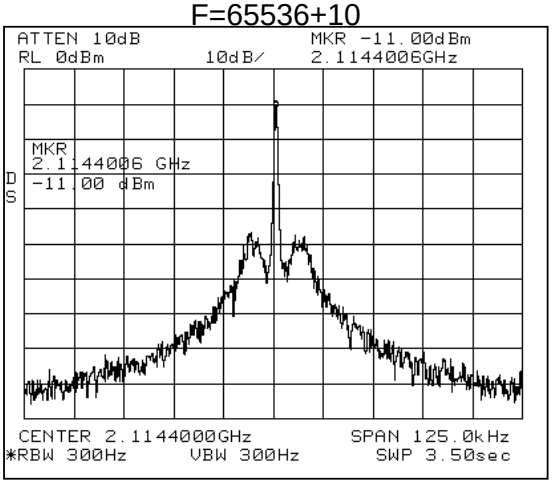
F=65536+5



F=131072+10

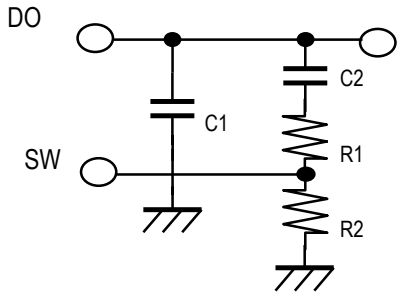


F=65536+10



➢ LOOP FILTER (Hi-Speed mode)

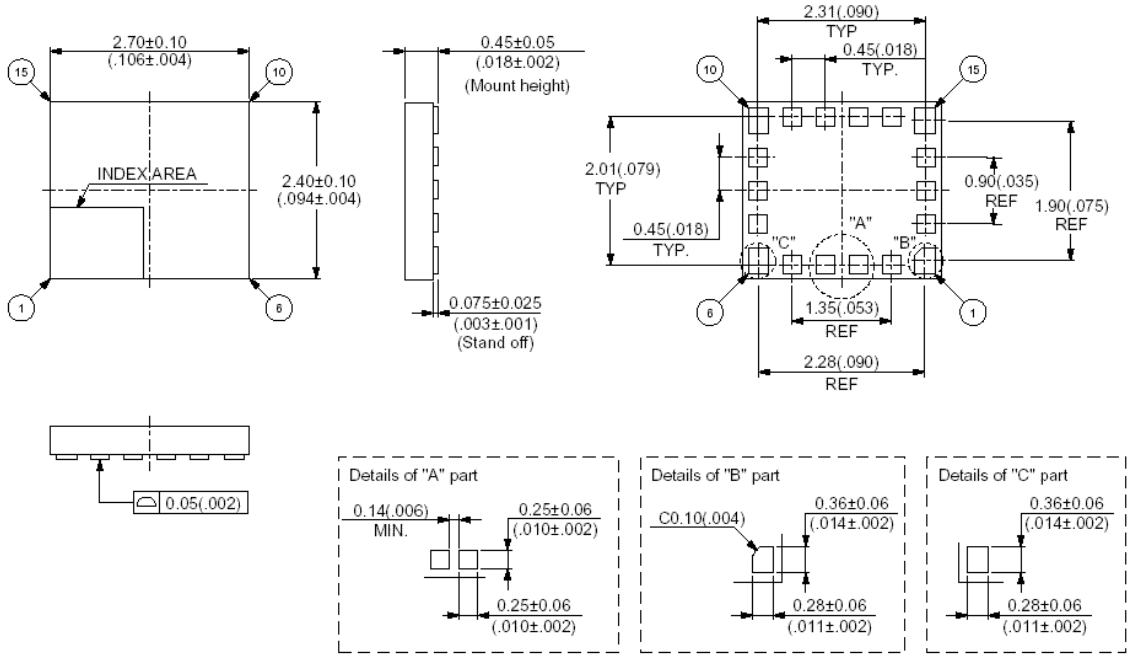
Option



➢ PACKAGE DIMENSION

Plastic BCC 18pin

(LCC-18P-M05)



Unit : mm(inches)

Note: ( )values:Reference