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## FDB8860\_F085

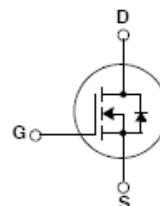
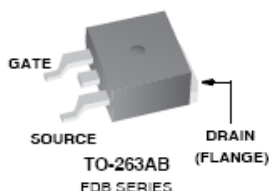
### N-Channel Logic Level PowerTrench® MOSFET 30V, 80A, 2.6mΩ

#### Features

- $R_{DS(ON)} = 1.9m\Omega$  (Typ),  $V_{GS} = 5V$ ,  $I_D = 80A$
- $Q_{g(5)} = 89nC$  (Typ),  $V_{GS} = 5V$
- Low Miller Charge
- Low  $Q_{RR}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

#### Applications

- 12V Automotive Load Control
- Start / Alternator Systems
- Electronic Power Steering Systems
- ABS
- DC-DC Converters



**MOSFET Maximum Ratings**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current Continuous ( $V_{GS} = 10\text{V}$ , $T_C < 163^\circ\text{C}$ )	80	A
	Continuous ( $V_{GS} = 5\text{V}$ , $T_C < 162^\circ\text{C}$ )	80	A
	Continuous ( $V_{GS} = 10\text{V}$ , $T_C = 25^\circ\text{C}$ , with $R_{\theta JA} = 43^\circ\text{C/W}$ )	31	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	947	mJ
$P_D$	Power Dissipation	254	W
	Derate above $25^\circ\text{C}$	1.7	$\text{W}/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

**Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance Junction to Case	0.59	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in <sup>2</sup> copper pad area	43	$^\circ\text{C/W}$

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB8860	FDB8860_F085	TO-263AB	330mm	24mm	800units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0\text{V}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1	1.7	3	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$	-	1.6	2.3	m $\Omega$
		$I_D = 80\text{A}$ , $V_{GS} = 5\text{V}$	-	1.9	2.6	
		$I_D = 80\text{A}$ , $V_{GS} = 4.5\text{V}$	-	2.1	2.7	
		$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$ , $T_J = 175^\circ\text{C}$	-	2.5	3.6	

**Dynamic Characteristics**

C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1MHz		-	9460	12585	pF
C <sub>OSS</sub>	Output Capacitance			-	1710	2275	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			-	1050	1575	pF
R <sub>G</sub>	Gate Resistance	f = 1MHz	V <sub>DD</sub> = 15V I <sub>D</sub> = 80A I <sub>g</sub> = 1.0mA	-	1.8	-	Ω
Q <sub>g(TOT)</sub>	Total Gate Charge at 10V	V <sub>GS</sub> = 0V to 10V		-	165	214	nC
Q <sub>g(5)</sub>	Total Gate Charge at 5V	V <sub>GS</sub> = 0V to 5V		-	89	115	nC
Q <sub>g(TH)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0V to 1V		-	9.1	12	nC
Q <sub>gs</sub>	Gate to Source Gate Charge			-	26	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau			-	18	-	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge			-	33	-	nC

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Switching Characteristics**

$t_{(on)}$	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 80\text{A}$ $V_{GS} = 5\text{V}, R_{GS} = 1\Omega$	-	-	340	ns
$t_{d(on)}$	Turn-On Delay Time		-	14	-	ns
$t_r$	Turn-On Rise Time		-	213	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	79	-	ns
$t_f$	Turn-Off Fall Time		-	49	-	ns
$t_{off}$	Turn-Off Time		-	-	192	ns

**Drain-Source Diode Characteristics**

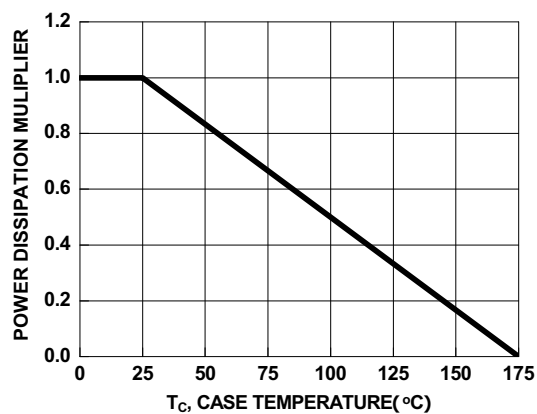
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	43	ns
$Q_{rr}$	Reverse Recovery Charge	$I_{SD} = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	29	nC

**Notes:**

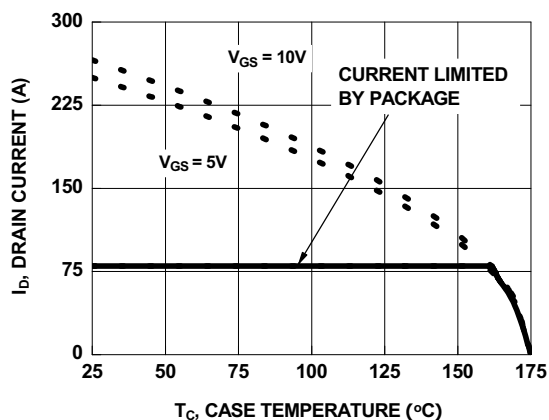
- 1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.47\text{mH}$ ,  $I_{AS} = 64\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $V_{GS} = 10\text{V}$ .  
2: Pulse width = 100s

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>  
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

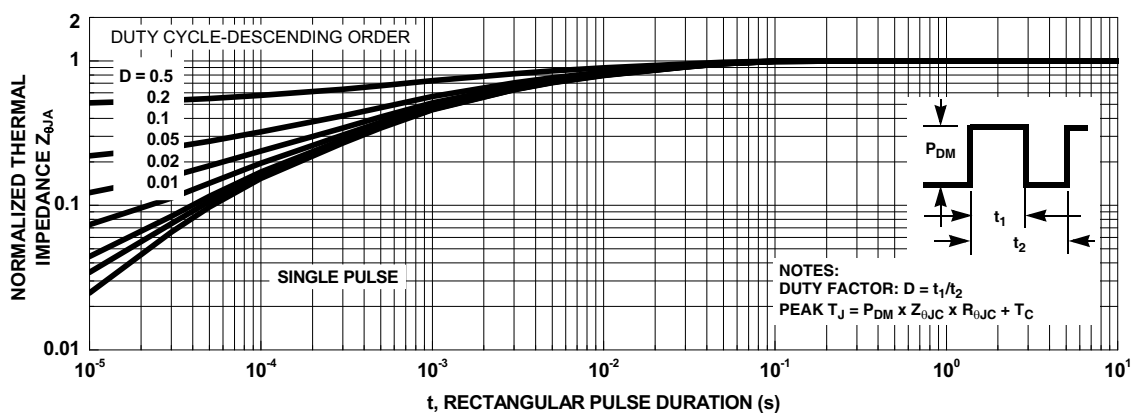
# **Typical Characteristics** $T_J = 25^\circ\text{C}$ unless otherwise noted



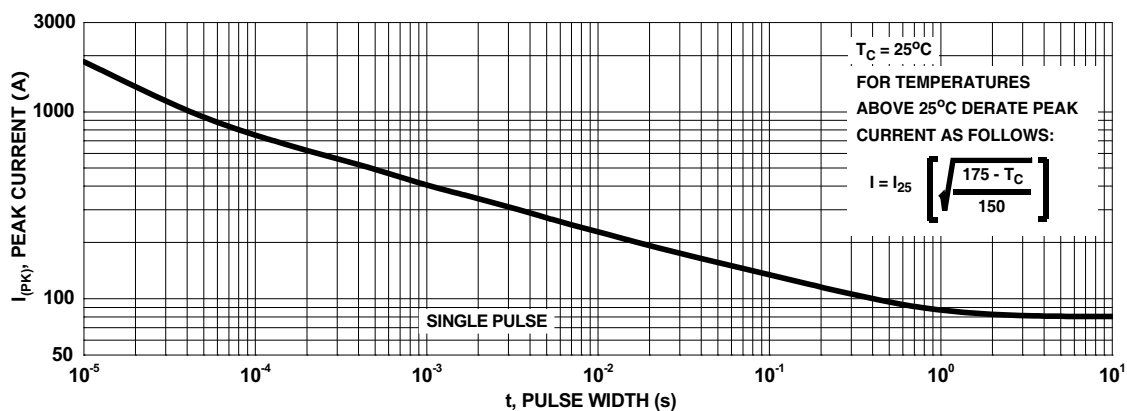
**Figure 1. Normalized Power Dissipation vs Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

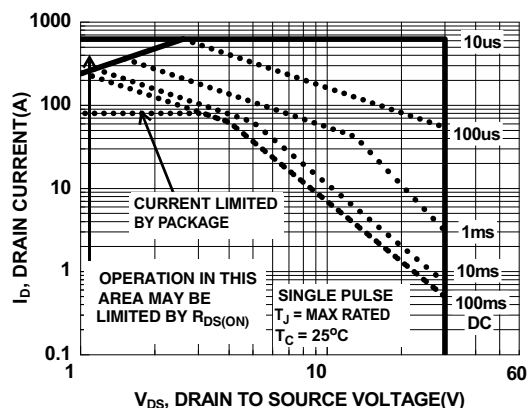
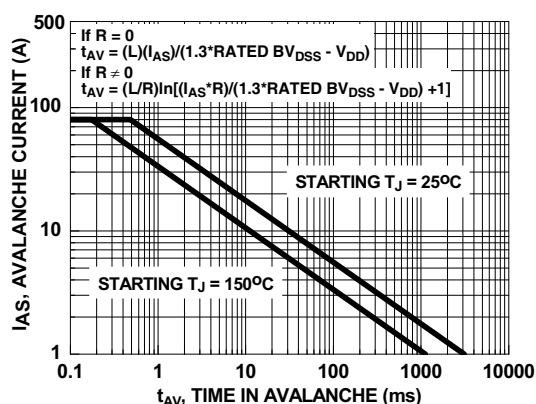


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

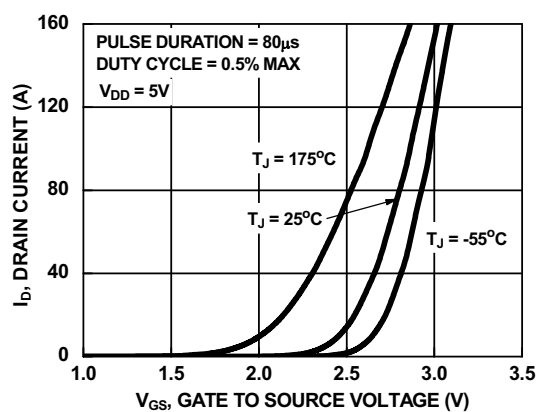


Figure 7. Transfer Characteristics

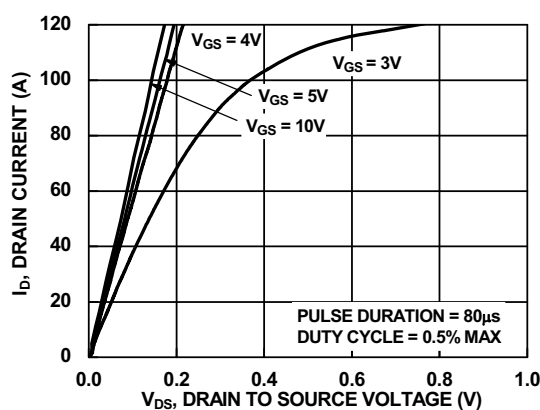


Figure 8. Saturation Characteristics

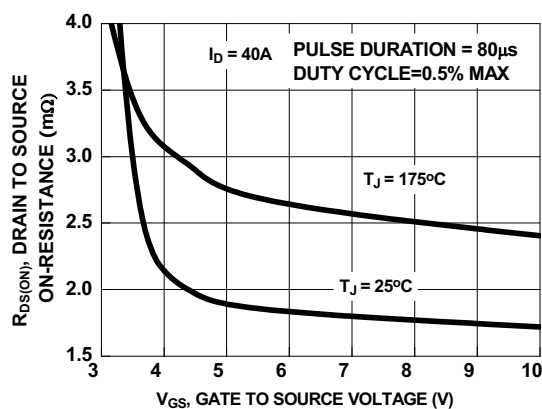


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

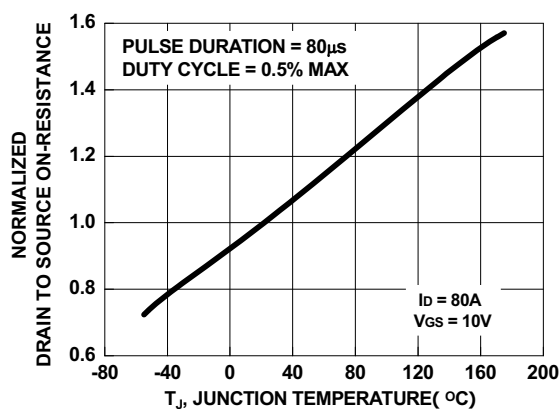


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

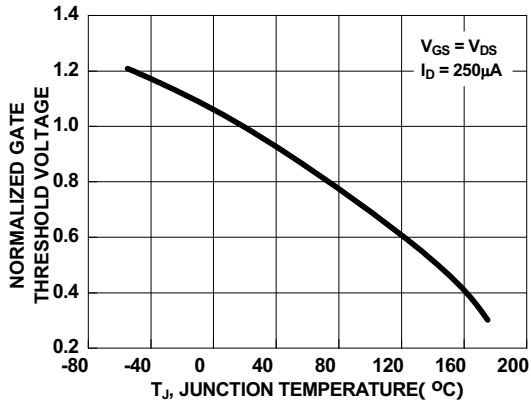


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

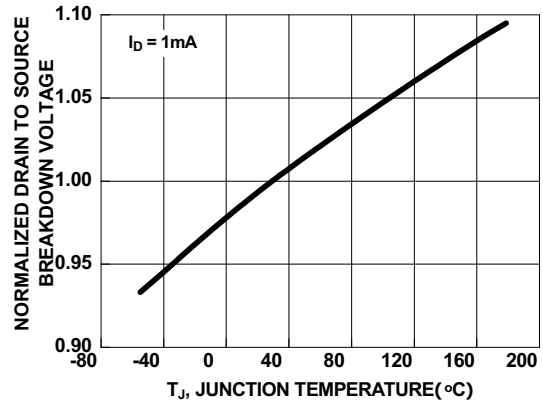


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

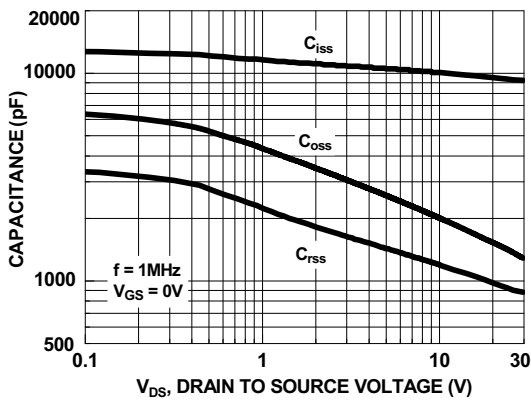


Figure 13. Capacitance vs Drain to Source Voltage

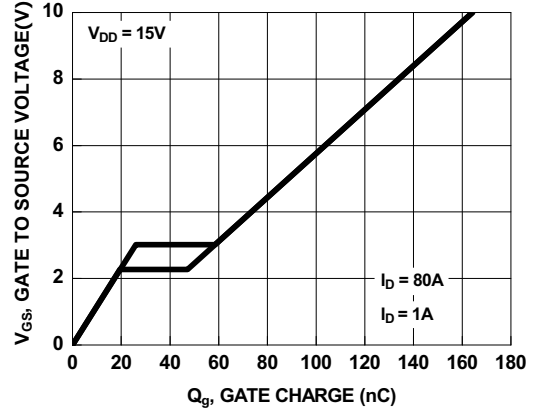


Figure 14. Gate Charge vs Gate to Source Voltage



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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