Ordering number : EN7778B

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA7567GVA — TV and VCR VIF/SIF IF Signal-Processing Circuit with NTSC SPLIT Support

Overview

The LA7567GVA is an NTSC SPLIT support VIF/SIF IF IC that adopts a semi-adjustment-free system. The VIF block adopts a technique that makes AFT adjustment unnecessary by adjusting the VCO, thus simplifying the adjustment steps in the manufacturing process. PLL detection is adopted in the FM detector. A 5V power-supply voltage is used to match that used in most multimedia systems. In addition, this IC also includes a buzz canceller to suppress Nyquist buzz and provide high audio quality.

Functions

- VIF block: VIF amplifier, PLL detector, BNC, RF AGC, EQ amplifier, AFT, IF AGC, buzz canceller.
- First SIF block: first SIF, first SIF detector, AGC.
- SIF block: multi-format SIF converter, limiter amplifier, PLL FM detector.

Features

- No AFT or SIF coils are required, making these circuits adjustment free.
- Built-in buzz canceller for excellent audio performance.
- V_{CC} = 5V, low power dissipation (250mW)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V_{13}, V_{17}		V_{CC}	V
Circuit current	I_6		–3	mA
	I_{10}		–10	mA
	I_{24}		–2	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C, when mounted on a PCB*.	600	mW
Operating temperature	T_{opr}		–20 to +70	°C
Storage temperature	T_{stg}		–55 to +150	°C

*: Printed circuit board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

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N2906 MS IM / 82905MS OT B8-7313 No.7778-1/20

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage range	V_{CC} op		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5.0V, fp = 45.75MHz

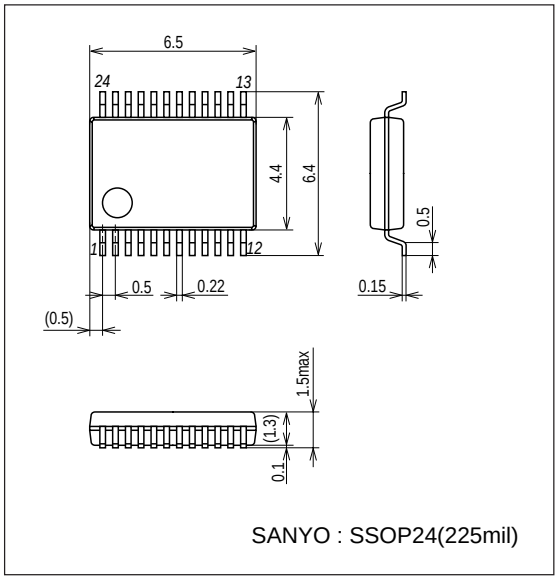
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VIF Block]						
Circuit current	I_5		40	47.5	54.5	mA
Maximum RF AGC voltage	V_{14H}		V_{CC} – 0.5	V_{CC}		V
Minimum RF AGC voltage	V_{14L}			0	0.5	V
Input sensi0tivity	V_I	S1 = OFF	27	33	39	dBµV
AGC range	G_R		53	58		dB
Maximum allowable input	V_I max		90	96		dBµV
No-signal video output voltage	V_6		2.1	2.4	2.7	V
Sync. signal tip voltage	V_6 tip		0.7	1.0	1.3	V
Video output level	V_O		0.95	1.1	1.25	Vp-p
Black noise threshold voltage	V_{BTH}		0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		1.2	1.5	1.8	V
Video signal-to-noise ratio	S/N		48	52		dB
C-S beat	I_{C-S}		38	43		dB
Frequency characteristics	f_C	6MHz	–3.0	–1.5		dB
Differential gain	D_G			3.0	6.5	%
Differential phase	D_P			3	5	deg
No-signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	V_{13H}		V_{CC} – 1	V_{CC} – 0.6	V_{CC}	V
Minimum AFT voltage	V_{13L}		0	0.18	0.5	V
AFT detection sensitivity	S_f		14	21	28	mV/kHz
VIF input resistance	R_i	45.75MHz		1.5		kΩ
VIF input capacitance	C_i	45.75MHz		3		pF
APC pull-in range (U)	f_{pu}		0.7	1.5		MHz
APC pull-in range (L)	f_{pl}			–2.0	–1.4	MHz
AFT tolerance frequency 1	d_{fa1}		–200	0	+200	kHz
VCO1 maximum variability range (U)	d_{fu}		1.0	1.5		MHz
VCO1 maximum variability range (L)	d_{fl}			–2.0	–1.4	MHz
VCO control sensitivity	B		1.2	3.2	5.0	kHz/mV
Sync. ratio	V_S		25.0	28.5	31.5	%
[First SIF Block]						
Conversion gain	V_G		27	33	39	dB
4.5 MHz output level	S_O		53	115	180	mVrms
First SIF maximum input	S_i max		8	16		mVrms
First SIF input resistance	R_i (SIF)	41.25MHz		2		kΩ
First SIF input capacitance	C_i (SIF)	41.25MHz		3		pF
[SIF Block]						
Limiting sensitivity	V_{Ii} (lim)		44	50	56	dBµV
FM detector output voltage	V_O (FM)	4.5MHz ±25kHz *	350	450	570	mVrms
AMR rejection ratio	AMR		50	60		dB
Total harmonic distortion	THD			0.3	0.8	%
SIF S/N	S/N (FM)		61	65		
[SIF Converter]						
Maximum output level	V_{max}		110	116	122	dBµV

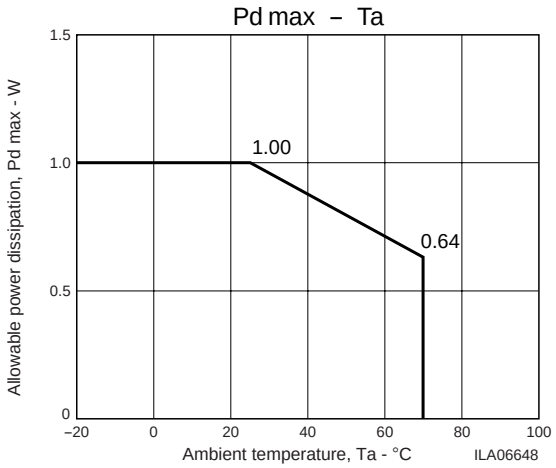
Note: *The FM detector output level can be reduced and the FM dynamic range can be increased by inserting a resistor and a capacitor in series between pin 23 and ground.

Package Dimensions

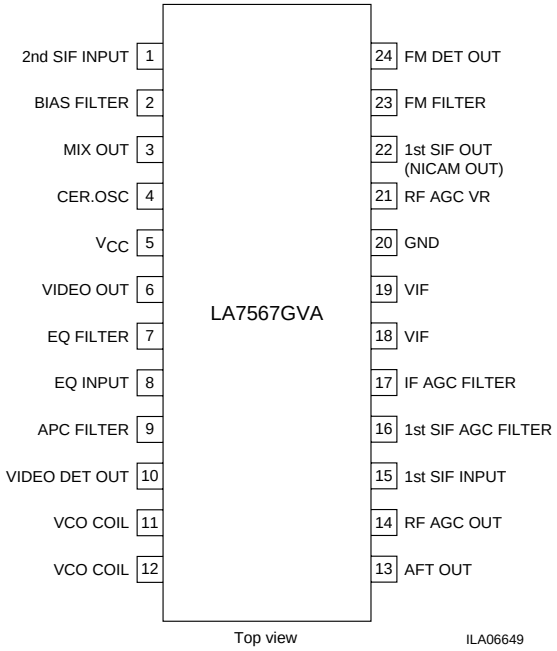
unit : mm (typ)

3287

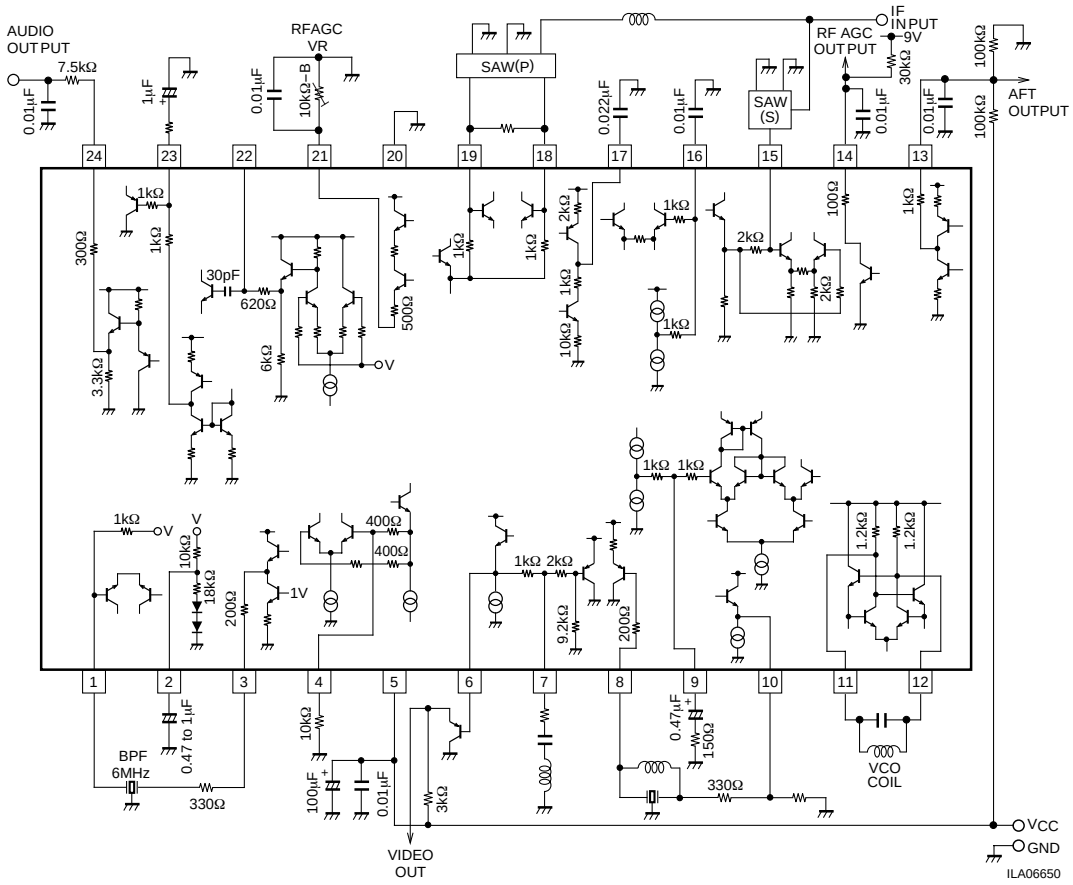




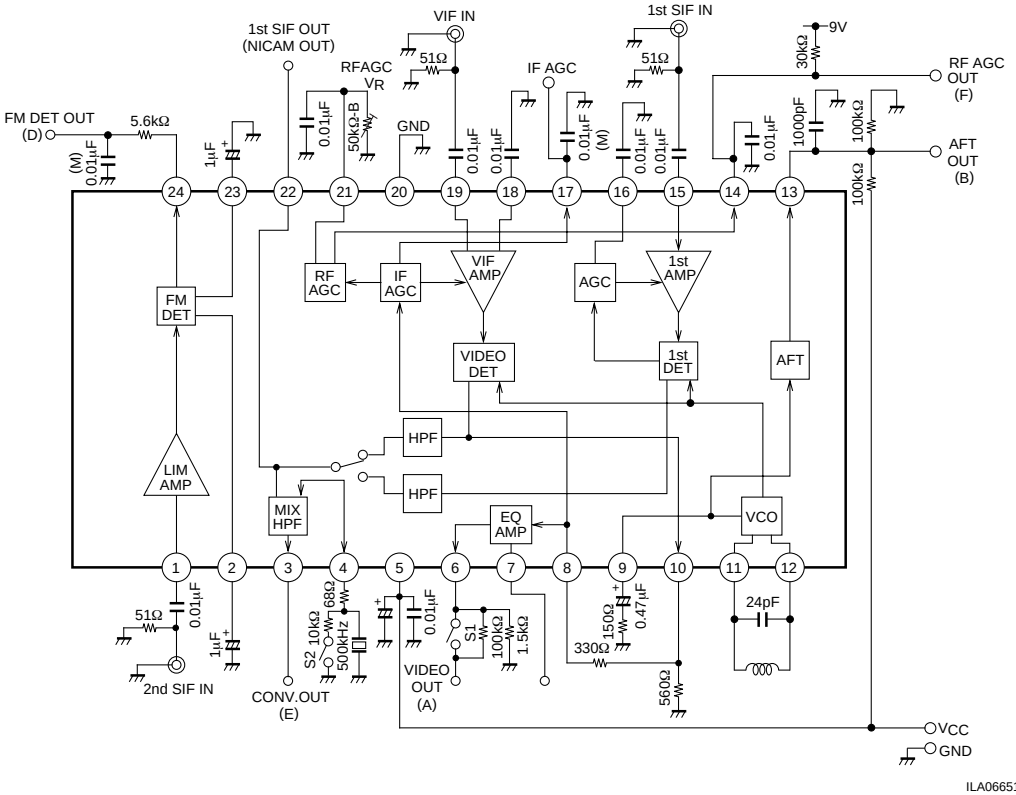
Pin Assignment



Internal Equivalent Circuit and External Components

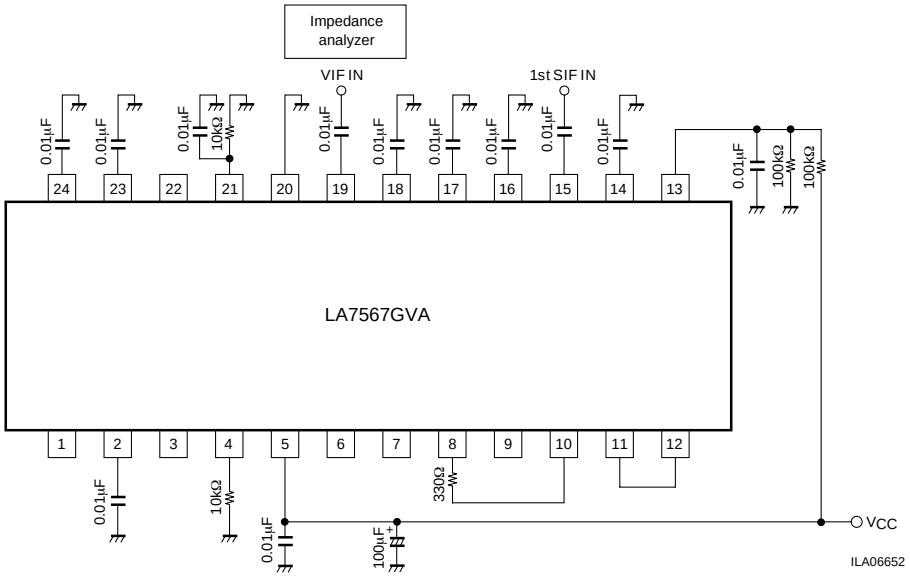


AC Characteristics Test Circuit



Test Circuit

Input Impedance Test Circuit (VIF and 1st SIF input impedance)



Test Conditions

V1. Circuit current . . . . . [I_5]

(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2.V3. Maximum RF AGC voltage, Minimum RF AGC voltage . . . . . [V_{14H}, V_{14L}]

(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistor value max.) and measure the maximum RF AGC voltage. (F)
(4) Adjust the RF AGC Vr (resistor value min.) and measure the minimum RF AGC voltage. (F)

V4. Input sensitivity. . . . . [V_i]

(1) Internal AGC
(2) fp = 45.75MHz 400Hz 40% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 400Hz detection output level at test point A becomes 0.35Vp-p.

V5. AGC range . . . . . [G_R]

(1) Apply the V_{CC} voltage to the external AGC IF AGC (pin 17).
(2) In the same manner as for the V4 (input sensitivity),measure the VIF input level at which the detection output level becomes 0.35Vp-p .....Vi1.
(3) $G_R = 20\log \frac{Vi1}{Vi}$ dB

V6. Maximum allowable input. . . . . [$V_{i\ max}$]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A is video output (Vo) ±1dB

V7. No-signal video output voltage . . . . . [V_6]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage of VIDEO output (A).

V8. Sync. signal tip voltage . . . . . [V_{6tip}]

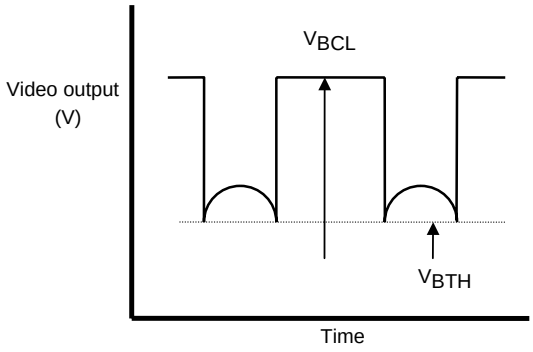
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage of VIDEO output (A).

V9. Video output level . . . . . [V_O]

(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM Vi = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. . . . . Vp-p

V10.V11. Black noise threshold level and clamp voltage . . . . . [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz 400Hz 40% AM 10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.

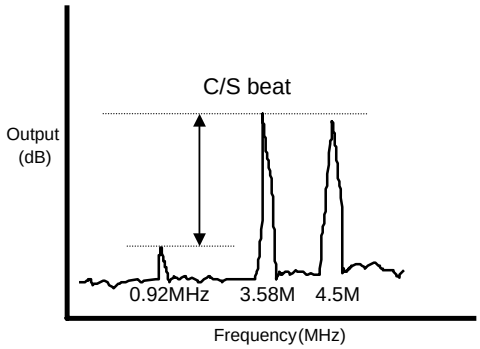


V12. Video S/N . . . . . [S/N]

(1) Internal AGC
(2) fp = 45.75MHz CW = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
.....Noise voltage (N)
(4) $S/N = 20 \log \frac{\text{Video portion (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20 \log \frac{1.12\text{Vp-p}}{\text{Noise voltage (Vrms)}}$ (dB)

V13. C/S beat . . . . . [I_{CS}]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz CW; 10mVrms
fc = 42.17MHz CW; 10mVrms-10dB
fs = 41.25MHz CW; 10mVrms-10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 0.72Vp-p.
(4) Measure the difference between the levels at 3.58MHz and 0.92MHz.



V14. Frequency characteristics . . . . . [f_C]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) SG1: 45.75MHz continuous wave 10mVrms
SG2: 45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p.....V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level.....V2
(5) Calculate as follows: $f_C = 20\log \frac{V2}{V1}$ (dB)

V15.V16. Differential gain, differential phase . . . [D_G, D_P]

(1) Internal AGC
(2) fp = 45.75MHz ALP 50% 87.5% modulation video signal Vi = 10mVrms
(3) Measure the DG and DP at test point A

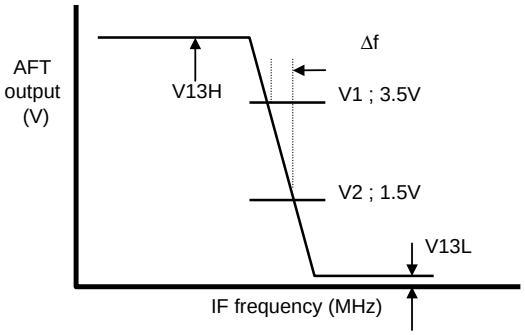
V17. No signal AFT voltage . . . . . [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18.V19.V20. Maximum minimum AFT output voltage, AFT detection sensitivity . . . . [V_{13H}, V_{13L}, S_f]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz Sweep = 10mVrms (VIF input)
(3) Maximum voltage: V_{13H}, minimum voltage: V_{13L}
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2.
.....Δf

$$Sf = \frac{2000(mV)}{\Delta f\,(kHz)}\ mV/kHz$$



V21.V22. VIF input resistance, Input capacitance . . . . . [R_i, C_i]

(1) Referring to the input impedance Test Circuit, measure Ri and Ci with an impedance analyzer.

V23.V24. APC pull-in range. . . . . [f_{pu}, f_{pl}]

(1) Internal AGC
(2) fp = 39MHz to 51MHz continuous wave; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note: GThe PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. .....(f1)
(5) Lower the SG signal frequency to bring the PLL to unlocked state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. .....(f2)
(7) Calculate as follows:
fpu = f1 - 45.75MHz
fpl = f2 - 45.75MHz

V25. AFT tolerance frequency . . . . . [ΔFa1]

(1) Internal AGC
(2) SG1: 43.75MHz to 47.75MHz variable continuous wave 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V17.)
(5) Apply 5V to the IFAGC (pin 17) and then pick up the VCO oscillation frequency from GND, etc. and measure the frequency (f2)
(6) Calculate as follows:
AFT tolerance frequency ΔFa1 = f2 - f1(kHz)

V26.V27. VCO Maximum variable range (U, L) . . [d_{fu}, d_{fl}]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so coil that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9). In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).
dfu = fu - 45.75MHz
dfl = fl - 45.75MHz

V28. VCO control sensitivity. . . . . [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) f1 is taken as the frequency when 3.0V applied to the APC pin (pin 9). In the same manner, f2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f2 - f1}{400} \left(\frac{kHz}{mV}\right)$$

V29. Synchronization ratio . . . . . [V_S]

(1) Internal AGC
(2) fp = 45.75MHz 87.5% 10 STEP B/W
Vi = 10mVrms
(3) Measure the output amplitude at the measuring point A . . . . . Vvideo
(4) Measure the pedestal voltage (DC) at the measuring point A . . . . . Vped
V_S = (Vped-V6tip)/Vvideo × 100 (%)

F1. First SIF conversion gain . . . . . [V_G]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 500μV (First SIF input) . . . V1
(3) Detection output level at test point C (Vrms) V2 (4.5MHz)
(4) $V_G = 20\log \frac{V2}{V1}$ dB

F2. 4.5MHz output level. . . . . [S_O]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (First SIF input) V1
(3) Detection output level at test point C (4.5MHz) . . . . . S_O(mVrms)

F3. First SIF maximum input . . . . . [S_i max]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; variable (First SIF input)
(3) Input level at which the detection output at test point C (4.5MHz) becomes S_O ±2dB.....S_i max

F4. F5. First SIF input resistance, input capacitance . . . . [R_i(SIF1), C_i(SIF1)]

(1) Using an input analyzer, measure Ri and Ci in the input impedance measuring circuit.

S1. SIF limiting sensitivity . . . . . [V_{Ii}(lim)]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz (SIF input)
(3) Set the SIF input level to 100mVrms and then measure the level at test point D.....V1
(4) Lower the SIF input level until V1-3dB occurs. Measure the input level at that moment.

S2. S4. FM detection output voltage, distortion factor . . . [V_O(FM, THD]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz ΔF = ±25kHz
(SIF input Vi=100mVrms)
(3) Assign the level at test point D to the FM detection output voltage and measure the distortion factor.

S3. AM rejection ratio . . . . . [AMR]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 4.5MHz fm = 400Hz AM = 30%
(SIF input Vi = 100mVrms)
(3) Measure the output level at test point D.....VAM
(4) $AMR = 20\log \frac{VO(DET)}{VAM}$ dB

S5. SIF S/N . . . . . [S/N]

(1) External AGC (V17=V_{CC})
(2) fs = 4.5MHz NO MOD Vi = 100mVrms
(3) Measure the output level at test point D.....Vn
(4) $S/N = 20\log \frac{VO(DET)}{Vn}$ dB

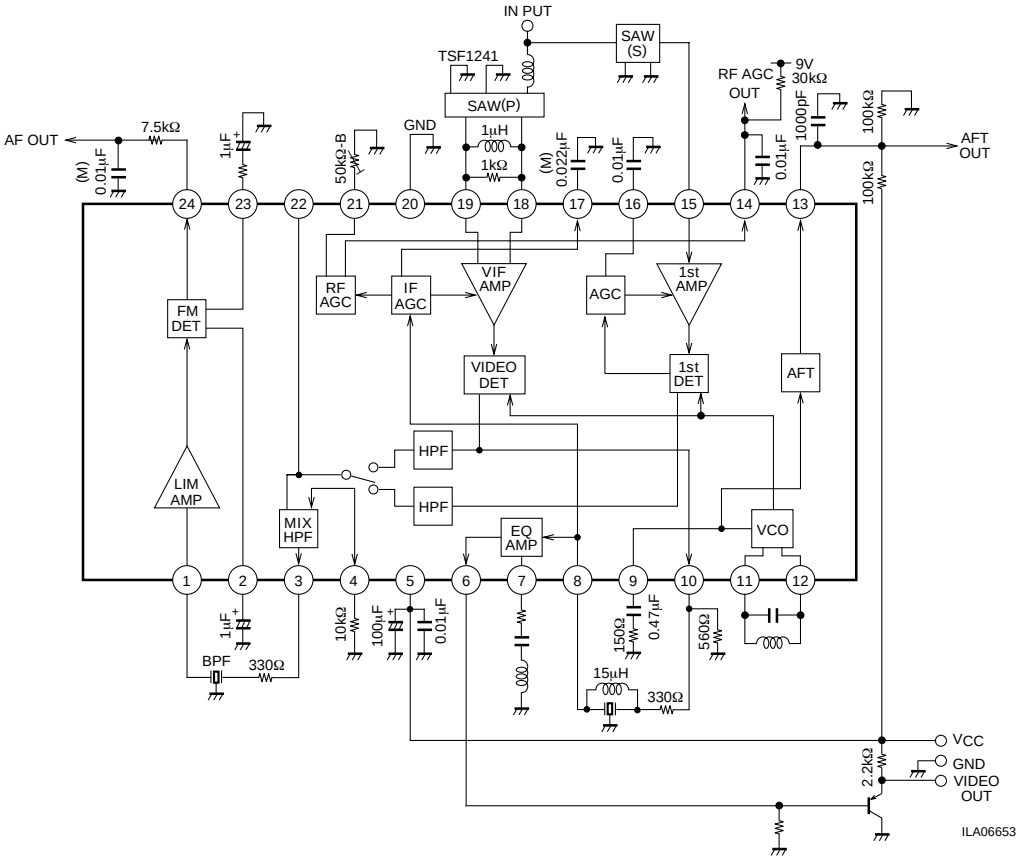
C2. SIF converter maximum output level . . . . . [V_{max}]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (First SIF input)
(3) Measure the 4.5MHz component at test point E (MIX output). .....Vmax(dBμV)

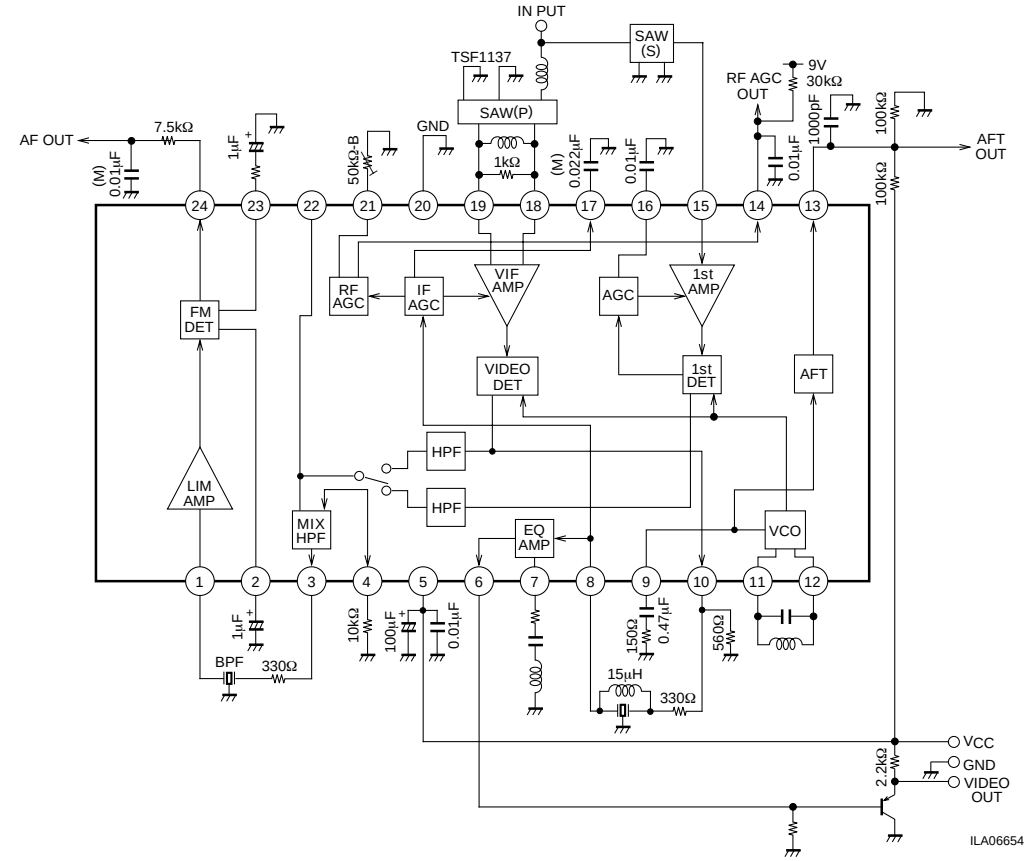
Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.75MHz.
Note 2) Unless otherwise specified, the SW1 must be ON.

Application Circuit Diagrams

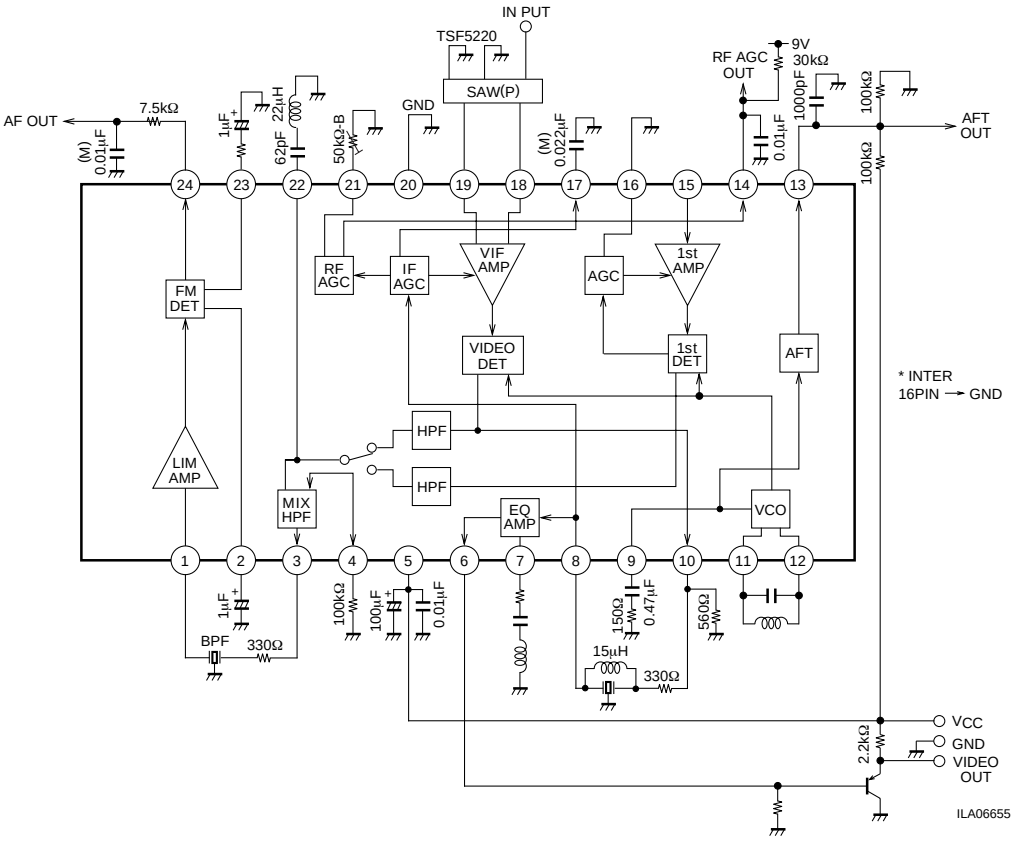
NT (US) SPLIT



JAPAN SPLIT



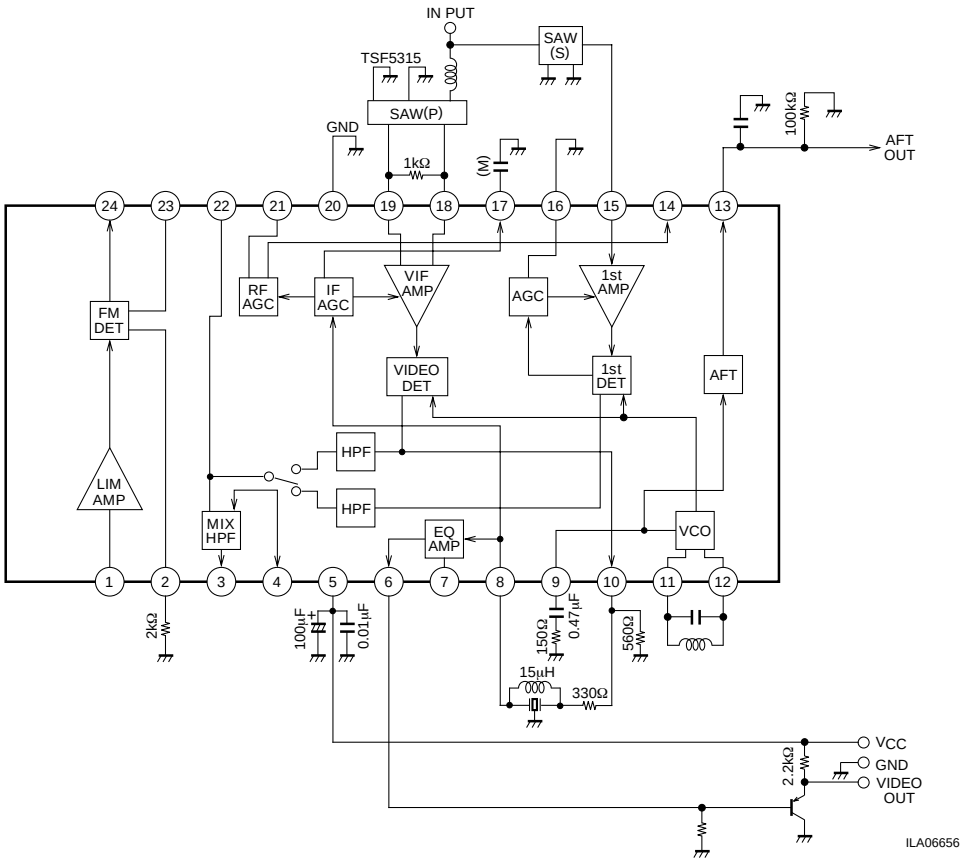
NT (US) INTER



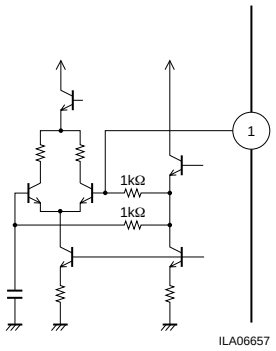
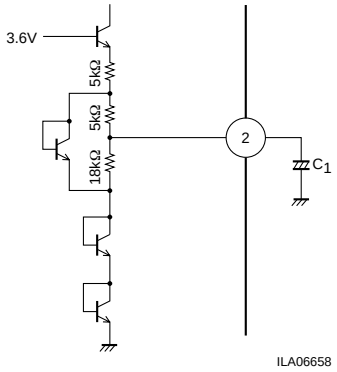
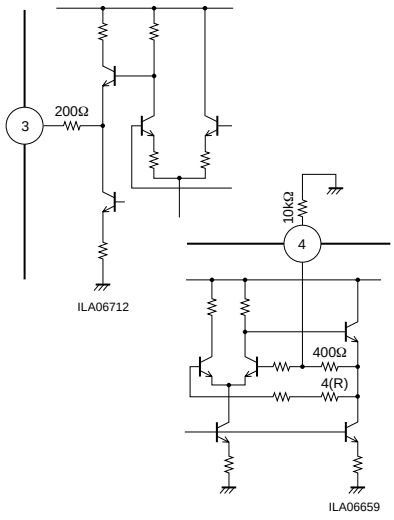
Sample Application Circuit

When the SIF, first SIF, AFT, and RF AGC circuits are not used:

- When the SIF circuit is not used:
  Leave pins 1, 23, and 24 open.
  Connect pin 2 to ground through a 2kΩ resistor.
- When the first SIF circuit is not used:
  Leave pins 3, 4, 15 and 22 open.
  Connect pin 16 to ground.
- When the AFT circuit is not used:
  Since there is no way to defeat the AFT circuit, connect a 100kΩ resistor and a 0.01µF capacitor in parallel between pin 13 and ground.
- When the RF AGC circuit is not used:
  Leave pins 14 and 21 open.
  Insert a 0.01µF capacitor between pin 21 and ground for oscillation prevention.



Pin Functions

Pin No.	Pin	Description	Equivalent circuit
1	SIF INPUT	• SIF input. The input impedance is about 1kΩ. Since buzzing and buzz beating can occur if interference enters this input pin, care must be taken when design the pattern layout for this pin. Note that the video and chrominance signals are especially likely to interfere with the audio signal. Also, the VIF carrier signal can also cause interference.	
2	FM power supply filter	• FM detector bias line filter input. Used to improve the FM detector signal-to-noise ratio. C1 should be at least 0.47µF, and 1µF is recommended. If the FM detector is not used, connect pin 2 to ground through a 2kΩ resistor. This stops the FM detector VCO.	
3 4	SIF converter	• Pin 3 is the SIF converter output. The signal is passed through a 6MHz bandpass filter and input to the SIF circuit.	
5	V_{CC}	• Use the shortest distance possible when decoupling V_{CC} and ground.	

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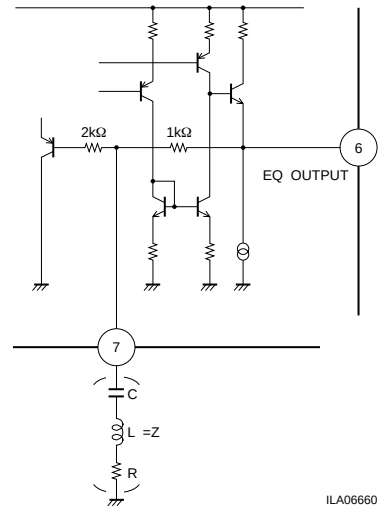
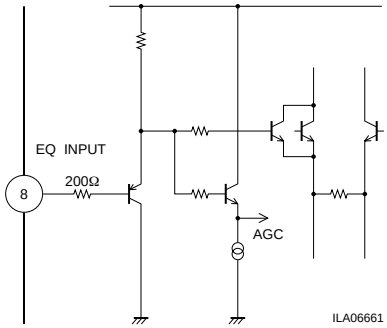
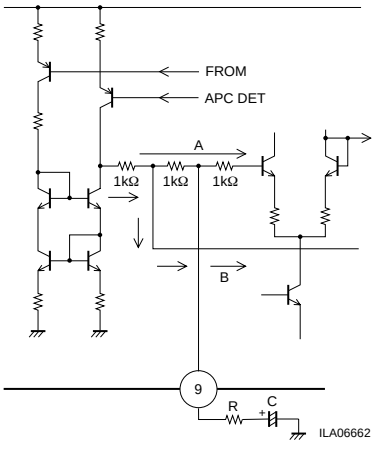
Pin No.	Pin	Description	Equivalent circuit
6 7 8	EQ amp	• Equalizer circuit. This circuit is used to correct the video signal frequency characteristics. Pin 8 is the EQ amplifier input. This amplifier amplifies a 1.5Vp-p video signal to 2Vp-p. • Notes on equalizer amplifier design The equalizer amplifier is designed as a voltage follower amplifier with a gain of about 0 dB. When used for frequency characteristics correction, a capacitor, inductor, and resistor must be connected in series between pin 7 and ground. • Approach used in the equalizer amplifier If vi is the input signal and vo is the output signal, then: $\frac{R1}{2}+1\ (vi + vin) = Vo \times G$ Where G is the voltage-follower amplifier gain. Assume: vin: Imaginary short G: About 0dB vin ≈ 0. Then: $AV = \frac{voG}{vi} = \frac{R1}{Z} + 1$ • R1 is the IC internal resistance, and is 1kΩ. In the application design, simply select Z to correspond to the desired characteristics. However, since the EQ amplifier gain will be maximum at the resonant point defined by Z, care is required to assure that distortion does not occur.	 
9	APC FILTER	• PLL detector APC filter connection. The APC time constant is switched internally in the IC. When locked, the VCO is controlled by loop A and the loop gain is reduced. When unlocked and during weak field reception, the VCO is controlled by loop B and the loop gain is increased. For this APC filter we recommend: R = 150 to 390Ω C = 0.47μF	

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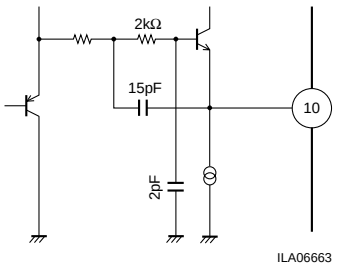
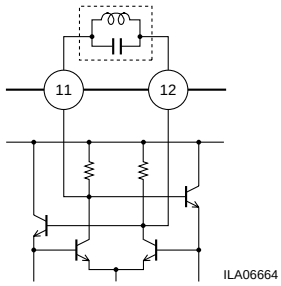
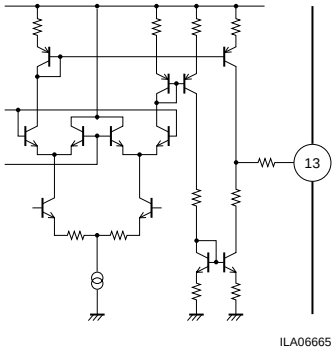
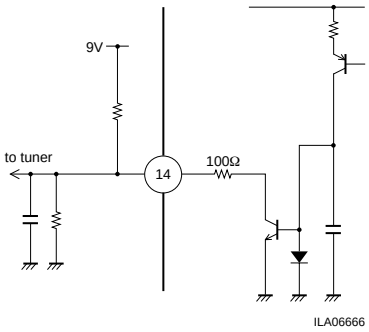
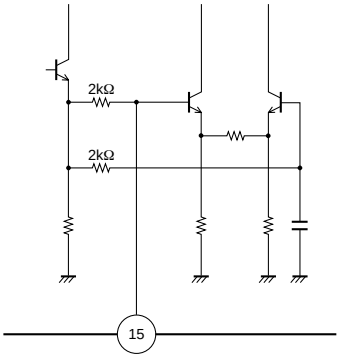
Pin No.	Pin	Description	Equivalent circuit
10	Composite video output	• Output for the video signal that includes the SIF carrier. A resistor must be inserted between pin 10 and ground to acquire adequate drive capability. R ≥ 430Ω	
11 12	VCO tank	• VCO tank circuit used for video signal detection. See the coil specifications provided separately for details on the tank circuit. This VCO is a vector synthesis VCO.	
13	AFT OUTPUT	• AFT output. The AFT center voltage is generated by an external bleeder resistor. The AFT gain is increased by increasing the resistance of this external bleeder resistor. However, this resistor must not exceed 390kΩ. This circuit includes a control function that controls the AFT voltage to naturally approach the center voltage during weak field reception.	
14	RF AGC OUTPUT	• RF AGC output. This output controls the tuner RF AGC. A protective 100Ω resistor is inserted in series with the open collector output. Determine the external bleeder resistor value in accordance with the specifications of the tuner.	
15	1st SIF INPUT	• First SIF input. A DC cut capacitor must be used in the input circuit. • If a SAW filter is used: The first SIF sensitivity can be increased by inserting an inductor between the SAW filter and the IC to neutralize the SAW filter output capacitance and the IC input capacitance. • When used in an intercarrier system: This pin (pin 15) may be left open.	

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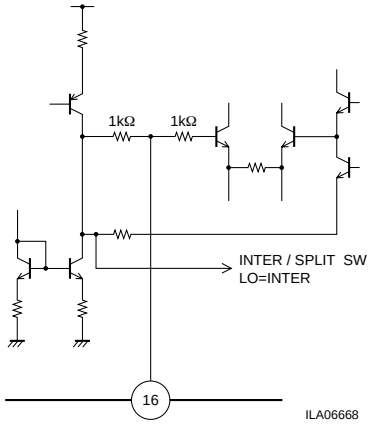
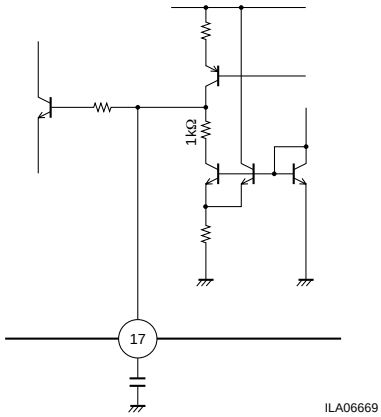
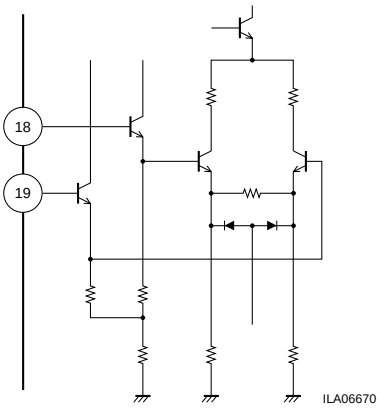
Pin No.	Pin	Description	Equivalent circuit
16	1st SIF AGC FILTER	• First SIF AGC filter connection. This IC adopts an average value AGC technique. The first SIF conversion gain is about 30dB, and the AGC range is over 50dB. A 0.01µF capacitor is normally used in filter connected to this pin. • When used in an intercarrier system: Connect this pin (pin 16) to ground. The IC internal switch will operate to connect the intercarrier output to the SIF converter input.	
17	IF AGC FILTER	• IF AGC filter connection The signal peak-detected by the built-in AGC detector is converted to the AGC voltage at pin 17. Additionally, a second AGC filter (a lag-lead filter) used to create the dual time constants is provided internally in the IC. Use a 0.022µF capacitor as the external capacitor, and adjust the value according to the sag, AGC speed, and other characteristics.	
18 19	VIF input	• VIF amplifier input. The input circuit is a balanced circuit, and the input circuit constants are: R ≈ 1.5kΩ C ≈ 3pF	
20	GND		

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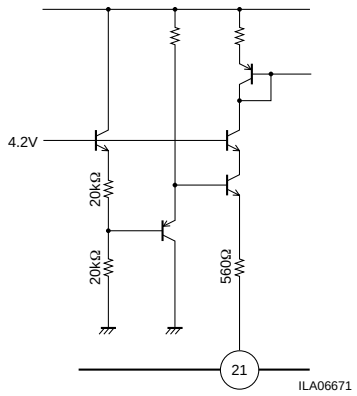
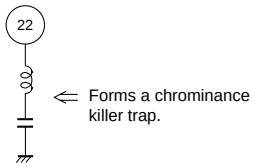
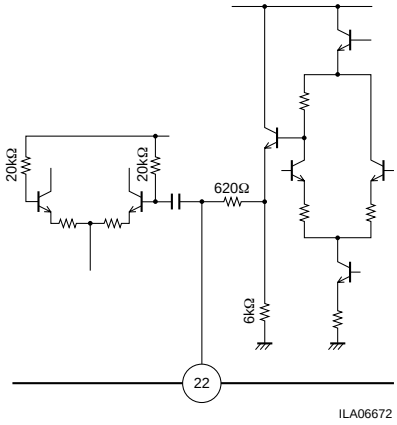
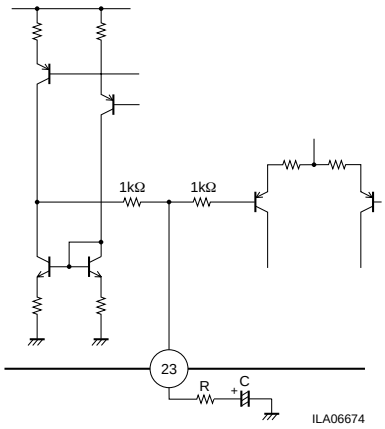
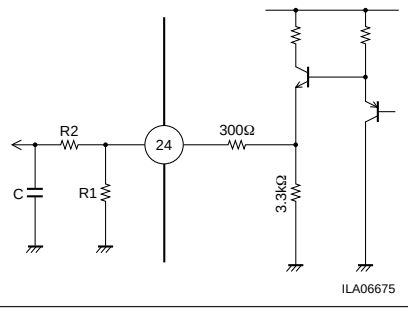
Pin No.	Pin	Description	Equivalent circuit
21	RF AGC VR	• RF AGC VR connection. This pin sets the tuner RF AGC operating point. Also, the FM output and the video output can both be muted at the same time by connecting this pin to ground.	
22	NICAM output	• First SIF output. Internally, this is an emitter-follower output with a 600Ω resistor attached. When used in an intercarrier system, the buzz characteristics can be improved by forming a chrominance carrier trap with this pin. 	
23	FM filter	• Connection for a filter used to hold the FM detector output DC voltage fixed. Normally, a 1µF electrolytic capacitor should be used. The capacitance should be increased if the low band (around 50Hz) frequency characteristics need to be improved. • The FM detector output level can be reduced and the FM dynamic range can be increased by inserting a resistor and a capacitor in series between pin 23 and ground.	
24	FM Detector output	• Audio FM detector output. A 300Ω resister is inserted in series with an emitter-follower output. • For applications that support stereo: Applications that input this signal to a stereo decoder may find that the input impedance is reduced, the left and right signals are distorted, and that the stereo characteristics are degraded. If this problem occurs, add a resistor between pin 24 and ground. R1 ≥ 5.1kΩ • For applications that support mono: Create an external deemphasis circuit. t = C × R2	

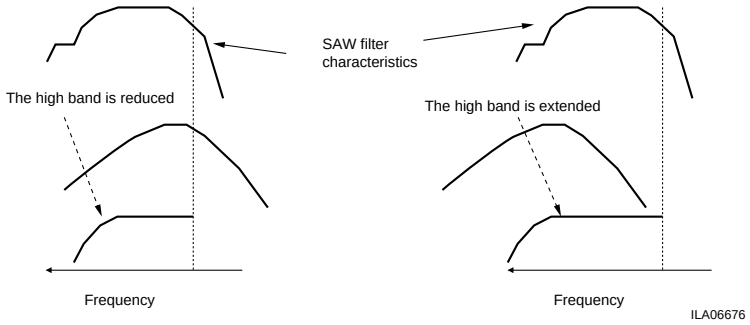
Notes on Sanyo SAW Filters

There are two types of SAW filters, which differ in the piezoelectric substrate material, as follows:

- Lithium tantalate (LiTaO3) SAW filter
  TSF11☐☐ ... Japan
  TSF12☐☐ ... US
  Although lithium tantalate SAW filters have the low temperature coefficient of –18ppm/°C, they suffer from a large insertion loss. However, it is possible, at the cost of increasing the number of external components required, to minimize this insertion loss by using a matching circuit consisting of coils and other components at the SAW filter output. At the same time as minimizing insertion loss, this technique also allows the frequency characteristics, level, and other aspects to be varied, and thus provides increased circuit design flexibility. Also, since the SAW filter reflected wave level is minimal, the circuit can be designed with a small in-band ripple level.
- Lithium niobate (LiNbO3) SAW filter
  TSF52☐☐ ... US
  TSF53☐☐ ... PAL
  Although lithium niobate SAW filters have the high temperature coefficient of –72ppm/°C, they feature an insertion loss about 10dB lower than that of lithium tantalate SAW filters. Accordingly, there is no need for a matching circuit at the SAW filter output. Although the in-band ripple is somewhat larger than with lithium tantalate SAW filters, since they have a low impedance and a small field slew, they are relatively immune to influences from peripheral circuit components and the geometry of the printed circuit board pattern. This allows stable out-of-band trap characteristics to be acquired. Due to the above considerations, lithium tantalate SAW filters are used in applications for the US and Japan that have a high IF frequency, and lithium niobate SAW filters are used in PAL and US applications that have a low IF frequency.

Notes on SAW Filter Matching

In SAW filter input circuit matching, rather than matching the IF frequency, flatter video band characteristics can be acquired by designing the tuning point to be in the vicinity of the audio carrier rather than near the chrominance carrier. The situation shown in figure on the right makes it easier to acquire flat band characteristics than that in figure on the left.



With the Tuning Set to the IF frequency **With the Tuning Set to the Vicinity of S and C**

Coil Specifications

	JAPAN f = 58.75MHz	US f = 45.75MHz	PAL f = 38.9MHz
VCO coil	S t=5t 0.12ø C=24pF ILA06677 Test production no. V291XCS-3220Z Toko Co., Ltd.	S t=6t 0.12ø C=24pF ILA06678 Test production no. 291XCS-3188Z Toko Co., Ltd.	S t=7t 0.12ø C=24pF ILA06679 Test production no. 292GCS-7538Z Toko Co., Ltd.
SAW filter (SPLIT)	Picture TSF1137U Sound	Picture TSF1241 Sound	Picture TSF5315 Sound
SAW filter (INTER)		TSF5220 TSF5221	TSF5321 TSF5344

Toko Co., Ltd. 2-1-17 Higashi-yukigaya, Ohta-ku, Tokyo, Japan
TEL: +81-3-3727-1167

Notes on VCO Tank Circuits

- Built-in capacitor VCO tank circuits
  When the power is turned on, the heat generated by the IC is transmitted through the printed circuit board to the VCO tank circuit. At this point, the VCO coil frame functions as a heat sink and the IC heat is dissipated. As a result, it becomes more difficult to transmit heat to the VCO tank circuit's built-in capacitor, and the influence of drift at power on is reduced. Therefore, it suffices to design the circuit so that the coil and capacitor thermal characteristics cancel. Ideally, it is better to use a coil with a core material that has low temperature coefficient characteristics.

- External capacitor VCO tank circuits
  When an external capacitor is used, heat generated by the IC is transmitted through the printed circuit board directly to the VCO tank circuit external capacitor. While this capacitor is heated relatively early after the power is turned on, the coil is not so influenced as much by this heat, and as a result the power-on drift is increased. Accordingly, a coil whose core material has low temperature coefficient characteristics must be used. It is also desirable to use a capacitor with similarly low temperature coefficient characteristics.

  Note: Applications that use an external capacitor here must use a chip capacitor. If an ordinary capacitor is used, problems such as the oscillator frequency changing with the capacitor orientation may occur.