International
IOR Rectifier

REFERENCE DESIGN IRDCiP1001-B

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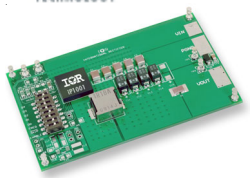
IRDCiP1001-B, 200kHz to 300kHz, 20A, $5V_{IN}$ to $12V_{IN}$ Single Phase Synchronous Buck Converter using iP1001

Overview

In this document, Table 1 and Figure 1 are provided to enable engineers to easily evaluate the iP1001 in a single phase configuration that is capable of providing up to 20A in a lab environment without airflow. Figures 3, 4, 5 and 6 and the complete bill of materials in Table 2 are provided as a reference design to enable engineers to very quickly and easily design a single phase converter. In order to optimize this design to your specific requirements, refer to the iP1001 data sheet for guidelines on external component selection and user adjustable limits and specifications for the iP1001. Custom designs may require layout modifications.

iPOWIR™ TECHNOLOGY



IRDCiP1001-B Demoboard Operatng Conditions		
	Min	Max
V_{IN}	4.5V	12V
V_{OUT}	0.925V	3.3V
I_{OUT}	See Fig.1	

Demoboard Quick Start Guide

Initial Settings:

- The output is set to 1.3V, but can be adjusted from 0.925V to 2.0V by setting SW1 according to the VID codes provided in Table 1. The output voltage can be adjusted to allow up to $3.3V_{OUT}$ by adding R3 & R4 with the DAC set to $2V_{OUT}$. Refer to equation 1 for R3 & R4 values. R4 should be removed for output voltages below 2V, and R3 should be set to zero ohms (see Table 2).
- The switching frequency is centered around 300kHz with the Freq pin floating.
- The input voltage range can be extended below $5V_{IN}$ by populating the mini-boost circuit on the demo board. Refer to IRDCiP1001-A reference design documentation for direction on changing the configuration of the demo board.

Procedure for Connecting and Powering Up Demoboard:

1. Apply input voltage (5V - 12V) across V_{IN} and PGND. The input voltage (V_{IN}) pin and logic power pin (V_{DD}) are provided as separate inputs. For $5V_{IN}$ operation only, the V_{IN} and V_{DD} pins can be connected together. For logic power (V_{DD}), connect 5V power source across +5V (TP1) and PGND (TP2).
2. Apply load across VOUT pad and PGND pad.
3. The ENABLE pin is controlled via switch 8 on SW1. This pin is supplied in low state. Once pulled high the output is enabled.
4. Adjust load accordingly.

IRDCiP1001-B Recommended Operating Conditions

(refer to the iP1001 datasheet for maximum operating conditions)

Input voltage: 4.5 - 12V (V_{DD} = 4.5V to 5.5V)
Output voltage: DAC selectable between 0.925V - 2.0V (with extended operating range to 3.3V with R3 & R4)
Output current: Up to 20A depending on duty factor (refer to load line curve in Fig. 1).
Switching Freq: 200kHz or 300kHz selectable.

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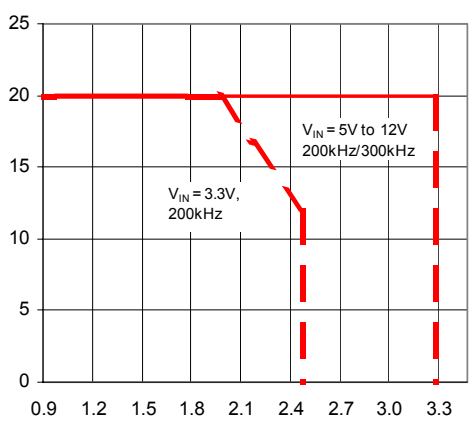

Fig. 1 - Load line curve

D4	D3	D2	D1	D0	Output Voltage (V)	D4	D3	D2	D1	D0	Output Voltage (V)
0	0	0	0	0	2.00	1	0	0	0	0	1.275
0	0	0	0	1	1.95	1	0	0	0	1	1.250
0	0	0	1	0	1.90	1	0	0	1	0	1.225
0	0	0	1	1	1.85	1	0	0	1	1	1.200
0	0	1	0	0	1.80	1	0	1	0	0	1.175
0	0	1	0	1	1.75	1	0	1	0	1	1.150
0	0	1	1	0	1.70	1	0	1	1	0	1.125
0	0	1	1	1	1.65	1	0	1	1	1	1.100
0	1	0	0	0	1.60	1	1	0	0	0	1.075
0	1	0	0	1	1.55	1	1	0	0	1	1.050
0	1	0	1	0	1.50	1	1	0	1	0	1.025
0	1	0	1	1	1.45	1	1	0	1	1	1.000
0	1	1	0	0	1.40	1	1	1	0	0	0.975
0	1	1	0	1	1.35	1	1	1	0	1	0.950
0	1	1	1	0	1.30	1	1	1	1	0	0.925
0	1	1	1	1	Shutdown*	1	1	1	1	1	Shutdown*

* Shutdown : Upon receipt of the shutdown code (per VID code table above), both FETs are turned OFF and the output is discharged as it enters UVP fault mode.

Table 1 - PWM IC Voltage Identification Codes

For output voltages above the DAC maximum setting of 2V, refer to Equation 1 below to calculate the required resistor values for R3 & R4 (needed in order to achieve the extended output voltage range).

Equation 1 : $Vout = V_F \times (1 + R3/R4)$

where V_F is equal to the DAC setting and R4 is recommended to be ~1kΩ

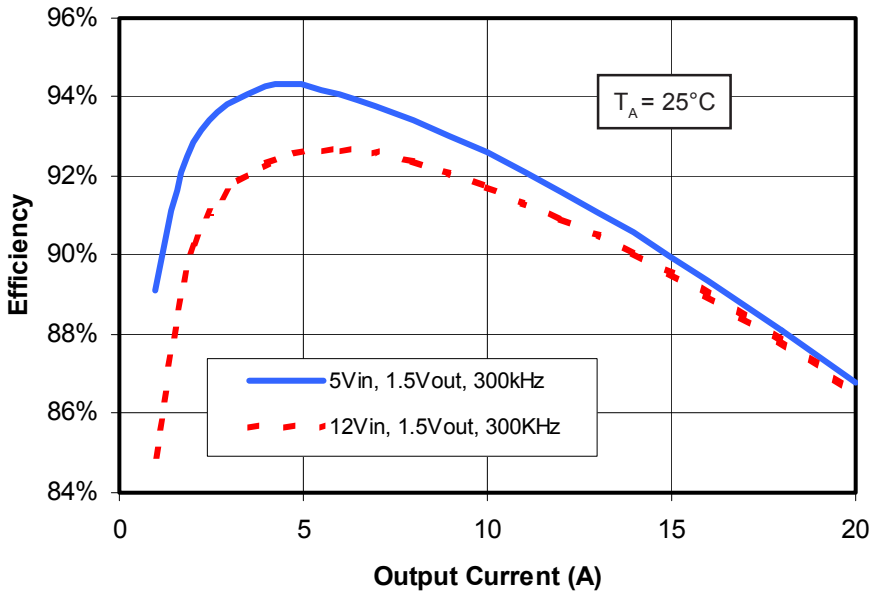

Fig. 2 - Typical Efficiency vs. Current

Refer to the following application notes for detailed guidelines and suggestions when implementing iP0WIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

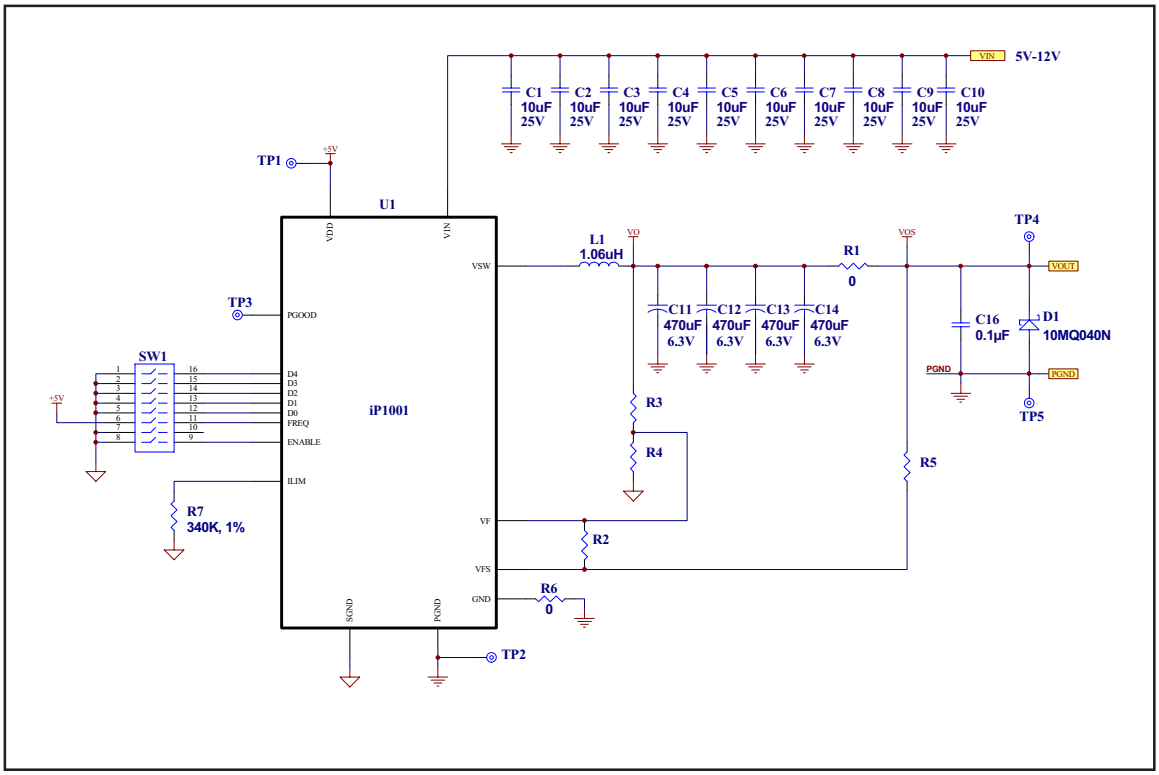

Fig. 3 - Reference Design Schematic

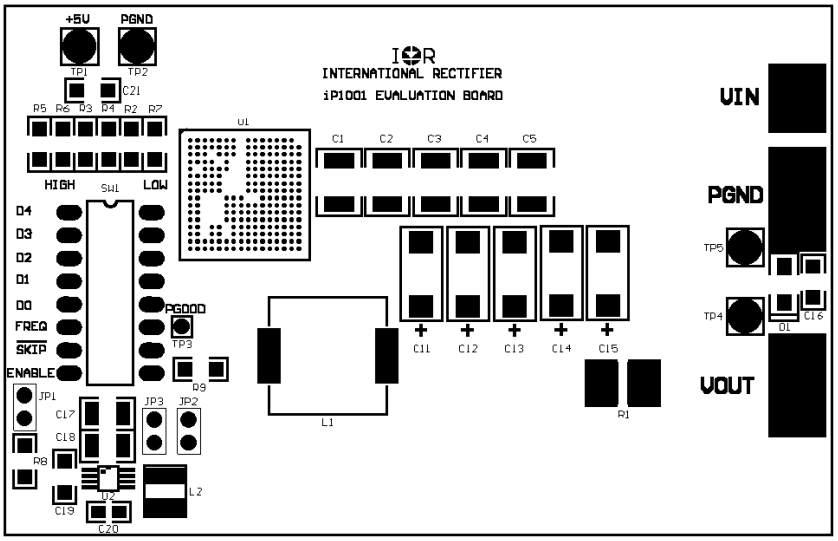

Fig. 4 - Component Placement Top Layer

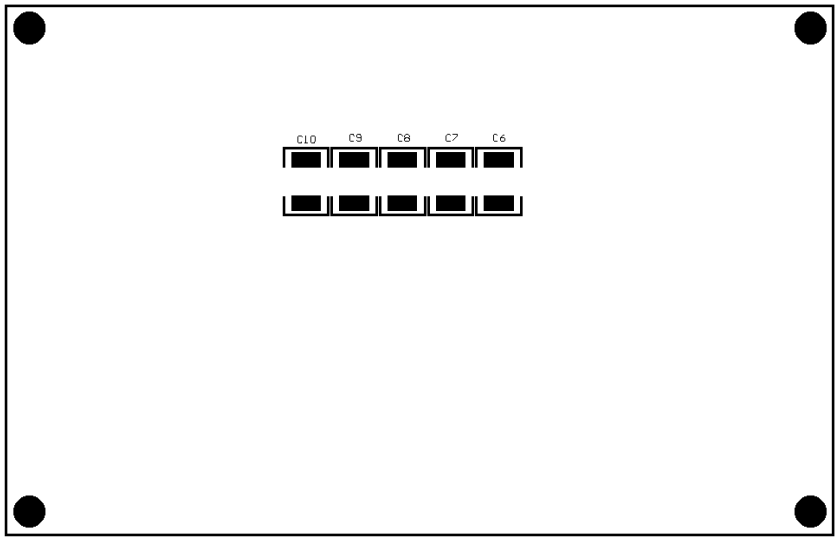

Fig. 5 - Component Placement Bottom Layer

IRDCiP1001-B (For operation $5V_{IN}$ to $12V_{IN}$)

Designator	Value	Part Type	Footprint	Mfr.	Mfr. P/N
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10	10.0uF	Capacitor, 25V, 10%, X5R	1812	MuRata	GRM43-2X5R106K25A
C11 C12 C13 C14	470uF	Capacitor, 6.3V, 20%, Tantalum	7343	Sanyo	6TPB470M
C16	0.100uF	Capacitor, 50V, 10%, X7R	1206	Novacap	1206B104K500N
C15, C17, C18, C19, C20, C21	-	Not Installed	-	-	-
D1	40V	Schottky Diode, 40V, 2.1A	D-64	International Rectifier	10MQ040N
JP1, JP2, JP3	-	Not Installed	-	-	-
JP1-1, JP2-1, JP3-1	-	Not Installed	-	-	-
L1	1.06uH	Inductor, 16A, 20%, Ferrite	SMT	Panasonic	ETQP6F1R1BFA
L2	-	Not Installed	-	-	-
R1	0Ω	Resistor, 0Ω Jumper	2716	Isotek Corp	SMT-R000
R2	-	For <2Vout, Not installed For >2Vout, Resistor, 0Ω Jumper	SMT	-	-
R3	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout see formula for value	SMT	-	-
R4	-	For <2Vout, Not installed For >2Vout recommend 1kΩ see formula for detail	SMT	-	-
R5	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout, Not installed	1206	Panasonic	ERJ-8GEY0R00
R6	0Ω	Resistor, 0Ω Jumper	1206	-	-
R7	340kΩ	Resistor, 340kΩ, 1% 340kΩ sets for 20A limit. See ILIM formula for other values	1206	ROHM	MCR18EZHF3403
R8, R9	-	Not Installed	-	-	-
SW1	-	8-position DIP switch	SMT	C&K Components	SD08H0SK
TP1 TP2 TP4 TP5	-	Test Point	-	Keystone	1502-2
TP3	-	Not Installed	-	-	-
U1	-	Power Block	SSBGA 14mmx14mm	International Rectifier	iP1001
U2	-	Not Installed	-	-	-

Table 2 - Reference Design Bill of Materials

Adjusting the Current Limit

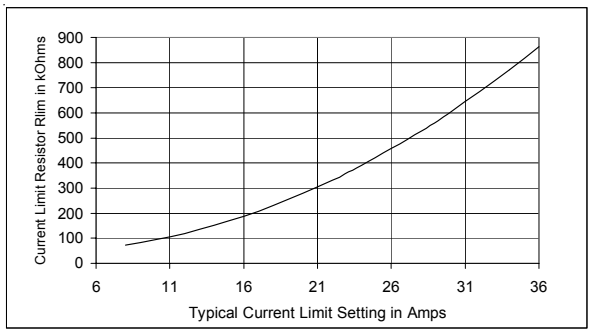

Fig. 6 Current Limit Adjustment using R_{LIM}

Use of this design for any application should be fully verified by the customer. International Rectifier cannot guarantee suitability for your applications, and is not liable for any result of usage for such applications including, without limitation, personal or property damage or violation of third party intellectual property rights.