



element14

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[IRLI630GPBF.](#)

EN

This Datasheet is presented by
the manufacturer

DE

Dieses Datenblatt wird vom
Hersteller bereitgestellt

FR

Cette fiche technique est
présentée par le fabricant

IRLI630GPbF

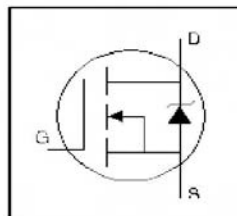
- Isolated Package
- High Voltage Isolation = 2.5KV RMS
- Sink to Lead Creepage Dist. 4.8mm
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4V$ & $5V$
- Fast Switching
- Ease of paralleling

- Lead-Free

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

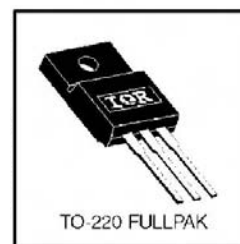
The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



$$V_{DSS} = 200V$$

$$R_{DS(on)} = 0.40\Omega$$

$$I_D = 6.2A$$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 5.0V	6.2	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 5.0V	3.9	
I_{DM}	Pulsed Drain Current ①	25	
P_D @ $T_C = 25^\circ C$	Power Dissipation	35	W
	Linear Derating Factor	0.28	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	125	mJ
I_{AR}	Avalanche Current ①	6.2	A
E_{AR}	Repetitive Avalanche Energy ①	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.40	Ω	$V_{GS} = 5.0V$, $I_D = 3.7A$ ②
		—	—	0.50		$V_{GS} = 4.0V$, $I_D = 3.1A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	4.8	—	—	S	$V_{DS} = 50V$, $I_D = 5.4A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	40	nC	$I_D = 9.0A$
Q_{gs}	Gate-to-Source Charge	—	—	5.5		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	24		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	57	—		$I_D = 9.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	33	—		$R_D = 11\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package and center of die contact
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	220	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	70	—		$f = 1.0MHz$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	25		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}$, $I_S = 6.2A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	230	350	ns	$T_J = 25^\circ\text{C}$, $I_F = 9.0A$
Q_{rr}	Reverse Recovery Charge	—	1.7	2.6	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $I_{SD} \leq 9.0A$, $di/dt \leq 120A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

③ $t = 60s$, $f = 60Hz$

④ $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 2.4mH$, $R_G = 25\Omega$, $I_{AS} = 6.2A$. (See Figure 12)

⑤ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

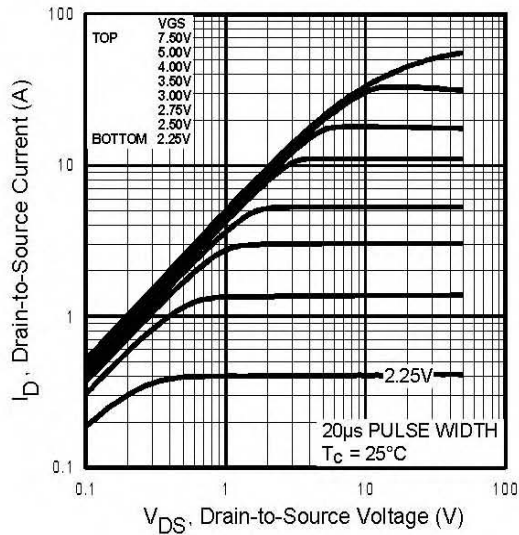


Fig 1. Typical Output Characteristics,
 $T_c = 25^\circ\text{C}$

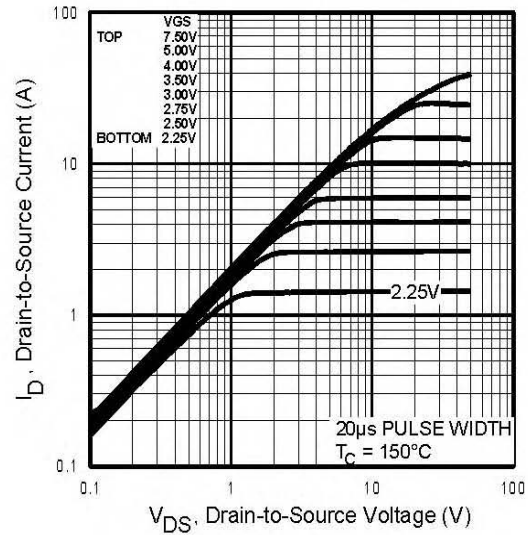


Fig 2. Typical Output Characteristics,
 $T_c = 150^\circ\text{C}$

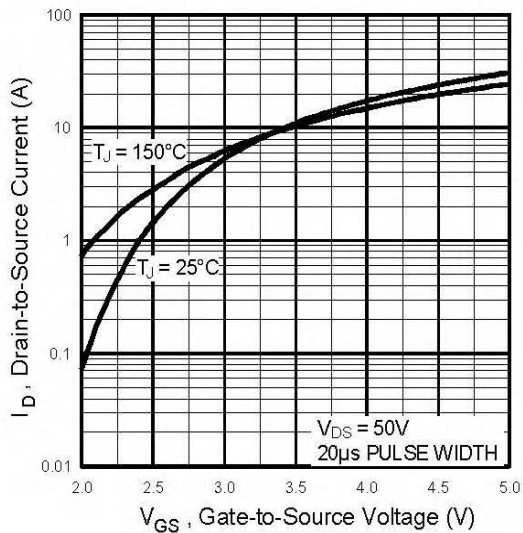


Fig 3. Typical Transfer Characteristics

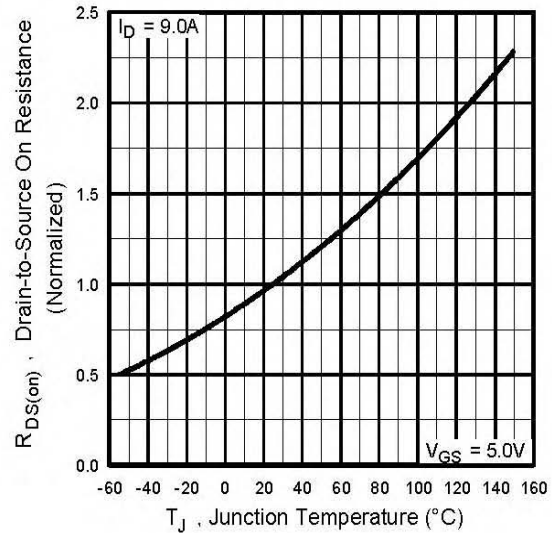


Fig 4. Normalized On-Resistance
Vs. Temperature

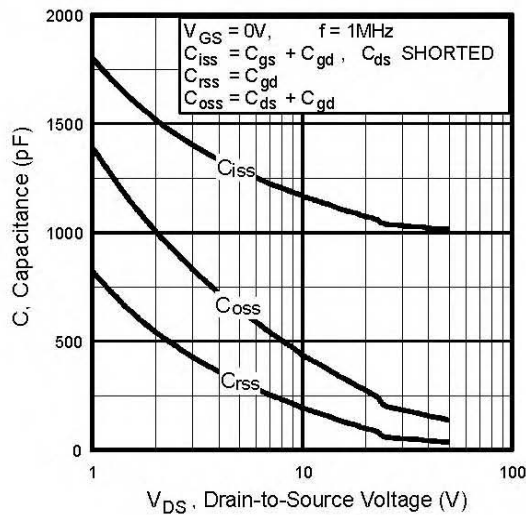


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

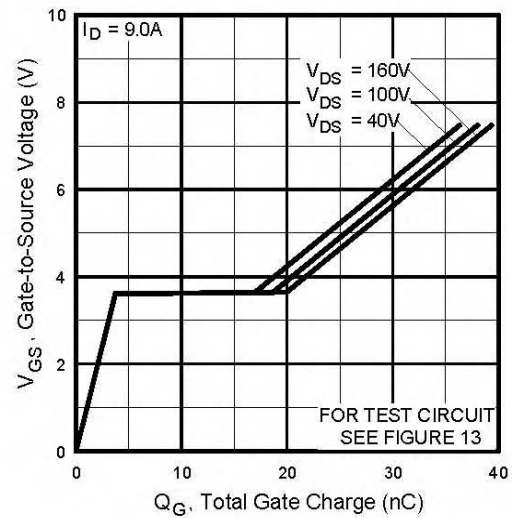


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

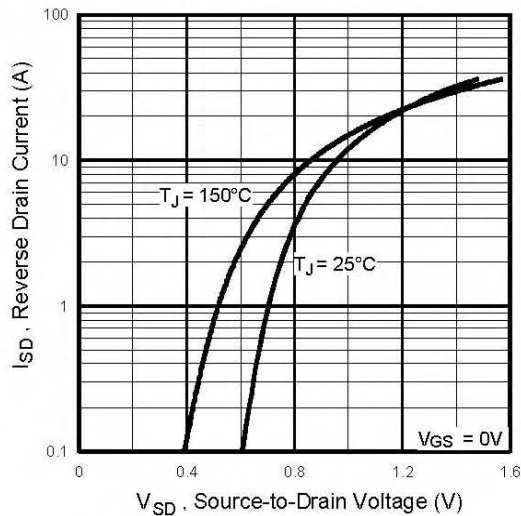


Fig 7. Typical Source-Drain Diode Forward Voltage

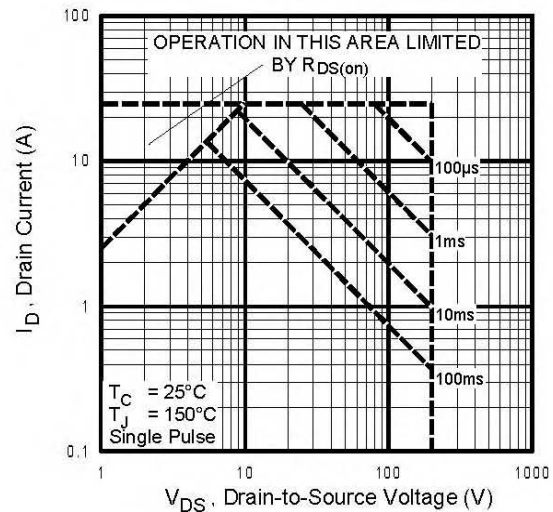


Fig 8. Maximum Safe Operating Area

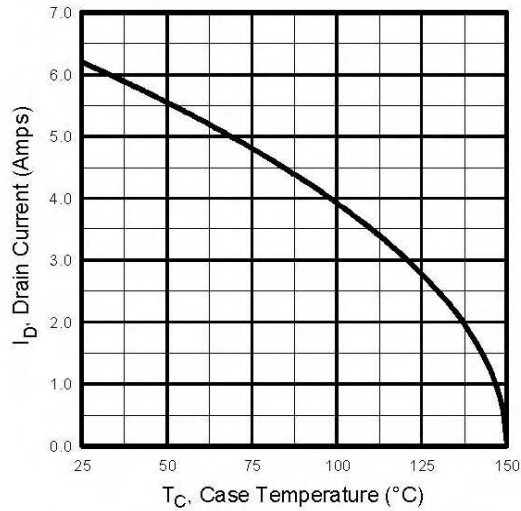


Fig 9. Maximum Drain Current Vs. Case Temperature

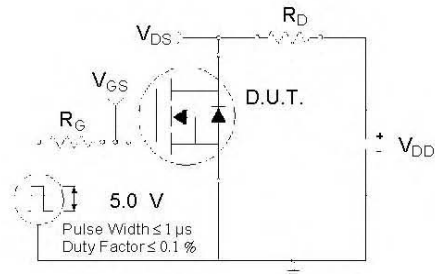


Fig 10a. Switching Time Test Circuit

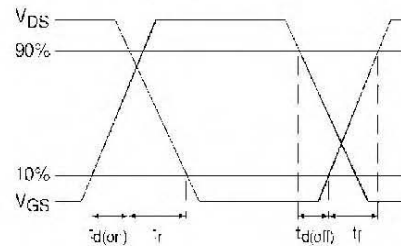


Fig 10b. Switching Time Waveforms

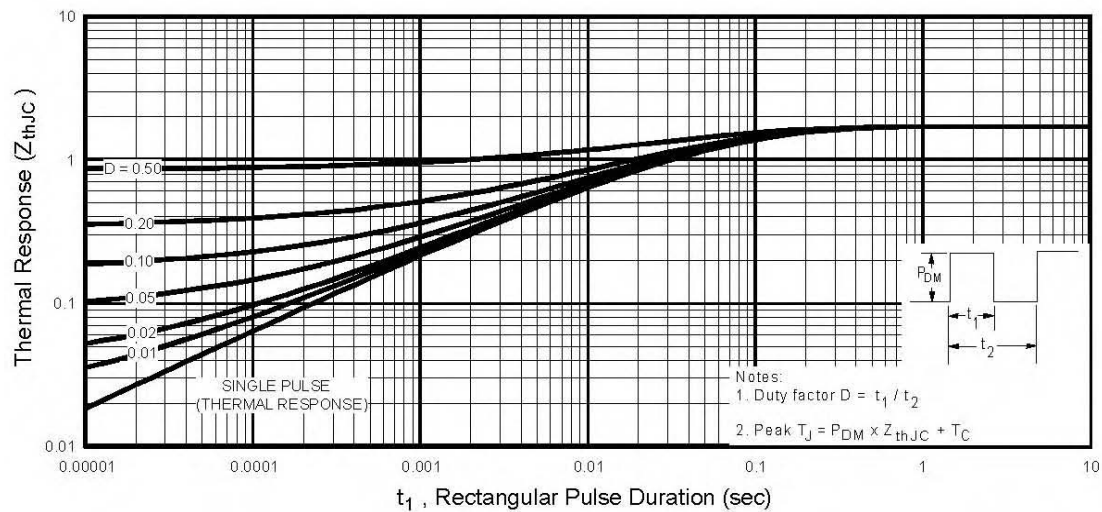


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

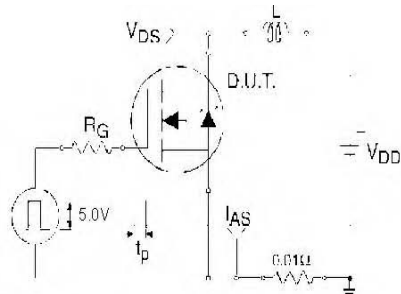


Fig 12a. Unclamped Inductive Test Circuit

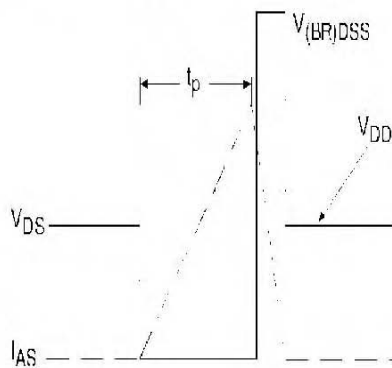


Fig 12b. Unclamped Inductive Waveforms

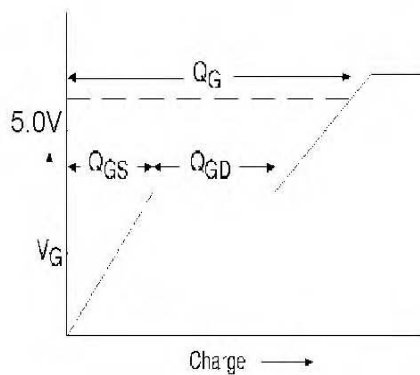


Fig 13a. Basic Gate Charge Waveform

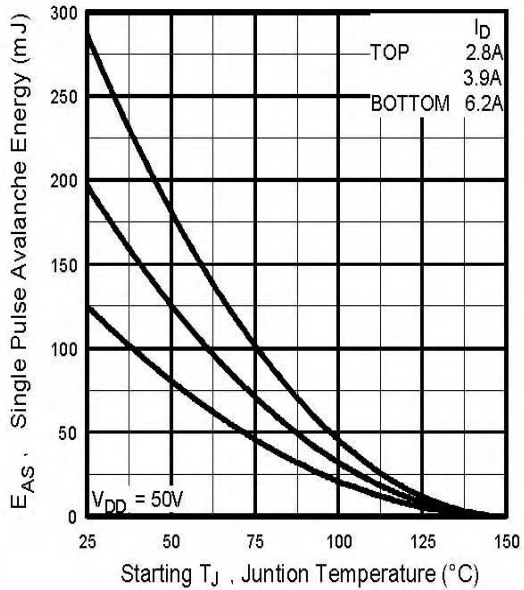


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

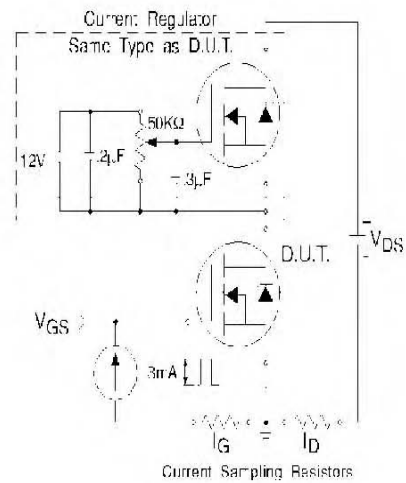
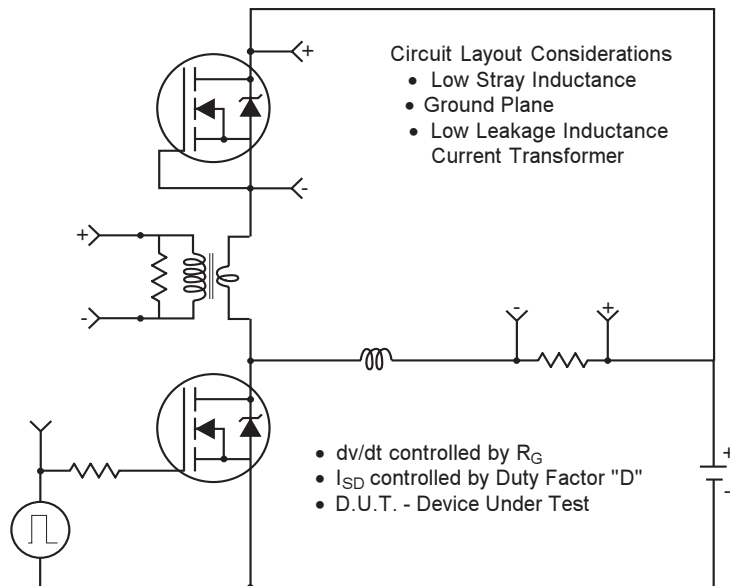


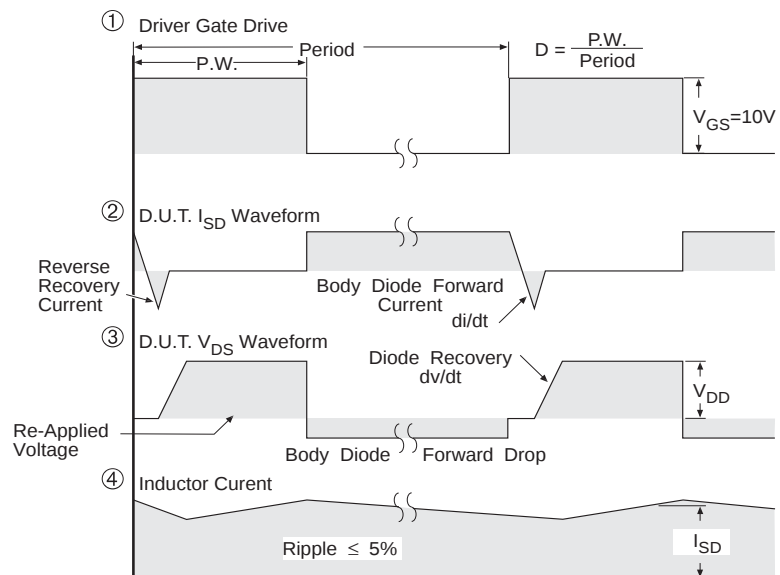
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

**** Use P-Channel Driver for P-Channel Measurements**



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig-14 For N Channel HEXFETS

International
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[illegible]

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	0.180	0.190	5	HEXFET 1. - GATE 2. - DRAIN 3. - SOURCE
A1	2.51	2.83	0.101	0.114		
A2	2.57	2.85	0.099	0.112		
b	0.622	0.89	0.024	0.035		
b1	0.622	0.838	0.024	0.033		
b2	1.229	1.400	0.048	0.055		
b3	1.229	1.400	0.048	0.055		
c	0.440	0.629	0.017	0.025		
cf	0.440	0.584	0.017	0.023		
D	8.65	9.80	0.341	0.386		
d	15.80	16.12	0.622	0.635		
d2	13.97	14.22	0.550	0.560		
d3	12.30	12.92	0.484	0.509		
d4	8.64	9.91	0.340	0.390	4	
E	10.36	10.63	0.408	0.419		
e	2.54 BSC		0.100 BSC			
L	13.20	13.73	0.520	0.541		
L1	3.10	3.50	0.122	0.138	3	
L	6.05	6.15	0.238	0.248		
u	3.05	3.45	0.120	0.136		
uP	2.40	2.50	0.094	0.098		
v	4.00	0.50	0.016	0.020	6	
ø	3"	7"	3"	7"		
ø1	45°		45°			

Diagram illustrating the markings on a MOSFET package (IRF1840G):

- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo.
- PART NUMBER**: Points to the text IRF1840G.
- DATE CODE**: Points to the text YEAR 9 = 1999, WEEK 24, LINE K.
- ASSEMBLY LOT CODE**: Points to the text 34 32.

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