Jameco Part Number 1862500

IS65LV256AL
IS62LV256AL

32K x 8 LOW VOLTAGE CMOS STATIC RAM

OCTOBER 2006

FEATURES

- High-speed access time: 20, 45 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  - — 17 µW (typical) CMOS standby
  - — 50 mW (typical) operating
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs
- Industrial and Automotive temperatures available
- Lead-free available

DESCRIPTION

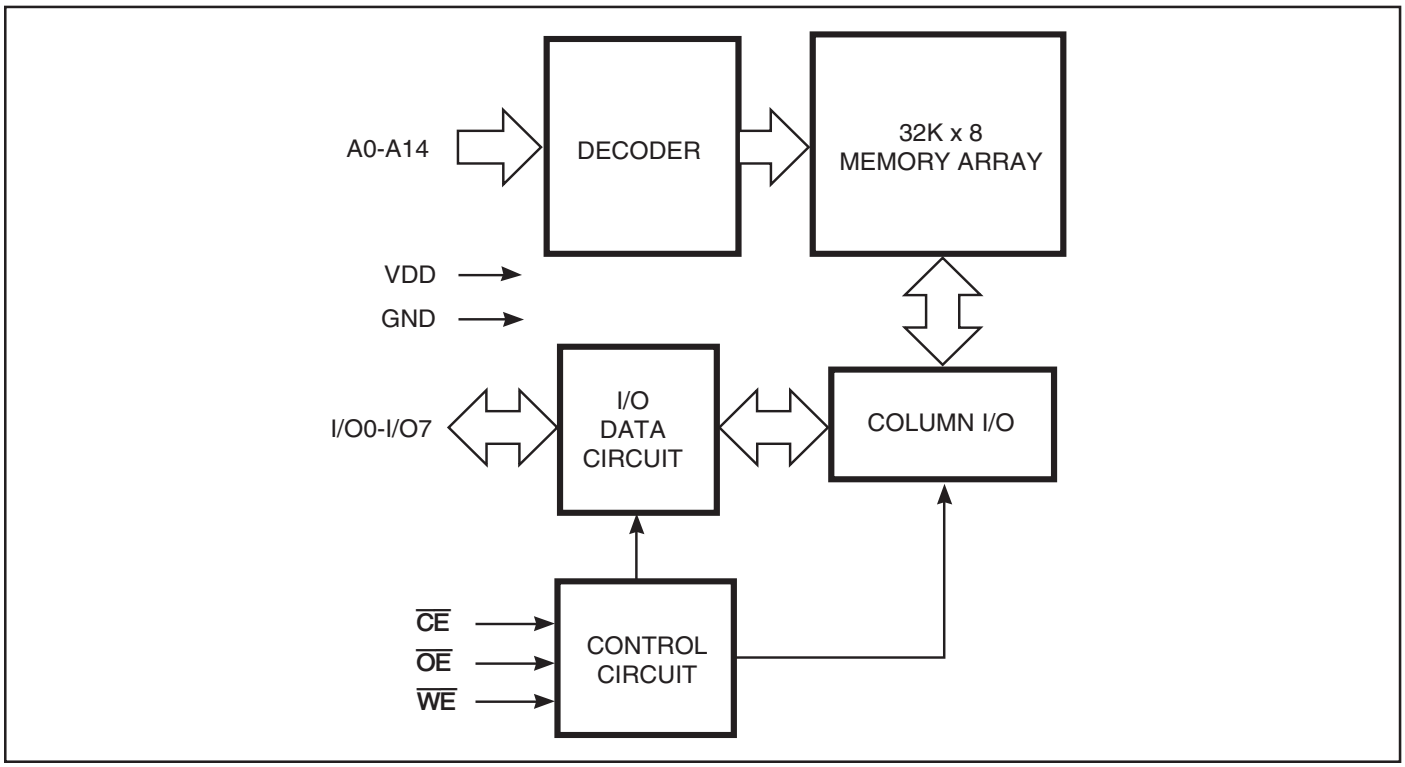
The *ISSI* IS62/65LV256AL is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 150 µW (typical) with CMOS input levels.

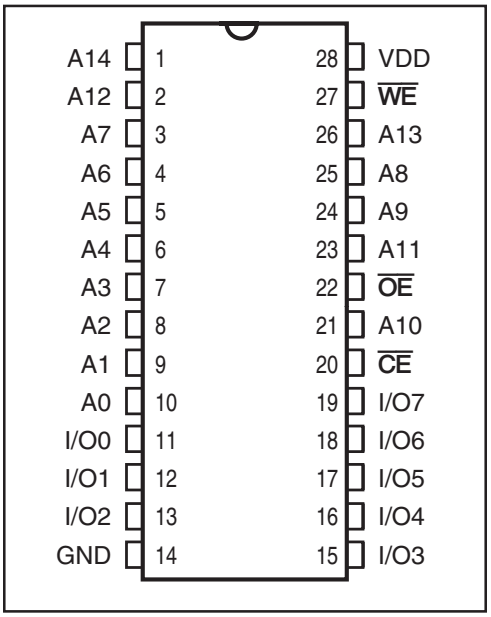
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$). The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62/65LV256AL is available in the JEDEC standard 28-pin SOJ, 28-pin SOP, and the 28-pin 450-mil TSOP package.

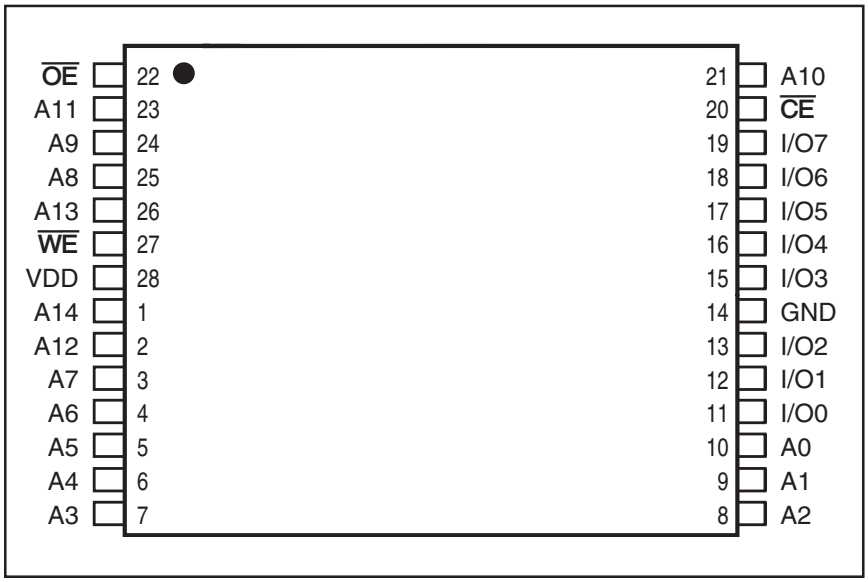
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin SOJ/ 28-pin SOP



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Part No.	Range	Ambient Temperature	V_{DD}
IS62LV256AL	Commercial	0°C to +70°C	3.3V +10%
IS62LV256AL	Industrial	–40°C to +85°C	3.3V ± 10%
IS65LV256AL	Automotive	–40°C to +125°C	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –2.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 4.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com. Ind. Auto.	–1 –2 –10	1 2 10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	Com. Ind. Auto.	–1 –2 –10	1 2 10	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-20 ns Min.	-20 ns Max.	-45 ns Min.	-45 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	4	—	4	mA
		I_{OUT} = 0 mA, f = 1 MHz	Ind.	—	5	—	5	
			Auto.	—	—	—	8	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	20	—	10	mA
		I_{OUT} = 0 mA, f = f_{MAX}	Ind.	—	25	—	12	
			Auto.	—	—	—	20	
			typ.[2]	15		7		
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	—	1.5	—	1.5	mA
		V_{IN} = V_{IH} or V_{IL}	Ind.	—	1.8	—	1.8	
		$\overline{CE}$ ≥ V_{IH}, f = 0	Auto.	—	—	—	2	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	—	15	—	15	µA
		$\overline{CE}$ ≤ V_{DD} – 0.2V,	Ind.	—	20	—	20	
		V_{IN} > V_{DD} – 0.2V, or	Auto.	—	—	—	50	
		V_{IN} ≤ 0.2V, f = 0	typ.[2]	2		2		

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{RC}	Read Cycle Time	20	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	45	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	10	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	9	0	20	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	9	0	20	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	18	—	30	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

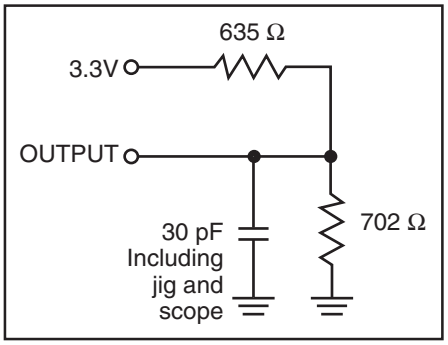


Figure 1.

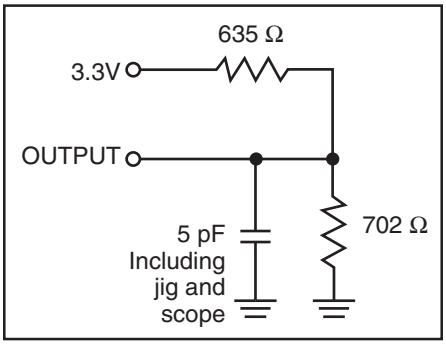
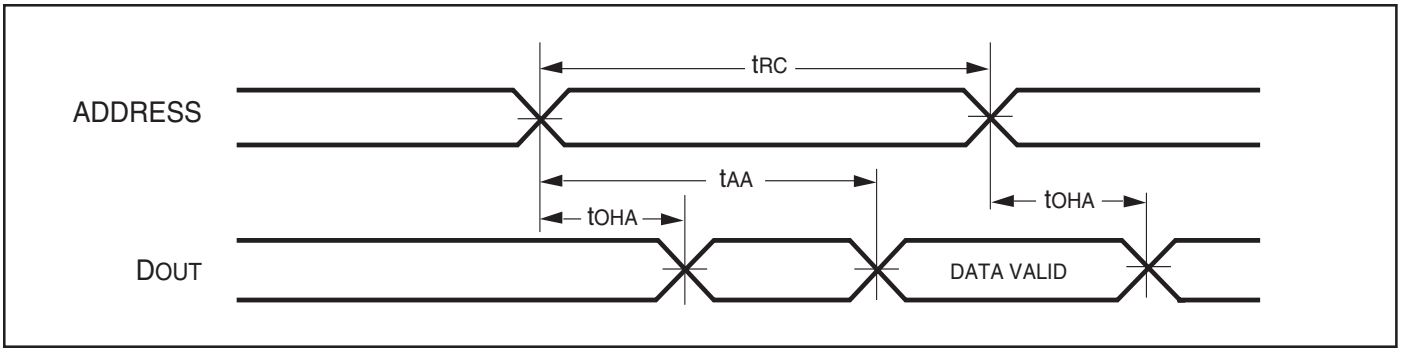


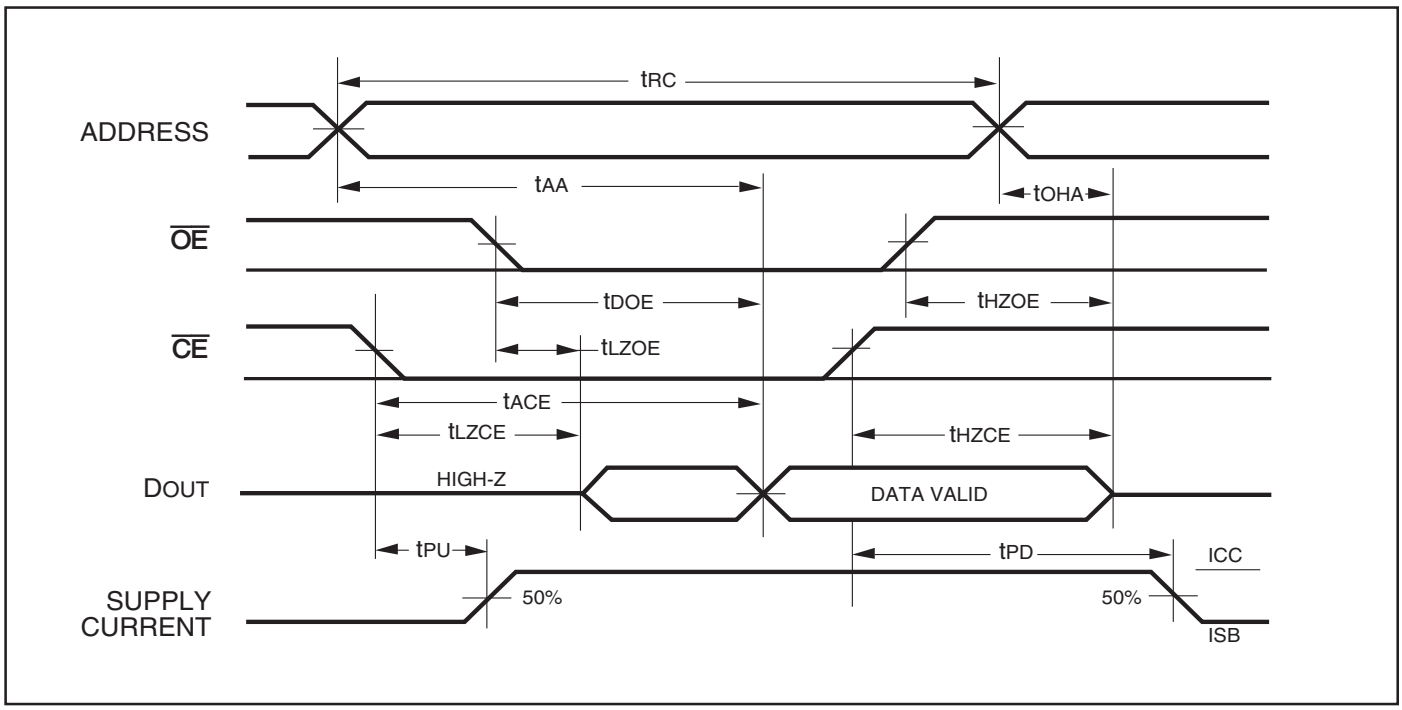
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

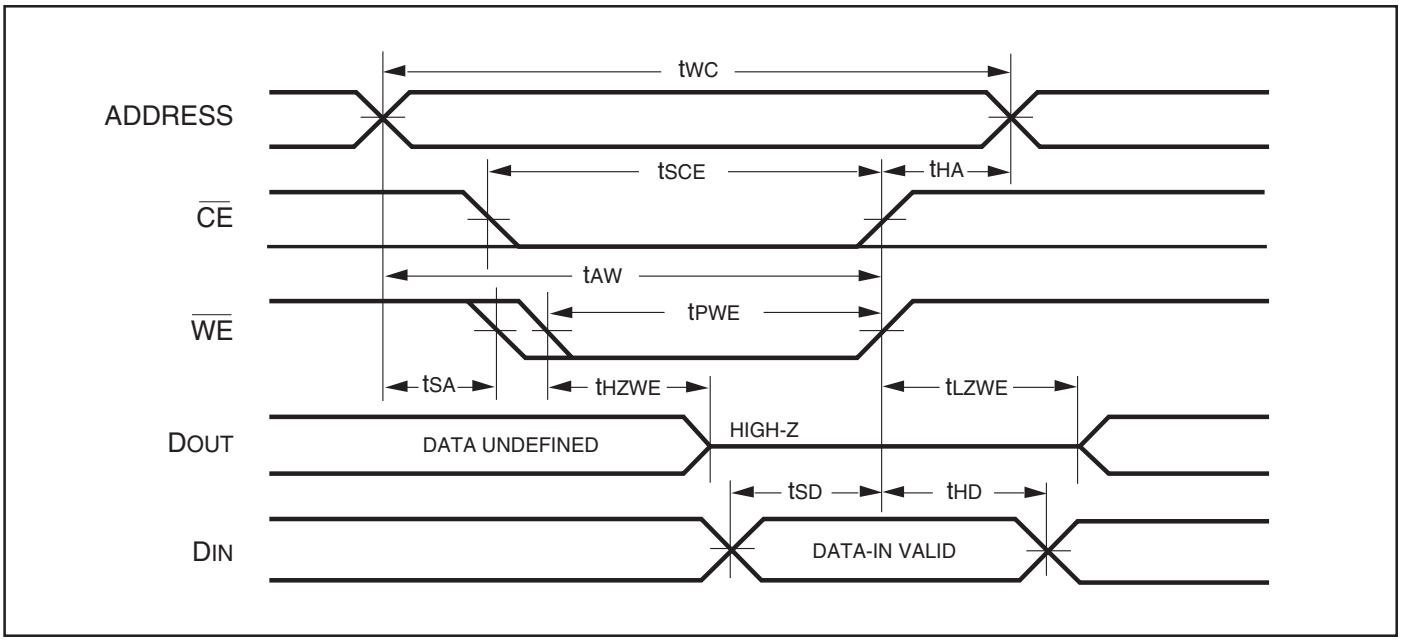
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{WC}	Write Cycle Time	20	—	45	—	ns
t_{SCE}	$\overline{CE}$ to Write End	15	—	35	—	ns
t_{AW}	Address Setup Time to Write End	14	—	25	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	14	—	25	—	ns
t_{SD}	Data Setup to Write End	13	—	20	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	8	—	20	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

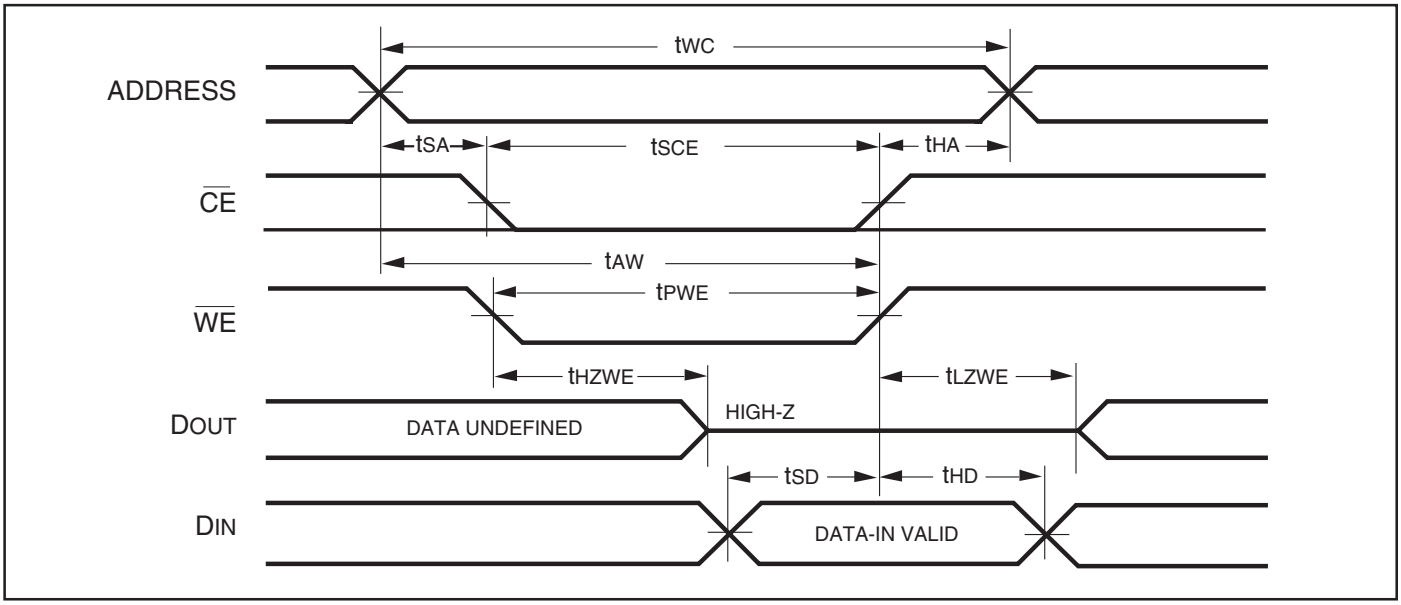
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]



Notes:

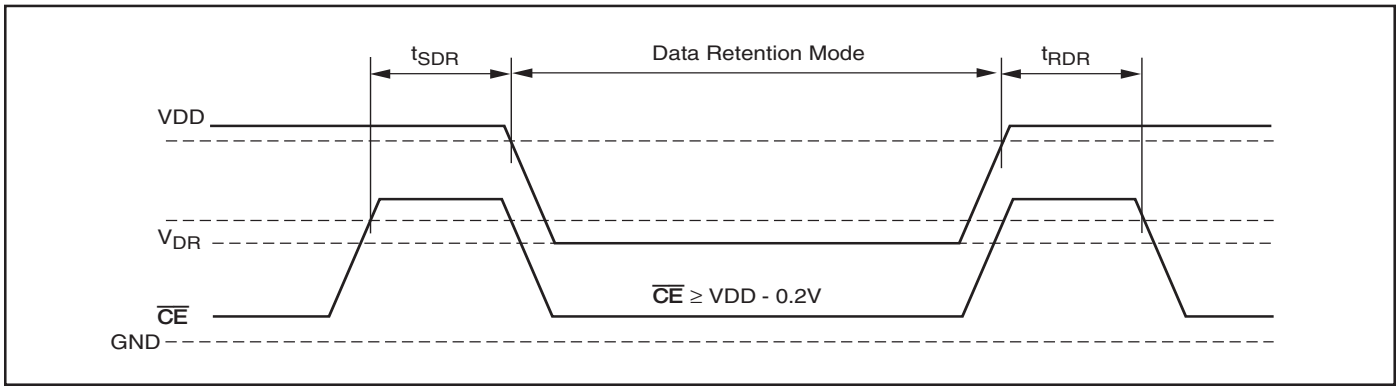
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	—	15	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	—	20	
			Auto.	—	—	50	
			typ.(1)		2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:
1. Typical Values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
20	IS62LV256AL-20T	450-mil TSOP
	IS62LV256AL-20TL	450-mil TSOP, Lead-free
	IS62LV256AL-20J	300-mil Plastic SOJ
	IS62LV256AL-20JL	300-mil Plastic SOJ, Lead-free
45	IS62LV256AL-45T	450-mil TSOP
	IS62LV256AL-45TL	450-mil TSOP, Lead-free
	IS62LV256AL-45J	300-mil Plastic SOJ

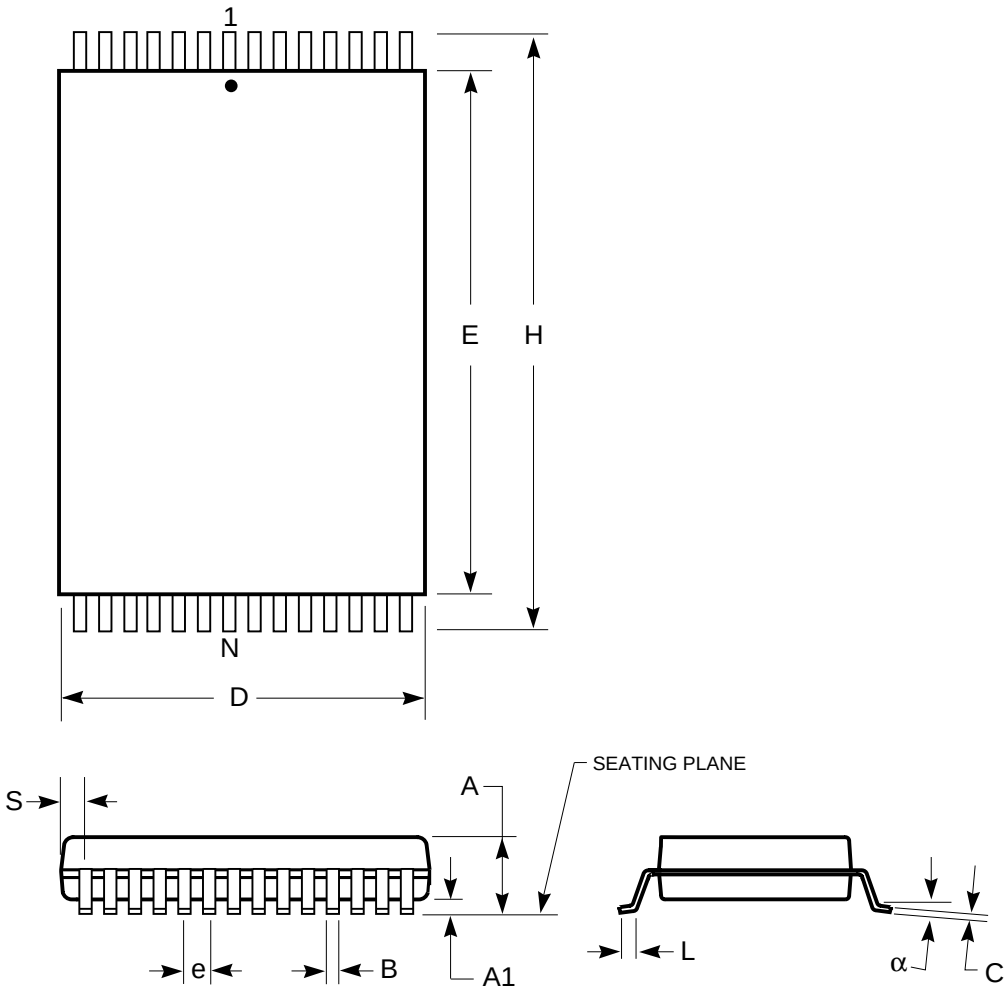
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
20	IS62LV256AL-20TI	450-mil TSOP
	IS62LV256AL-20TLI	450-mil TSOP, Lead-free
	IS62LV256AL-20JI	300-mil Plastic SOJ
	IS62LV256AL-20JLI	300-mil Plastic SOJ, Lead-free
45	IS62LV256AL-45TI	450-mil TSOP
	IS62LV256AL-45TLI	450-mil TSOP, Lead-free
	IS62LV256AL-45JI	300-mil Plastic SOJ
	IS62LV256AL-45UI	330-mil Plastic SOP
	IS62LV256AL-45ULI	330-mil Plastic SOP, Lead-free

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
45	IS65LV256AL-45TA3	450-mil TSOP
	IS65LV256AL-45TLA3	450-mil TSOP, Lead-free
	IS65LV256AL-45UA3	330-mil Plastic SOP
	IS65LV256AL-45ULA3	330-mil Plastic SOP, Lead-free

Plastic TSOP - 28-pins
Package Code: T (Type I)

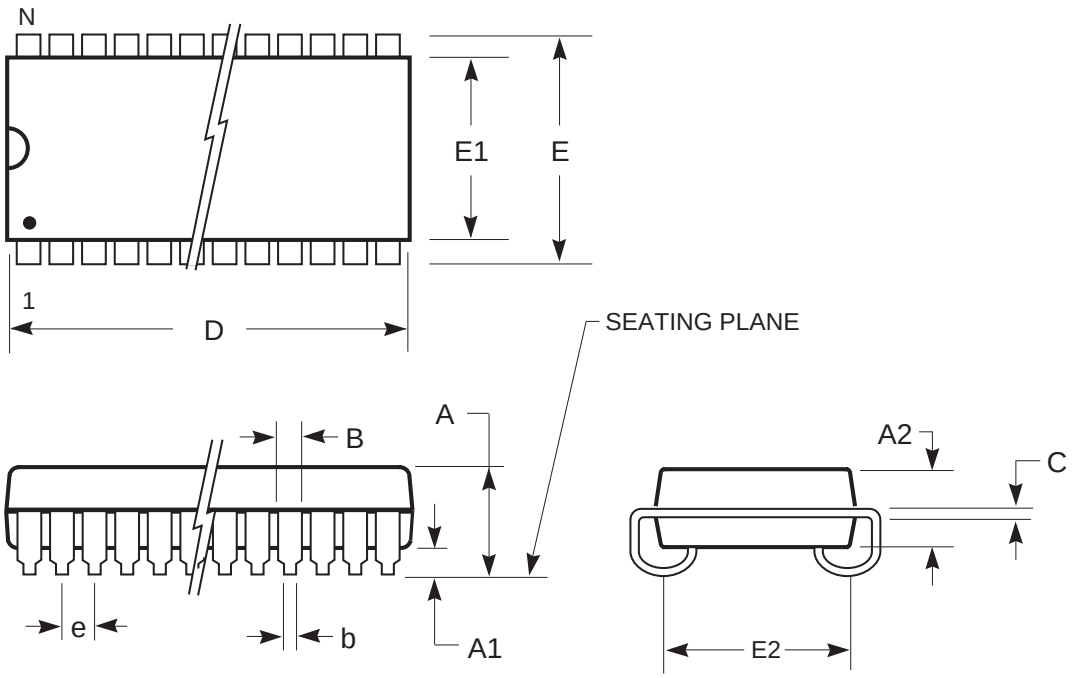


Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		28		
A	1.00	1.20	0.037	0.047
A1	0.05	0.20	0.002	0.008
B	0.16	0.27	0.006	0.011
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.308	0.316
E	11.70	11.90	0.456	0.465
H	13.20	13.60	0.515	0.531
e	0.55 BSC		0.022 BSC	
L	0.30	0.70	0.011	0.027
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

300-mil Plastic SOJ
Package Code: J



	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**24/26**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	17.02	—	17.27	0.670	—	0.680
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

ISSI®

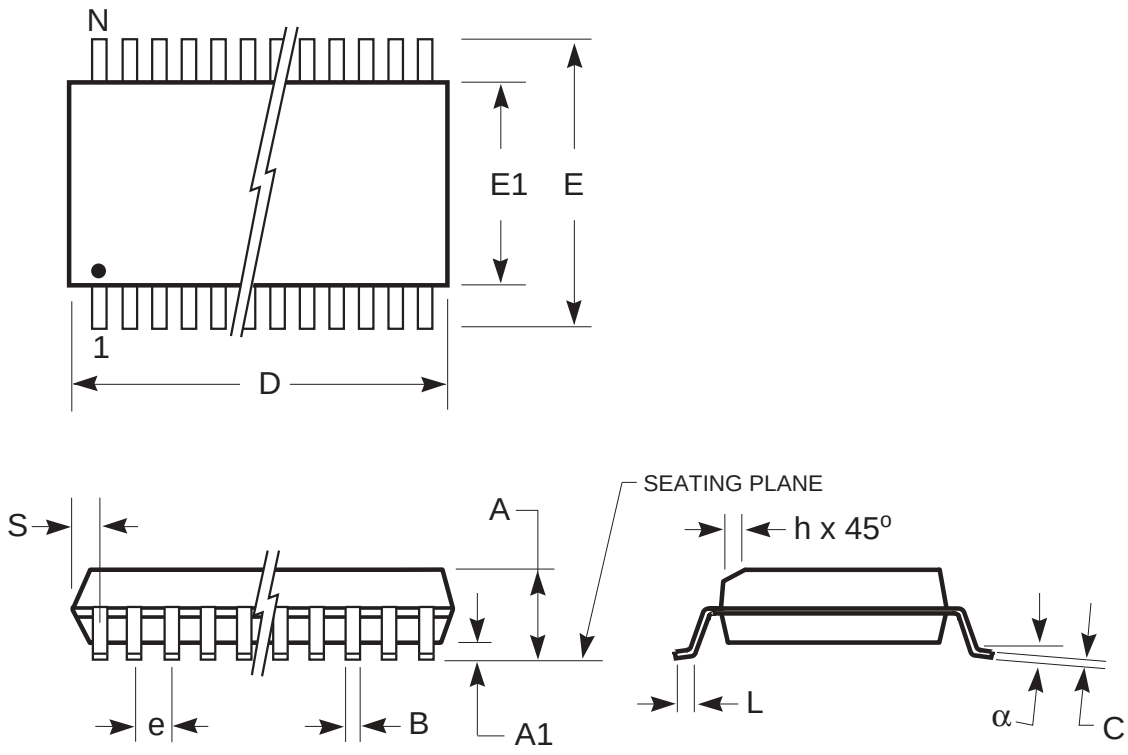
300-mil Plastic SOJ
Package Code: J

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**28**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	18.29	—	18.54	0.720	—	0.730
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**32**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	20.83	—	21.08	0.820	—	0.830
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e	1.27 BSC			0.050 BSC		

PACKAGING INFORMATION

330-mil Plastic SOP
Package Code: U (28-pin)



	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
No. Leads	**28**		**28**	
A	—	2.84	—	0.112
A1	0.10	—	0.004	—
B	0.36	0.51	0.014	0.020
C	0.25	—	0.010	—
D	17.98	18.24	0.708	0.718
E	11.51	12.12	0.453	0.477
E1	8.28	8.53	0.326	0.336
e	1.27 BSC		0.050 BSC	
h	0.30	0.51	0.012	0.020
L	0.71	1.14	0.028	0.045
α	0°	8°	0°	8°
S	0.58	1.19	0.023	0.047

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.