82341
ISA PERIPHERAL COMBO CHIP

- **Combines the following PC/AT Peripheral Chips:**
  - **16C450 UART - COM1:**
  - **16C450 UART - COM2:**
  - **Parallel Printer Port - LPT1:**
  - **Keyboard/Mouse Ctrl. - KBD**
  - **Real Time Clock**
- **Serial Ports Fully 16C450 Compatible**
- **Bidirectional Line Printer Port**
- **Software Control of PS/2*-Compatible Enhancements (LPT Port, Mouse)**
- **CMOS Direct Drive of Centronics-Type Parallel Interface**
- **PC/AT- or PS/2-Compatible Keyboard and Mouse Controller**
- **146818A-Compatible Real Time Clock (RTC)**
- **16 Bytes of Additional Standby RAM (66 Bytes Total)**
- **IDE Bus Control Signals Included (Two External 74LS245 and One 74LS244—or Equivalent—Buffers are Required)**
- **Seven Battery-Backed Programmable Chip Select Registers for Auto Configuration**
- **Preprogrammed Default Chip Selects**
- **Programmable Wait State Generation**
- **5 μA Standby Current for RTC, RAM, and Chip Select Registers**
- **Single 128-Pin Plastic Quad Flatpack**

1

The 82341 Peripheral Combo chip replaces with a single 128-pin chip, several of the commonly used peripherals found in PC/AT-compatible computers. This chip when used with the Intel PC/AT-compatible chip set allows designers to implement a very cost effective, minimum chip count motherboard containing functions that are common to virtually all PCs.

The on-chip UARTs are completely software compatible with the 16C450 Asynchronous Communication Element.

The bidirectional parallel port provides a PS/2 software compatible interface between a Centronics-type printer and the 82341. Direct drive is provided so that all that is necessary to interface to the line printer port is a resistor-capacitor network. The bidirectional feature (option) is software programmable for backwards PC/AT-compatibility.

The keyboard/mouse controller is selectable as PC/AT-or PS/2-compatible.

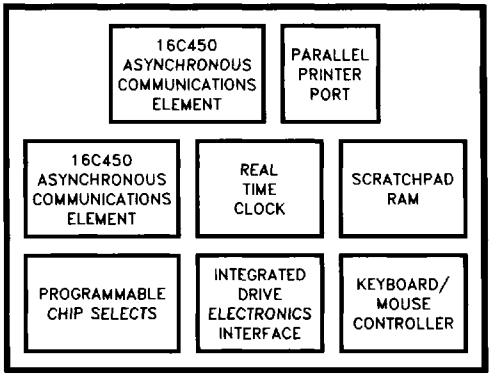
The Real Time Clock is 146818A-compatible and offers a standby current drain of 5 μA at 3.0V.

Ordering Information

Part Number	Package
82341	128-Pin Plastic Quad Flatpack

NOTE:
Operating temperature range is 0°C to +70°C.

Internal Functional Diagram



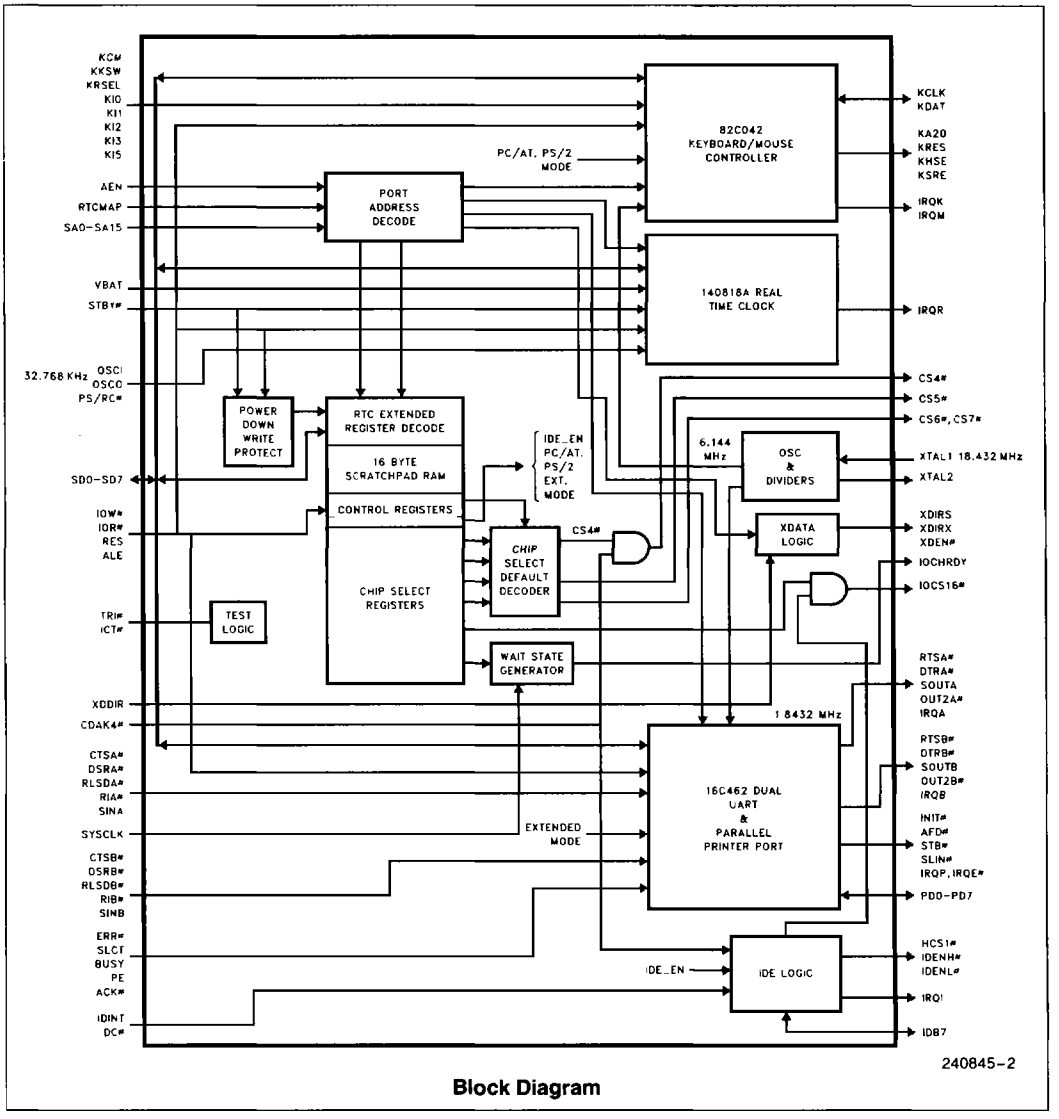
240845-1

*PC/AT® and PS/2® are registered trademarks of International Business Machines Corp.

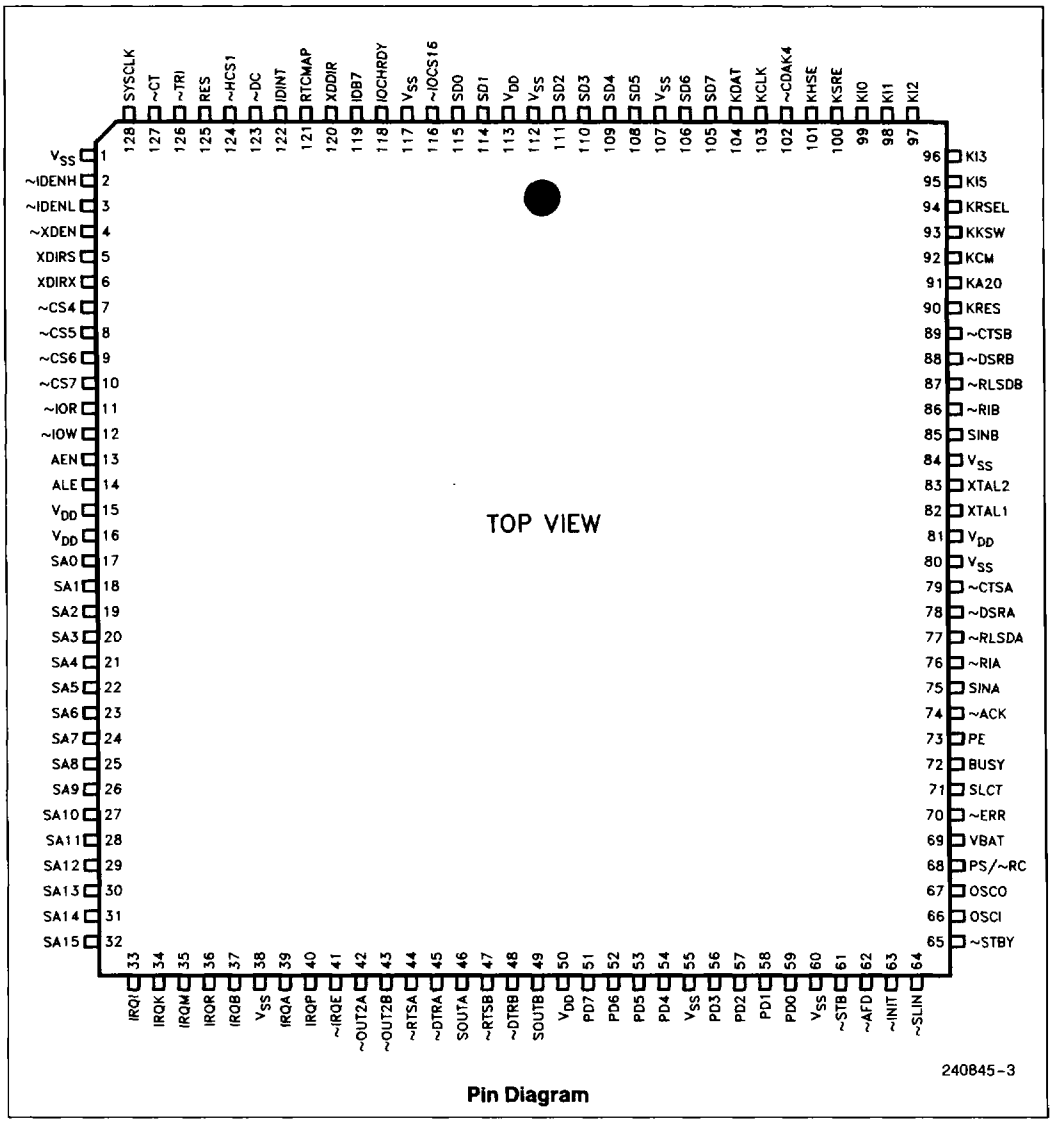
October 1990
Order Number: 240845-001

Included is the control logic necessary for the support of the Integrated Drive Electronics (IDE) hard disk bus interface.

The Peripheral Combo chip also includes seven programmable chip selects, three internal and four external. Each chip select has a programmable 16-bit base address and a mask register that allows the number of bytes corresponding to each chip select to be programmed (e.g. 3F8H–3FFH has a base address of 3F8H and a range of 8 bytes). Each chip select can be programmed for number of wait states (0–7) and 8- or 16-bit operation. 16-bit decoding is used for all I/O addresses. A default fixed decode is provided on reset for the on-chip serial ports, printer port, and off-chip floppy and hard disk controllers, which may be changed to battery-backed programmable chip selects via control bit.



Block Diagram


TOP VIEW
1 VSS
2 ~IDENH
3 ~IDENL
4 ~XDEN
5 XDIRS
6 XDIRX
7 ~CS4
8 ~CS5
9 ~CS6
10 ~CS7
11 ~IOR
12 ~IOW
13 AEN
14 ALE
15 VDD
16 VDD
17 SA0
18 SA1
19 SA2
20 SA3
21 SA4
22 SA5
23 SA6
24 SA7
25 SA8
26 SA9
27 SA10
28 SA11
29 SA12
30 SA13
31 SA14
32 SA15
33 IRQI
34 IRQK
35 IRQM
36 IRQR
37 IRQB
38 VSS
39 IRQA
40 IRQP
41 ~IRQE
42 ~OUT2A
43 ~OUT2B
44 ~RTSA
45 ~DTRA
46 SOUTA
47 ~RTSB
48 ~DTRB
49 SOUTB
50 VDD
51 PD7
52 PD6
53 PD5
54 PD4
55 VSS
56 PD3
57 PD2
58 PD1
59 PD0
60 VSS
61 ~STB
62 ~AFD
63 ~INIT
64 ~SLIN
65 ~STBY
66 OSCI
67 OSCO
68 PS/~RC
69 VBAT
70 ~ERR
71 SLCT
72 BUSY
73 PE
74 ~ACK
75 SINA
76 ~RIA
77 ~RLSDA
78 ~DSRA
79 ~CTSA
80 VSS
81 VDD
82 XTAL1
83 XTAL2
84 VSS
85 SINB
86 ~RIB
87 ~RLSDB
88 ~DSRB
89 ~CTSB
90 KRES
91 KA20
92 KCM
93 KKSW
94 KRSEL
95 KI5
96 KI3
97 KI2
98 KI1
99 KI0
100 KSRE
101 KHSE
102 ~CDAK4
103 KCLK
104 KDAT
105 SD7
106 SD6
107 VSS
108 SD5
109 SD4
110 SD3
111 SD2
112 VSS
113 VDD
114 SD1
115 SD0
116 ~IOCS16
117 VSS
118 IOCHRDY
119 IDB7
120 XDDIR
121 RTCMAP
122 IDINT
123 ~DC
124 ~HCS1
125 RES
126 ~TRI
127 ~CT
128 SYSCLK
240845-3

Pin Diagram

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
COMMUNICATIONS PORT A			
RTSA#	44	O1	Request to Send, Port A
DTRA#	45	O1	Data Terminal Ready, Port A
SOUTA	46	O1	Serial Data Output, Port A
CTSA#	79	I4	Clear to Send, Port A
DSRA#	78	I4	Data Set Ready, Port A
RLSDA#	77	I4	Receive Line Signal Detect, Port A
RIA#	76	I4	Ring Indicator, Port A
SINA	75	I4	Serial Input, Port A
IRQA	39	O6	Interrupt Request, Port A
OUT2A#	42	O1	Output 2, Port A
COMMUNICATIONS PORT B			
RTSB#	47	O1	Request to Send, Port B
DTRB#	48	O1	Data Termina Ready, Port B
SOUTB	49	O1	Serial Data Output, Port B
CTSB#	89	I4	Clear to Send, Port B
DSRB#	88	I4	Data Set Ready, Port B
RLSDB#	87	I4	Receive Line Signal Detect, Port B
RIB#	86	I4	Ring Indicator, Port B
SINB	85	I4	Serial Input, Port B
IRQB	37	O6	Interrupt Request, Port B
OUT2B#	43	O1	Output 2, Port B
PARALLEL PRINTER PORT			
PD0	59	IO5	Printer Data Port, Bit 0
PD1	58	IO5	Printer Data Port, Bit 1
PD2	57	IO5	Printer Data Port, Bit 2
PD3	56	IO5	Printer Data Port, Bit 3
PD4	54	IO5	Printer Data Port, Bit 4
PD5	53	IO5	Printer Data Port, Bit 5
PD6	52	IO5	Printer Data Port, Bit 6
PD7	51	IO5	Printer Data Port, Bit 7
INIT#	63	O4	Initialize Printer Signal
AFD#	62	O4	Autofeed Printer Signal
STB#	61	O4	Data Strobe to Printer
SLIN#	64	O4	Select Signal from Printer
ERR#	70	I4	Error Signal from Priner
SLCT	71	I4	Select Signal from Printer

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
PARALLEL PRINTER PORT (Continued)			
BUSY	72	I4	Busy Signal from Printer
PE	73	I4	Paper Error Signal from Printer
ACK#	74	I4	Acknowledge Signal from Printer
IRQP	40	O6	Printer Interrupt Request Output
IRQE#	41	O1	Printer Interrupt Request Enable Signal
REAL TIME CLOCK PORT			
VBAT	69	NA	Standby Power—Normally 3V to 5V, battery backed
STBY#	65	I5	Power Down Control
OSCI	66	NA	Crystal Connection Input—32 kHz
OSCO	67	NA	Crystal Connection Output—32 kHz
PS/RC#	68	I5	Power Sense/RAM Clear Input
IRQR	36	O1	Real Time Clock Interrupt Request Output
RTCMAP	121	I4	High—RTC is mapped to 70H and 71H, Low—RTC is mapped to 170H and 171H
KEYBOARD CONTROLLER PORT			
KCLK	103	IO4	Keyboard Clock
KDAT	104	IO4	Keyboard Data
KCM	92	I4	General Purpose Input, Normally Color/Monochrome
KKSW	93	I4	General Purpose Input, Normally Keyboard Switch
KA20	91	O1	General Purpose Output, Normally A20 Gate
KRES	90	O1	General Purpose Output, Normally Reset
KHSE	101	O1/IO4	General Purpose Input, Normally Speed Select
KSRE	100	O1/IO4	General Purpose Output, Normally Shadow RAM Enable
IRQK	34	O1	Keyboard Interrupt Request
IRQM	35	O1	Mouse Interrupt Request
KRSEL	94	I4	General Purpose Input, Normally RAM Select
K10	99	I4	General Purpose Input, Bit 0
K11	98	I4	General Purpose Input, Bit 1
K12	97	I4	General Purpose Input, Bit 2
K13	96	I4	General Purpose Input, Bit 3
K15	95	I4	General Purpose Input, Bit 5
IDE BUS I/O			
IDENH#	2	O1	IDE Bus Transceiver High Byte Enable
IDENL#	3	O1	IDE Bus Transceiver Low Byte Enable
IDINT	122	I4	IDE Bus Interrupt Request Input
IDB7	119	IO6	IDE Bus Data Bit 7
DC#	123	I4	Floppy Disk Change Signal
HCS1#	124	O1	IDE Host Chip Select 1
IRQI#	33	O6	IDE Interrupt Request Output

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
COMMON BUS I/O			
SD0	115	IO2	System Bus Data, Bit 0
SD1	114	IO2	System Bus Data, Bit 1
SD2	111	IO2	System Bus Data, Bit 2
SD3	110	IO2	System Bus Data, Bit 3
SD4	109	IO2	System Bus Data, Bit 4
SD5	108	IO2	System Bus Data, Bit 5
SD6	106	IO2	System Bus Data, Bit 6
SD7	105	IO2	System Bus Data, Bit 7
SA0	17	I1	System Bus Address, Bit 0
SA1	18	I1	System Bus Address, Bit 1
SA2	19	I1	System Bus Address, Bit 2
SA3	20	I1	System Bus Address, Bit 3
SA4	21	I1	System Bus Address, Bit 4
SA5	22	I1	System Bus Address, Bit 5
SA6	23	I1	System Bus Address, Bit 6
SA7	24	I1	System Bus Address, Bit 7
SA8	25	I1	System Bus Address, Bit 8
SA9	26	I1	System Bus Address, Bit 9
SA10	27	I1	System Bus Address, Bit 10
SA11	28	I1	System Bus Address, Bit 11
SA12	29	I1	System Bus Address, Bit 12
SA13	30	I1	System Bus Address, Bit 13
SA14	31	I1	System Bus Address, Bit 14
SA15	32	I1	System Bus Address, Bit 15
XTAL1	82	NA	Crystal Clock Input—18.432 MHz
XTAL2	83	NA	Crystal Clock Output—18.432 MHz
IOR#	11	I1	System Bus I/O Read
IOW#	12	I1	System Bus I/O Write
RES	125	I1	System Reset
AEN	13	I1	System Bus Address Enable
ALE	14	I1	System Bus Address Latch Enable
IOCS16#	116	O8	System Bus I/O Chip Select 16
IOCHRDY	118	O8	System Bus I/O Channel Ready
SYSCLK	128	I1	System Clock—Processor Clock Divide by 2
CS4#	7	O1	Chip Select 4—Normally for External Floppy Disk Controller
CS5#	8	O1	Chip Select 5—Normally HCS0# for IDE
CS6#	9	O1	Chip Select 6—Normally for External Floppy Disk Controller
CS7#	10	O1	Chip Select 7—Normally for External Floppy Disk Controller
CDAK4#	102	I1	DMA Acknowledge Forces —CS4 Active
XDDIR	120	I1	X Data Bus Transceiver Direction
XDIRS	5	O1	Modified X Data Bus Transceiver Direction Control Signal—Excludes Real Time Clock and Keyboard Controller Decodes
XDIRX	6	O1	X Data Bus Transceiver Control Signal—Includes All CS Decodes Generated On Chip

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
COMMON BUS I/O (Continued)			
XDEN#	4	O1	X Data Bus Transceiver Enable
TRI#	126	I4	Three-State Control Input—For All Outputs to Isolate Chip for Board Tests
ICT#	127	I4	In Circuit Test Mode Control
POWER, GROUND, AND UNCOMMITTED			
VDD	15, 16, 50, 81, 113		System Power: + 5V
VSS	1, 38, 55, 60, 80, 84, 107, 112, 117		System Ground

1

I/O LEGEND

Pin Type	mA	Type	Comment
01	2	TTL	
02	24	TTL	
04	12	TTL-OD	Open Drain, Weak Pull-Up, No VDD Diode
06	4	TTL-TS	Three-State
07	24	TTL-TS	Three-State
08	24	TTL-OD	Open Drain, Fast Active Pull-Up
I1	—	TTL	
I2	—	CMOS	
I4	—	TTL	30 kΩ Pull-Up
I5	—	TTL	Schmitt-Trigger
I02	24	TTL-TS	Three-State
I04	12	TTL-OD	Open Drain, Slow Turn-On
I05	12	TTL-TS	Three-State
I06	24	TTL-TS	Three-State, 30 kΩ Pull-Up