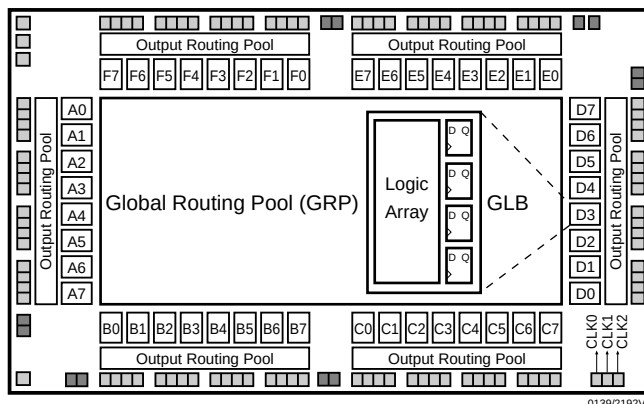


## Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 8000 PLD Gates
  - 96 I/O Pins, Nine or Twelve Dedicated Inputs
  - 192 Registers
  - High Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Pinout Compatible with ispLSI 2096V and 2096VE
- **3.3V LOW VOLTAGE ARCHITECTURE**
  - Interfaces with Standard 5V TTL Devices
- **HIGH PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max}$  = 225MHz Maximum Operating Frequency
  - $t_{pd}$  = 4.0ns Propagation Delay
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - 100% Tested at Time of Manufacture
  - Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - 3.3V In-System Programmability (ISP<sup>™</sup>) Using Boundary Scan Test Access Port (TAP)
  - Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - Enhanced Pin Locking Capability
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Programmable Output Slew Rate Control
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **LEAD-FREE PACKAGE OPTIONS**

## Functional Block Diagram



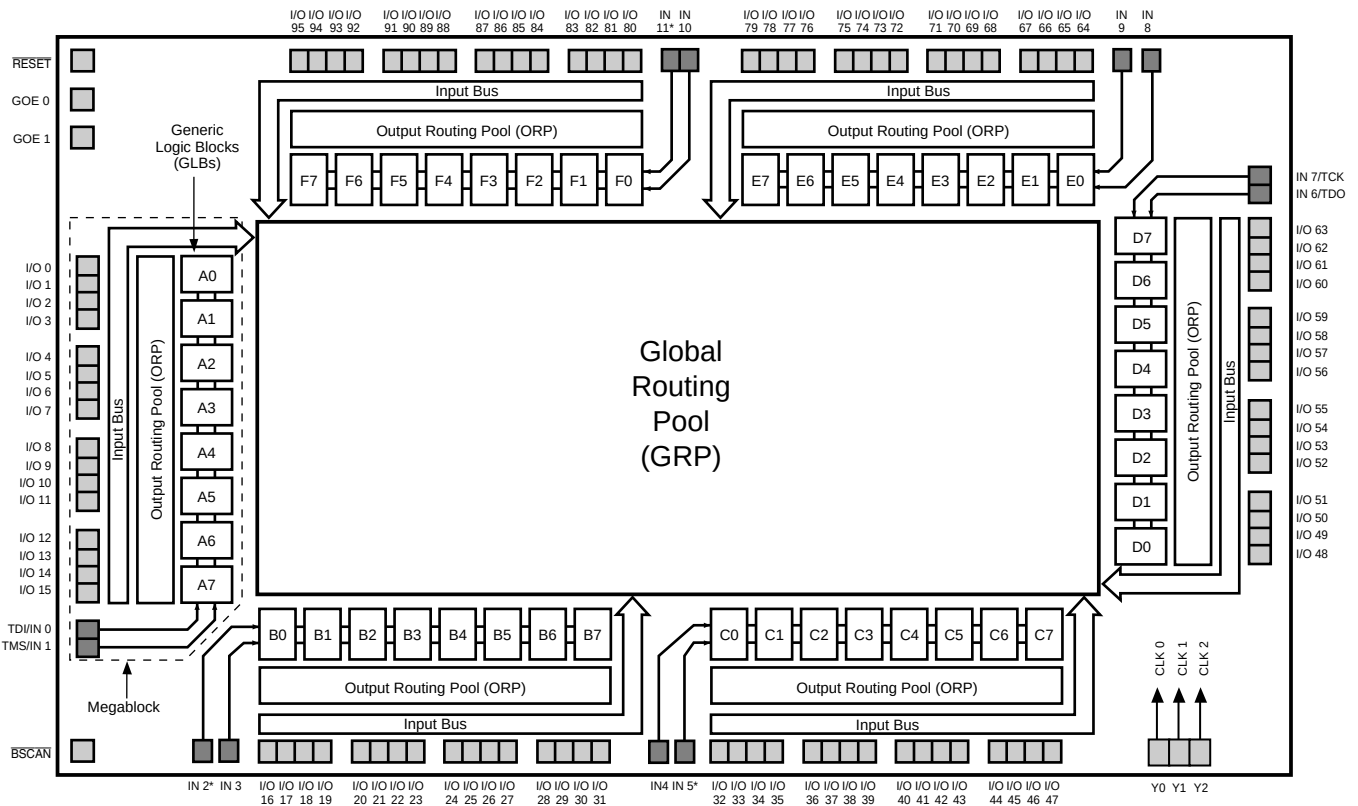
## Description

The ispLSI 2192VE is a High Density Programmable Logic Device containing 192 Registers, nine or twelve Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2192VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2192VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2192VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see Figure 1). There are a total of 48 GLBs in the ispLSI 2192VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

## Functional Block Diagram

Figure 1. ispLSI 2192VE Functional Block Diagram



\*Note: Dedicated Inputs 2, 5 and 11 are not available with 128-pin packages.

2192VE Block.eps

The 2192VE contains 96 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4mA or sink 8mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5V signal levels to support mixed-voltage systems.

Eight GLBs, 16 I/O cells, two dedicated inputs and an ORP are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 2192VE device contains six Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2192VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

### Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2192VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice software tools.

## Absolute Maximum Ratings <sup>1</sup>

Supply Voltage  $V_{CC}$  ..... -0.5 to +5.4V  
 Input Voltage Applied ..... -0.5 to +5.6V  
 Off-State Output Voltage Applied ..... -0.5 to +5.6V  
 Storage Temperature ..... -65 to 150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Condition

| SYMBOL   | PARAMETER          |                                                           | MIN.           | MAX. | UNITS |
|----------|--------------------|-----------------------------------------------------------|----------------|------|-------|
| $V_{CC}$ | Supply Voltage     | Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | 3.0            | 3.6  | V     |
| $V_{IL}$ | Input Low Voltage  |                                                           | $V_{SS} - 0.5$ | 0.8  | V     |
| $V_{IH}$ | Input High Voltage |                                                           | 2.0            | 5.25 | V     |

Table 2-0005/2192VE

## Capacitance ( $T_A=25^\circ\text{C}$ , $f=1.0\text{ MHz}$ )

| SYMBOL | PARAMETER                                  | TYPICAL | UNITS | TEST CONDITIONS                                  |
|--------|--------------------------------------------|---------|-------|--------------------------------------------------|
| $C_1$  | Dedicated Input Capacitance                | 8       | pf    | $V_{CC} = 3.3\text{V}$ , $V_{IN} = 0.0\text{V}$  |
| $C_2$  | I/O Capacitance                            | 8       | pf    | $V_{CC} = 3.3\text{V}$ , $V_{I/O} = 0.0\text{V}$ |
| $C_3$  | Clock and Global Output Enable Capacitance | 12      | pf    | $V_{CC} = 3.3\text{V}$ , $V_Y = 0.0\text{V}$     |

Table 2-0006/2192VE

## Erase Reprogram Specifications

| PARAMETER              | MINIMUM | MAXIMUM | UNITS  |
|------------------------|---------|---------|--------|
| Erase/Reprogram Cycles | 10,000  | —       | Cycles |

Table 2-0008/2192VE

## Switching Test Conditions

|                                |                                |
|--------------------------------|--------------------------------|
| Input Pulse Levels             | GND to 3.0V                    |
| Input Rise and Fall Time       | $\leq 1.5\text{ns}$ 10% to 90% |
| Input Timing Reference Levels  | 1.5V                           |
| Output Timing Reference Levels | 1.5V                           |
| Output Load                    | See Figure 2                   |

3-state levels are measured 0.5V from steady-state active level.

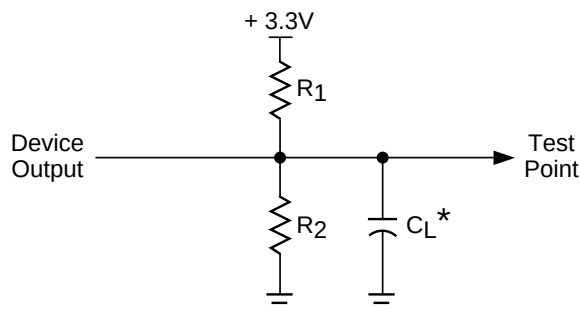
Table 2-0003/2192VE

## Output Load Conditions (see Figure 2)

| TEST CONDITION |                                   | R1           | R2           | CL   |
|----------------|-----------------------------------|--------------|--------------|------|
| A              |                                   | 316 $\Omega$ | 348 $\Omega$ | 35pF |
| B              | Active High                       | $\infty$     | 348 $\Omega$ | 35pF |
|                | Active Low                        | 316 $\Omega$ | 348 $\Omega$ | 35pF |
| C              | Active High to Z at $V_{OH}-0.5V$ | $\infty$     | 348 $\Omega$ | 5pF  |
|                | Active Low to Z at $V_{OL}+0.5V$  | 316 $\Omega$ | 348 $\Omega$ | 5pF  |

Table 2-0004/2192VE

Figure 2. Test Load



\* $C_L$  includes Test Fixture and Probe Capacitance.

0213A/2192VE

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| SYMBOL         | PARAMETER                                           | CONDITION                                                    | MIN. | TYP. <sup>3</sup> | MAX. | UNITS         |
|----------------|-----------------------------------------------------|--------------------------------------------------------------|------|-------------------|------|---------------|
| $V_{OL}$       | Output Low Voltage                                  | $I_{OL} = 8\text{ mA}$                                       | —    | —                 | 0.4  | V             |
| $V_{OH}$       | Output High Voltage                                 | $I_{OH} = -4\text{ mA}$                                      | 2.4  | —                 | —    | V             |
| $I_{IL}$       | Input or I/O Low Leakage Current                    | $0V \leq V_{IN} \leq V_{IL} (\text{Max.})$                   | —    | —                 | -10  | $\mu\text{A}$ |
| $I_{IH}$       | Input or I/O High Leakage Current                   | $(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$                    | —    | —                 | 10   | $\mu\text{A}$ |
|                |                                                     | $V_{CC} \leq V_{IN} \leq 5.25V$                              | —    | —                 | 10   | $\mu\text{A}$ |
| $I_{IL-isp}$   | $\overline{\text{BSCAN}}$ Input Low Leakage Current | $0V \leq V_{IN} \leq V_{IL}$                                 | —    | —                 | -150 | $\mu\text{A}$ |
| $I_{IL-PU}$    | I/O Active Pull-Up Current                          | $0V \leq V_{IN} \leq V_{IL}$                                 | —    | —                 | -150 | $\mu\text{A}$ |
| $I_{OS}^1$     | Output Short Circuit Current                        | $V_{CC} = 3.3V, V_{OUT} = 0.5V$                              | —    | —                 | -100 | mA            |
| $I_{CC}^{2,4}$ | Operating Power Supply Current                      | $V_{IL} = 0.0V, V_{IH} = 3.0V$<br>$f_{CLOCK} = 1\text{ MHz}$ | —    | 275               | —    | mA            |

Table 2-0007/2192VE

- One output at a time for a maximum duration of one second.  $V_{OUT} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using twelve 16-bit counters.
- Typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ\text{C}$ .
- Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER                     | TEST COND. <sup>3</sup> | #  | DESCRIPTION <sup>1</sup>                                                 | -225 |      | -180 |      | UNITS |
|-------------------------------|-------------------------|----|--------------------------------------------------------------------------|------|------|------|------|-------|
|                               |                         |    |                                                                          | MIN. | MAX. | MIN. | MAX. |       |
| <b>t<sub>pd1</sub></b>        | A                       | 1  | Data Propagation Delay, 4PT Bypass, ORP Bypass                           | –    | 4.0  | –    | 5.0  | ns    |
| <b>t<sub>pd2</sub></b>        | A                       | 2  | Data Propagation Delay                                                   | –    | 6.2  | –    | 7.5  | ns    |
| <b>f<sub>max</sub></b>        | A                       | 3  | Clock Frequency with Internal Feedback <sup>2</sup>                      | 225  | –    | 180  | –    | MHz   |
| <b>f<sub>max</sub> (Ext.)</b> | –                       | 4  | Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ ) | 150  | –    | 125  | –    | MHz   |
| <b>f<sub>max</sub> (Tog.)</b> | –                       | 5  | Clock Frequency, Max. Toggle                                             | 250  | –    | 200  | –    | MHz   |
| <b>t<sub>su1</sub></b>        | –                       | 6  | GLB Reg. Setup Time before Clock, 4 PT Bypass                            | 2.5  | –    | 3.5  | –    | ns    |
| <b>t<sub>co1</sub></b>        | A                       | 7  | GLB Reg. Clock to Output Delay, ORP Bypass                               | –    | 3.2  | –    | 3.5  | ns    |
| <b>t<sub>h1</sub></b>         | –                       | 8  | GLB Reg. Hold Time after Clock, 4 PT Bypass                              | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>su2</sub></b>        | –                       | 9  | GLB Reg. Setup Time before Clock                                         | 3.5  | –    | 4.5  | –    | ns    |
| <b>t<sub>co2</sub></b>        | A                       | 10 | GLB Reg. Clock to Output Delay                                           | –    | 3.7  | –    | 4.5  | ns    |
| <b>t<sub>h2</sub></b>         | –                       | 11 | GLB Reg. Hold Time after Clock                                           | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>r1</sub></b>         | A                       | 12 | Ext. Reset Pin to Output Delay, ORP Bypass                               | –    | 6.0  | –    | 7.0  | ns    |
| <b>t<sub>rw1</sub></b>        | –                       | 13 | Ext. Reset Pulse Duration                                                | 3.5  | –    | 4.0  | –    | ns    |
| <b>t<sub>ptoen</sub></b>      | B                       | 14 | Input to Output Enable                                                   | –    | 6.0  | –    | 10.0 | ns    |
| <b>t<sub>ptodis</sub></b>     | C                       | 15 | Input to Output Disable                                                  | –    | 6.0  | –    | 10.0 | ns    |
| <b>t<sub>goeen</sub></b>      | B                       | 16 | Global OE Output Enable                                                  | –    | 4.5  | –    | 5.0  | ns    |
| <b>t<sub>goedis</sub></b>     | C                       | 17 | Global OE Output Disable                                                 | –    | 4.5  | –    | 5.0  | ns    |
| <b>t<sub>wh</sub></b>         | –                       | 18 | External Synchronous Clock Pulse Duration, High                          | 2.0  | –    | 2.5  | –    | ns    |
| <b>t<sub>wl</sub></b>         | –                       | 19 | External Synchronous Clock Pulse Duration, Low                           | 2.0  | –    | 2.5  | –    | ns    |

Table 2-0030A/2192VE

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.

2. Standard 16-bit counter using GRP feedback.

3. Reference Switching Test Conditions section.

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER                     | TEST COND. <sup>3</sup> | #  | DESCRIPTION <sup>1</sup>                                                 | -135 |      | -100 |      | UNITS |
|-------------------------------|-------------------------|----|--------------------------------------------------------------------------|------|------|------|------|-------|
|                               |                         |    |                                                                          | MIN. | MAX. | MIN. | MAX. |       |
| <b>t<sub>pd1</sub></b>        | A                       | 1  | Data Propagation Delay, 4PT Bypass, ORP Bypass                           | –    | 7.5  | –    | 10.0 | ns    |
| <b>t<sub>pd2</sub></b>        | A                       | 2  | Data Propagation Delay                                                   | –    | 10.0 | –    | 13.0 | ns    |
| <b>f<sub>max</sub></b>        | A                       | 3  | Clock Frequency with Internal Feedback <sup>2</sup>                      | 135  | –    | 100  | –    | MHz   |
| <b>f<sub>max</sub> (Ext.)</b> | –                       | 4  | Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ ) | 100  | –    | 77   | –    | MHz   |
| <b>f<sub>max</sub> (Tog.)</b> | –                       | 5  | Clock Frequency, Max. Toggle                                             | 143  | –    | 100  | –    | MHz   |
| <b>t<sub>su1</sub></b>        | –                       | 6  | GLB Reg. Setup Time before Clock, 4 PT Bypass                            | 5.0  | –    | 6.5  | –    | ns    |
| <b>t<sub>co1</sub></b>        | A                       | 7  | GLB Reg. Clock to Output Delay, ORP Bypass                               | –    | 4.0  | –    | 5.0  | ns    |
| <b>t<sub>h1</sub></b>         | –                       | 8  | GLB Reg. Hold Time after Clock, 4 PT Bypass                              | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>su2</sub></b>        | –                       | 9  | GLB Reg. Setup Time before Clock                                         | 6.0  | –    | 8.0  | –    | ns    |
| <b>t<sub>co2</sub></b>        | A                       | 10 | GLB Reg. Clock to Output Delay                                           | –    | 5.0  | –    | 6.0  | ns    |
| <b>t<sub>h2</sub></b>         | –                       | 11 | GLB Reg. Hold Time after Clock                                           | 0.0  | –    | 0.0  | –    | ns    |
| <b>t<sub>r1</sub></b>         | A                       | 12 | Ext. Reset Pin to Output Delay, ORP Bypass                               | –    | 9.0  | –    | 12.5 | ns    |
| <b>t<sub>rw1</sub></b>        | –                       | 13 | Ext. Reset Pulse Duration                                                | 5.0  | –    | 6.5  | –    | ns    |
| <b>t<sub>ptoen</sub></b>      | B                       | 14 | Input to Output Enable                                                   | –    | 12.0 | –    | 15.0 | ns    |
| <b>t<sub>ptoedis</sub></b>    | C                       | 15 | Input to Output Disable                                                  | –    | 12.0 | –    | 15.0 | ns    |
| <b>t<sub>goeen</sub></b>      | B                       | 16 | Global OE Output Enable                                                  | –    | 7.0  | –    | 9.0  | ns    |
| <b>t<sub>goedis</sub></b>     | C                       | 17 | Global OE Output Disable                                                 | –    | 7.0  | –    | 9.0  | ns    |
| <b>t<sub>wh</sub></b>         | –                       | 18 | External Synchronous Clock Pulse Duration, High                          | 3.5  | –    | 5.0  | –    | ns    |
| <b>t<sub>wl</sub></b>         | –                       | 19 | External Synchronous Clock Pulse Duration, Low                           | 3.5  | –    | 5.0  | –    | ns    |

Table 2-0030B/2192VE

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.

2. Standard 16-bit counter using GRP feedback.

3. Reference Switching Test Conditions section.

## Internal Timing Parameters<sup>1</sup>

### Over Recommended Operating Conditions

| PARAMETER            | # <sup>2</sup> | DESCRIPTION                                           | -225 |      | -180 |      | UNITS |
|----------------------|----------------|-------------------------------------------------------|------|------|------|------|-------|
|                      |                |                                                       | MIN. | MAX. | MIN. | MAX. |       |
| Inputs               |                |                                                       |      |      |      |      |       |
| t <sub>io</sub>      | 20             | Input Buffer Delay                                    | –    | 0.3  | –    | 0.5  | ns    |
| t <sub>din</sub>     | 21             | Dedicated Input Delay                                 | –    | 0.5  | –    | 1.1  | ns    |
| GRP                  |                |                                                       |      |      |      |      |       |
| t <sub>grp</sub>     | 22             | GRP Delay                                             | –    | 0.2  | –    | 0.6  | ns    |
| GLB                  |                |                                                       |      |      |      |      |       |
| t <sub>4ptbpc</sub>  | 23             | 4 Product Term Bypass Path Delay (Combinatorial)      | –    | 1.5  | –    | 1.9  | ns    |
| t <sub>4ptbpr</sub>  | 24             | 4 Product Term Bypass Path Delay (Registered)         | –    | 2.2  | –    | 2.4  | ns    |
| t <sub>1ptxor</sub>  | 25             | 1 Product Term/XOR Path Delay                         | –    | 3.2  | –    | 3.4  | ns    |
| t <sub>20ptxor</sub> | 26             | 20 Product Term/XOR Path Delay                        | –    | 3.2  | –    | 3.4  | ns    |
| t <sub>xoradj</sub>  | 27             | XOR Adjacent Path Delay <sup>3</sup>                  | –    | 3.2  | –    | 3.4  | ns    |
| t <sub>gbp</sub>     | 28             | GLB Register Bypass Delay                             | –    | 0.0  | –    | 0.0  | ns    |
| t <sub>gsu</sub>     | 29             | GLB Register Setup Time before Clock                  | 0.7  | –    | 1.2  | –    | ns    |
| t <sub>gh</sub>      | 30             | GLB Register Hold Time after Clock                    | 1.8  | –    | 2.3  | –    | ns    |
| t <sub>gco</sub>     | 31             | GLB Register Clock to Output Delay                    | –    | 0.3  | –    | 0.3  | ns    |
| t <sub>gro</sub>     | 32             | GLB Register Reset to Output Delay                    | –    | 0.3  | –    | 0.6  | ns    |
| t <sub>ptre</sub>    | 33             | GLB Product Term Reset to Register Delay              | –    | 4.0  | –    | 4.3  | ns    |
| t <sub>ptoe</sub>    | 34             | GLB Product Term Output Enable to I/O Cell Delay      | –    | 2.9  | –    | 5.9  | ns    |
| t <sub>ptck</sub>    | 35             | GLB Product Term Clock Delay                          | 0.8  | 3.2  | 1.0  | 4.0  | ns    |
| ORP                  |                |                                                       |      |      |      |      |       |
| t <sub>orp</sub>     | 36             | ORP Delay                                             | –    | 0.9  | –    | 1.4  | ns    |
| t <sub>orpbp</sub>   | 37             | ORP Bypass Delay                                      | –    | 0.4  | –    | 0.4  | ns    |
| Outputs              |                |                                                       |      |      |      |      |       |
| t <sub>ob</sub>      | 38             | Output Buffer Delay                                   | –    | 1.6  | –    | 1.6  | ns    |
| t <sub>sl</sub>      | 39             | Output Slew Limited Delay Adder                       | –    | 2.0  | –    | 2.0  | ns    |
| t <sub>oen</sub>     | 40             | I/O Cell OE to Output Enabled                         | –    | 2.6  | –    | 3.0  | ns    |
| t <sub>odis</sub>    | 41             | I/O Cell OE to Output Disabled                        | –    | 2.6  | –    | 3.0  | ns    |
| t <sub>goe</sub>     | 42             | Global Output Enable                                  | –    | 1.9  | –    | 2.0  | ns    |
| Clocks               |                |                                                       |      |      |      |      |       |
| t <sub>gy0</sub>     | 43             | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 0.9  | 0.9  | 1.2  | 1.2  | ns    |
| t <sub>gy1/2</sub>   | 44             | Clock Delay, Y1 or Y2 to Global GLB Clock Line        | 1.1  | 1.1  | 1.4  | 1.4  | ns    |
| Global Reset         |                |                                                       |      |      |      |      |       |
| t <sub>gr</sub>      | 45             | Global Reset to GLB                                   | –    | 3.7  | –    | 4.4  | ns    |

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

Table 2-0036E/2192VE v0.1

## Internal Timing Parameters<sup>1</sup>

Over Recommended Operating Conditions

| PARAMETER            | # <sup>2</sup> | DESCRIPTION                                           | -135 |      | -100 |      | UNITS |
|----------------------|----------------|-------------------------------------------------------|------|------|------|------|-------|
|                      |                |                                                       | MIN. | MAX. | MIN. | MAX. |       |
| Inputs               |                |                                                       |      |      |      |      |       |
| t <sub>io</sub>      | 20             | Input Buffer Delay                                    | –    | 0.5  | –    | 0.7  | ns    |
| t <sub>din</sub>     | 21             | Dedicated Input Delay                                 | –    | 1.7  | –    | 2.5  | ns    |
| GRP                  |                |                                                       |      |      |      |      |       |
| t <sub>grp</sub>     | 22             | GRP Delay                                             | –    | 1.2  | –    | 1.8  | ns    |
| GLB                  |                |                                                       |      |      |      |      |       |
| t <sub>4ptbpc</sub>  | 23             | 4 Product Term Bypass Path Delay (Combinatorial)      | –    | 3.7  | –    | 5.2  | ns    |
| t <sub>4ptbpr</sub>  | 24             | 4 Product Term Bypass Path Delay (Registered)         | –    | 3.7  | –    | 4.7  | ns    |
| t <sub>1ptxor</sub>  | 25             | 1 Product Term/XOR Path Delay                         | –    | 4.7  | –    | 6.2  | ns    |
| t <sub>20ptxor</sub> | 26             | 20 Product Term/XOR Path Delay                        | –    | 4.7  | –    | 6.2  | ns    |
| t <sub>xoradj</sub>  | 27             | XOR Adjacent Path Delay <sup>3</sup>                  | –    | 4.7  | –    | 6.2  | ns    |
| t <sub>gbp</sub>     | 28             | GLB Register Bypass Delay                             | –    | 0.5  | –    | 1.0  | ns    |
| t <sub>gsu</sub>     | 29             | GLB Register Setup Time before Clock                  | 1.2  | –    | 1.7  | –    | ns    |
| t <sub>gh</sub>      | 30             | GLB Register Hold Time after Clock                    | 3.8  | –    | 4.8  | –    | ns    |
| t <sub>gco</sub>     | 31             | GLB Register Clock to Output Delay                    | –    | 0.3  | –    | 0.3  | ns    |
| t <sub>gro</sub>     | 32             | GLB Register Reset to Output Delay                    | –    | 1.1  | –    | 3.1  | ns    |
| t <sub>ptre</sub>    | 33             | GLB Product Term Reset to Register Delay              | –    | 6.1  | –    | 7.1  | ns    |
| t <sub>ptoe</sub>    | 34             | GLB Product Term Output Enable to I/O Cell Delay      | –    | 6.9  | –    | 9.1  | ns    |
| t <sub>ptck</sub>    | 35             | GLB Product Term Clock Delay                          | 1.6  | 4.6  | 2.6  | 5.6  | ns    |
| ORP                  |                |                                                       |      |      |      |      |       |
| t <sub>orp</sub>     | 36             | ORP Delay                                             | –    | 1.5  | –    | 1.7  | ns    |
| t <sub>orpbp</sub>   | 37             | ORP Bypass Delay                                      | –    | 0.5  | –    | 0.7  | ns    |
| Outputs              |                |                                                       |      |      |      |      |       |
| t <sub>ob</sub>      | 38             | Output Buffer Delay                                   | –    | 1.6  | –    | 1.6  | ns    |
| t <sub>sl</sub>      | 39             | Output Slew Limited Delay Adder                       | –    | 2.0  | –    | 2.0  | ns    |
| t <sub>oen</sub>     | 40             | I/O Cell OE to Output Enabled                         | –    | 3.4  | –    | 3.4  | ns    |
| t <sub>odis</sub>    | 41             | I/O Cell OE to Output Disabled                        | –    | 3.4  | –    | 3.4  | ns    |
| t <sub>goe</sub>     | 42             | Global Output Enable                                  | –    | 3.6  | –    | 5.6  | ns    |
| Clocks               |                |                                                       |      |      |      |      |       |
| t <sub>gy0</sub>     | 43             | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 1.6  | 1.6  | 2.4  | 2.4  | ns    |
| t <sub>gy1/2</sub>   | 44             | Clock Delay, Y1 or Y2 to Global GLB Clock Line        | 1.8  | 1.8  | 2.6  | 2.6  | ns    |
| Global Reset         |                |                                                       |      |      |      |      |       |
| t <sub>gr</sub>      | 45             | Global Reset to GLB                                   | –    | 5.8  | –    | 7.1  | ns    |

1. Internal Timing Parameters are not tested and are for reference only.

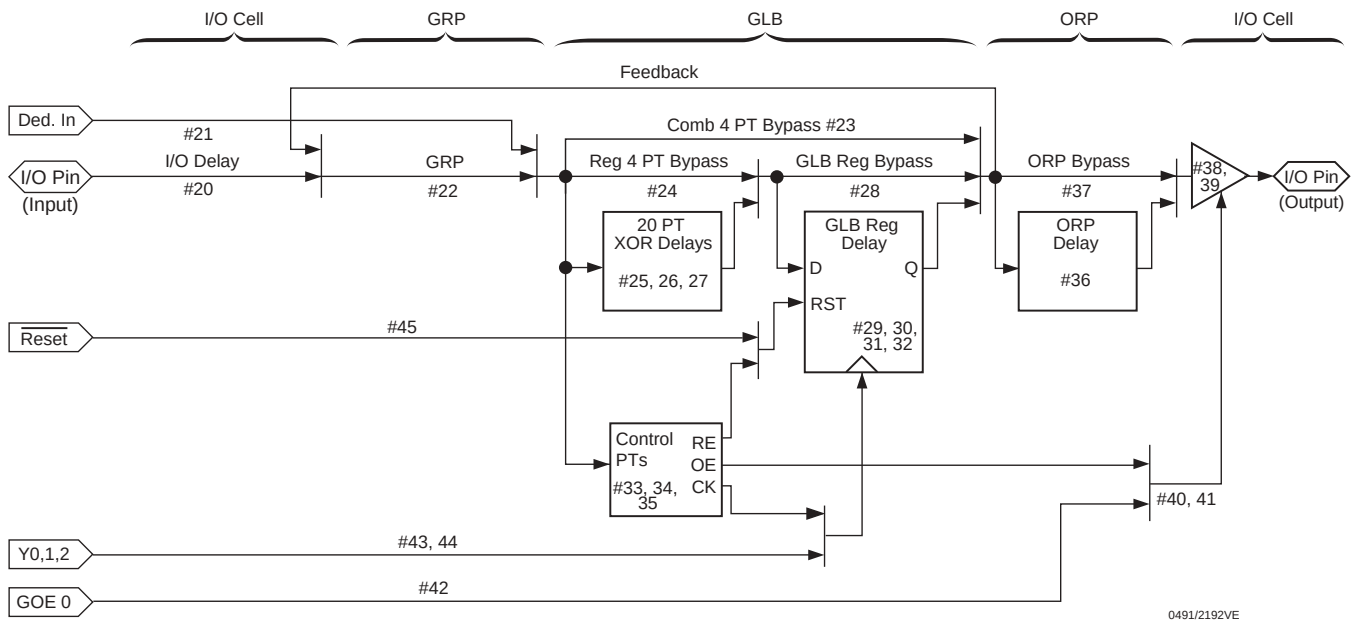
2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

Table 2-0036D/2192VE v0.1



## ispLSI 2192VE Timing Model



### Derivations of tsu, th and tco from the Product Term Clock

$$\begin{aligned}
 \text{tsu} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\
 &= (\text{tio} + \text{tgrp} + \text{t20ptxor}) + (\text{tgsu}) - (\text{tio} + \text{tgrp} + \text{tptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 3.1\text{ns} &= (0.3 + 0.2 + 3.2) + (0.7) - (0.3 + 0.2 + 0.8) \\
 \text{th} &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\
 &= (\text{tio} + \text{tgrp} + \text{tptck(max)}) + (\text{tgh}) - (\text{tio} + \text{tgrp} + \text{t20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 1.8\text{ns} &= (0.3 + 0.2 + 3.2) + (1.8) - (0.3 + 0.2 + 3.2) \\
 \text{tco} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\
 &= (\text{tio} + \text{tgrp} + \text{tptck(max)}) + (\text{tgco}) + (\text{torp} + \text{tob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 6.5\text{ns} &= (0.3 + 0.2 + 3.2) + (0.3) + (0.9 + 1.6)
 \end{aligned}$$

Note: Calculations are based upon timing specifications for the ispLSI 2192VE-225L.

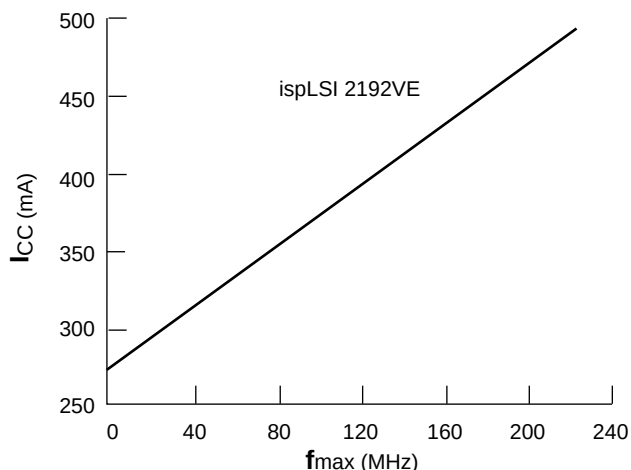
Table 2-0042A/2192VE v0.1

## Power Consumption

Power consumption in the ispLSI 2192VE device depends on two primary factors: the speed at which the device is operating and the number of Product Terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of twelve 16-bit counters  
Typical current at 3.3V, 25° C

ICC can be estimated for the ispLSI 2192VE using the following equation:

$$I_{CC} = 25 + (\# \text{ of PTs} * 0.670) + (\# \text{ of nets} * \text{max freq} * 0.0051)$$

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127/2192VE

## Signal Descriptions

| Signal Name     | Description                                                                                                                                                                                                    |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RESET           | Active Low (0) Reset pin resets all the registers in the device.                                                                                                                                               |
| GOE 0, GOE1     | Global Output Enable input pins.                                                                                                                                                                               |
| Y0, Y1, Y2      | Dedicated Clock Input – These clock inputs are connected to one of the clock inputs of all the GLBs in the device.                                                                                             |
| BSCAN           | Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.                              |
| TDI/IN 0        | Input – This pin performs two functions. When BSCAN is logic low, it functions as a serial data input pin to load programming data into the device. When BSCAN is high, it functions as a dedicated input pin. |
| TCK/IN 7        | Input – This pin performs two functions. When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. When BSCAN is high, it functions as a dedicated input pin.                  |
| TMS/IN 1        | Input – This pin performs two functions. When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. When BSCAN is high, it functions as a dedicated input pin.           |
| TDO/IN 6        | Output/Input – This pin performs two functions. When BSCAN is logic low, it functions as an output pin to read serial shift register data. When BSCAN is high, it functions as a dedicated input pin.          |
| IN 2-5, IN 8-11 | Dedicated Input Pins to the device.                                                                                                                                                                            |
| GND             | Ground (GND)                                                                                                                                                                                                   |
| VCC             | Vcc                                                                                                                                                                                                            |
| NC <sup>1</sup> | No Connect                                                                                                                                                                                                     |
| I/O             | Input/Output Pins – These are the general purpose I/O pins used by the logic array.                                                                                                                            |

1. NC pins are not to be connected to any active signals, VCC or GND.

## Signal Locations

| Signal Name     | 128-Pin TQFP                     | 144-Ball fpBGA                                                   |
|-----------------|----------------------------------|------------------------------------------------------------------|
| RESET           | 15                               | G4                                                               |
| GOE 0, GOE 1    | 80, 17                           | F12, G2                                                          |
| Y0, Y1, Y2      | 14, 83, 78                       | F3, F10, G11                                                     |
| BSCAN           | 19                               | F1                                                               |
| TDI/IN 0        | 20                               | G3                                                               |
| TMS/IN 1        | 48                               | J6                                                               |
| TDO/IN 6        | 112                              | C7                                                               |
| TCK/IN 7        | 77                               | G12                                                              |
| IN 2-5, IN 8-11 | —, 49, 82, —, 84, 113, 13, —     | M7, J7, F9, G10, E12, B6, F2, E1                                 |
| GND             | 18, 34, 50, 63, 79, 98, 111, 127 | A1, A12, D4, D9, E5, E8, F6, F7, G6, G7, H5, H8, J4, J9, M1, M12 |
| VCC             | 2, 16, 31, 47, 66, 81, 95, 114   | B1, B12, E6, E7, F5, F8, G5, G8, H6, H7, L1, L12                 |
| NC <sup>1</sup> | —                                | K2                                                               |

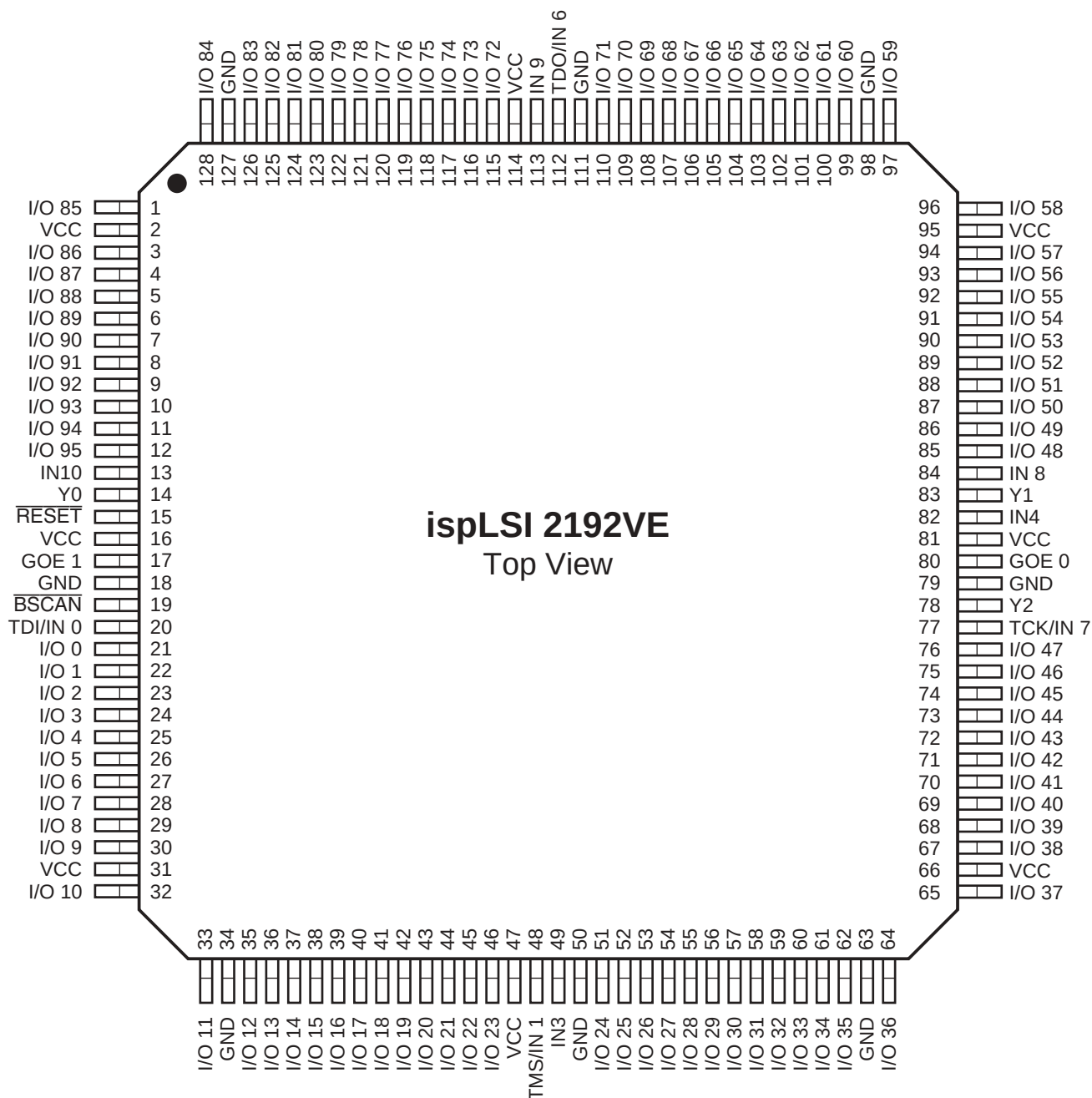
1. NC pins are not to be connected to any active signals, VCC or GND.

## I/O Locations

| Signal | 128<br>TQFP | 144<br>fpBGA | Signal | 128<br>TQFP | 144<br>fpBGA |
|--------|-------------|--------------|--------|-------------|--------------|
| I/O 0  | 21          | H4           | I/O 48 | 85          | F11          |
| I/O 1  | 22          | G1           | I/O 49 | 86          | D12          |
| I/O 2  | 23          | H2           | I/O 50 | 87          | E9           |
| I/O 3  | 24          | H1           | I/O 51 | 88          | E10          |
| I/O 4  | 25          | H3           | I/O 52 | 89          | E11          |
| I/O 5  | 26          | J1           | I/O 53 | 90          | C12          |
| I/O 6  | 27          | J3           | I/O 54 | 91          | D10          |
| I/O 7  | 28          | K1           | I/O 55 | 92          | D11          |
| I/O 8  | 29          | J2           | I/O 56 | 93          | B11          |
| I/O 9  | 30          | M2           | I/O 57 | 94          | C11          |
| I/O 10 | 32          | L2           | I/O 58 | 96          | C10          |
| I/O 11 | 33          | L3           | I/O 59 | 97          | A11          |
| I/O 12 | 35          | K3           | I/O 60 | 99          | B10          |
| I/O 13 | 36          | M3           | I/O 61 | 100         | A10          |
| I/O 14 | 37          | L4           | I/O 62 | 101         | C9           |
| I/O 15 | 38          | K4           | I/O 63 | 102         | B9           |
| I/O 16 | 39          | M4           | I/O 64 | 103         | A9           |
| I/O 17 | 40          | J5           | I/O 65 | 104         | D8           |
| I/O 18 | 41          | M5           | I/O 66 | 105         | B8           |
| I/O 19 | 42          | K5           | I/O 67 | 106         | C8           |
| I/O 20 | 43          | L5           | I/O 68 | 107         | A8           |
| I/O 21 | 44          | M6           | I/O 69 | 108         | B7           |
| I/O 22 | 45          | L6           | I/O 70 | 109         | A7           |
| I/O 23 | 46          | K6           | I/O 71 | 110         | D7           |
| I/O 24 | 51          | L7           | I/O 72 | 115         | C6           |
| I/O 25 | 52          | K7           | I/O 73 | 116         | A6           |
| I/O 26 | 53          | J8           | I/O 74 | 117         | D6           |
| I/O 27 | 54          | M8           | I/O 75 | 118         | B5           |
| I/O 28 | 55          | L8           | I/O 76 | 119         | C5           |
| I/O 29 | 56          | K8           | I/O 77 | 120         | A5           |
| I/O 30 | 57          | M9           | I/O 78 | 121         | D5           |
| I/O 31 | 58          | L9           | I/O 79 | 122         | C4           |
| I/O 32 | 59          | K9           | I/O 80 | 123         | B4           |
| I/O 33 | 60          | M10          | I/O 81 | 124         | A4           |
| I/O 34 | 61          | L10          | I/O 82 | 125         | C3           |
| I/O 35 | 62          | M11          | I/O 83 | 126         | B3           |
| I/O 36 | 64          | K10          | I/O 84 | 128         | A3           |
| I/O 37 | 65          | K11          | I/O 85 | 1           | C2           |
| I/O 38 | 67          | L11          | I/O 86 | 3           | B2           |
| I/O 39 | 68          | K12          | I/O 87 | 4           | D2           |
| I/O 40 | 69          | J11          | I/O 88 | 5           | A2           |
| I/O 41 | 70          | J12          | I/O 89 | 6           | D3           |
| I/O 42 | 71          | J10          | I/O 90 | 7           | E2           |
| I/O 43 | 72          | H9           | I/O 91 | 8           | C1           |
| I/O 44 | 73          | H11          | I/O 92 | 9           | E3           |
| I/O 45 | 74          | H12          | I/O 93 | 10          | E4           |
| I/O 46 | 75          | H10          | I/O 94 | 11          | D1           |
| I/O 47 | 76          | G9           | I/O 95 | 12          | F4           |

**Pin Configuration**

ispLSI 2192VE 128-Pin TQFP Pinout Diagram



0124-2192VE

## Signal Configuration

### ispLSI 2192VE 144-Ball fpBGA Signal Diagram

|   | 12           | 11     | 10     | 9      | 8      | 7            | 6            | 5      | 4      | 3            | 2               | 1      |   |
|---|--------------|--------|--------|--------|--------|--------------|--------------|--------|--------|--------------|-----------------|--------|---|
| A | GND          | I/O 59 | I/O 61 | I/O 64 | I/O 68 | I/O 70       | I/O 73       | I/O 77 | I/O 81 | I/O 84       | I/O 88          | GND    | A |
| B | VCC          | I/O 56 | I/O 60 | I/O 63 | I/O 66 | I/O 69       | IN 9         | I/O 75 | I/O 80 | I/O 83       | I/O 86          | VCC    | B |
| C | I/O 53       | I/O 57 | I/O 58 | I/O 62 | I/O 67 | TDO/<br>IN 6 | I/O 72       | I/O 76 | I/O 79 | I/O 82       | I/O 85          | I/O 91 | C |
| D | I/O 49       | I/O 55 | I/O 54 | GND    | I/O 65 | I/O 71       | I/O 74       | I/O 78 | GND    | I/O 89       | I/O 87          | I/O 94 | D |
| E | IN 8         | I/O 52 | I/O 51 | I/O 50 | GND    | VCC          | VCC          | GND    | I/O 93 | I/O 92       | I/O 90          | IN 11  | E |
| F | GOE 0        | I/O 48 | Y1     | IN 4   | VCC    | GND          | GND          | VCC    | I/O 95 | Y0           | IN 10           | BSCAN  | F |
| G | TCK/<br>IN 7 | Y2     | IN 5   | I/O 47 | VCC    | GND          | GND          | VCC    | RESET  | TDI/<br>IN 0 | GOE 1           | I/O 1  | G |
| H | I/O 45       | I/O 44 | I/O 46 | I/O 43 | GND    | VCC          | VCC          | GND    | I/O 0  | I/O 4        | I/O 2           | I/O 3  | H |
| J | I/O 41       | I/O 40 | I/O 42 | GND    | I/O 26 | IN 3         | TMS/<br>IN 1 | I/O 17 | GND    | I/O 6        | I/O 8           | I/O 5  | J |
| K | I/O 39       | I/O 37 | I/O 36 | I/O 32 | I/O 29 | I/O 25       | I/O 23       | I/O 19 | I/O 15 | I/O 12       | NC <sup>1</sup> | I/O 7  | K |
| L | VCC          | I/O 38 | I/O 34 | I/O 31 | I/O 28 | I/O 24       | I/O 22       | I/O 20 | I/O 14 | I/O 11       | I/O 10          | VCC    | L |
| M | GND          | I/O 35 | I/O 33 | I/O 30 | I/O 27 | IN 2         | I/O 21       | I/O 18 | I/O 16 | I/O 13       | I/O 9           | GND    | M |
|   | 12           | 11     | 10     | 9      | 8      | 7            | 6            | 5      | 4      | 3            | 2               | 1      |   |

144-BGA/2192VE

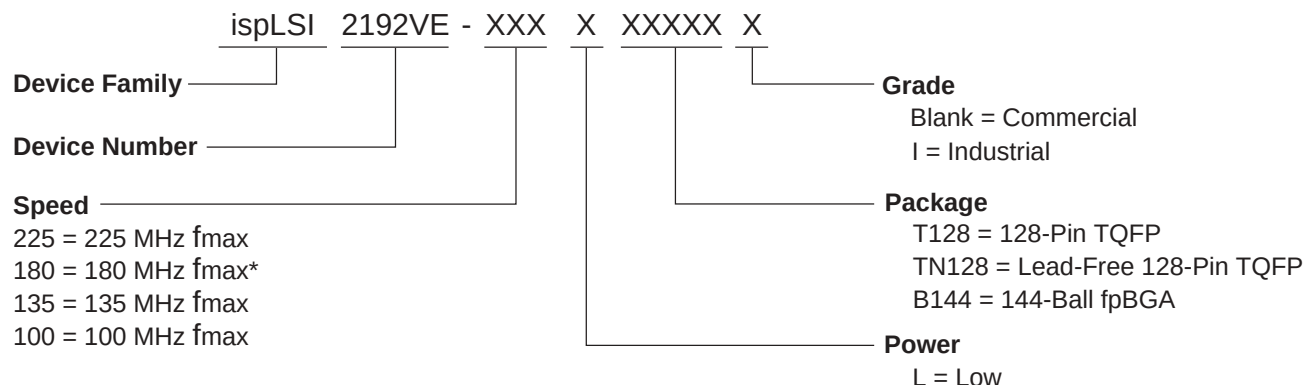
### ispLSI 2192VE

Bottom View

<sup>1</sup>NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

## Part Number Description



\*ispLSI 2192VE-225 recommended for new designs.

0212B/2192VE

## ispLSI 2192VE Ordering Information

### Conventional Packaging

#### COMMERCIAL

| FAMILY | f <sub>max</sub> (MHz) | tpd (ns) | ORDERING NUMBER         | PACKAGE        |
|--------|------------------------|----------|-------------------------|----------------|
| ispLSI | 225                    | 4.0      | ispLSI 2192VE-225LT128  | 128-Pin TQFP   |
|        | 225                    | 4.0      | ispLSI 2192VE-225LB144  | 144-Ball fpBGA |
|        | 180                    | 5.0      | ispLSI 2192VE-180LT128* | 128-Pin TQFP   |
|        | 180                    | 5.0      | ispLSI 2192VE-180LB144* | 144-Ball fpBGA |
|        | 135                    | 7.5      | ispLSI 2192VE-135LT128  | 128-Pin TQFP   |
|        | 135                    | 7.5      | ispLSI 2192VE-135LB144  | 144-Ball fpBGA |
|        | 100                    | 10       | ispLSI 2192VE-100LT128  | 128-Pin TQFP   |
|        | 100                    | 10       | ispLSI 2192VE-100LB144  | 144-Ball fpBGA |

\*ispLSI 2192VE-225 recommended for new designs.

Table 2-0041D/2192VE

#### INDUSTRIAL

| FAMILY | f <sub>max</sub> (MHz) | tpd (ns) | ORDERING NUMBER         | PACKAGE      |
|--------|------------------------|----------|-------------------------|--------------|
| ispLSI | 180                    | 5.0      | ispLSI 2192VE-180LT128I | 128-Pin TQFP |

Table 2-0041A/2192VE

### Lead-Free Packaging

#### COMMERCIAL

| FAMILY | f <sub>max</sub> (MHz) | tpd (ns) | ORDERING NUMBER         | PACKAGE                |
|--------|------------------------|----------|-------------------------|------------------------|
| ispLSI | 225                    | 4.0      | ispLSI 2192VE-225LTN128 | Lead-Free 128-Pin TQFP |
|        | 135                    | 7.5      | ispLSI 2192VE-135LTN128 | Lead-Free 128-Pin TQFP |
|        | 100                    | 10       | ispLSI 2192VE-100LTN128 | Lead-Free 128-Pin TQFP |

#### INDUSTRIAL

| FAMILY | f <sub>max</sub> (MHz) | tpd (ns) | ORDERING NUMBER          | PACKAGE                |
|--------|------------------------|----------|--------------------------|------------------------|
| ispLSI | 180                    | 7.5      | ispLSI 2192VE-180LTN128I | Lead-Free 128-Pin TQFP |

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