# KSZ8873MLL/FLL/RLL

## Integrated 3-Port 10/100 Managed Switch with PHYs

Revision 1.6

## General Description

The KSZ8873MLL/FLL/RLL are highly-integrated 3-port switches on a chip ICs in the industry's smallest footprint. They are designed to enable a new generation of low port count, cost-sensitive, and power-efficient 10/100Mbps switch systems. Low power consumption, advanced power management and sophisticated QoS features (e.g., IPv6 priority classification support) make these devices ideal for IPTV, IP-STB, VoIP, automotive, and industrial applications.

The KSZ8873 family is designed to support the GREEN requirement in today's switch systems. Advanced power management schemes include hardware power down, software power down, per port power down and the energy detect mode that shuts downs the transceiver when a port is idle.

KSZ8873MLL/FLL/RLL also offers a by-pass mode. In this mode, the processor connected to the switch through the MII interface can be shut down without impacting the normal switch operation.

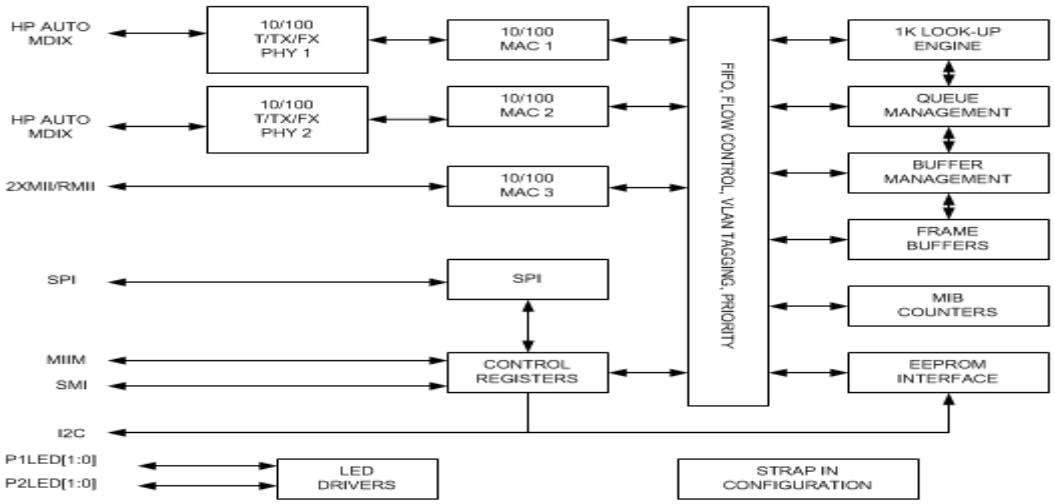
The configurations provided by the KSZ8873 family enables the flexibility to meet requirements of different applications:

- KSZ8873MLL: Two 10/100BASE-T/TX transceivers and one MII interface.
- KSZ8873RLL: Two 10/100BASE-T/TX transceivers and one RMII interface.
- KSZ8873FLL: Two 100BASE-FX transceivers and one MII interface.

The device is available in RoHS-compliant 64-pin LQFP package. Industrial-grade and qualified AEC-Q100 Automotive-grade version are also available (see *Ordering Information* section)

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

## Functional Diagram



## Features

### Advanced Switch Features

- IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN IDs)
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
- Programmable rate limiting at the ingress and egress on a per port basis
- Broadcast storm protection with % control (global and per port basis)
- IEEE 802.1d rapid spanning tree protocol support
- tail tag mode (1 byte added before FCS) support at port3 to inform the processor which ingress port receives the packet and its priority
- Bypass feature which Automatically sustains the switch function between Port1 and Port2 when CPU (Port 3 interface) goes to the sleep mode
- Self-address filtering
- Individual MAC address for port1 and port2
- Support RMII interface and 50 MHz reference clock output
- MAC MII interface supports both MAC mode and PHY mode
- IGMP snooping (Ipv4) support for multicast packet Filtering
- IPv4/IPv6 QoS support.
- MAC filtering function to forward unknown unicast packets to specified port

### Comprehensive Configuration Register Access

- Serial management interface (SMI) to all internal registers
- MII management (MIIM) interface to PHY registers
- High speed SPI and $I^2C$ Interface to all internal registers
- I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)

### QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based
- Re-mapping of 802.1p priority field per port basis Four priority levels

### Proven Integrated 3-Port 10/100 Ethernet Switch

- 3rd generation switch with three MACs and two
- PHYs fully compliant with IEEE 802.3u standard
- Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC address lookup table and a store-and-forward architecture
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option
- Half-duplex back pressure flow control
- HP Auto MDI-X for reliable detection of and correction for straight-through and crossover cables with disable and enable option
- Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling on Port 2
- Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed
- HBM ESD Rating 3kV

### Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
- MIB counters for fully compliant statistics gathering 34 MIB counters per port
- Loopback modes for remote diagnostic of failure

### Low Power Dissipation:

- Full-chip hardware power-down (register configuration not saved)
- Full-chip software power-down (register configuration not saved)
- Energy-detect mode support
- Dynamic clock tree shutdown feature
- Per port based software power-save on PHY (idle link detection, register configuration preserved)
- Voltages: Single 3.3V supply with internal 1.8V LDO for 3.3V VDDIO
- Optional 3.3V, 2.5V and 1.8V for VDDIO
- Transceiver power 3.3V for VDDA_3.3

**Industrial Temperature Range: –40°C to +85°C**

**Available in 64-Pin LQFP, Lead-Free package**

## Applications

- VoIP phone
- Set-top/game box
- Automotive Ethernet
- Industrial control
- IPTV POF
- SOHO residential gateway
- Broadband gateway/firewall/VPN
- Integrated DSL/cable modem
- Wireless LAN access point + gateway
- Standalone 10/100 switch

## Ordering Information

| Part Number | Temperature Range | Package | Lead Finish/Grade |
|---|---|---|---|
| KSZ8873MLL | 0°C to 70°C | 64-Pin LQFP | Pb-Free/Commercial |
| KSZ8873MLLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free/Industrial |
| KSZ8873MLL AM | –40°C to +85°C | 64-Pin LQFP | Pb-Free/Automotive grade 3 |
| KSZ8873FLL | 0°C to 70°C | 64-Pin LQFP | Pb-Free/Commercial |
| KSZ8873FLLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free/Industrial |
| KSZ8873RLL | 0°C to 70°C | 64-Pin LQFP | Pb-Free/Commercial |
| KSZ8873RLLI | –40°C to +85°C | 64-Pin LQFP | Pb-Free/Industrial |
| KSZ8873RLLU | –40°C to +85°C | 64-Pin LQFP | Pb-Free/Automotive grade 3 |

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.0 | 03/25/08 | Initial release |
| 1.1 | 06/26/09 | Combined Register Description to initial release. |
| 1.2 | 09/08/09 | Removed LinkMD feature.<br>Updated the Electrical Characteristics. |
| | 09/23/09 | Added LinkMD feature on Port 2.<br>Fixed the typo on Register 194 |
| | 10/01/09 | Modified Pin 31(SMRXD31) description. |
| 1.3 | 08/10/10 | Removed Turbo MII feature and its timing, add MDC/MDIO timing, update the descriptions of the by-pass mode, tag insertion, power management, pins, registers, and so on. Update max rating, RMII timing and electrical characteristics. |
| 1.4 | 05/25/11 | Updated Register 6 with strap pins description, Junction Thermal and so on. Added the descriptions of the registers from Registers 175-186. Added a note for port register control 12, updated the description for some registers, updated reset timing diagram. |
| 1.5 | 07/28/11 | Updated description for MDC/MDIO SMI mode and IGMP mode. ESD rating updated to 3kV. Update data of lead temperature. |
| | 11/01/11 | Correct typo error in ordering information table. |
| | 11/15/11 | Correct typo error for MDI-X status in the PHY Register 31. |
| 1.6 | 04/11/13 | Add or update the notes for Pin SCRS3 description, the port register control 0 bit 2 and the port register control 5 bit 7. Update the operation voltage Min/Max for different VDDIO. Update the pin description for Pin 30 and Pin 33. Change TTL I/O to CMOS I/O. Update the Register 166 description and the default value. Add KSZ8873RLLU Automotive device in order information Table. Add a note for Register 195 bits [5:4]. |

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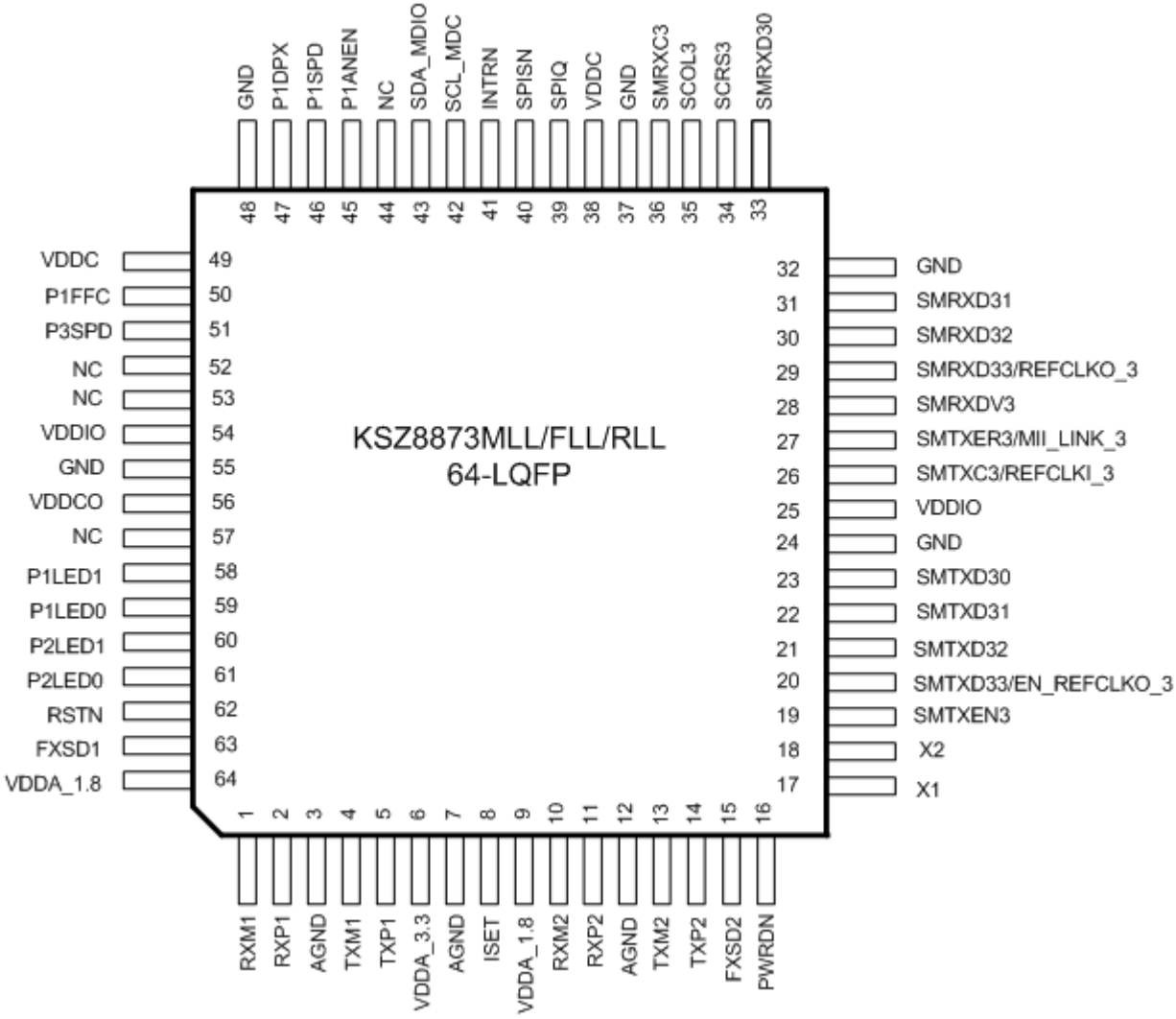
## Pin Configuration




**64-Pin LQFP**
**(Top View)**

## Pin Description and I/O Assignment

| Pin Number | Pin Name | Type (1) | Description |
|---|---|---|---|
| 1 | RXM1 | I/O | Physical receive or transmit signal (– differential) |
| 2 | RXP1 | I/O | Physical receive or transmit signal (+ differential) |
| 3 | AGND | GND | Analog ground |
| 4 | TXM1 | I/O | Physical transmit or receive signal (– differential) |
| 5 | TXP1 | I/O | Physical transmit or receive signal (+ differential) |
| 6 | VDDA_3.3 | P | 3.3V analog $V_{DD}$ |
| 7 | AGND | GND | Analog ground. |
| 8 | ISET | O | Set physical transmit output current.<br>Pull-down this pin with an 11.8K 1% resistor to ground. |
| 9 | VDDA_1.8 | P | 1.8V analog core power input from VDDCO (Pin 56). |
| 10 | RXM2 | I/O | Physical receive or transmit signal (– differential) |
| 11 | RXP2 | I/O | Physical receive or transmit signal (+ differential) |
| 12 | AGND | GND | Analog ground. |
| 13 | TXM2 | I/O | Physical transmit or receive signal (– differential) |
| 14 | TXP2 | I/O | Physical transmit or receive signal (+ differential) |
| 15 | FXSD2 | I | MLL/RLL: connect to analog ground by pull-down resistor.<br>FLL: Fiber signal detect / factory test pin |
| 16 | PWRND | Ipu | Chip power down input (active low). |
| 17 | X1 | I | 25MHz or 50MHz crystal/oscillator clock connections.<br>Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect.<br>Note: Clock is ± 50ppm for crystal and oscillator, the clock should be applied to X1 pin before reset voltage goes high. |
| 18 | X2 | O | |
| 19 | SMTXEN3 | Ipu | Switch MII transmit enable |
| 20 | SMTXD33/<br>EN_REFCLKO_3 | Ipu/I | MLL/FLL: Switch MII transmit data bit 3<br>RLL: **Strap option**: RMII mode Clock selection<br>PU = Enable REFCLKO_3 output<br>PD = Disable REFCLKO_3 output |
| 21 | SMTXD32/<br>NC | Ipu | MLL/FLL: Switch MII transmit data bit 2<br>RLL: No connection |
| 22 | SMTXD31 | Ipu | Switch MII/RMII transmit data bit 1 |
| 23 | SMTXD30 | Ipu | Switch MII/RMII transmit data bit 0 |
| 24 | GND | GND | Digital ground |
| 25 | VDDIO | P | 3.3V, 2.5V or 1.8V digital VDD input power supply for IO with well decoupling capacitors. |

## Pin Description and I/O Assignment (Continued)

| Pin Number | Pin Name | Type (1) | Description |
|---|---|---|---|
| 26 | SMTXC3/<br>REFCLKI_3 | I/O | MLL/FLL: Switch MII transmit clock (MII modes only)<br>Output in PHY MII mode and SNI mode<br>Input in MAC MII and RMII mode.<br>RLL: Reference clock input<br>Note: pull-down by resistor is needed if internal reference clock is used in RLL by register 198 bit 3. |
| 27 | SMTXER3/<br>MII_LINK_3 | Ipd | Switch MII transmit error in MII mode<br>0= MII link indicator from host in MII PHY mode.<br>1= No link on port 3 MII PHY mode and enable By-pass mode. |
| 28 | SMRXDV3 | Ipu/O | Switch MII receive data valid<br>**Strap option**: MII mode selection<br>PU = PHY mode.<br>PD = MAC mode (In MAC mode, port 3 MII has to connect a powered active external PHY for the normal operation) |
| 29 | SMRXD33/<br>REFCLKO_3 | Ipu/O | MLL/FLL: Switch MII receive data bit 3<br>RLL: Output reference clock in RMII mode.<br>**Strap option**: enable auto-negotiation on port 2 (P2ANEN)<br>PU = enable P2ANEN<br>PD = disable P2ANEN |
| 30 | SMRXD32 | Ipu/O | Switch MII receive data bit 2<br>**Strap option**: Force the speed on port 2<br>PU = force port 2 to 100BT if P2ANEN = 0<br>PD = force port 2 to 10BT if P2ANEN = 0 |
| 31 | SMRXD31 | Ipu/O | Switch MII/RMII receive data bit 1<br>**Strap option**: Force duplex mode (P2DPX)<br>PU = port 2 default to full duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0.<br>PD = Port 2 set to half duplex mode if P2ANEN = 1 and auto-negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0. |
| 32 | GND | Gnd | Digital ground |
| 33 | SMRXD30 | Ipu/O | Switch MII/RMII receive data bit 0<br>**Strap option**: Force flow control on port 2 (P2FFC)<br>PU = always enable (force) port 2 flow control feature, regardless of Auto-Negotiation result.<br>PD = port 2 flow control is enabled by auto- negotiation result. |
| 34 | SCRS3/<br>NC | Ipu/O | MLL/FLL: Switch MII carrier sense<br>RLL: No connection, Internal pull up.<br>Note: For MLL/FLL part, when chip is configured as MAC mode, this pin should be driven from CRS pin of PHY or from CRS pin of FPGA with a logic of (TXEN \| RXDV). If only full duplex is used, then this pin should be pull-down by 1K resister. |

## Pin Description and I/O Assignment (Continued)

| Pin Number | Pin Name | Type (1) | Description |
|---|---|---|---|
| 35 | SCOL3/<br>NC | Ipu/O | MLL/FLL: Switch MII collision detect<br>RLL: No connection, Internal pull up. |
| 36 | SMRXC3/<br>NC | I/O | MLL/FLL: Switch MII receive clock.<br>Output in PHY MII mode<br>Input in MAC MII mode<br>RLL: No Connection. |
| 37 | GND | Gnd | Digital ground |
| 38 | VDDC | P | 1.8V digital core power input from VDDCO (Pin 56). |
| 39 | SPIQ | Ipu/O | SPI slave mode: serial data output<br>Note: an external pull-up is needed on this pin when it is in use.<br>Strap option: XCLK Frequency Selection<br>PU = 25 MHz<br>PD = 50 MHz |
| 40 | SPISN | Ipu | SPI slave mode: chip select (active low)<br>When SPISN is high, the KSZ8873MLL/FLL/RLL is deselected and SPIQ is held in high impedance state.<br>A high-to-low transition is used to initiate SPI data transfer.<br>Note: an external pull-up is needed on this pin when it is in use. |
| 41 | INTRN | Opu | Interrupt<br>Active Low signal to host CPU to indicate an interrupt status bit is set when lost link. Refer to Register 187 and 188. |
| 42 | SCL_MDC | I/O | SPI slave mode / $I^2C$ slave mode: clock input<br>$I^2C$ master mode: clock output<br>MIIM clock input |
| 43 | SDA_MDIO | Ipu/O | SPI slave mode: serial data input<br>$I^2C$ master/slave mode: serial data input/output<br>MIIM: data input/out<br>Note: an external pull-up is needed on this pin when it is in use. |
| 44 | NC | NC | Unused pin, only this NC pin can be pulled down by a pull-down resistor for better EMI. |
| 45 | P1ANEN | Ipu/O | PU = enable auto-negotiation on port 1<br>PD = disable auto-negotiation on port 1 |
| 46 | P1SPD | Ipu/O | PU = force port 1 to 100BT if P1ANEN = 0<br>PD = force port 1 to 10BT if P1ANEN = 0 |
| 47 | P1DPX | Ipu/O | PU = port 1 default to full duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in full-duplex mode if P1ANEN = 0.<br>PD = port 1 default to half duplex mode if P1ANEN = 1 and auto- negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0. |
| 48 | GND | GND | Digital ground |

## Pin Description and I/O Assignment (Continued)

| Pin Number | Pin Name | Type (1) | Description |
|---|---|---|---|
| 49 | VDDC | P | 1.8V digital core power input from VDDCO (Pin 56). |
| 50 | P1FFC | Ipu/O | PU = always enable (force) port 1 flow control feature<br>PD = port 1 flow control feature enable is determined by auto negotiation result. |
| 51 | P3SPD | Ipd/O | PU = force port 3 to 10BT<br>PD = force port 3 to 100BT (default) |
| 52 | NC | NC | Unused pin. No external connection. |
| 53 | NC | NC | Unused pin. No external connection. |
| 54 | VDDIO | P | 3.3V, 2.5V or 1.8V digital VDD input power supply for IO with well decoupling capacitors. |
| 55 | GND | GND | Digital ground |
| 56 | VDDCO | P | 1.8V core power voltage output (internal 1.8V LDO regulator output), this 1.8V output pin provides power to both VDDA_1.8 and VDDC input pins.<br>Note: Internally 1.8V LDO regulator input comes from VDDIO. Do not connect an external power supply to VDDCO pin. The ferrite bead is requested between analog and digital 1.8V core power. |
| 57 | NC | NC | Unused pin. No external connection. |
| 58 | P1LED1 | Ipu/O | **Port 1 LED Indicators**: Default: Speed (refer to Register 195 bit[5:4])<br>**Strap option**: Port 3 flow control selection(P3FFC)<br>PU = always enable (force) port 3 flow control feature (default)<br>PD = disable |
| 59 | P1LED0 | Ipd/O | **Port 1 LED Indicators**: Default: Link/Act. (refer to Register 195 bit[5:4])<br>**Strap option**: Port 3 duplex mode selection(P3DPX)<br>PU = port 3 to half duplex mode<br>PD = port 3 to full duplex mode (default)<br>Note: P1LED0 has weaker internal pull-down, recommend an external pull-down by a 0.5KΩ resistor. |

## Pin Description and I/O Assignment (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (1)</th><th>Description</th></tr>
<tr><td>60</td><td>P2LED1</td><td>Ipu/O</td><td>
Port 2 LED Indicators:<br>
Default: Speed (refer to Register 195 bit[5:4])<br>
Strap option: Serial bus configuration<br>
Port 2 LED Indicators:<br>
Default: Link/Act. (refer to Register 195 bit[5:4])<br>
Strap option: Serial bus configuration<br>
Serial bus configuration pins to select mode of access to KSZ8873MLL/FLL/RLL internal registers.<br>
[P2LED1, P2LED0] = [0, 0] — I$^2$C master (EEPROM) mode<br>
(If EEPROM is not detected, the KSZ8873MLL/FLL/RLL will be configured with the default values of its registers and the values of its strap-in pins.)
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
<tr><td>SCL_MDC</td><td>O</td><td>I$^2$C clock</td></tr>
<tr><td>SDA_MDIO</td><td>I/O</td><td>I$^2$C data I/O</td></tr>
<tr><td>SPISN</td><td>I</td><td>Not used</td></tr>
</table>
[P2LED1, P2LED0] = [0, 1] — I$^2$C slave mode<br>
The external I$^2$C master will drive the SCL_MDC clock.<br>
The KSZ8873MLL/FLL/RLL device addresses are:<br>
1011_1111 <read>; 1011_1110 <write>
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr>
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<tr><td>SDA_MDIO</td><td>I/O</td><td>I$^2$C data I/O</td></tr>
<tr><td>SPISN</td><td>I</td><td>Not used</td></tr>
</table>
[P2LED1, P2LED0] = [1, 0] — SPI slave mode
<table>
<tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr>
<tr><td>SPIQ</td><td>O</td><td>SPI data out</td></tr>
<tr><td>SCL_MDC</td><td>I</td><td>SPI clock</td></tr>
<tr><td>SDA_MDIO</td><td>I</td><td>SPI data In</td></tr>
<tr><td>SPISN</td><td>I</td><td>SPI chip select</td></tr>
</table>
[P2LED1, P2LED0] = [1, 1] – SMI/MIIM-mode<br>
In SMI mode, the KSZ8873MLL/FLL/RLL provides access to all its internal 8-bit registers through its SCL_MDC and SDA_MDIO pins.<br>
In MIIM mode, the KSZ8873MLL/FLL/RLL provides access to its 16-bit MIIM registers through its SDC_MDC and SDA_MDIO pins.
</td></tr>
<tr><td>61</td><td>P2LED0</td><td>Ipu/O</td><td></td></tr>
<tr><td>62</td><td>RSTN</td><td>Ipu</td><td>Hardware reset pin (active low)</td></tr>
</table>

## Pin Description and I/O Assignment (Continued)

| Pin Number | Pin Name | Type [1] | Description |
|---|---|---|---|
| 63 | FXSD1 | I | MLL/RLL: connect to analog ground by pull-down resistor.<br>FLL: Fiber signal detect |
| 64 | VDDA_1.8 | P | 1.8 analog VDD input power supply from VDDCO (Pin 56) through external Ferrite bead and capacitors. |

**Notes:**

1. Speed : Low (100BASE-TX), High (10BASE-T)
   Full duplex : Low (full duplex), High (half duplex)
   Act : Toggle (transmit / receive activity)
   Link : Low (link), High (no link)
2. P = Power supply.
   GND = Ground.
   I = Input.
   Ipu/O = Input with internal pull-up during reset, output pin otherwise.
   Ipu = Input w/ internal pull-up.
   Ipd = Input w/ internal pull-down.
   Opu = Output w/ internal pull-up.
   Opd = Output w/ internal pull-down.

## Functional Description

The KSZ8873MLL/FLL/RLL contains two 10/100 physical layer transceivers and three MAC units with an integrated Layer 2 managed switch.

The KSZ8873MLL/FLL/RLL has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KSZ8873MLL/FLL/RLL via the SMI interface, MIIM interface, SPI bus, or $I^2C$ bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KSZ8873MLL/FLL/RLL supports IEEE 802.3 10BASE-T and 100BASE-TX on both PHY ports. Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

## Functional Overview: Physical Layer Transceiver

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 11.8KΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

### 100BASE-TX Transmit

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

### PLL Clock Synthesizer

The KSZ8873MLL/FLL/RLL generates 125MHz, 62.5MHz, and 31.25MHz clocks for system timing. Internal clocks are generated from an external 25MHz or 50MHz crystal or oscillator. KSZ8873RLL can generate a 50MHz reference clock for the RMII interface.

### Scrambler/De-Scrambler (100BASE-TX Only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

### 100BASE-FX Operation

100BASE-FX operation is similar to 100BASE-TX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In addition, auto-negotiation is bypassed and auto MDI/MDI-X is disabled.

### 100BASE-FX Signal Detection

In 100BASE-FX operation, FXSD (fiber signal detect), input Pins 15 and 63, is usually connected to the fiber transceiver SD (signal detect) output pin. The fiber signal threshold can be selected by Register 192 bit 7 and 6 respectively for port 2 and port 1, When FXSD is less than the threshold, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD is over the threshold, the fiber signal is detected.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD input pin is tied high to force 100BASE-FX mode.

100BASE-FX signal detection is summarized in Table 1:

**Table 1. FX Signal Threshold**

| Register 192 bit 7 (port 2), bit 6 (port 1) | Fiber Signal Threshold at FXSD |
|---|---|
| 1 | 2.0V |
| 0 | 1.2V |

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD pin's input voltage threshold.

### 100BASE-FX Far-End Fault

A far-end fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KSZ8873FLL detects a FEF when its FXSD input is Fiber Signal Threshold. When a FEF is detected, the KSZ8873FLL signals its fiber link partner that a FEF has occurred by sending 84 1's followed by a zero in the idle period between frames.

By default, FEF is enabled. FEF can be disabled through register setting.

### 10BASE-T Transmit

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

### 10BASE-T Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8873MLL/FLL/RLL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

### MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8873MLL/FLL/RLL supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8873MLL/FLL/RLL device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 2:

**Table 2. MDI/MDI-X Pin Definitions**

| MDI | | MDI-X | |
|---|---|---|---|
| **RJ-45 Pins** | **Signals** | **RJ-45 Pins** | **Signals** |
| 1 | TD+ | 1 | RD+ |
| 2 | TD- | 2 | RD- |
| 3 | RD+ | 3 | TD+ |
| 6 | RD- | 6 | TD- |

### *Straight Cable*

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 1 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

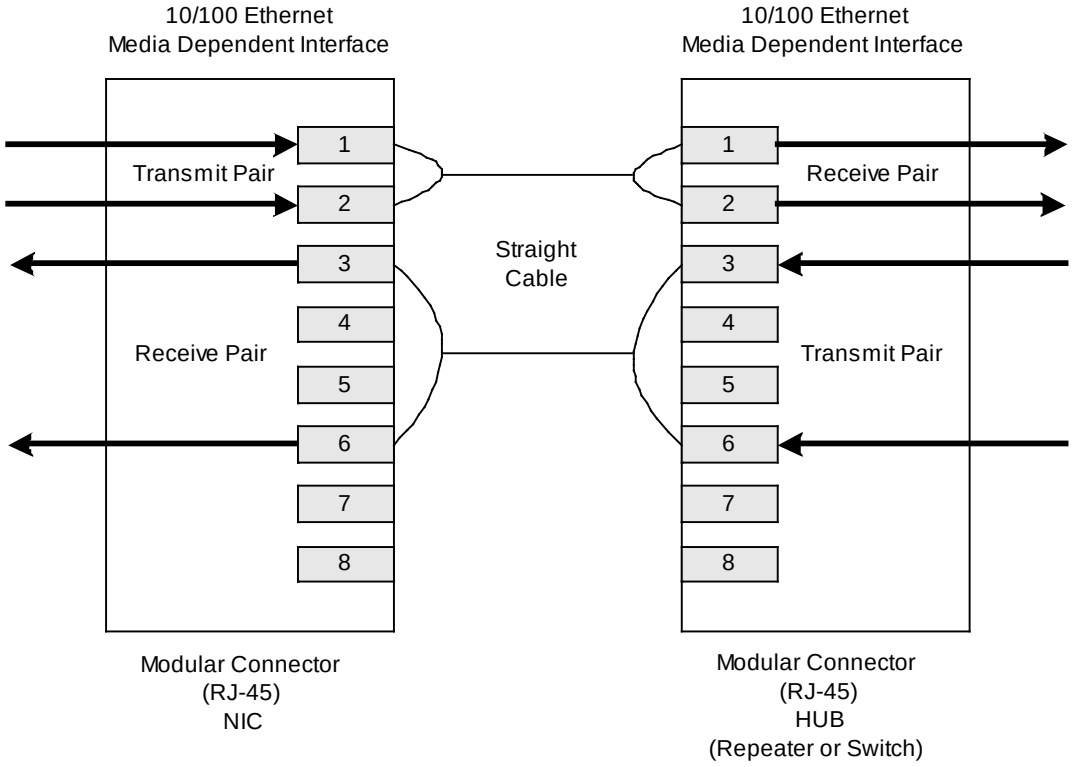



**Figure 1. Typical Straight Cable Connection**

***Crossover Cable***

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices):

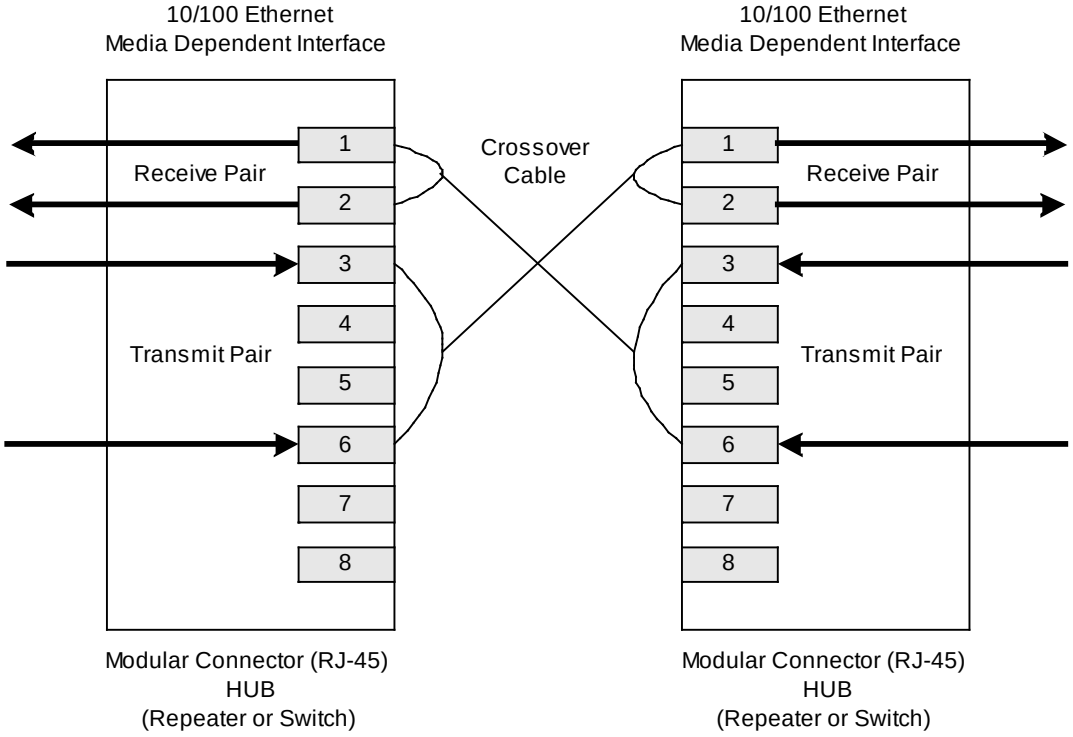



**Figure 2. Typical Crossover Cable Connection**

**Auto-Negotiation**

The KSZ8873MLL/FLL/RLL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, link partners advertise their capabilities across the link to each other. If auto-negotiation is not supported or the KSZ8873MLL/FLL/RLL link partner is forced to bypass auto-negotiation, the KSZ8873MLL/FLL/RLL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8873MLL/FLL/RLL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The link up process is shown in Figure 3:

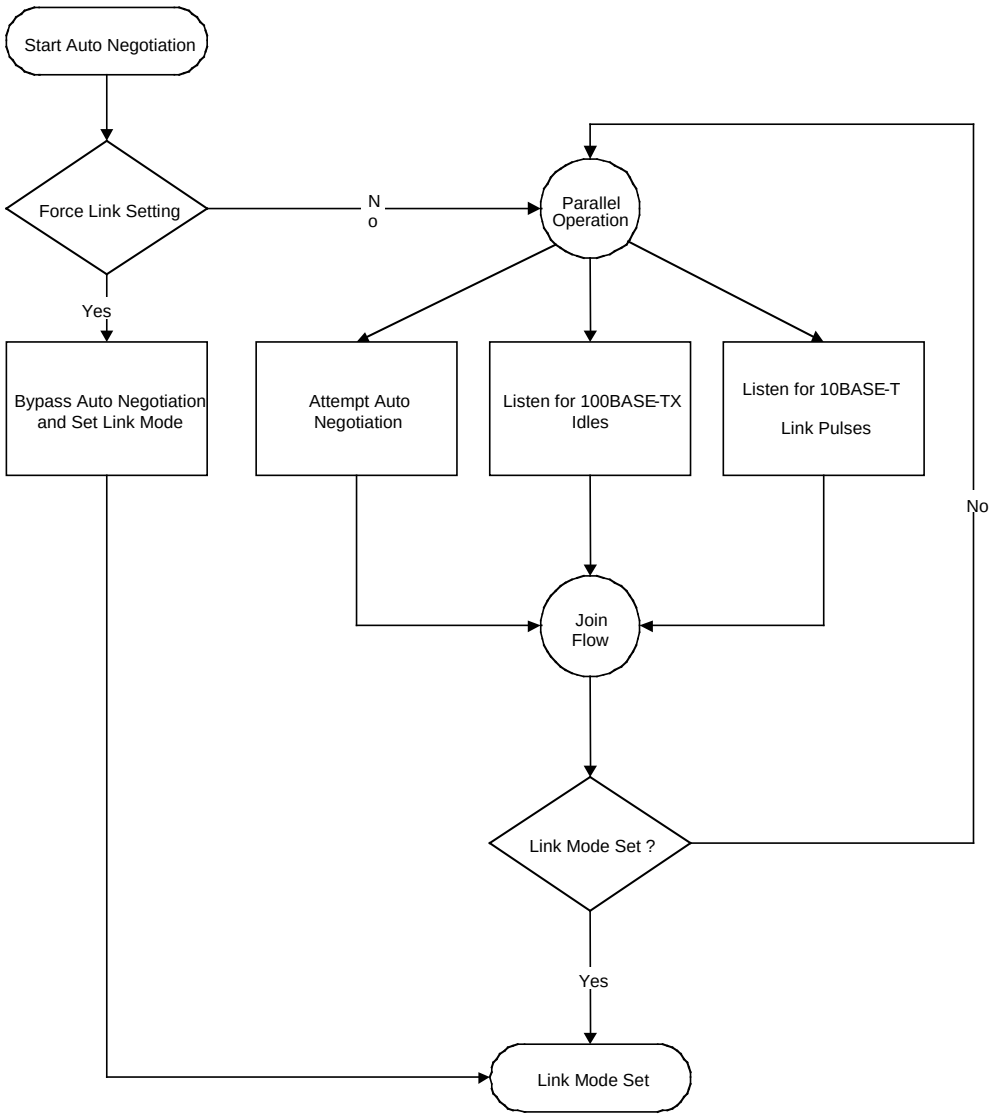



**Figure 3. Auto-Negotiation and Parallel Operation**

### LinkMD® Cable Diagnostics

KSZ8873MLL/FLL/RLL supports the LinkMD®. The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault. Internal circuitry displays the TDR information in a user-readable digital format.

**Note**: Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

#### *Access*

LinkMD® is initiated by accessing the PHY special control/status registers {26, 42} and the LinkMD result registers {27, 43} for ports 1 and 2 respectively; and in conjunction with the port registers control 13 for ports 1and 2 respectively to disable Auto MDI/MDIX.

Alternatively, the MIIM PHY registers 0 and 29 can be used for LinkMD® access.

#### *Usage*

The following is a sample procedure for using LinkMD® with registers {42,43,45} on port 2:

1. Disable auto MDI/MDI-X by writing a '1' to Register 45, bit [2] to enable manual control over the differential pair used to transmit the LinkMD® pulse.
2. Start cable diagnostic test by writing a '1' to Register 42, bit [4]. This enable bit is self-clearing.
3. Wait (poll) for Register 42, bit [4] to return a '0', indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 42, bits [6:5]. The results are as follows:

   00 = normal condition (valid test)
   01 = open condition detected in cable (valid test)
   10 = short condition detected in cable (valid test)
   11 = cable diagnostic test failed (invalid test)

   The '11' case, invalid test, occurs when the KSZ8873MLL/FLL/RLL is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the KSZ8873MLL/FLL/RLL to determine if the detected signal is a reflection of the signal generated or a signal from another source.
5. Get distance to fault by concatenating Register 42, bit [0] and Register 43, bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

   **D (distance to cable fault) = 0.4 x {( Register 26, bit [0]),(Register 27, bits [7:0])}**

   D (distance to cable fault) is expressed in meters.
   Concatenated value of Registers 42 and 43 is converted to decimal before multiplying by 0.4.
   The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

## Functional Overview: Power Management

The KSZ8873MLL/FLL/RLL supports enhanced power management feature in low power state with energy detection to ensure low-power dissipation during device idle periods. There are five operation modes under the power management function which is controlled by two bits in Register 195 (0xC3) and one bit in Register 29 (0x1D),45(0x2D) as shown below:

Register 195 bit[1:0] = 00 Normal Operation Mode

Register 195 bit[1:0] = 01 Energy Detect Mode

Register 195 bit[1:0] = 10 Soft Power-Down Mode

Register 195 bit[1:0] = 11 Power-Saving Mode

Register 29,45 bit 3 =1 Port-Based Power-Down Mode

Table 3 indicates all internal function blocks status under four different power management operation modes.

**Table 3. Internal Function Block Status**

| KSZ8873MLL/FLL/RLL Function Blocks | Power Management Operation Modes | | | |
|---|---|---|---|---|
| | Normal Mode | Power Saving Mode | Energy Detect Mode | Soft Power Down Mode |
| Internal PLL Clock | Enabled | Enabled | Disabled | Disabled |
| Tx/Rx PHY | Enabled | Rx unused block disabled | Energy detect at Rx | Disabled |
| MAC | Enabled | Enabled | Disabled | Disabled |
| Host Interface | Enabled | Enabled | Disabled | Disabled |

### Normal Operation Mode

This is the default setting bit[1:0]=00 in Register 195 after the chip power-up or hardware reset . When KSZ8873MLL/FLL/RLL is in this normal operation mode, all PLL clocks are running, PHY and MAC are on and the host interface is ready for CPU read or write.

During the normal operation mode, the host CPU can set the bit[1:0] in Register 195 to transit the current normal operation mode to any one of the other three power management operation modes.

### Energy-Detect Mode

The energy-detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8873MLL/FLL/RLL is not connected to an active link partner. In this mode, the device will save up to 50% of the power. If the cable is not plugged, the KSZ8873MLL/FLL/RLL can automatically enter to a low power state, a.k.a., the energy-detect mode. In this mode, KSZ8873MLL/FLL/RLL will keep transmitting 120ns width pulses at 1 pulse/s rate. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8873MLL/FLL/RLL can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8873MLL/FLL/RLL reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bit[1:0]=01 in Register 195. When the KSZ8873MLL/FLL/RLL is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than pre-configured value at bit[7:0] Go-Sleep time in Register 196, KSZ8873MLL/FLL/RLL will go into a low power state. When KSZ8873MLL/FLL/RLL is in low power state, it will keep monitoring the cable energy. Once the energy is detected from the cable, KSZ8873MLL/FLL/RLL will enter normal power state. When KSZ8873MLL/FLL/RLL is at normal power state, it is able to transmit or receive packet from the cable.

It will save about 87% of the power when MII interface is in PHY mode, Pin SMTXER3/MII_LINK_3 is connected to High, Register 195 bit [1:0] =01, bit 2 =1(Disable PLL), not cables are connected.

### Soft Power-Down Mode

The soft power-down mode is entered by setting bit[1:0]=10 in Register 195. When KSZ8873MLL/FLL/RLL is in this mode, all PLL clocks are disabled, the PHY and the MAC are off, all internal registers value will not change. When the host set bit[1:0]=00 in Register 195, this device will be back from current soft power down mode to normal operation mode

### Power-Saving Mode

The power saving mode is entered when auto-negotiation mode is enabled, cable is disconnected, and by setting bit[1:0]=11 in Register 195. When KSZ8873MLL/FLL/RLL is in this mode, all PLL clocks are enabled, MAC is on, all internal registers value will not change, and host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off based on line status to achieve power saving. The PHY remains transmitting and only turns off the unused receiver block. Once activity resumes due to plugging a cable or attempting by the far end to establish link, the KSZ8873MLL/FLL/RLL can automatically enabled the PHY power up to normal power state from power saving mode.

During this power saving mode, the host CPU can set bit[1:0] =0 in Register 195 to transit the current power saving mode to any one of the other three power management operation modes.

### Port-Based Power-Down Mode

In addition, the KSZ8873MLL/FLL/RLL features a per-port power-down mode. To save power, a PHY port that is not in use can be powered down via port control Register 29 or 45 bit 3, or MIIM PHY register. It will saves about 15mA per port.

### Hardware Power Down

KSZ8873 supports a hardware power-down mode. When the Pin PWRDN is activated low, the entire chip is powered down.

## Functional Overview: MAC and Switch

### Address Lookup

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8873MLL/FLL/RLL is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

### Learning

The internal lookup engine updates its table with a new entry if the following conditions are met:

1. The received packet's source address (SA) does not exist in the lookup table.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

### Migration

The internal lookup engine also monitors whether a station has moved. If a station has moved, it will update the table accordingly. Migration happens when the following conditions are met:

1. The received packet's SA is in the table but the associated source port information is different.
2. The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine will update the existing record in the table with the new source port information.

### Aging

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and will continuously remove aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through Register 3 (0x03) bit [2].

### Forwarding

The KSZ8873MLL/FLL/RLL forwards packets using the algorithm that is depicted in the following flowcharts. Figure 4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 5. The packet is sent to PTF2.

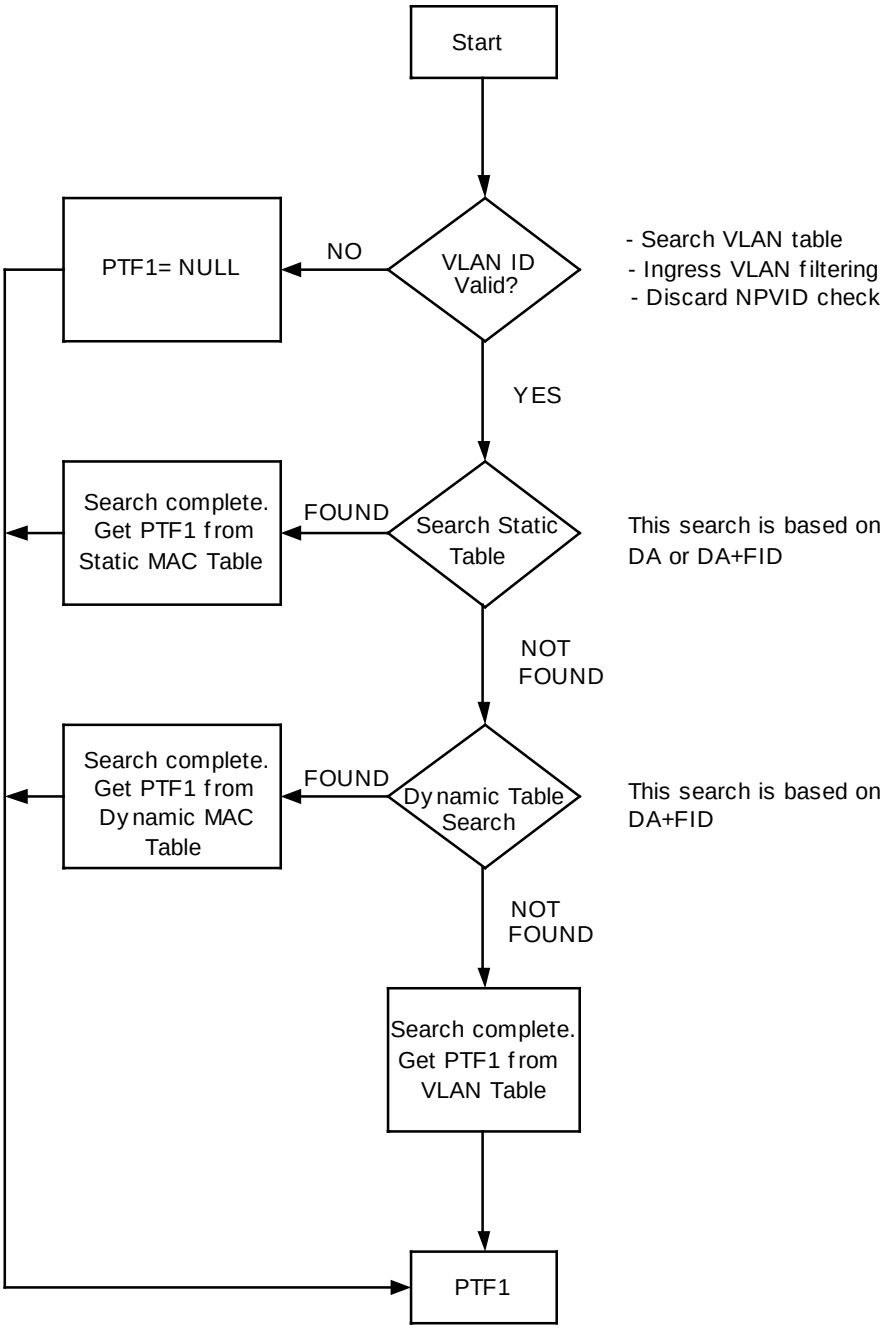



**Figure 4. Destination Address Lookup Flow Chart – Stage 1**

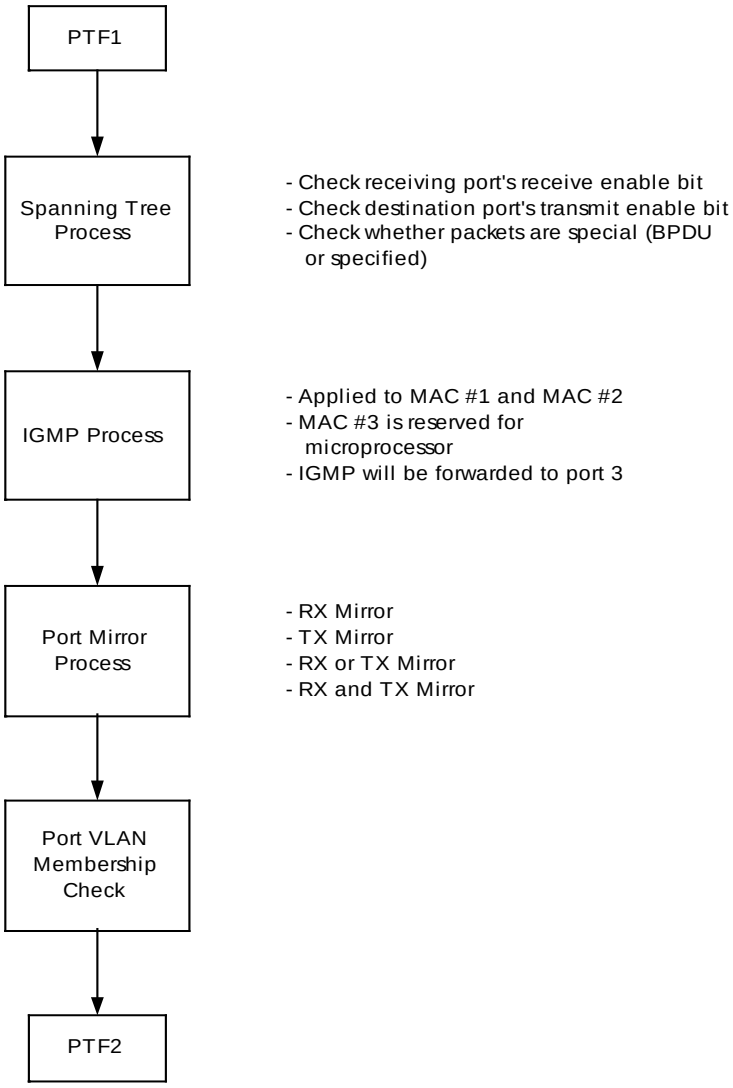



**Figure 5. Destination Address Resolution Flow Chart – Stage 2**

The KSZ8873MLL/FLL/RLL will not forward the following packets:

1. Error packets

   These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.

2. IEEE802.3x PAUSE frames

   KSZ8873MLL/FLL/RLL intercepts these packets and performs full duplex flow control accordingly.

3. "Local" packets

   Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

### Switching Engine

The KSZ8873MLL/FLL/RLL features a high-performance switching engine to move data to and from the MACs' packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32kB internal frame buffer. This buffer pool is shared between all three ports. There are a total of 256 buffers available. Each buffer is sized at 128 bytes.

### MAC Operation

The KSZ8873MLL/FLL/RLL strictly abides by IEEE 802.3 standards to maximize compatibility.

#### *Inter Packet Gap (IPG)*

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

#### *Back-Off Algorithm*

The KSZ8873MLL/FLL/RLL implements the IEEE 802.3 standard for the binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet is optionally dropped depending on the switch configuration for Register 4 (0x04) bit [3].

#### *Late Collision*

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

#### *Illegal Frames*

The KSZ8873MLL/FLL/RLL discards frames less than 64 bytes, and can be programmed to accept frames up to1518 bytes, 1536 bytes or 1916 bytes. These maximum frame size settings are programmed in Register 4 (0x04). Since the KSZ8873MLL/FLL/RLL supports VLAN tags, the maximum sizing is adjusted when these tags are present.

#### *Full Duplex Flow Control*

The KSZ8873MLL/FLL/RLL supports standard IEEE 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8873MLL/FLL/RLL receives a pause control frame, the KSZ8873MLL/FLL/RLL will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8873MLL/FLL/RLL are transmitted.

On the transmit side, the KSZ8873MLL/FLL/RLL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8873MLL/FLL/RLL will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8873MLL/FLL/RLL issues a flow control frame (XOFF), containing the maximum pause time defined by the IEEE 802.3x standard. Once the resource is freed up, the KSZ8873MLL/FLL/RLL sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

The KSZ8873MLL/FLL/RLL flow controls all ports if the receive queue becomes full.

#### *Half-Duplex Backpressure*

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as full duplex flow control. If backpressure is required, the KSZ8873MLL/FLL/RLL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8873MLL/FLL/RLL discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10 BASE-T or 100 BASE-TX half duplex modes, the user must enable the following:

1. Aggressive back-off (Register 3 (0x03), bit [0])
2. No excessive collision drop (Register 4 (0x04), bit [3])

**Note**: These bits are not set as defaults, as this is not the IEEE standard.

***Broadcast Storm Protection***

The KSZ8873MLL/FLL/RLL has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8873MLL/FLL/RLL has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 67ms interval for 100BT and a 500ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Register 6 (0x06) and 7 (0x07). The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec * 67ms/interval * 1% = 99 frames/interval (approx.) = 0x63

**Note**: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-TX with 12 bytes of IPG and 8 bytes of preamble between two packets.

***Port Individual MAC Address and Source Port Filtering***

The KSZ8873MLL/FLL/RLL provide individual MAC address for port 1 and port 2 respectively. They can be set at Register 142-147 and 148-153. With this feature, the CPU connected to the port 3 can receive the packets from two internet subnets which has their own MAC address.

The packet will be filtered if its source address matches the MAC address of port 1 or port 2 when the Register 21 and 37 bit 6 is set to 1 respectively. For example, the packet will be dropped after it completes the loop of a ring network.

**MII Interface Operation**

The media independent interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between physical layer and MAC layer devices. The MII provided by the KSZ8873MLL/FLL is connected to the device’s third MAC. The interface contains two distinct groups of signals: one for transmission and the other for reception. Table 4 describes the signals used by the MII bus.

**Table 4. MII Signals**

| PHY-Mode Connections | | | MAC-Mode Connections | |
|---|---|---|---|---|
| **External MAC Controller Signals** | **KSZ8873MLL/FL PHY Signals** | **Pin Descriptions** | **External PHY Signals** | **KSZ8873MLL/FLL MAC Signals** |
| MTXEN | SMTXEN3 | Transmit enable | MTXEN | SMRXDV3 |
| MTXER | SMTXER3 | Transmit error | MTXER | (not used) |
| MTXD3 | SMTXD33 | Transmit data bit 3 | MTXD3 | SMRXD33 |
| MTXD2 | SMTXD32 | Transmit data bit 2 | MTXD2 | SMRXD32 |
| MTXD1 | SMTXD31 | Transmit data bit 1 | MTXD1 | SMRXD31 |
| MTXD0 | SMTXD30 | Transmit data bit 0 | MTXD0 | SMRXD30 |
| MTXC | SMTXC3 | Transmit clock | MTXC | SMRXC3 |
| MCOL | SCOL3 | Collision detection | MCOL | SCOL3 |
| MCRS | SCRS3 | Carrier sense | MCRS | SCRS3 |
| MRXDV | SMRXDV3 | Receive data valid | MRXDV | SMTXEN3 |
| MRXER | (not used) | Receive error | MRXER | SMTXER3 |
| MRXD3 | SMRXD33 | Receive data bit 3 | MRXD3 | SMTXD33 |
| MRXD2 | SMRXD32 | Receive data bit 2 | MRXD2 | SMTXD32 |
| MRXD1 | SMRXD31 | Receive data bit 1 | MRXD1 | SMTXD31 |
| MRXD0 | SMRXD30 | Receive data bit 0 | MRXD0 | SMTXD30 |
| MRXC | SMRXC3 | Receive clock | MRXC | SMTXC3 |

The MII operates in either PHY mode or MAC mode. The data interface is a nibble wide and runs at ¼ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Similarly, the receive side has signals that convey when the data is valid and without physical layer errors. For half duplex operation, the SCOL signal indicates if a collision has occurred during transmission.

The KSZ8873MLL/FLL does not provide the MRXER signal for PHY mode operation and the MTXER signal for MAC mode operation. Normally, MRXER indicates a receive error coming from the physical layer device and MTXER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8873MLL/FLL. So, for PHY mode operation, if the device interfacing with the KSZ8873MLL/FLL has an MRXER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8873MLL/FLL has an MTXER input pin, it also needs to be tied low.

The KSZ8873MLL/FLL provides a bypass feature in the MII PHY mode. Pin SMTXER3/MII_LINK is used for MII link status. If the host is power down, Pin MII_LINK will go to high. In this case, no new ingress frames from port1 or port 2 will be sent out through port 3, and the frames for port 3 already in packet memory will be flushed out.

**RMII Interface Operation**

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

1. Ports 10Mbps and 100Mbps data rates.
2. Uses a single 50 MHz clock reference (provided internally or externally).
3. Provides independent 2-bit wide (di-bit) transmit and receive data paths.
4. Contains two distinct groups of signals: one for transmission and the other for reception

When EN_REFCLKO_3 is high, KSZ8873RLL will output a 50MHz in REFCLKO_3. Register 198 bit[3] is used to select internal or external reference clock. Internal reference clock means that the clock for the RMII of KSZ8873RLL will be

provided by the KSZ8873RLL internally and the REFCLKI_3 pin is unconnected. For the external reference clock, the clock will provide to KSZ8873RLL via REFCLKI_3.

**Note**: If the reference clock is not provided by the KSZ8873RLL, this 50MHz reference clock has to be used in X1 pin instead of the 25MHz crystal since the clock skew of these two clock sources will impact on the RMII timing. The SPIQ clock selection strapping option pin is connected to low to select the 50MHz input.

**Table 5. RMII Clock Setting**

| Reg198[3] | EN_REFCLKO_3 | Clock Source | Note |
|---|---|---|---|
| 0 | 0 | External 50MHz OSC input to REFCLKI_3 | EN_REFCLKO_3 = 0 to Disable REFCLKO_3 for better EMI |
| 0 | 1 | REFCLKO_3 Output Is Feedback to REFCLKI_3 | EN_REFCLKO_3 = 1 to Enable REFCLKO_3 |
| 1 | 1 | Internal Clock Source<br>REFCLKI_3 is unconnected | EN_REFCLKO_3 = 1 to Enable REFCLKO_3 |
| 1 | 0 | | Not suggested |

The RMII provided by the KSZ8873RLL is connected to the device's third MAC. It complies with the RMII Specification. Table 6 describes the signals used by the RMII bus. Refer to RMII Specification for full detail on the signal description.

**Table 6. RMII Signal Description**

| RMII Signal Name | Direction (with respect to the PHY) | Direction (with respect to the MAC) | RMII Signal Description | KSZ8873RLL RMII Signal (direction) |
|---|---|---|---|---|
| REF_CLK | Input | Input or Output | Synchronous 50 MHz clock reference for receive, transmit and control interface | REFCLKI_3 (input) |
| CRS_DV | Output | Input | Carrier sense/Receive data valid | SMRXDV3 (output) |
| RXD1 | Output | Input | Receive data bit 1 | SMRXD31 (output) |
| RXD0 | Output | Input | Receive data bit 0 | SMRXD30 (output) |
| TX_EN | Input | Output | Transmit enable | SMTXEN3 (input) |
| TXD1 | Input | Output | Transmit data bit 1 | SMTXD31 (input) |
| TXD0 | Input | Output | Transmit data bit 0 | SMTXD30 (input) |
| RX_ER | Output | Input (not required) | Receive error | (not used) |
| – | – | – | – | SMTXER3* (input)<br>*** Connects to RX_ER signal of RMII PHY device** |

The KSZ8873RLL filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the SMTXER3 input signal of the KSZ8873RLL is connected to the RXER output signal of the RMII PHY device.

Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie MII signals, SMTXD3[3:2] and SMTXER3, to ground if they are not used.

The KSZ8873RLL RMII can interface with RMII PHY and RMII MAC devices. The latter allows two KSZ8873RLL devices to be connected back-to-back. Table 7 shows the KSZ8873RLL RMII pin connections with an external RMII PHY and an external RMII MAC, such as another KSZ8873RLL device.

**Table 7. RMII Signal Connections**

| KSZ8873RLL PHY-MAC Connections | | | KSZ8873RLL MAC-MAC Connections | |
|---|---|---|---|---|
| **External PHY Signals** | **KSZ8873RLL MAC Signals** | **Pin Descriptions** | **KSZ8873RLL MAC Signals** | **External MAC Signals** |
| REF_CLK | REFCLKI_3 | Reference Clock | REFCLKI_3 | REF_CLK |
| TX_EN | SMRXDV3 | Carrier sense/ Receive data valid | SMRXDV3 | CRS_DV |
| TXD1 | SMRXD31 | Receive data bit 1 | SMRXD31 | RXD1 |
| TXD0 | SMRXD30 | Receive data bit 0 | SMRXD30 | RXD0 |
| CRS_DV | SMTXEN3 | Transmit enable | SMTXEN3 | TX_EN |
| RXD1 | SMTXD31 | Transmit data bit 1 | SMTXD31 | TXD1 |
| RXD0 | SMTXD30 | Transmit data bit 0 | SMTXD30 | TXD0 |
| RX_ER | SMTXER3 | Receive error | (not used) | (not used) |

### MII Management (MIIM) Interface

The KSZ8873MLL/FLL/RLL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8873MLL/FLL/RLL. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further detail on the MIIM interface is found in Clause 22.2.4.5 of the IEEE 802.3u Specification and refer to 802.3 section 22.3.4 for the timing.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (SDA_MDIO) and the clock line (SCL_MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8873MLL/FLL/RLL device.
- Access to a set of eight 16-bit registers, consisting of six standard MIIM registers [0:5] and two custom MIIM registers [29, 31].

The MIIM Interface can operate up to a maximum clock speed of 5MHz.

Table 8 depicts the MII Management Interface frame format.

**Table 8. MII Management Interface Frame Format**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

### Serial Management Interface (SMI)

The SMI is the KSZ8873MLL/FLL/RLL non-standard MIIM interface that provides access to all KSZ8873MLL/FLL/RLL configuration registers. This interface allows an external device to completely monitor and control the states of the KSZ8873MLL/FLL/RLL.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (SDA_MDIO) and the clock line (SCL_MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8873MLL/FLL/RLL device.
- Access to all KSZ8873MLL/FLL/RLL configuration registers. Register access includes the Global, Port and Advanced Control registers 0-198 (0x00 – 0xC6), and indirect access to the standard MIIM registers [0:5] and custom MIIM registers [29, 31].

Table 9 depicts the SMI frame format.

**Table 9. Serial Management Interface (SMI) Frame Format**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 00 | 1xRRR | RRRRR | Z0 | 0000_0000_DDDD_DDDD | Z |
| **Write** | 32 1's | 01 | 00 | 0xRRR | RRRRR | 10 | xxxx_xxxx_DDDD_DDDD | Z |

SMI register read access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '1'. SMI register write access is selected when OP Code is set to "00" and bit 4 of the PHY address is set to '0'. PHY address bit[3] is undefined for SMI register access, and hence can be set to either '0' or '1' in read/write operations.

To access the KSZ8873MLL/FLL/RLL Registers 0-196 (0x00 – 0xC6), the following applies:

- PHYAD[2:0] and REGAD[4:0] are concatenated to form the 8-bit address; that is, {PHYAD[2:0], REGAD[4:0]} = bits [7:0] of the 8-bit address.
- TA bits [1:0] are 'Z0' means the processor MDIO pin is changed to input Hi-Z from output mode and the followed '0' is the read response from device.
- TA bits [1:0] are set to '10' when write registers.
- Registers are 8 data bits wide.
  - For read operation, data bits [15:8] are read back as 0's.
  - For write operation, data bits [15:8] are not defined, and hence can be set to either '0' or '1'.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

## Advanced Switch Functions

### Bypass Mode

The KSZ8873MLL/FLL/RLL also offer a by-pass mode which enables system-level power saving. When the CPU (connected to Port 3) enters a power saving mode of power down or sleeping mode, the CPU can control the Pin 27 SMTXER3/MII_LINK_3 which can be tied high so that the KSZ8873MLL/FLL/RLL detect this change and automatically switches to the by-pass mode in which the switch function between Port1 and Port2 is sustained. In the by-pass mode, the packets with DA to port 3 will be dropped and by pass the internal buffer memory, make the buffer memory more efficiency for the data transfer between port 1 and port 2. Specially, the power saving get more in energy detect mode with the by-pass to be used.

### IEEE 802.1Q VLAN Support

The KSZ8873MLL/FLL/RLL supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8873MLL/FLL/RLL provides a 16-entries VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN Table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

**Table 10. FID + DA Lookup in VLAN Mode**

| DA found in Static MAC Table? | Use FID flag? | FID match? | DA+FID found in Dynamic MAC Table? | Action |
|---|---|---|---|---|
| No | Don't care | Don't care | No | Broadcast to the membership ports defined in the *VLAN Table* bits [18:16] |
| No | Don't care | Don't care | Yes | Send to the destination port defined in the *Dynamic MAC Address Table* bits [53:52] |
| Yes | 0 | Don't care | Don't care | Send to the destination port(s) defined in the *Static MAC Address Table* bits [50:48] |
| Yes | 1 | No | No | Broadcast to the membership ports defined in the *VLAN Table* bits [18:16] |
| Yes | 1 | No | Yes | Send to the destination port defined in the *Dynamic MAC Address Table* bits [53:52] |
| Yes | 1 | Yes | Don't care | Send to the destination port(s) defined in the *Static MAC Address Table* bits [50:48] |

**Table 11. FID + SA Lookup in VLAN Mode**

| FID+SA found in Dynamic MAC Table? | Action |
|---|---|
| No | Learn and add FID+SA to the Dynamic MAC Address Table |
| Yes | Update time stamp |

Advanced VLAN features, such as "Ingress VLAN filtering" and "Discard Non PVID packets" are also supported by the KSZ8873MLL/FLL/RLL. These features can be set on a per port basis, and are defined in register 18, 34 and 50 for ports 1, 2 and 3, respectively.

### QoS Priority Support

The KSZ8873MLL/FLL/RLL provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit [0] of Registers 16, 32 and 48 is used to enable split transmit queues for ports 1, 2 and 3, respectively. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first or use weighted fair queuing for the four priority queues. This global option is set and explained in bit [3] of Register 5.

### Port-Based Priority

With port-based priority, each ingress port is individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits [4:3] of Registers 16, 32 and 48 are used to enable port-based priority for ports 1, 2 and 3, respectively.

### 802.1p-Based Priority

For 802.1p-based priority, the KSZ8873MLL/FLL/RLL examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the Registers 12 and 13. The “priority mapping” value is programmable.

Figure 6 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

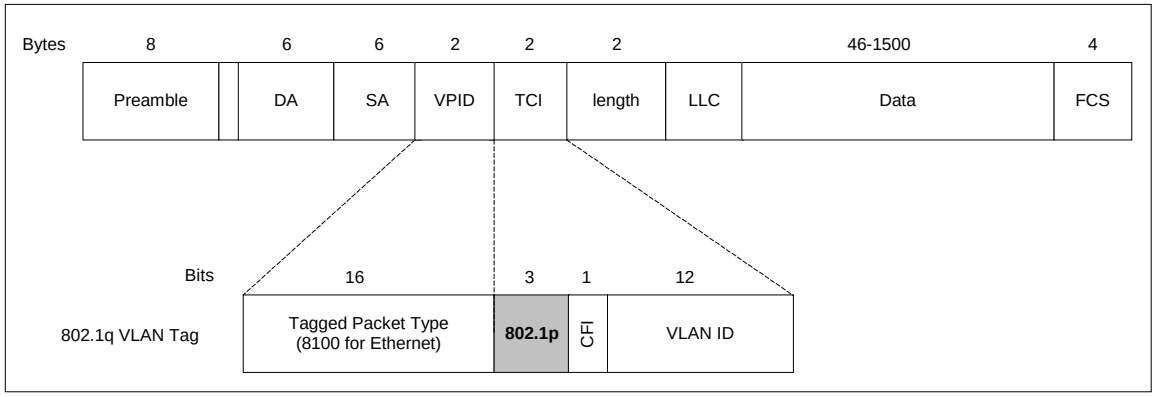



**Figure 6. 802.1p Priority Field Format**

802.1p-based priority is enabled by bit [5] of Registers 16, 32 and 48 for ports 1, 2 and 3, respectively.

The KSZ8873MLL/FLL/RLL provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2-byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

**Tag Insertion** is enabled by bit [2] of the port registers control 0 and the Register 194 to select which source port (ingress port) PVID can be inserted on the egress port for ports 1, 2 and 3, respectively. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets {19,20}, {35,36} and {51,52} for ports 1, 2 and 3, respectively and the source port VID has to be inserted at selected egress ports by bit[5:0] of register 194. The KSZ8873MLL/FLL/RLL will not add tags to already tagged packets.

**Tag Removal** is enabled by bit [1] of Registers 16, 32 and 48 for ports 1, 2 and 3, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8873MLL/FLL/RLL will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

**802.1p Priority Field Re-Mapping** is a QoS feature that allows the KSZ8873MLL/FLL/RLL to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field.

### *DiffServ-Based Priority*

DiffServ-based priority uses the ToS registers (Registers 96 to 111) in the Advanced Control Registers section. The ToS priority control registers implement a fully decoded, 64-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

### Spanning Tree Support

To support spanning tree, port 3 is designated as the processor port.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings in Registers 18 and 34 for ports 1 and 2, respectively. Table 12 shows the port setting and software actions taken for each of the five spanning tree states.

**Table 12. Spanning Tree States**

| **Disable State** | **Port Setting** | **Software Action** |
|---|---|---|
| The port should not forward or receive any packets. Learning is disabled. | "transmit enable = 0, receive enable = 0, learning disable =1" | The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "static MAC table" with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state. |
| **Blocking State** | **Port Setting** | **Software Action** |
| Only packets to the processor are forwarded. Learning is disabled. | "transmit enable = 0, receive enable = 0, learning disable =1" | The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state. |
| **Listening State** | **Port Setting** | **Software Action** |
| Only packets to and from the processor are forwarded. Learning is disabled. | "transmit enable = 0, receive enable = 0, learning disable =1" | The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See "Tail Tagging Mode" for details. Address learning is disabled on the port in this state. |
| **Learning State** | **Port Setting** | **Software Action** |
| Only packets to and from the processor are forwarded. Learning is enabled. | "transmit enable = 0, receive enable = 0, learning disable = 0" | The processor should program the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. See "Tail Tagging Mode" for details. Address learning is enabled on the port in this state. |
| **Forwarding State** | **Port Setting** | **Software Action** |
| Packets are forwarded and received normally. Learning is enabled. | "transmit enable = 1, receive enable = 1, learning disable = 0" | The processor programs the "Static MAC table" with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. See "Tail Tagging Mode" for details. Address learning is enabled on the port in this state. |

**Rapid Spanning Tree Support**

There are three operational states of the Discarding, Learning, and Forwarding assigned to each port for RSTP:

Discarding ports do not participate in the active topology and do not learn MAC addresses.

*Discarding state: the state includs three states of the disable, blocking and listening of STP.*

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1."

Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. When disable the port’s learning capability (learning disable=’1’), set the Register 2 bit 5 and bit 4 will flush rapidly the port related entries in the dynamic MAC table and static MAC table.

**Note**: processor is connected to port 3 via MII interface. Address learning is disabled on the port in this state.

Ports in Learning states learn MAC addresses, but do not forward user traffic.

*Learning state: only packets to and from the processor are forwarded. Learning is enabled.*

Port setting: “transmit enable = 0, receive enable = 0, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see *Tail Tagging Mode* section for details. Address learning is enabled on the port in this state.

Ports in Forwarding states fully participate in both data forwarding and MAC learning.

*Forwarding state: packets are forwarded and received normally. Learning is enabled.*

Port setting: “transmit enable = 1, receive enable = 1, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see *Tail Tagging Mode* section for details. Address learning is enabled on the port in this state.

RSTP uses only one type of BPDU called RSTP BPDUs. They are similar to STP Configuration BPDUs with the exception of a type field set to “version 2” for RSTP and “version 0” for STP, and a flag field carrying additional information.

**Tail Tagging Mode**

The Tail Tag is only seen and used by the port 3 interface, which should be connected to a processor. It is an effective way to retrieve the ingress port information for spanning tree protocol IGMP snooping and other applications. The Bit 1 and bit 0 in the one byte tail tagging is used to indicate the source/destination port in port 3. Bit 3 and bit 2 are used for the priority setting of the ingress frame in port 3. Other bits are not used. The Tail Tag feature is enabled by setting Register 3 bit 6.


**Figure 7. Tail Tag Frame Format**

**Table 13. Tail Tag Rules**

| Ingress to Port 3 (Host -> KSZ8873MLL/FLL/RLL) | |
|---|---|
| **Bit [1,0]** | **Destination Port** |
| 0,0 | Normal (Address Look up) |
| 0,1 | Port 1 |
| 1,0 | Port 2 |
| 1,1 | Port 1 and 2 |
| Bit [3,2] | Frame Priority |
| 0,0 | Priority 0 |
| 0,1 | Priority 1 |
| 1,0 | Priority 2 |
| 1,1 | Priority 3 |
| **Egress from Port 3 (KSZ8873MLL/FLL/RLL->Host)** | |
| **Bit [0]** | **Source Port** |
| 0 | Port 1 |
| 1 | Port 2 |

### IGMP Support

For Internet Group Management Protocol (IGMP) support in layer 2, the KSZ8873MLL/FLL/RLL provides two components, IGMP snooping and IGMP send-back to the subscribed port.

#### *IGMP Snooping*

The KSZ8873MLL/FLL/RLL traps IGMP packets and forwards them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

#### *IGMP Send-Back to the Subscribed Port*

Once the host responds the received IGMP packet, the host should knows the original IGMP ingress port and send back the IGMP packet to this port only, otherwise this IGMP packet will be broadcasted to all port to downgrade the performance.

Enable the tail tag mode, the host will know the IGMP packet received port from tail tag bits [0] and can send back the response IGMP packet to this subscribed port by setting the bits [1,0] in the tail tag. Enable “Tail tag mode” by setting Register 3 bit 6. The tail tag will be removed automatically when the IGMP packet is sent out from the subscribed port.

### Port Mirroring Support

KSZ8873MLL/FLL/RLL supports “Port Mirroring” comprehensively as:

- “receive only” mirror on a port
- All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8873MLL/FLL/RLL forwards the packet to both port 2 and port 3. The KSZ8873MLL/FLL/RLL can optionally even forward “bad” received packets to the “sniffer port”.
- “transmit only” mirror on a port
- All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and port 3 is programmed to be the “sniffer port”. A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8873MLL/FLL/RLL forwards the packet to both port 1 and port 3.
- “receive and transmit” mirror on two ports

- All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set Register 5 bit [0] to ‘1’. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff”, and port 3 is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8873MLL/FLL/RLL forwards the packet to both port 2 and port 3.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through Registers 17, 33, and 49 for ports 1, 2 and 3, respectively.

**Rate Limiting Support**

The KSZ8873MLL/FLL/RLL provides a fine resolution hardware rate limiting from 64Kbps to 99Mbps. The rate step is 64Kbps when the rate range is from 64Kbps to 960Kbps and 1Mbps for 1Mbps to 100Mbps(100BT) or to 10Mbps(10BT) (refer to Data Rate Limit Table). The rate limit is independently on the “receive side” and on the “transmit side” on a per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up Ingress Rate Control Registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up Egress Rate Control Registers. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8873MLL/FLL/RLL provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8873MLL/FLL/RLL counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the Leaky Bucket algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

**Unicast MAC Address Filtering**

The unicast MAC address filtering function works in conjunction with the static MAC address table. First, the static MAC address table is used to assign a dedicated MAC address to a specific port. If a unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8873MLL/FLL/RLL is then configured with the option to either filter or forward unicast packets for an unknown MAC address. This option is enabled and configured in Register 14.

This function is useful in preventing the broadcast of unicast packets that could degrade the quality of the port in applications such as voice over Internet Protocol (VoIP).

**Configuration Interface**

The KSZ8873MLL/FLL/RLL can operate as both a managed switch and an unmanaged switch.

In unmanaged mode, the KSZ8873MLL/FLL/RLL is typically programmed using an EEPROM. If no EEPROM is present, the KSZ8873MLL/FLL/RLL is configured using its default register settings. Some default settings are configured via strap-in pin options. The strap-in pins are indicated in the “Pin Description and I/O Assignment” table.

***$I^2C$ Master Serial Bus Configuration***

With an additional $I^2C$ (“2-wire”) EEPROM, the KSZ8873MLL/FLL/RLL can perform more advanced switch features like “broadcast storm protection” and “rate control” without the need of an external processor.

For KSZ8873MLL/FLL/RLL I2C Master configuration, the EEPROM stores the configuration data for Register 0 to Register 120 (as defined in the KSZ8873MLL/FLL/RLL register map) with the exception of the “Read Only” status registers. After the de-assertion of reset, the KSZ8873MLL/FLL/RLL sequentially reads in the configuration data for all control registers, starting from Register 0.

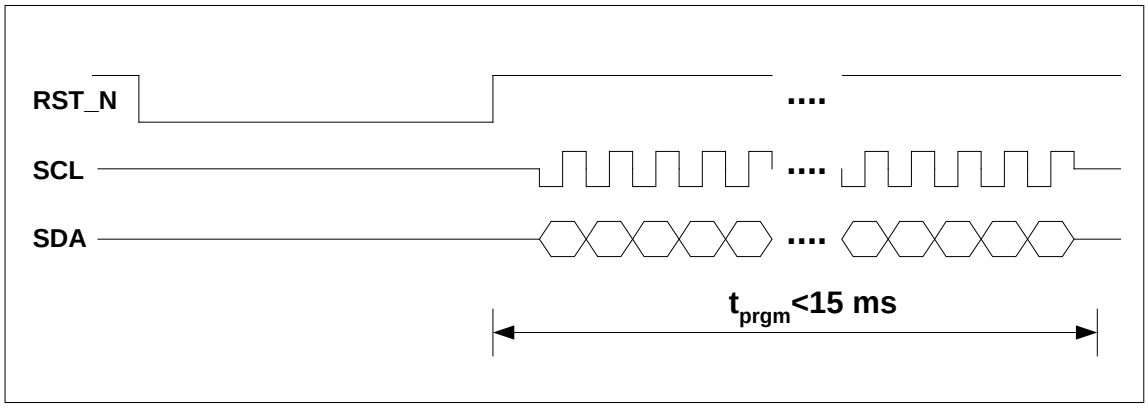



**Figure 8. EEPROM Configuration Timing Diagram**

The following is a sample procedure for programming the KSZ8873MLL/FLL/RLL with a pre-configured EEPROM:

1. Connect the KSZ8873MLL/FLL/RLL to the EEPROM by joining the SCL and SDA signals of the respective devices.
2. Enable $I^2C$ master mode by setting the KSZ8873MLL/FLL/RLL strap-in pins, P2LED[1:0] to “00”.
3. Check to ensure that the KSZ8873MLL/FLL/RLL reset signal input, RSTN, is properly connected to the external reset source at the board level.
4. Program the desired configuration data into the EEPROM.
5. Place the EEPROM on the board and power up the board.
6. Assert an active-low reset to the RSTN pin of the KSZ8873MLL/FLL/RLL. After reset is de-asserted, the KSZ8873MLL/FLL/RLL begins reading the configuration data from the EEPROM. The KSZ8873MLL/FLL/RLL checks that the first byte read from the EEPROM is “88”. If this value is correct, EEPROM configuration continues. If not, EEPROM configuration access is denied and all other data sent from the EEPROM is ignored by the KSZ8873MLL/FLL/RLL.

**Note**: For proper operation, check to ensure that the KSZ8873MLL/FLL/RLL PWRDN input signal is not asserted during the reset operation. The PWRDN input is active low.

### *$I^2C$ Slave Serial Bus Configuration*

In managed mode, the KSZ8873MLL/FLL/RLL can be configured as an I2C slave device. In this mode, an I2C master device (external controller/CPU) has complete programming access to the KSZ8873MLL/FLL/RLL’s 198 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table,” and “MIB Counters.” The tables and counters are indirectly accessed via registers 121 to 131.

In $I^2C$ slave mode, the KSZ8873MLL/FLL/RLL operates like other I2C slave devices. Addressing the KSZ8873MLL/FLL/RLL’s 8-bit registers is similar to addressing Atmel’s AT24C02 EEPROM’s memory locations. Details of $I^2C$ read/write operations and related timing information can be found in the AT24C02 Datasheet.

Two fixed 8-bit device addresses are used to address the KSZ8873MLL/FLL/RLL in I2C slave mode. One is for read; the other is for write. The addresses are as follow:

1011_1111 <read>

1011_1110 <write>

The following is a sample procedure for programming the KSZ8873MLL/FLL/RLL using the $I^2C$ slave serial bus:

1. Enable $I^2C$ slave mode by setting the KSZ8873MLL/FLL/RLL strap-in Pins P2LED[1:0] to "01".
2. Power up the board and assert reset to the KSZ8873MLL/FLL/RLL. Configure the desired register settings in the KSZ8873MLL/FLL/RLL, using the I2C write operation.
3. Read back and verify the register settings in the KSZ8873MLL/FLL/RLL, using the I2C read operation.

Some of the configuration settings, such as "Aging enable", "Auto Negotiation Enable", "Force Speed" and "Power down" can be programmed after the switch has been started.

***SPI Slave Serial Bus Configuration***

In managed mode, the KSZ8873MLL/FLL/RLL can be configured as a SPI slave device. In this mode, a SPI master device (external controller/CPU) has complete programming access to the KSZ8873MLL/FLL/RLL's 198 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the "Static MAC Table", "VLAN Table", "Dynamic MAC Table" and "MIB Counters". The tables and counters are indirectly accessed via registers 121 to 131.

The KSZ8873MLL/FLL/RLL supports two standard SPI commands: '0000_0011' for data read and '0000_0010' for data write. SPI multiple read and multiple write are also supported by the KSZ8873MLL/FLL/RLL to expedite register read back and register configuration, respectively.

SPI multiple read is initiated when the master device continues to drive the KSZ8873MLL/FLL/RLL SPISN input pin (SPI Slave Select signal) low after a byte (a register) is read. The KSZ8873MLL/FLL/RLL internal address counter increments automatically to the next byte (next register) after the read. The next byte at the next register address is shifted out onto the KSZ8873MLL/FLL/RLL SPIQ output pin. SPI multiple read continues until the SPI master device terminates it by de-asserting the SPISN signal to the KSZ8873MLL/FLL/RLL.

Similarly, SPI multiple write is initiated when the master device continues to drive the KSZ8873MLL/FLL/RLL SPISN input pin low after a byte (a register) is written. The KSZ8873MLL/FLL/RLL internal address counter increments automatically to the next byte (next register) after the write. The next byte that is sent from the master device to the KSZ8873MLL/FLL/RLL SDA input pin is written to the next register address. SPI multiple write continues until the SPI master device terminates it by de-asserting the SPISN signal to the KSZ8873MLL/FLL/RLL.

For both SPI multiple read and multiple write, the KSZ8873MLL/FLL/RLL internal address counter wraps back to register address zero once the highest register address is reached. This feature allows all 198 KSZ8873MLL/FLL/RLL registers to be read, or written with a single SPI command from any initial register address.

The KSZ8873MLL/FLL/RLL is capable of supporting a SPI bus.

The following is a sample procedure for programming the KSZ8873MLL/FLL/RLL using the SPI bus:

1. At the board level, connect the KSZ8873MLL/FLL/RLL pins as illustrated in Table 13:

**Table 14. SPI Connections**

| KSZ8873MLL/FLL/RLL Pin Number | KSZ8873MLL/FLL/RLL Signal Name | External Processor Signal Description |
|---|---|---|
| 40 | SPISN | SPI Slave Select |
| 42 | SCL (SPIC) | SPI Clock |
| 43 | SDA (SPID) | SPI Data (Master output; Slave input) |
| 39 | SPIQ | SPI Data (Master input; Slave output) |

2. Enable SPI slave mode by setting the KSZ8873MLL/FLL/RLL strap-in Pins P2LED[1:0] to “10”.
3. Power up the board and assert reset to the KSZ8873MLL/FLL/RLL.
4. Configure the desired register settings in the KSZ8873MLL/FLL/RLL, using the SPI write or multiple write command.
5. Read back and verify the register settings in the KSZ8873MLL/FLL/RLL, using the SPI read or multiple read command.

Some of the configuration settings, such as “Aging enable”, “Auto Negotiation Enable”, “Force Speed” and “Power down” can be programmed after the switch has been started.

Figure 9 through Figure 12 illustrate the SPI data cycles for “Write”, “Read”, “Multiple Write” and “Multiple Read”. The read data is registered out of SPIQ on the falling edge of SPIC, and the data input on SPID is registered on the rising edge of SPIC.

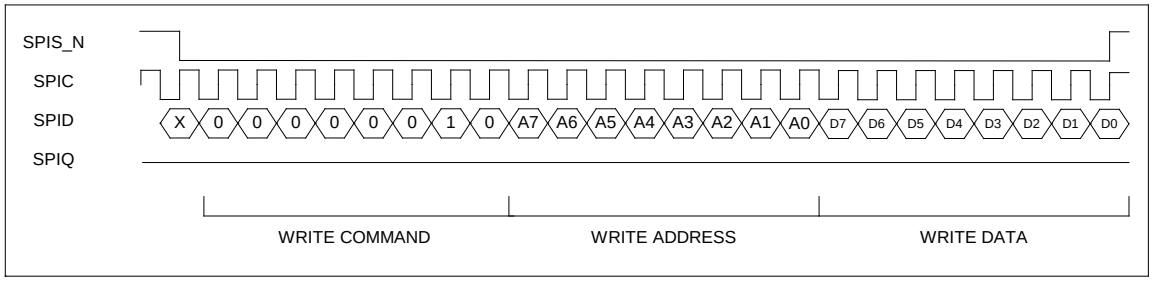



**Figure 9. SPI Write Data Cycle**

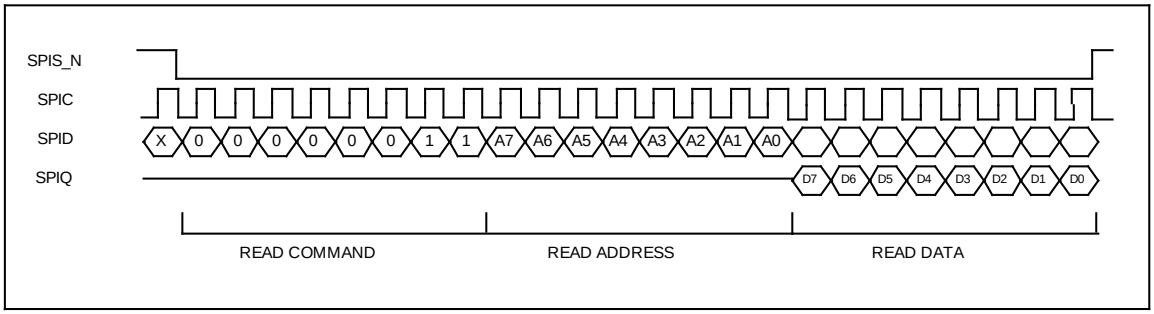



**Figure 10. SPI Read Data Cycle**

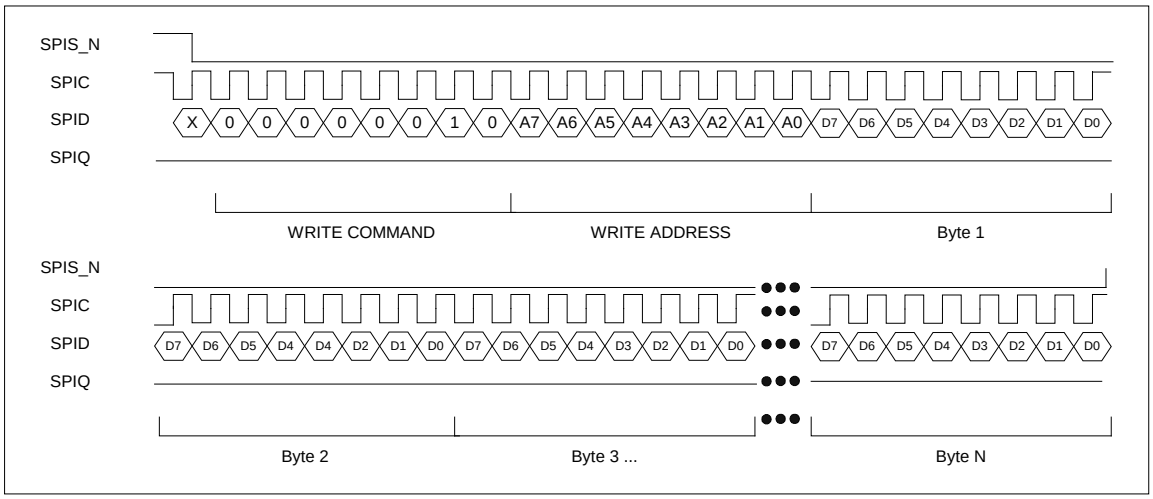



**Figure 11. SPI Multiple Write**

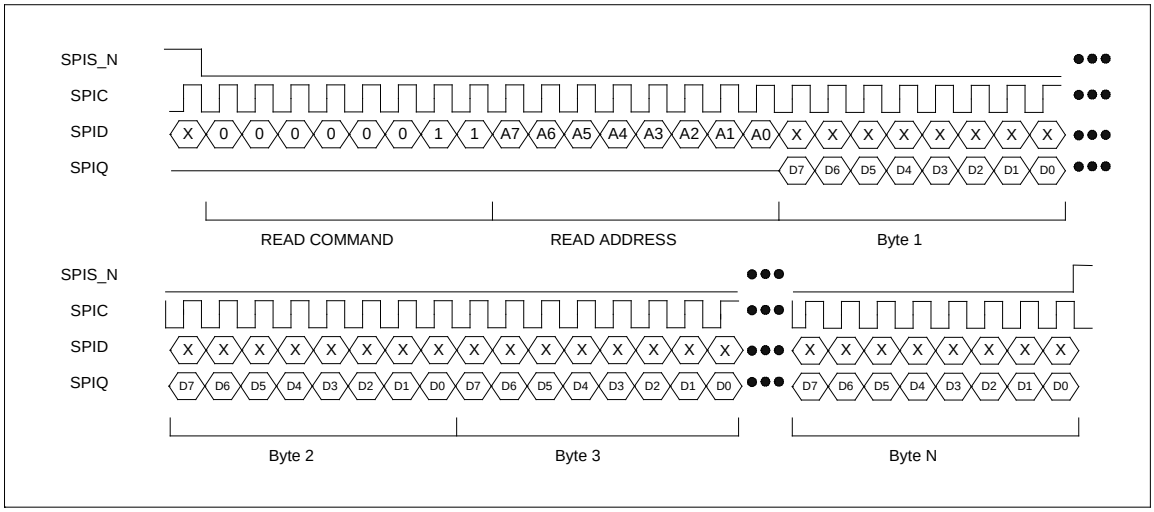



**Figure 12. SPI Multiple Read**

**Loopback Support**

The KSZ8873MLL/FLL/RLL provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports needs to be set to 100BASE-TX. Two types of loopback are supported: Far-end Loopback and Near-end (Remote) Loopback.

***Far-End Loopback***

Far-end loopback is conducted between the KSZ8873MLL/FLL/RLL's two PHY ports. The loopback is limited to a few packages at a time for diagnosis purpose and cannot support large traffic. The loopback path starts at the "Originating." PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit [0] of registers 29 and 45 is used to enable far-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 0, bit [14] can be used to enable far-end loopback.

The far-end loopback path is illustrated in Figure 13.

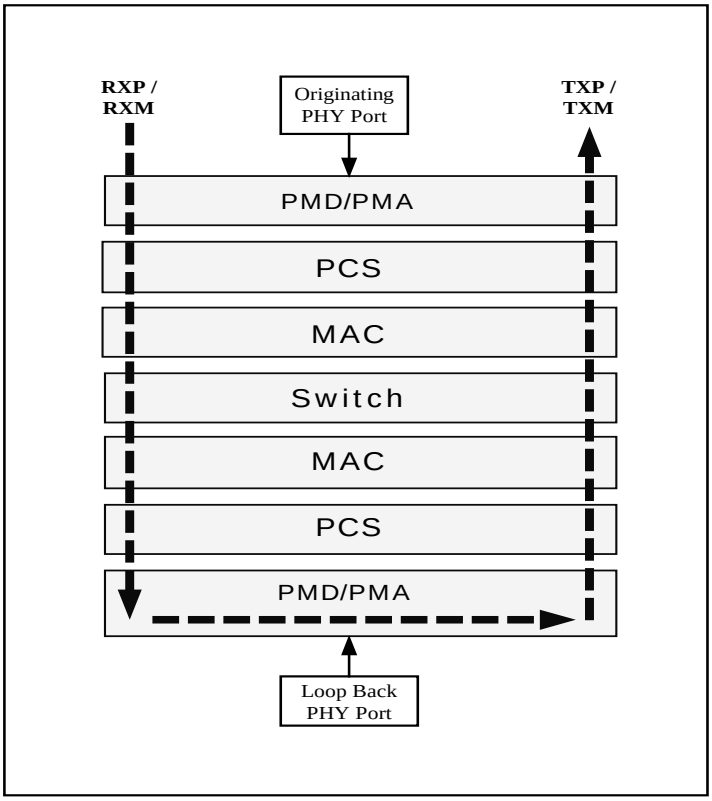



**Figure 13. Far-End Loopback Path**

***Near-End (Remote) Loopback***

Near-end (Remote) loopback is conducted at either PHY port 1 or PHY port 2.of the KSZ8873MLL/FLL/RLL. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers 26 and 42 is used to enable near-end loopback for ports 1 and 2, respectively. Alternatively, the MII Management register 31, bit [1] can be used to enable near-end loopback.

The near-end loopback paths are illustrated in Figure 14.

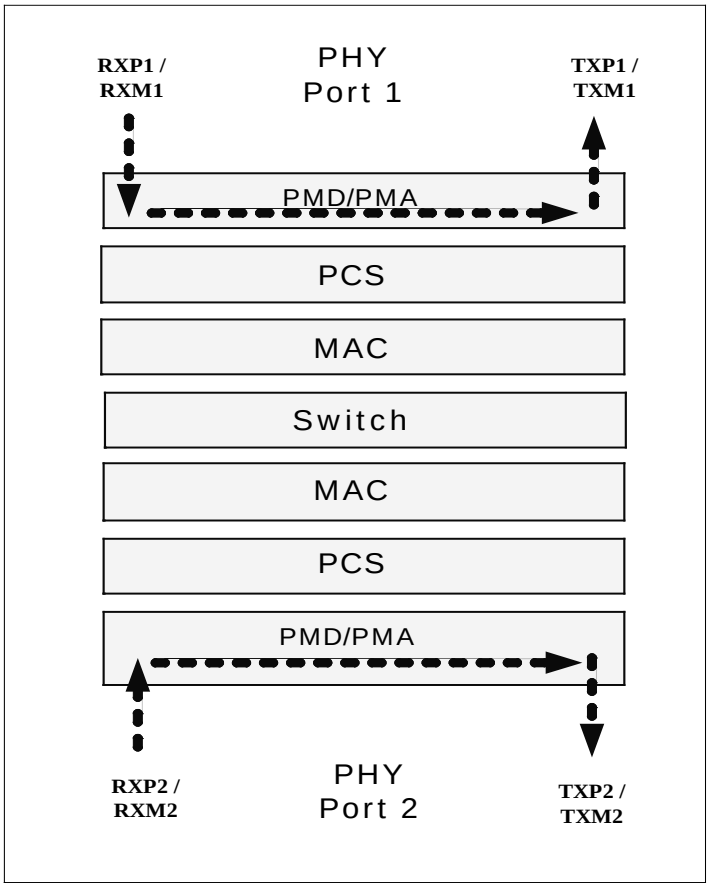



**Figure 14. Near-End (Remote) Loopback Path**

## MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers defined in this section. The SPI, $I^2C$, and SMI interfaces can also be used to access some of these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface.

The “PHYADs” by defaults are assigned “0x1” for PHY1 (port 1) and “0x2” for PHY2 (port 2). Additionally, these “PHYADs” can be programmed to the PHY addresses specified in bits[7:3] of Register 15 (0x0F): Global Control 13.

The “REGAD” supported are 0x0-0x5, 0x1D and 0x1F.

| Register Number | Description |
|---|---|
| PHYAD = 0x1, REGAD = 0x0 | PHY1 Basic Control Register |
| PHYAD = 0x1, REGAD = 0x1 | PHY1 Basic Status Register |
| PHYAD = 0x1, REGAD = 0x2 | PHY1 Physical Identifier I |
| PHYAD = 0x1, REGAD = 0x3 | PHY1 Physical Identifier II |
| PHYAD = 0x1, REGAD = 0x4 | PHY1 Auto-Negotiation Advertisement Register |
| PHYAD = 0x1, REGAD = 0x5 | PHY1 Auto-Negotiation Link Partner Ability Register |
| PHYAD = 0x1, 0x6 – 0x1C | PHY1 Not supported |
| PHYAD = 0x1, 0x1D | PHY1 Not supported |
| PHYAD = 0x1, 0x1E | PHY1 Not supported |
| PHYAD = 0x1, 0x1F | PHY1 Special Control/Status |
| PHYAD = 0x2, REGAD = 0x0 | PHY2 Basic Control Register |
| PHYAD = 0x2, REGAD = 0x1 | PHY2 Basic Status Register |
| PHYAD = 0x2, REGAD = 0x2 | PHY2 Physical Identifier I |
| PHYAD = 0x2, REGAD = 0x3 | PHY2 Physical Identifier II |
| PHYAD = 0x2, REGAD = 0x4 | PHY2 Auto-Negotiation Advertisement Register |
| PHYAD = 0x2, REGAD = 0x5 | PHY2 Auto-Negotiation Link Partner Ability Register |
| PHYAD = 0x2, 0x6 – 0x1C | PHY2 Not supported |
| PHYAD = 0x2, 0x1D | PHY2 LinkMD Control/Status |
| PHYAD = 0x2, 0x1E | PHY2 Not supported |
| PHYAD = 0x2, 0x1F | PHY2 Special Control/Status |

**PHY1 Register 0 (PHYAD = 0x1, REGAD = 0x0): MII Basic Control**

**PHY2 Register 0 (PHYAD = 0x2, REGAD = 0x0): MII Basic Control**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Soft reset | RO | NOT SUPPORTED | 0 | |
| 14 | Loopback | R/W | =1, Perform loopback, as indicated:<br>**Port 1 Loopback (reg. 29, bit 0 = '1')**<br>Start: RXP2/RXM2 (port 2)<br>Loopback: PMD/PMA of port 1's PHY<br>End: TXP2/TXM2 (port 2)<br>**Port 2 Loopback (reg. 45, bit 0 = '1')**<br>Start: RXP1/RXM1 (port 1)<br>Loopback: PMD/PMA of port 2's PHY<br>End: TXP1/TXM1 (port 1)<br>=0, Normal operation | 0 | Reg. 29, bit 0<br>Reg. 45, bit 0 |
| 13 | Force 100 | R/W | =1, 100 Mbps<br>=0, 10 Mbps | 0 | Reg. 28, bit 6<br>Reg. 44, bit 6 |
| 12 | AN enable | R/W | =1, Auto-negotiation enabled<br>=0, Auto-negotiation disabled | 1 | Reg. 28, bit 7<br>Reg. 44, bit 7 |
| 11 | Power down | R/W | =1, Power down<br>=0, Normal operation | 0 | Reg. 29, bit 3<br>Reg. 45, bit 3 |
| 10 | Isolate | RO | NOT SUPPORTED | 0 | |
| 9 | Restart AN | R/W | =1, Restart auto-negotiation<br>=0, Normal operation | 0 | Reg. 29, bit 5<br>Reg. 45, bit 5 |
| 8 | Force full duplex | R/W | =1, Full duplex<br>=0, Half duplex | 0 | Reg. 28, bit 5<br>Reg. 44, bit 5 |
| 7 | Collision test | RO | NOT SUPPORTED | 0 | |
| 6 | Reserved | RO | | 0 | |
| 5 | Hp_mdix | R/W | =1, HP Auto MDI/MDI-X mode<br>=0, Micrel Auto MDI/MDI-X mode | 1 | Reg. 31, bit 7<br>Reg. 47, bit 7 |
| 4 | Force MDI | R/W | =1, Force MDI (transmit on RXP / RXM pins)<br>=0, Normal operation (transmit on TXP / TXM pins) | 0 | Reg. 29, bit 1<br>Reg. 45, bit 1 |
| 3 | Disable MDIX | R/W | =1, Disable auto MDI-X<br>=0, Enable auto MDI-X | 0 | Reg. 29, bit 2<br>Reg. 45, bit 2 |
| 2 | Disable far-end fault | R/W | =1, Disable far-end fault detection<br>=0, Normal operation | 0 | Reg. 29, bit 4 |
| 1 | Disable transmit | R/W | =1, Disable transmit<br>=0, Normal operation | 0 | Reg. 29, bit 6<br>Reg. 45, bit 6 |
| 0 | Disable LED | R/W | =1, Disable LED<br>=0, Normal operation | 0 | Reg. 29, bit 7<br>Reg. 45, bit 7 |

**PHY1 Register 1 (PHYAD = 0x1, REGAD = 0x1): MII Basic Status**

**PHY2 Register 1 (PHYAD = 0x2, REGAD = 0x1): MII Basic Status**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | T4 capable | RO | =0, Not 100 BASE-T4 capable | 0 | |
| 14 | 100 Full capable | RO | =1, 100BASE-TX full duplex capable<br>=0, Not capable of 100BASE-TX full duplex | 1 | Always 1 |
| 13 | 100 Half capable | RO | =1, 100BASE-TX half duplex capable<br>=0, Not 100BASE-TX half duplex capable | 1 | Always 1 |
| 12 | 10 Full capable | RO | =1, 10BASE-T full duplex capable<br>=0, Not 10BASE-T full duplex capable | 1 | Always 1 |
| 11 | 10 Half capable | RO | =1, 10BASE-T half duplex capable<br>=0, Not 10BASE-T half duplex capable | 1 | Always 1 |
| 10-7 | Reserved | RO | | 0000 | |
| 6 | Preamble suppressed | RO | NOT SUPPORTED | 0 | |
| 5 | AN complete | RO | =1, Auto-negotiation complete<br>=0, Auto-negotiation not completed | 0 | Reg. 30, bit 6<br>Reg. 46, bit 6 |
| 4 | Far-end fault | RO | =1, Far-end fault detected<br>=0, No far-end fault detected | 0 | Reg. 31, bit 0 |
| 3 | AN capable | RO | =1, Auto-negotiation capable<br>=0, Not auto-negotiation capable | 1 | Reg. 28, bit 7<br>Reg. 44, bit 7 |
| 2 | Link status | RO | =1, Link is up<br>=0, Link is down | 0 | Reg. 30, bit 5<br>Reg. 46, bit 5 |
| 1 | Jabber test | RO | NOT SUPPORTED | 0 | |
| 0 | Extended capable | RO | =0, Not extended register capable | 0 | |

**PHY1 Register 2 (PHYAD = 0x1, REGAD = 0x2): PHYID High**

**PHY2 Register 2 (PHYAD = 0x2, REGAD = 0x2): PHYID High**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15-0 | PHYID high | RO | High order PHYID bits | 0x0022 |

**PHY1 Register 3 (PHYAD = 0x1, REGAD = 0x3): PHYID Low**

**PHY2 Register 3 (PHYAD = 0x2, REGAD = 0x3): PHYID Low**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15-0 | PHYID low | RO | Low order PHYID bits | 0x1430 |

**PHY1 Register 4 (PHYAD = 0x1, REGAD = 0x4): Auto-Negotiation Advertisement Ability**

**PHY2 Register 4 (PHYAD = 0x2, REGAD = 0x4): Auto-Negotiation Advertisement Ability**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Next page | RO | NOT SUPPORTED | 0 | |
| 14 | Reserved | RO | | 0 | |
| 13 | Remote fault | RO | NOT SUPPORTED | 0 | |
| 12-11 | Reserved | RO | | 00 | |
| 10 | Pause | R/W | =1, Advertise pause ability<br>=0, Do not advertise pause ability | 1 | Reg. 28, bit 4<br>Reg. 44, bit 4 |
| 9 | Reserved | R/W | | 0 | |
| 8 | Adv 100 Full | R/W | =1, Advertise 100 full duplex ability<br>=0, Do not advertise 100 full duplex ability | 1 | Reg. 28, bit 3<br>Reg. 44, bit 3 |
| 7 | Adv 100 Half | R/W | =1, Advertise 100 half duplex ability<br>=0, Do not advertise 100 half duplex ability | 1 | Reg. 28, bit 2<br>Reg. 44, bit 2 |
| 6 | Adv 10 Full | R/W | =1, Advertise 10 full duplex ability<br>=0, Do not advertise 10 full duplex ability | 1 | Reg. 28, bit 1<br>Reg. 44, bit 1 |
| 5 | Adv 10 Half | R/W | =1, Advertise 10 half duplex ability<br>=0, Do not advertise 10 half duplex ability | 1 | Reg. 28, bit 0<br>Reg. 44, bit 0 |
| 4-0 | Selector field | RO | 802.3 | 00001 | |

**PHY1 Register 5 (PHYAD = 0x1, REGAD = 0x5): Auto-Negotiation Link Partner Ability**

**PHY2 Register 5 (PHYAD = 0x2, REGAD = 0x5): Auto-Negotiation Link Partner Ability**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Next page | RO | NOT SUPPORTED | 0 | |
| 14 | LP ACK | RO | NOT SUPPORTED | 0 | |
| 13 | Remote fault | RO | NOT SUPPORTED | 0 | |
| 12-11 | Reserved | RO | | 00 | |
| 10 | Pause | RO | Link partner pause capability | 0 | Reg. 30, bit 4<br>Reg. 46, bit 4 |
| 9 | Reserved | RO | | 0 | |
| 8 | Adv 100 Full | RO | Link partner 100 full capability | 0 | Reg. 30, bit 3<br>Reg. 46, bit 3 |
| 7 | Adv 100 Half | RO | Link partner 100 half capability | 0 | Reg. 30, bit 2<br>Reg. 46, bit 2 |
| 6 | Adv 10 Full | RO | Link partner 10 full capability | 0 | Reg. 30, bit 1<br>Reg. 46, bit 1 |
| 5 | Adv 10 Half | RO | Link partner 10 half capability | 0 | Reg. 30, bit 0<br>Reg. 46, bit 0 |
| 4-0 | Reserved | RO | | 00000 | |

**PHY1 Register 29 (PHYAD = 0x1, REGAD = 0x1D): Not supported**

**PHY2 Register 29 (PHYAD = 0x2, REGAD = 0x1D): LinkMD Control/Status**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Vct_enable | R/W (SC) | =1, Enable cable diagnostic. After VCT test has completed, this bit will be self-cleared.<br>=0, Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read. | 0 | Reg. 42, bit 4 |
| 14-13 | Vct_result | RO | =00, Normal condition<br>=01, Open condition detected in cable<br>=10, Short condition detected in cable<br>=11, Cable diagnostic test has failed | 00 | Reg 42, bit[6:5] |
| 12 | Vct 10M Short | RO | =1, Less than 10 meter short | 0 | Reg. 42, bit 7 |
| 11-9 | Reserved | RO | Reserved | 000 | |
| 8-0 | Vct_fault_count | RO | Distance to the fault.<br>It's approximately 0.4m*vct_fault_count[8:0] | {0, (0x00)} | {(Reg. 42, bit 0),<br>(Reg. 43, bit[7:0])} |

**PHY1 Register 31 (PHYAD = 0x1, REGAD = 0x1F): PHY Special Control/Status**

**PHY2 Register 31 (PHYAD = 0x2, REGAD = 0x1F): PHY Special Control/Status**

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15-6 | Reserved | RO | Reserved | {(0x00),00} | |
| 5 | Polrvs | RO | =1, Polarity is reversed<br>=0, Polarity is not reversed | 0 | Reg. 31, bit 5<br>Reg. 47, bit 5<br>Note: This bit is only valid for 10BT |
| 4 | MDI-X status | RO | =1, MDI<br>=0, MDI-X | 0 | Reg. 30, bit 7<br>Reg. 46, bit 7 |
| 3 | Force_lnk | R/W | =1, Force link pass<br>=0, Normal Operation | 0 | Reg. 26, bit 3<br>Reg. 42, bit 3 |
| 2 | Pwrsave | R/W | =0, Enable power saving<br>=1, Disable power saving | 1 | Reg. 26, bit 2<br>Reg. 42, bit 2 |
| 1 | Remote Loopback | R/W | =1, Perform Remote loopback, as follows:<br>**Port 1 (reg. 26, bit 1 = '1')**<br>Start: RXP1/RXM1 (port 1)<br>Loopback: PMD/PMA of port 1's PHY<br>End: TXP1/TXM1 (port 1)<br>**Port 2 (reg. 42, bit 1 = '1')**<br>Start: RXP2/RXM2 (port 2)<br>Loopback: PMD/PMA of port 2's PHY<br>End: TXP2/TXM2 (port 2)<br>=0, Normal Operation | 0 | Reg. 26, bit 1<br>Reg. 42, bit 1 |
| 0 | Reserved | R/W | Reserved<br>Do not change the default value. | 0 | |

# Memory Map (8-Bit Registers)

### Global Registers

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 0-1 | 0x00-0x01 | Chip ID Registers |
| 2-15 | 0x02-0x0F | Global Control Registers |

### Port Registers

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 16-29 | 0x10-0x1D | Port 1 Control Registers, including MII PHY Registers |
| 30-31 | 0x1E-0x1F | Port 1 Status Registers, including MII PHY Registers |
| 32-45 | 0x20-0x2D | Port 2 Control Registers, including MII PHY Registers |
| 46-47 | 0x2E-0x2F | Port 2 Status Registers, including MII PHY Registers |
| 48-57 | 0x30-0x39 | Port 3 Control Registers |
| 58-62 | 0x3A-0x3E | Reserved |
| 63 | 0x3F | Port 3 Status Register |
| 64-95 | 0x40-0x5F | Reserved |

### Advanced Control Registers

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 96-111 | 0x60-0x6F | TOS Priority Control Registers |
| 112-117 | 0x70-0x75 | Switch Engine's MAC Address Registers |
| 118-120 | 0x76-0x78 | User Defined Registers |
| 121-122 | 0x79-0x7A | Indirect Access Control Registers |
| 123-131 | 0x7B-0x83 | Indirect Data Registers |
| 142-153 | 0x8E-0x99 | Station Address |
| 154-165 | 0x9A-0xA5 | Egress data rate limit |
| 166 | 0xA6 | Device mode indicator |
| 167-170 | 0xA7-0xAA | High-Priority Packet Buffer Reserved |
| 171-174 | 0xAB-0xAE | PM Usage Flow Control Select Mode |
| 175-186 | 0xAF-0xBA | TXQ Split |
| 187-188 | 0xBB-0xBC | Link Change Interrupt register |
| 189 | 0xBD | Force Pause Off Iteration Limit Enable |
| 192 | 0xC0 | Fiber Signal Threshold |
| 194 | 0xC2 | Insert SRC PVID |
| 195 | 0xC3 | Power Management and LED Mode |
| 196 | 0xC4 | Sleep Mode |
| 198 | 0xC6 | Forward Invalid VID Frame and Host Mode |

# Register Description

### Global Registers (Registers 0 – 15)

***Register 0 (0x00): Chip ID0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Family ID | RO | Chip family | 0x88 |

***Register 1 (0x01): Chip ID1 / Start Switch***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-4 | Chip ID | RO | 0x3 is assigned to M series. (73M) | 0x3 |
| 3-1 | Revision ID | RO | Revision ID | - |
| 0 | Start Switch | RW | =1, start the switch (default)<br>0=, stop the switch | 1 |

***Register 2 (0x02): Global Control 0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | New Back-off Enable | R/W | New back-off algorithm designed for UNH<br>=1, Enable<br>=0, Disable | 0 |
| 6 | Rserved | RO | Rserved | 0 |
| 5 | Flush Dynamic MAC Table | R/W | =1, Enable flush dynamic MAC table for spanning tree application<br>=0, Disable | 0 |
| 4 | Flush Static MAC Table | R/W | =1, Enable flush static MAC table for spanning tree application<br>=0, Disable | 0 |
| 3 | Pass Flow Control Packet | R/W | =1, Switch will pass 802.1x “flow control” packets<br>=0, Switch will drop 802.1x “flow control” packets | 0 |
| 2 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 1 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 0 | Reserved | RO | Rserved | 0 |

***Register 3 (0x03): Global Control 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Pass All Frames | R/W | =1, Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with sniffer mode only. | 0 |
| 6 | Port 3 Tail Tag Mode Enable | R/W | =1, Enable port 3 tail tag mode.<br>=0, Disable. | 0 |
| 5 | IEEE 802.3x Transmit Direction Flow Control Enable | R/W | =1, Will enable transmit direction flow control feature.<br>=0, Will not enable transmit direction flow control feature. Switch will not generate any flow control (PAUSE) frame. | 1 |
| 4 | IEEE 802.3x Receive Direction Flow Control Enable | R/W | =1, Will enable receive direction flow control feature.<br>=0, Will not enable receive direction flow control feature. Switch will not react to any flow control (PAUSE) frame it receives. | 1 |
| 3 | Frame Length Field Check | R/W | =1, Will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500).<br>=0, Not check | 0 |
| 2 | Aging Enable | R/W | =1, Enable age function in the chip<br>=0, Disable age function in the chip | 1 |
| 1 | Fast Age Enable | R/W | =1, Turn on fast age (800us) | 0 |
| 0 | Aggressive Back-Off Enable | R/W | =1, Enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard. | 0 |

***Register 4 (0x04): Global Control 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Unicast Port-VLAN Mismatch Discard | R/W | This feature is used with port-VLAN (described in reg. 17, reg. 33, …)<br>=1, All packets can not cross VLAN boundary<br>=0, Unicast packets (excluding unkown/multicast/ broadcast) can cross VLAN boundary<br>Note: Port mirroring is not supported if this bit is set to “0”. | 1 |
| 6 | Multicast Storm Protection Disable | R/W | =1, “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets will be regulated.<br>=0, “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = 1 packets. | 1 |
| 5 | Back Pressure Mode | R/W | =1, Carrier sense based backpressure is selected<br>=0, Collision based backpressure is selected | 1 |
| 4 | Flow Control and Back Pressure Fair Mode | R/W | =1, Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time.<br>=0, In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port. | 1 |
| 3 | No Excessive Collision Drop | R/W | =1, The switch will not drop packets when 16 or more collisions occur.<br>=0, The switch will drop packets when 16 or more collisions occur. | 0 |

***Register 4 (0x04): Global Control 2 (Continued)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 2 | Huge Packet Support | R/W | =1, Will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of this register.<br>=0, The max packet size will be determined by bit 1 of this register. | 0 |
| 1 | Legal Maximum Packet Size Check Enable | R/W | =0, Will accept packet sizes up to 1536 bytes (inclusive).<br>=1, 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped. | 0 |
| 0 | Reserved | R/W | Reserved<br>Do not change the default value. | 0 |

***Register 5 (0x05): Global Control 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | 802.1Q VLAN Enable | R/W | =1, 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation.<br>=0, 802.1Q VLAN is disabled. | 0 |
| 6 | IGMP Snoop Enable on Switch MII Interface | R/W | =1, IGMP snoop is enabled. All IGMP packets will be forwarded to the Switch MII port.<br>=0, IGMP snoop is disabled. | 0 |
| 5 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 4 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 3 | Weighted Fair Queue Enable | R/W | =0, Priority method set by the registers 175-186 bit [7]=0 for port 1, port 2 and port 3.<br>=1, Weighted Fair Queueing enabled. When all four queues have packets waiting to transmit, the bandwidth allocation is q3:q2:q1:q0 = 8:4:2:1.<br>If any queues are empty, the highest non-empty queue gets one more weighting. For example, if q2 is empty, q3:q2:q1:q0 becomes (8+1):0:2:1. | 0 |
| 2 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 1 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 0 | Sniff Mode Select | R/W | =1, Will do RX AND TX sniff (both source port and destination port need to match)<br>=0, Will do RX OR TX sniff (either source port or destination port needs to match). This is the mode used to implement RX only sniff. | 0 |

***Register 6 (0x06): Global Control 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 6 | Port 3 Duplex Mode Selection | R/W | =1, Enable Port 3 MII to half-duplex mode.<br>=0, Enable Port 3 MII to full-duplex mode. | 0<br>Pin P1LED0 strap option.<br>Pull-up(1): Half -duplex mode<br>Pull-down(0): Full-duplex mode (default)<br>Note: P1LED0 has internal pull-down. |
| 5 | Port 3 Flow Control Enable | R/W | =1, Enable full duplex flow control on Switch port 3 MII interface.<br>=0, Disable full duplex flow control on Switch port 3 MII interface. | 1<br>Pin P1LED1 strap option.<br>Pull- up(1): Enable flow control<br>Pull-down(0): Disable flow control<br>Note: P1LED1 has internal pull-up. |
| 4 | Port 3 Speed selection | R/W | =1, The port 3 MII switch interface is in 10Mbps mode<br>=0, The port 3 MII switch interface is in 100Mbps mode | 0<br>Pin P3SPD strap option.<br>Pull-up(1): Enable 10Mbps<br>Pull-down(0): Enable 100Mbps (default)<br>Note: P3SPD has internal pull-down. |
| 3 | Null VID Replacement | R/W | =1, Will replace NULL VID with port VID (12 bits)<br>=0, No replacement for NULL VID | 0 |
| 2-0 | Broadcast Storm Protection Rate[(1)]<br>Bit [10:8] | R/W | This register along with the next register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100BT or 500ms for 10BT. The default is 1%. | 000 |

***Register 7 (0x07): Global Control 5***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Broadcast Storm Protection Rate[(3)]<br>Bit [7:0] | R/W | This register along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100BT or 500ms for 10BT. The default is 1%. | 0x63 |

**Note:**

3. 100BT Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63.

***Register 8 (0x08): Global Control 6***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory Testing | RO | Reserved<br>Do not change the default values. | 0x00 |

***Register 9 (0x09): Global Control 7***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory Testing | RO | Reserved<br>Do not change the default values. | 0x24 |

***Register 10 (0x0A): Global Control 8***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory Testing | RO | Reserved<br>Do not change the default values. | 0x35 |

***Register 11 (0x0B): Global Control 9***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | CPU interface Clock Selection | R/W | =00, 31.25MHz supports SPI speed below 6MHz<br>=01, 62.5MHz supports SPI speed between 6MHz to 12.5MHz<br>=10, 125MHz supports SPI speed above 12.5MHz<br>Note: Lower clock speed will save more power consumption, It is better set to to 31.25MHz if SPI doesn't request a high speed. | 10 |
| 5-4 | Reserved | RO | N/A Don't change | 00 |
| 3-2 | Reserved | RO | N/A Don't change | 10 |
| 1 | Reserved | RO | N/A Don't change | 0 |
| 0 | Reserved | RO | N/A Don't change | 0 |

***Register 12 (0x0C): Global Control 10***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | Tag_0x3 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x3. | 01 |
| 5-4 | Tag_0x2 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x2. | 01 |
| 3-2 | Tag_0x1 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x1. | 00 |
| 1-0 | Tag_0x0 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x0. | 00 |

***Register 13 (0x0D): Global Control 11***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | Tag_0x7 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x7. | 11 |
| 5-4 | Tag_0x6 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x6. | 11 |
| 3-2 | Tag_0x5 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x5. | 10 |
| 1-0 | Tag_0x4 | R/W | IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x4. | 10 |

***Register 14 (0x0E): Global Control 12***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Unknown Packet Default Port Enable | R/W | Send packets with unknown destination MAC addresses to specified port(s) in bits [2:0] of this register.<br>=0, Disable<br>=1, Enable | 0 |
| 6 | Drive Strength of I/O Pad | R/W | =1, 16mA<br>=0, 8mA | 1 |
| 5 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 4 | Reserved | RO | Reserved | 0 |
| 3 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 2-0 | Unknown Packet Default Port | R/W | Specify which port(s) to send packets with unknown destination MAC addresses. This feature is enabled by bit [7] of this register.<br>Bit 2 stands for port 3.<br>Bit 1 stands for port 2.<br>Bit 0 stands for port 1.<br>An '1' includes a port.<br>An '0' excludes a port. | 111 |

***Register 15 (0x0F): Global Control 13***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-3 | PHY Address | R/W | 00000 : N/A<br>00001 : Port 1 PHY address is 0x1<br>00010 : Port 1 PHY address is 0x2<br>…<br>11101 : Port 1 PHY address is 0x29<br>11110 : N/A<br>11111 : N/A<br><br>Note:<br>Port 2 PHY address = (Port 1 PHY address) + 1 | 00001 |
| 2-0 | Reserved | RO | Reserved<br>Do not change the default values. | 000 |

**Port Registers (Registers 16 – 95)**

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

***Register 16 (0x10): Port 1 Control 0***

***Register 32 (0x20): Port 2 Control 0***

***Register 48 (0x30): Port 3 Control 0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Broadcast Storm Protection Enable | R/W | =1, Enable broadcast storm protection for ingress packets on port<br>=0, Disable broadcast storm protection | 0 |
| 6 | DiffServ Priority Classification Enable | R/W | =1, Enable DiffServ priority classification for ingress packets (IPv4) on port<br>=0, Disable DiffServ function | 0 |
| 5 | 802.1p Priority Classification Enable | R/W | =1, Enable 802.1p priority classification for ingress packets on port<br>=0, Disable 802.1p | 0 |

***Register 16 (0x10): Port 1 Control 0***

***Register 32 (0x20): Port 2 Control 0***

***Register 48 (0x30): Port 3 Control 0 (Continued)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 4-3 | Port-Based Priority Classification | R/W | =00, Ingress packets on port will be<br>classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify.<br>=01, Ingress packets on port will be<br>classified as priority 1 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify.<br>=10, Ingress packets on port will be<br>classified as priority 2 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify.<br>=11, Ingress packets on port will be<br>classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify.<br>Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority. | 00 |
| 2 | Tag Insertion | R/W | =1, When packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”.<br>=0, Disable tag insertion<br>Note: For the tag insertion available, the register 194 bits [5-0] have to be set first. | 0 |
| 1 | Tag Removal | R/W | =1, When packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags.<br>=0, Disable tag removal | 0 |
| 0 | TXQ Split Enable | R/W | =1, Split TXQ to 4 queue configuration. It cannot be enable at the same time with split 2 queue at register 18, 34,50 bit 7.<br>=0, No split, treated as 1 queue configuration | 0 |

***Register 17 (0x11): Port 1 Control 1***

***Register 33 (0x21): Port 2 Control 1***

***Register 49 (0x31): Port 3 Control 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Sniffer Port | R/W | =1, Port is designated as sniffer port and will transmit packets that are monitored.<br>=0, Port is a normal port | 0 |
| 6 | Receive Sniff | R/W | =1, All packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port”<br>=0, No receive monitoring | 0 |
| 5 | Transmit Sniff | R/W | =1, All packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port”<br>=0, No transmit monitoring | 0 |
| 4 | Double Tag | R/W | =1, All packets will be tagged with port default tag of ingress port regardless of the original packets are tagged or not<br>=0, Do not double tagged on all packets | 0 |
| 3 | User Priority Ceiling | R/W | =1, If the packet’s “user priority field” is greater than the “user priority field” in the port default tag register, replace the packet’s “user priority field” with the “user priority field” in the port default tag register.<br>=0, Do not compare and replace the packet’s ‘user priority field” | 0 |
| 2-0 | Port VLAN membership | R/W | Define the port’s egress port VLAN membership. The port can only communicate within the membership. Bit 2 stands for port 3, bit 1 stands for port 2, bit 0 stands for port 1.<br>An ‘1’ includes a port in the membership.<br>An ‘0’ excludes a port from membership. | 111 |

***Register 18 (0x12): Port 1 Control 2***

***Register 34 (0x22): Port 2 Control 2***

***Register 50 (0x32): Port 3 Control 2***

| Bit[4] | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Enable 2 Queue Split of Tx Queue | R/W | =1, Enable<br>It cannot be enabled at the same time with split 4 queue at register 16, 32, and 48 bit 0.<br>=0, Disable | 0 |
| 6 | Ingress VLAN Filtering | R/W | =1,The switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port.<br>=0, No ingress VLAN filtering. | 0 |
| 5 | Discard non PVID Packets | R/W | =1, The switch will discard packets whose VID does not match ingress port default VID.<br>=0, No packets will be discarded | 0 |

***Register 18 (0x12): Port 1 Control 2***

***Register 34 (0x22): Port 2 Control 2***

***Register 50 (0x32): Port 3 Control 2 (Continued)***

| Bit[4] | Name | R/W | Description | Default |
|---|---|---|---|---|
| 4 | Force Flow Control | R/W | =1, Will always enable full duplex flow control on the port, regardless of AN result.<br>=0, Full duplex flow control is enabled based on AN result. | Pin value during reset:<br>For port 1, P1FFC pin<br>For port 2, SMRXD30 pin<br>For port 3, this bit has no meaning. Flow control is set by Reg. 6 bit 5. |
| 3 | Back Pressure Enable | R/W | =1, Enable port's half duplex back pressure<br>=0, Disable port's half duplex back pressure | 0 |
| 2 | Transmit Enable | R/W | =1, Enable packet transmission on the port<br>=0, Disable packet transmission on the port | 1 |
| 1 | Receive Enable | R/W | =1, Enable packet reception on the port<br>=0, Disable packet reception on the port | 1 |
| 0 | Learning Disable | R/W | =1, Disable switch address learning capability<br>=0, Enable switch address learning | 0 |

**Note:**

4. Bits [2:0] are used for spanning tree support.

***Register 19[5] (0x13): Port 1 Control 3***

***Register 35 (0x23): Port 2 Control 3***

***Register 51 (0x33): Port 3 Control 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Default Tag [15:8] | R/W | Port's default tag, containing<br>7-5 : User priority bits<br>4 : CFI bit<br>3-0 : VID[11:8] | 0x00 |

***Register 20[5] (0x14): Port 1 Control 4***

***Register 36 (0x24): Port 2 Control 4***

***Register 52 (0x34): Port 3 Control 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Default Tag [7:0] | R/W | Port's default tag, containing<br>7-0 : VID[7:0] | 0x01 |

**Note:**

5. Registers 19 and 20 (and those corresponding to other ports) serve two purposes:
   a. Associated with the ingress untagged packets, and used for egress tagging.
   b. Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

***Register 21 (0x15): Port 1 Control 5***

***Register 37 (0x25): Port 2 Control 5***

***Register 53 (0x35): Port 3 Control 5***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Port 3 MII Mode Selection | R/W | =1, Port 3 MII MAC mode<br>=0, Port 3 MII PHY mode<br><br>Note:<br>Bit 7 is reserved in the port 1 and port 2 of the port register control 5. But request to set the register 21 port 1 control 5 bit [7] = '1' for better EMI, because this bit 7 of the register 21 is for port 1 MII of the MML part. In the MLL/FLL/RLL parts, setting this bit will disable the unused internal 25MHz clock for the unused port 1 MII PHY mode circuits. | Inversion of power strapped value of SMRXDV3. |
| 6 | Self-Address Filtering Enable MACA1 (not for 0x35) | R/W | =1, Enable port 1 self-address filtering MACA1<br>=0, Disable | 0 |

***Register 21 (0x15): Port 1 Control 5***

***Register 37 (0x25): Port 2 Control 5***

***Register 53 (0x35): Port 3 Control 5 (Continued)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 5 | Self-Address Filtering Enable<br>MACA2<br>(not for 0x35) | R/W | =1, Enable port 2 Self-address filtering MACA2<br>=0, Disable | 0 |
| 4 | Drop Ingress Tagged Frame | R/W | =1, Enable<br>=0, Disable | 0 |
| 3-2 | Limit Mode | R/W | **Ingress Limit Mode**<br>These bits determine what kinds of frames are limited and counted against ingress rate limiting.<br>=00, Limit and count all frames<br>=01, Limit and count Broadcast, Multicast, and flooded unicast frames<br>=10, Limit and count Broadcast and Multicast frames only<br>=11, Limit and count Broadcast frames only | 00 |
| 1 | Count IFG | R/W | **Count IFG Bytes**<br>=1, Each frame's minimum inter frame gap<br>(IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations.<br>=0, IFG bytes are not counted. | 0 |
| 0 | Count Pre | R/W | **Count Preamble Bytes**<br>=1, Each frame's preamble bytes (8 per<br>frame) are included in Ingress and Egress rate limiting calculations.<br>=0, Preamble bytes are not counted. | 0 |

***Register 22[6:0] (0x16): Port 1 Q0 Ingress Data Rate Limit***

***Register 38[6:0] (0x26): Port 2 Q0 Ingress Data Rate Limit***

***Register 54[6:0] (0x36): Port 3 Q0 Ingress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | RMII REFCLK INVERT | R/W | =1, Port 3 inverted refclk selected<br>=0, Port 3 original refclk selected<br><br>Note:<br>Bit 7 is available on port 3 in the RLL device. Other ports and devices will be reserved for this bit. | 0<br>Note: Not Applied to Reg.38(Port 2) |
| 6-0 | Q0 Ingress Data Rate limit | R/W | **Ingress data rate limit for priority 0 frames**<br>Ingress traffic from this priority queue is shaped according to the ingress Data Rate Limit Table. | 0 |

***Register 23[6:0] (0x17): Port 1 Q1 Ingress Data Rate Limit***

***Register 39[6:0] (0x27): Port 2 Q1 Ingress Data Rate Limit***

***Register 55[6:0] (0x37): Port 3 Q1 Ingress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q1 Ingress Data Rate Limit | R/W | **Ingress data rate limit for priority 1 frames**<br>Ingress traffic from this priority queue is shaped according to the ingress Data Rate Limit Table. | 0 |

***Register 24[6:0] (0x18): Port 1 Q2 Ingress Data Rate Limit***

***Register 40[6:0] (0x28): Port 2 Q2 Ingress Data Rate Limit***

***Register 56[6:0] (0x38): Port 3 Q2 Ingress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q2 Ingress Data Rate Limit | R/W | **Ingress data rate limit for priority 2 frames**<br>Ingress traffic from this priority queue is shaped according to ingress Data Rate Limit Table. | 0 |

***Register 25[6:0] (0x19): Port 1 Q3 Ingress Data Rate Limit***

***Register 41[6:0] (0x29): Port 2 Q3 Ingress Data Rate Limit***

***Register 57[6:0] (0x39): Port 3 Q3 Ingress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q3 Ingress Data Rate Limit | R/W | **Ingress data rate limit for priority 3 frames**<br>Ingress traffic from this priority queue is shaped according to ingress Data Rate Limit Table. | 0 |

**Note:**

Most of the contents in registers 26-31 and registers 42-47 for ports 1 and 2, respectively, can also be accessed with the MIIM PHY registers.

**Table 15. Data Rate Limit Table**

| Data Rate Limit for Ingress or Egress | 100BT<br>Register bit[6:0], Q=0..3 | 10BT<br>Register bit[6:0], Q=0..3 |
|---|---|---|
| | 1 to 0x63 for the Rate<br>1Mbps to 99Mbps. | 1 to 0x09 for the rate<br>1Mbps to 9Mbps |
| | 0 or 0x64 for the rate<br>100Mbps | 0 or 0x0A for the rate<br>10Mbps |
| 64 Kbps | 0x65 | |
| 128 Kbps | 0x66 | |
| 192 Kbps | 0x67 | |
| 256 Kbps | 0x68 | |
| 320 Kbps | 0x69 | |
| 384 Kbps | 0x6A | |
| 448 Kbps | 0x6B | |
| 512 Kbps | 0x6C | |
| 576 Kbps | 0x6D | |
| 640 Kbps | 0x6E | |
| 704 Kbps | 0x6F | |
| 768 Kbps | 0x70 | |
| 832 Kbps | 0x71 | |
| 896 Kbps | 0x72 | |
| 960 Kbps | 0x73 | |

***Register 26 (0x1A): Port 1 PHY Special Control/Status***

***Register 42 (0x2A): Port 2 PHY Special Control/Status***

***Register 58 (0x3A): Reserved, Not Applied to Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Vct 10M Short | RO | = 1, Less than 10 meter short | 0 |
| 6-5 | Vct_result | RO | = 00, Normal condition<br>= 01, Open condition detected in cable<br>= 10, Short condition detected in cable<br>= 11, Cable diagnostic test has failed | 00 |
| 4 | Vct_en | R/W (SC) | = 1, Enable cable diagnostic test. After VCT test has completed, this bit will be self-cleared.<br>= 0, Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read. | 0 |
| 3 | Force_lnk | R/W | = 1, Force link pass<br>= 0, Normal Operation | 0 |
| 2 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 1 | Remote Loopback | R/W | = 1, Perform Remote loopback, as follows:<br>**Port 1 (reg. 26, bit 1 = '1')**<br>Start: RXP1/RXM1 (port 1)<br>Loopback: PMD/PMA of port 1's PHY<br>End: TXP1/TXM1 (port 1)<br>**Port 2 (reg. 42, bit 1 = '1')**<br>Start: RXP2/RXM2 (port 2)<br>Loopback: PMD/PMA of port 2's PHY<br>End: TXP2/TXM2 (port 2)<br>= 0, Normal Operation | 0 |
| 0 | Vct_fault_count[8] | RO | **Bit[8] of VCT fault count**<br>Distance to the fault.<br>It's approximately 0.4m*vct_fault_count[8:0] | 0 |

***Register 27 (0x1B): Port 1 Not Support***

***Register 43 (0x2B): LinkMD Result***

***Register 59 (0x3B): Reserved, Not Applied to Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Vct_fault_count[7:0] | RO | **Bits[7:0] of VCT fault count**<br>Distance to the fault.<br>It's approximately 0.4m*Vct_fault_count[8:0] | 0x00 |

***Register 28 (0x1C): Port 1 Control 12***

***Register 44 (0x2C): Port 2 Control 12***

***Register 60 (0x3C): Reserved, Not Applied to Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Auto Negotiation Enable | R/W | =1, Auto negotiation is on<br>=0, Disable auto negotiation; speed and duplex are determined by bits 6 and 5 of this register. | 1<br>For port 1, P1ANEN pin value during reset.<br>For port 2, SMRXD33 pin value during reset |
| 6 | Force Speed | R/W | =1, Forced 100BT if AN is disabled (bit 7)<br>=0, Forced 10BT if AN is disabled (bit 7) | 1<br>For port 1, P1SPD pin value during reset.<br>For port 2, SMRXD32 pin value during reset. |
| 5 | Force Duplex | R/W | =1, Forced full duplex if (1) AN is disabled or (2) AN is enabled but failed.<br>=0, Forced half duplex if (1) AN is disabled or (2) AN is enabled but failed.<br>Note: This bit or strap pin should be set to '0' for the correct duplex mode indication of LED and register status when the link-up is AN to force mode. | 1<br>For port 1, P1DPX pin value during reset.<br>For port 2, SMRXD31 pin value during reset. |
| 4 | Advertise Flow Control capability | R/W | =1, Advertise flow control (pause) capability<br>=0, Suppress flow control (pause) capability from transmission to link partner | 1 |
| 3 | Advertise 100BT Full Duplex Capability | R/W | =1, Advertise 100BT full duplex capability<br>=0, Suppress 100BT full duplex capability from transmission to link partner | 1 |
| 2 | Advertise 100BT Half Duplex Capability | R/W | =1, Advertise 100BT half-duplex capability<br>=0, Suppress 100BT half-duplex capability from transmission to link partner | 1 |
| 1 | Advertise 10BT Full Duplex Capability | R/W | =1, Advertise 10BT full duplex capability<br>=0, Suppress 10BT full duplex capability from transmission to link partner | 1 |
| 0 | Advertise 10BT Half Duplex Capability | R/W | =1, Advertise 10BT half-duplex capability<br>=0, Suppress 10BT half-duplex capability from transmission to link partner | 1 |

***Register 29 (0x1D): Port 1 Control 13***

***Register 45 (0x2D): Port 2 Control 13***

***Register 61 (0x3D): Reserved, Not Applied to Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | LED Off | R/W | =1, Turn off all port's LEDs (LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one.<br>=0, Normal operation | 0 |
| 6 | Txdis | R/W | =1, Disable the port's transmitter<br>=0, Normal operation | 0 |
| 5 | Restart AN | R/W | =1, Restart auto-negotiation<br>=0, Normal operation | 0 |
| 4 | Disable Far-end Fault | R/W | =1, Disable far-end fault detection and pattern transmission.<br>=0, Enable far-end fault detection and pattern transmission | 0 |
| 3 | Power Down | R/W | =1, Power down<br>=0, Normal operation | 0 |
| 2 | Disable Auto MDI/MDI-X | R/W | =1, Disable auto MDI/MDI-X function<br>=0, Enable auto MDI/MDI-X function | 0 |
| 1 | Force MDI | R/W | If auto MDI/MDI-X is disabled,<br>=1, Force PHY into MDI mode (transmit on RXP/RXM pins)<br>=0, Force PHY into MDI-X mode (transmit on TXP/TXM pins) | 0 |
| 0 | Loopback | R/W | =1, Perform loopback, as indicated:<br>**Port 1 Loopback (reg. 29, bit 0 = '1')**<br>Start: RXP2/RXM2 (port 2)<br>Loopback: PMD/PMA of port 1's PHY<br>End: TXP2/TXM2 (port 2)<br>**Port 2 Loopback (reg. 45, bit 0 = '1')**<br>Start: RXP1/RXM1 (port 1)<br>Loopback: PMD/PMA of port 2's PHY<br>End: TXP1/TXM1 (port 1)<br>=0, Normal operation | 0 |

***Register 30 (0x1E): Port 1 Status 0***

***Register 46 (0x2E): Port 2 Status 0***

***Register 62 (0x3E): Reserved, Not Applied to Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | MDI-X Status | RO | =1, MDI<br>=0, MDI-X | 0 |
| 6 | AN Done | RO | =1, Auto-negotiation completed<br>=0, Auto-negotiation not completed | 0 |
| 5 | Link Good | RO | =1, Link good<br>=0, Link not good | 0 |
| 4 | Partner Flow Control Capability | RO | =1, Link partner flow control (pause) capable<br>=0, Link partner not flow control (pause) capable | 0 |
| 3 | Partner 100BT Full Duplex Capability | RO | =1, Link partner 100BT full duplex capable<br>=0, Link partner not 100BT full duplex capable | 0 |
| 2 | Partner 100BT Half Duplex Capability | RO | =1, Link partner 100BT half duplex capable<br>=0, Link partner not 100BT half duplex capable | 0 |
| 1 | Partner 10BT Full Duplex Capability | RO | =1, Link partner 10BT full duplex capable<br>=0, Link partner not 10BT full duplex capable | 0 |
| 0 | Partner 10BT Half Duplex Capability | RO | =1, Link partner 10BT half duplex capable<br>=0, Link partner not 10BT half duplex capable | 0 |

***Register 31 (0x1F): Port 1 Status 1***

***Register 47 (0x2F): Port 2 Status 1***

***Register 63 (0x3F): Port 3 Status 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Hp_mdix | R/W | =1, HP Auto MDI/MDI-X mode<br>=0, Micrel Auto MDI/MDI-X mode | 1<br>Note: Only ports 1 and 2 are PHY ports.<br>This bit is not applicable to port 3 (MII). |
| 6 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 5 | Polrvs | RO | =1, Polarity is reversed<br>=0, Polarity is not reversed | 0<br>Note: This bit is not applicable to port 3 (MII).<br>This bit is only valid for 10BT |
| 4 | Transmit Flow Control Enable | RO | =1, Transmit flow control feature is active<br>=0, Transmit flow control feature is inactive | 0 |
| 3 | Receive Flow Control Enable | RO | =1, Receive flow control feature is active<br>=0, Receive flow control feature is inactive | 0 |
| 2 | Operation Speed | RO | =1, Link speed is 100Mbps<br>=0, Link speed is 10Mbps | 0 |
| 1 | Operation Duplex | RO | =1, Link duplex is full<br>=0, Link duplex is half | 0 |
| 0 | Far-end Fault | RO | =1, Far-end fault status detected<br>=0, No Far-end fault status detected | 0<br>This bit is applicable to port 1 only. |

***Register 67 (0x43): Reset***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 4 | Software Reset | R/W | =1, Software reset<br>=0, Clear<br>Note: Software reset will reset all registers to the initial values of the power-on reset or warm reset (keep the strap values). | 0 |
| 0 | PCS Reset | R/W | =1, PCS reset is used when is doing software reset for a compelete reset<br>=0, Clear<br>Note: PCS reset will reset the state machine and clock domain in PHY's PCS layer. | 0 |

**Advanced Control Registers (Registers 96-198)**

The IPv4/IPv6 type-of-service (ToS) Priority Control Registers implement a fully decoded, 128-bit differentiated services code point (DSCP ) register set that is used to determine priority from the ToS field in the IP header. The most significant 6 bits of the ToS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority.

***Register 96 (0x60): TOS Priority Control Register 0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[7:6] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x03. | 00 |
| 5-4 | DSCP[5:4] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x02. | 00 |
| 3-2 | DSCP[3:2] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x01. | 00 |
| 1-0 | DSCP[1:0] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x00. | 00 |

***Register 97 (0x61): TOS Priority Control Register 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[15:14] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x07. | 00 |
| 5-4 | DSCP[13:12] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x06. | 00 |
| 3-2 | DSCP[11:10] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x05. | 00 |
| 1-0 | DSCP[9:8] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x04. | 00 |

***Register 98 (0x62): TOS Priority Control Register 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[23:22] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0B. | 00 |
| 5-4 | DSCP[21:20] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0A. | 00 |
| 3-2 | DSCP[19:18] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x09. | 00 |
| 1-0 | DSCP[17:16] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x08. | 00 |

***Register 99 (0x63): TOS Priority Control Register 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[31:30] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0F. | 00 |
| 5-4 | DSCP[29:28] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0E. | 00 |
| 3-2 | DSCP[27:26] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0D. | 00 |
| 1-0 | DSCP[25:24] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x0C. | 00 |

***Register 100 (0x64): TOS Priority Control Register 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[39:38] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x13. | 00 |
| 5-4 | DSCP[37:36] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x12. | 00 |
| 3-2 | DSCP[35:34] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x11. | 00 |
| 1-0 | DSCP[33:32] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x10. | 00 |

***Register 101 (0x65): TOS Priority Control Register 5***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[47:46] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x17. | 00 |
| 5-4 | DSCP[45:44] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x16. | 00 |
| 3-2 | DSCP[43:42] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x15. | 00 |
| 1-0 | DSCP[41:40] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x14. | 00 |

***Register 102 (0x66): TOS Priority Control Register 6***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[55:54] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1B. | 00 |
| 5-4 | DSCP[53:52] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1A. | 00 |
| 3-2 | DSCP[51:50] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x19. | 00 |
| 1-0 | DSCP[49:48] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x18. | 00 |

***Register 103 (0x67): TOS Priority Control Register 7***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[63:62] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1F. | 00 |
| 5-4 | DSCP[61:60] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1E. | 00 |
| 3-2 | DSCP[59:58] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1D. | 00 |
| 1-0 | DSCP[57:56] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x1C. | 00 |

***Register 104 (0x68): TOS Priority Control Register 8***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[71:70] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x23. | 00 |
| 5-4 | DSCP[69:68] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x22. | 00 |
| 3-2 | DSCP[67:66] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x21. | 00 |
| 1-0 | DSCP[65:64] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x20. | 00 |

***Register 105 (0x69): TOS Priority Control Register 9***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[79:78] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x27. | 00 |
| 5-4 | DSCP[77:76] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x26. | 00 |
| 3-2 | DSCP[75:74] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x25. | 00 |
| 1-0 | DSCP[73:72] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x24. | 00 |

***Register 106 (0x6A): TOS Priority Control Register 10***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[87:86] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2B. | 00 |
| 5-4 | DSCP[85:84] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2A. | 00 |
| 3-2 | DSCP[83:82] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x29. | 00 |
| 1-0 | DSCP[81:80] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x28. | 00 |

***Register 107 (0x6B): TOS Priority Control Register 11***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[95:94] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2F. | 00 |
| 5-4 | DSCP[93:92] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2E. | 00 |
| 3-2 | DSCP[91:90] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2D. | 00 |
| 1-0 | DSCP[89:88] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x2C. | 00 |

***Register 108 (0x6C): TOS Priority Control Register 12***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[103:102] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x33. | 00 |
| 5-4 | DSCP[101:100] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x32. | 00 |
| 3-2 | DSCP[99:98] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x31. | 00 |
| 1-0 | DSCP[97:96] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x30. | 00 |

***Register 109 (0x6D): TOS Priority Control Register 13***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[111:110] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x37. | 00 |
| 5-4 | DSCP[109:108] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x36. | 00 |
| 3-2 | DSCP[107:106] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x35. | 00 |
| 1-0 | DSCP[105:104] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x34. | 00 |

***Register 110 (0x6E): TOS Priority Control Register 14***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[119:118] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3B. | 00 |
| 5-4 | DSCP[117:116] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3A. | 00 |
| 3-2 | DSCP[115:114] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x39. | 00 |
| 1-0 | DSCP[113:112] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x38. | 00 |

***Register 111 (0x6F): TOS Priority Control Register 15***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | DSCP[127:126] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3F. | 00 |
| 5-4 | DSCP[125:124] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3E. | 00 |
| 3-2 | DSCP[123:122] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3D. | 00 |
| 1-0 | DSCP[121:120] | R/W | The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x3C. | 00 |

**Registers 112 to 117**

Registers 112 to 117 contain the switch engine's MAC address. This 48-bit address is used as the Source Address for the MAC's full duplex flow control (PAUSE) frame.

**Register 112 (0x70): MAC Address Register 0**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[47:40] | R/W | | 0x00 |

***Register 113 (0x71): MAC Address Register 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[39:32] | R/W | | 0x10 |

***Register 114 (0x72): MAC Address Register 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[31:24] | R/W | | 0xA1 |

***Register 115 (0x73): MAC Address Register 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[23:16] | R/W | | 0xFF |

***Register 116 (0x74): MAC Address Register 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[15:8] | R/W | | 0xFF |

***Register 117 (0x75): MAC Address Register 5***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[7:0] | R/W | | 0xFF |

**Registers 118 to 120**

Registers 118 to 120 are User Defined Registers (UDRs). These are general purpose read/write registers that can be used to pass user defined control and status information between the KSZ8873 and the external processor.

***Register 118 (0x76): User Defined Register 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR1 | R/W | | 0x00 |

***Register 119 (0x77): User Defined Register 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR2 | R/W | | 0x00 |

***Register 120 (0x78): User Defined Register 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR3 | R/W | | 0x00 |

**Registers 121 to 131**

Registers 121 to 131 provide read and write access to the static MAC address table, VLAN table, dynamic MAC address table, and MIB counters.

***Register 121 (0x79): Indirect Access Control 0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-5 | Reserved | R/W | Reserved<br>Do not change the default values. | 000 |
| 4 | Read High / Write Low | R/W | =1, Read cycle<br>=0, Write cycle | 0 |
| 3-2 | Table Select | R/W | =00, Static MAC address table selected<br>=01, VLAN table selected<br>=10, Dynamic MAC address table selected<br>=11, MIB counter selected | 00 |
| 1-0 | Indirect Address High | R/W | Bits [9:8] of indirect address | 00 |

***Register 122 (0x7A): Indirect Access Control 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Address Low | R/W | Bits [7:0] of indirect address | 0000_0000 |

**Note:**

A write to register 122 triggers the read/write command. Read or write access is determined by register 121 bit 4.

***Register 123 (0x7B): Indirect Data Register 8***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | CPU Read Status | RO | This bit is applicable only for dynamic MAC address table and MIB counter reads.<br>=1, Read is still in progress<br>=0, Read has completed | 0 |
| 6-3 | Reserved | RO | Reserved | 0000 |
| 2-0 | Indirect Data [66:64] | RO | Bits [66:64] of indirect data | 000 |

***Register 124 (0x7C): Indirect Data Register 7***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [63:56] | R/W | Bits [63:56] of indirect data | 0000_0000 |

***Register 125 (0x7D): Indirect Data Register 6***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [55:48] | R/W | Bits [55:48] of indirect data | 0000_0000 |

***Register 126 (0x7E): Indirect Data Register 5***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [47:40] | R/W | Bits [47:40] of indirect data | 0000_0000 |

***Register 127 (0x7F): Indirect Data Register 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [39:32] | R/W | Bits [39:32] of indirect data | 0000_0000 |

***Register 128 (0x80): Indirect Data Register 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [31:24] | R/W | Bits [31:24] of indirect data | 0000_0000 |

***Register 129 (0x81): Indirect Data Register 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [23:16] | R/W | Bits [23:16] of indirect data | 0000_0000 |

***Register 130 (0x82): Indirect Data Register 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [15:8] | R/W | Bits [15:8] of indirect data | 0000_0000 |

***Register 131 (0x83): Indirect Data Register 0***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect Data [7:0] | R/W | Bits [7:0] of indirect data | 0000_0000 |

***Register 147~142(0x93~0x8E): Station MAC Address 1 MACA1***

***Register 153~148 (0x99~0x94): Station MAC Address 2 MACA2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47-0 | Station address | R/W | 48-bit Station address MACA1 and MACA2.<br><br>Note: This address is used for self MAC address filtering, see the port register control 5 bits [6,5] for detail. | 48'h0<br>Note: the MSB bit[47-40] of the MAC is the register 147 and 153.<br>The LSB bit[7-0] of MAC is the register 142 and 148. |

***Register 154[6:0] (0x9A): Port 1 Q0 Egress Data Rate Limit***

***Register 158[6:0] (0x9E): Port 2 Q0 Egress Data Rate Limit***

***Register 162[6:0] (0xA2): Port 3 Q0 Egress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Egress Rate Limit Flow Control Enable | R/W | =1, Enable egress rate limit flow control.<br>=0, Disable | 0 |
| 6-0 | Q0 Egress Data Rate limit | R/W | **Egress data rate limit for priority 0 frames**<br>Egress traffic from this priority queue is shaped according to the Data Rate Limit Table. | 0 |

***Register 155[6:0] (0x9B): Port 1 Q1 Egress Data Rate Limit***

***Register 159[6:0] (0x9F): Port 2 Q1 Egress Data Rate Limit***

***Register 163[6:0] (0xA3): Port 3 Q1 Egress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q1 Egress data Rate limit | R/W | **Egress data rate limit for priority 1 frames**<br>Egress traffic from this priority queue is shaped according to the Data Rate Limit Table. | 0 |

***Register 156[6:0] (0x9C): Port 1 Q2 Egress Data Rate Limit***

***Register 160[6:0] (0xA0): Port 2 Q2 Egress Data Rate Limit***

***Register 164[6:0] (0xA4): Port 3 Q2 Egress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q2 Egress Data Rate limit | R/W | **Egress data rate limit for priority 2 frames**<br>Egress traffic from this priority queue is shaped according to the Data Rate Limit Table. | 0 |

***Register 157[6:0] (0x9D): Port 1 Q3 Egress Data Rate Limit***

***Register 161[6:0] (0xA1): Port 2 Q3 Egress Data Rate Limit***

***Register 165[6:0] (0xA5): Port 3 Q3 Egress Data Rate Limit***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 6-0 | Q3 Egress Data Rate limit | R/W | **Egress data rate limit for priority 3 frames**<br>Egress traffic from this priority queue is shaped according to the Data Rate Limit Table. | 0 |

***Register 166 (0xA6): KSZ8873 Mode Indicator***

| Bit | Name | RO | Description | Default |
|---|---|---|---|---|
| 7-0 | KSZ8873 Mode Indicator | RO | bit7: 1: 2 MII mode<br>bit6: 1: 48P pkg of 2 PHY mode<br>bit5: 1: Reserved 0: Reserved<br>bit4: 1: Port 3 RMII 0: Port 3 MII<br>bit3: 1: Reserved 0: Reserved<br>bit2: 1: Port 3 MAC MII 0: Port 3 PHY MII<br>bit1: 1: Port 1 Copper 0: Port 1 Fiber<br>bit0: 1: Port 2 Copper 0: Port 2 Fiber | 0x03 MLL<br>0x13 RLL<br>0x00FLL |

***Register 167 (0xA7): High-Priority Packet Buffer Reserved for Q3***

| Bit | Name | RW | Description | Default |
|---|---|---|---|---|
| 7-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x45 |

***Register 168 (0xA8): High-Priority Packet Buffer Reserved for Q2***

| Bit | Name | RW | Description | Default |
|---|---|---|---|---|
| 7-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x35 |

***Register 169 (0xA9): High-Priority Packet Buffer Reserved for Q1***

| Bit | Name | RW | Description | Default |
|---|---|---|---|---|
| 7-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x25 |

***Register 170 (0xAA): High-Priority Packet Buffer Reserved for Q0***

| Bit | Name | RW | Description | Default |
|---|---|---|---|---|
| 7-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x15 |

***Register 171 (0xAB): PM Usage Flow Control Select Mode 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 6 | Reserved | RO | Reserved<br>Do not change the default values. | 1 |
| 5-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x18 |

***Register 172 (0xAC): PM Usage Flow Control Select Mode 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 5-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x10 |

***Register 173 (0xAD): PM Usage Flow Control Select Mode 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | Reserved | RO | Reserved<br>Do not change the default values. | 00 |
| 5-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x08 |

***Register 174 (0xAE): PM Usage Flow Control Select Mode 4***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-4 | Reserved | RO | Reserved<br>Do not change the default values. | 0 |
| 3-0 | Reserved | RO | Reserved<br>Do not change the default values. | 0x05 |

***Register 175 (0xAF): TXQ Split for Q3 in Port 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 176/177/178 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 176/177/178 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 8 |

***Register 176 (0xB0): TXQ Split for Q2 in Port 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 175/177/178 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 175/177/178 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 4 |

***Register 177 (0xB1): TXQ Split for Q1 in Port 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 175/176/178 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 175/176/178 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 2 |

***Register 178 (0xB2): TXQ Split for Q0 in Port 1***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 175/176/177 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 175/176/177 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 1 |

***Register 179 (0xB3): TXQ Split for Q3 in Port 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 180/181/182 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 180/181/182 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 8 |

***Register 180 (0xB4): TXQ Split for Q2 in Port 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 179/181/182 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 179/181/182 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 4 |

***Register 181 (0xB5): TXQ Split for Q1 in Port 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 179/180/182 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 179/180/182 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 2 |

***Register 182 (0xB6): TXQ Split for Q0 in Port 2***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 179/180/181 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 179/180/181 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 1 |

***Register 183 (0xB7): TXQ Split for Q3 Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 184/185/186 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 184/185/186 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 8 |

***Register 184 (0xB8): TXQ Split for Q2 Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 183/185/186 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 183/185/186 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 4 |

***Register 185 (0xB9): TXQ Split for Q1 in Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 183/184/186 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 183/184/186 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 2 |

***Register 186 (0xBA): TXQ Split for Q0 in Port 3***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Priority Select | R/W | 0 = enable straight priority with Reg 183/184/185 bits[7]=0 and Reg 5 bit[3]=0 for higher priority first<br>1= priority ratio is 8:4:2:1 for 4 queues and 2:1 for 2 queues with Reg 183/184/185 bits[7]=1. | 1 |
| 6:0 | Reserved | RO | Reserved<br>Do not change the default values. | 1 |

***Register 187 (0xBB): Interrupt Enable Register***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Interrupt Enable Register | R/W | Interrupt enable register corresponding to bits in Register 188<br>Note: Set register 187 first and then set register 188 (W1C= Write ‘1’ Clear) to wait the interrupt at Pin 35 INTRN for the link to be changed. | 0x00 |

***Register 188 (0xBC): Link Change Interrupt***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | P1 or P2 Link Change (LC) Interrupt | R/W | Set to 1 when P1 or P2 link changes in analog interface (W1C). | 0 |
| 6-3 | Reserved | R/W | Reserved<br>Do not change the default values. | 0 |
| 2 | P3 Link Change (LC) Interrupt | R/W | Set to 1 when P3 link changes in MII interface (W1C). | 0 |
| 1 | P2 Link Change (LC) Interrupt | R/W | Set to 1 when P2 link changes in analog interface (W1C). | 0 |
| 0 | P1 MII Link Change (LC) Interrupt | R/W | Set to 1 when P1 link changes in analog interface or MII interface (W1C). | 0 |

***Register 189 (0xBD): Force Pause Off Iteration Limit Enable***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Force Pause Off Iteration Limit Enable | R/W | =1, Enable, It is 160ms before requesting to invalidate flow control.<br>=0, Disable | 0 |

***Register 192 (0xC0): Fiber Signal Threshold***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Port 2 Fiber Signal Threshold | R/W | =1, Threshold is 2.0V<br>=0, Threshold is 1.2V | 0 |
| 6 | Port 1 Fiber Signal Threshold | R/W | =1, Threshold is 2.0V<br>=0, Threshold is 1.2V | 0 |
| 5-0 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |

***Register 193 (0xC1): Internal 1.8V LDO Control***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 6 | Internal 1.8V LDO Disable | R/W | =1, Disable internal 1.8V LDO<br>=0, Enable internal 1.8V LDO | 0 |
| 5-0 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |

***Register 194 (0xC2): Insert SRC PVID***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-6 | Reserved | RO | Reserved<br>Do not change the default value. | 00 |
| 5 | Insert SRC port 1 PVID at Port 2 | R/W | 1= insert SRC port 1 PVID for untagged frame at egress port 2 | 0 |
| 4 | Insert SRC port 1 PVID at Port 3 | R/W | 1= insert SRC port 1 PVID for untagged frame at egress port 3 | 0 |
| 3 | Insert SRC port 2 PVID at Port 1 | R/W | 1= insert SRC port 2 PVID for untagged frame at egress port 1 | 0 |
| 2 | Insert SRC port 2 PVID at Port 3 | R/W | 1= insert SRC port 2 PVID for untagged frame at egress port 3 | 0 |
| 1 | Insert SRC port 3 PVID at Port 1 | R/W | 1= insert SRC port 3 PVID for untagged frame at egress port 1 | 0 |
| 0 | Insert SRC port 3 PVID at Port 2 | R/W | 1= insert SRC port 3 PVID for untagged frame at egress port 2 | 0 |

***Register 195 (0xC3): Power Management and LED Mode***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | CPU Interface Power Down | R/W | CPU interface clock tree power down enable.<br>=1, Enable<br>=0, Disable<br>Note: Power save a little bit when MII interface is used and the traffic is stopped in the power management with normal mode | 0 |
| 6 | Switch Power Down | R/W | Switch clock tree power down enable.<br>=1, Enable<br>=0, Disable<br>Note: Power save a little bit when MII interface is used and the traffic is stopped in the power management with normal mode | 0 |
| 5-4 | LED Mode Selection | R/W | =00, LED0 -> Link/ACT, LED1-> Speed<br>=01, LED0 -> Link, LED1 -> ACT<br>=10, LED0 -> Link/ACT, LED1 -> Duplex<br>=11, LED0 -> Link, LED1 -> Duplex<br><br>Note:<br>**Item / Pin State / LED Definition**<br>No Link / H / OFF<br>Link / L / ON<br>100 Speed / L / ON<br>10 Speed / H / OFF (Link is ON)<br>Full Duplex / L / ON<br>Half Duplex / H / OFF (Link is ON)<br>ACT / Toggle / Blinking | 00 |
| 3 | LED Output Mode | R/W | =1, The internal stretched energy signal from the analog module will be negated and output to LED1 and the internal device ready signal will be negated and output to LED0.<br>=0, The LED1/LED0 pins will indicate the regular LED outputs.<br>(Note. This is for debugging purpose.) | 0 |
| 2 | PLL Off Enable | R/W | =1, PLL power down enable<br>=0, Disable<br>Note: This bit is used in Energy Detect mode with Pin 27 MII_LINK_3 pull-up in the by-pass mode for saving power | 0 |
| 1-0 | Power Management Mode | R/W | Power management mode<br>=00, Normal Mode<br>=01, Energy Detection Mode<br>=10, Software Power Down Mode<br>=11, Power Saving Mode | 00 |

***Register 196(0xC4): Sleep Mode***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Sleep Mode | R/W | This value is used to control the minimum period the no energy event has to be detected consecutively before the device enters the low power state when the ED mode is on.<br>The unit is 20ms. The default go sleep time is 1.6 seconds. | 0x50 |

***Register 198 (0xC6): Forward Invalid VID Frame and Host Mode***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | Reserved<br>Do not change the default value. | 0 |
| 6-4 | Forward Invid VID Frame | R/W | Forwarding ports for frame with invalid VID | 3b'0 |
| 3 | P3 RMII Clock Selection | R/W | =1, Internal<br>=0, External | 0 |
| 2 | P1 RMII Clock Selection | R/W | =1, Internal<br>=0, External | 0 |
| 1-0 | Host Interface Mode | R/W | =00, $I^2C$ master mode<br>=01, $I^2C$ slave mode<br>=10, SPI slave mode<br>=11, SMI mode | Strapped value of P2LED1, P2LED0. |

## Static MAC Address Table

The KSZ8873 supports both a static and a dynamic MAC address table. In response to a destination address (DA) look up, the KSZ8873 searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. The entries in the static table will not be aged out by the KSZ8873.

The static table is accessed by an external processor via the SMI, SPI or $I^2C$ interfaces. The external processor performs all addition, modification and deletion of static MAC table entries.

**Table 16. Format of Static MAC Table (8 Entries)**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 57-54 | FID | R/W | Filter VLAN ID – identifies one of the 16 active VLANs | 0000 |
| 53 | Use FID | R/W | =1, Use (FID+MAC) for static table look ups<br>=0, Use MAC only for static table look ups | 0 |
| 52 | Override | R/W | =1, Override port setting “transmit enable=0” or “receive enable=0” setting<br>=0, No override | 0 |
| 51 | Valid | R/W | =1, This entry is valid, the lookup result will be used<br>=0, This entry is not valid | 0 |
| 50-48 | Forwarding Ports | R/W | These 3 bits control the forwarding port(s):<br>001, forward to port 1<br>010, forward to port 2<br>100, forward to port 3<br>011, forward to port 1 and port 2<br>110, forward to port 2 and port 3<br>101, forward to port 1 and port 3<br>111, broadcasting (excluding the ingress port) | 000 |
| 47-0 | MAC Address | R/W | 48-bit MAC Address | 0x0000_0000_0000 |

**Examples**:

**1. Static Address Table Read (Read the 2nd Entry)**

Write to reg. 121 (0x79) with 0x10 // Read static table selected

Write to reg. 122 (0x7A) with 0x01 // Trigger the read operation

Then,

Read reg. 124 (0x7C), static table bits [57:56]

Read reg. 125 (0x7D), static table bits [55:48]

Read reg. 126 (0x7E), static table bits [47:40]

Read reg. 127 (0x7F), static table bits [39:32]

Read reg. 128 (0x80), static table bits [31:24]

Read reg. 129 (0x81), static table bits [23:16]

Read reg. 130 (0x82), static table bits [15:8]

Read reg. 131 (0x83), static table bits [7:0]

**2. Static Address Table Write (Write the 8th Entry)**

Write to reg. 124 (0x7C), static table bits [57:56]

Write to reg. 125 (0x7D), static table bits [55:48]

Write to reg. 126 (0x7E), static table bits [47:40]

Write to reg. 127 (0x7F), static table bits [39:32]

Write to reg. 128 (0x80), static table bits [31:24]

Write to reg. 129 (0x81), static table bits [23:16]

Write to reg. 130 (0x82), static table bits [15:8]

Write to reg. 131 (0x83), static table bits [7:0]

Write to reg. 121 (0x79) with 0x00 // Write static table selected

Write to reg. 122 (0x7A) with 0x07 // Trigger the write operation

## VLAN Table

The KSZ8873 uses the VLAN table to perform look ups. If 802.1Q VLAN mode is enabled (register 5, bit 7 = 1), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described in Table 17.

**Table 17. Format of Static VLAN Table (16 Entries)**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 19 | Valid | R/W | = 1, entry is valid<br>= 0, entry is invalid | 1 |
| 18-16 | Membership | R/W | Specify which ports are members of the VLAN. If a DA lookup fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example, 101 means port 3 and 1 are in this VLAN. | 111 |
| 15-12 | FID | R/W | Filter ID. KSZ8873 supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA. | 0x0 |
| 11-0 | VID | R/W | IEEE 802.1Q 12 bits VLAN ID | 0x001 |

If 802.1Q VLAN mode is enabled, KSZ8873 will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

**Examples:**

**1. VLAN Table Read (Read the 3rd Entry)**

Write to reg. 121 (0x79) with 0x14 // Read VLAN table selected

Write to reg. 122 (0x7A) with 0x02 // Trigger the read operation

Then,

Read reg. 129 (0x81), VLAN table bits [19:16]

Read reg. 130 (0x82), VLAN table bits [15:8]

Read reg. 131 (0x83), VLAN table bits [7:0]

**2. VLAN Table Write (Write the 7th Entry)**

Write to reg. 129 (0x81), VLAN table bits [19:16]

Write to reg. 130 (0x82), VLAN table bits [15:8]

Write to reg. 131 (0x83), VLAN table bits [7:0]

Write to reg. 121 (0x79) with 0x04 // Write VLAN table selected

Write to reg. 122 (0x7A) with 0x06 // Trigger the write operation

## Dynamic MAC Address Table

The KSZ8873 maintains the dynamic MAC address table. Read access is allowed only.

**Table 18. Format of Dynamic MAC Address Table (1K Entries)**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 71 | Data Not Ready | RO | = 1, entry is not ready, continue retrying until this bit is set to 0<br>= 0, entry is ready | |
| 70-67 | Reserved | RO | Reserved | |
| 66 | MAC Empty | RO | = 1, there is no valid entry in the table<br>= 0, there are valid entries in the table | 1 |
| 65-56 | No of Valid Entries | RO | Indicates how many valid entries in the table<br>0x3ff means 1K entries<br>0x001 means 2 entries<br>0x000 and bit 66 = 0 means 1 entry<br>0x000 and bit 66 = 1 means 0 entry | 00_0000_0000 |
| 55-54 | Time Stamp | RO | 2 bits counter for internal aging | |
| 53-52 | Source Port | RO | The source port where FID+MAC is learned<br>00 : port 1<br>01 : port 2<br>10 : port 3 | 00 |
| 51-48 | FID | RO | Filter ID | 0x0 |
| 47-0 | MAC Address | RO | 48-bit MAC Address | 0x0000_0000_0000 |

**Example:**

**1. Dynamic MAC Address Table Read (Read the 1st Entry and Retrieve the MAC Table Size)**

Write to reg. 121 (0x79) with 0x18 // Read dynamic table selected

Write to reg. 122 (0x7A) with 0x00 // Trigger the read operation

Then,

Read reg. 123 (0x7B), bit [7] // if bit 7 = 1, restart (reread)
from this register dynamic table bits [66:64]

Read reg. 124 (0x7C), dynamic table bits [63:56]

Read reg. 125 (0x7D), dynamic table bits [55:48]

Read reg. 126 (0x7E), dynamic table bits [47:40]

Read reg. 127 (0x7F), dynamic table bits [39:32]

Read reg. 128 (0x80), dynamic table bits [31:24]

Read reg. 129 (0x81), dynamic table bits [23:16]

Read reg. 130 (0x82), dynamic table bits [15:8]

Read reg. 131 (0x83), dynamic table bits [7:0]

## Management Information Base (MIB) Counters

The KSZ8873 provides 34 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: “Per Port” and “All Port Dropped Packet.”

**Table 19. Format of “Per Port” MIB Counters**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31 | Overflow | RO | = 1, counter overflow<br>= 0, no counter overflow | 0 |
| 30 | Count Valid | RO | = 1, counter value is valid<br>= 0, counter value is not valid | 0 |
| 29-0 | Counter Values | RO | Counter value | 0 |

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

Port 1, base is 0x00 and range is (0x00-0x1f)

Port 2, base is 0x20 and range is (0x20-0x3f)

Port 3, base is 0x40 and range is (0x40-0x5f)

Port 1 MIB counters are read using the indirect memory offsets in Table 20.

**Table 20. Port 1's "Per Port" MIB Counters Indirect Memory Offsets**

| Offset | Counter Name | Description |
|---|---|---|
| 0x0 | RxLoPriorityByte | Rx lo-priority (default) octet count including bad packets |
| 0x1 | RxHiPriorityByte | Rx hi-priority octet count including bad packets |
| 0x2 | RxUndersizePkt | Rx undersize packets w/ good CRC |
| 0x3 | RxFragments | Rx fragment packets w/ bad CRC, symbol errors or alignment errors |
| 0x4 | RxOversize | Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes) |
| 0x5 | RxJabbers | Rx packets longer than 1522 bytes w/ either CRC errors, alignment errors, or symbol errors (depends on max packet size setting) |
| 0x6 | RxSymbolError | Rx packets w/ invalid data symbol and legal packet size. |
| 0x7 | RxCRCError | Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on max packet size setting) |
| 0x8 | RxAlignmentError | Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting) |
| 0x9 | RxControl8808Pkts | Number of MAC control frames received by a port with 88-08h in EtherType field |
| 0xA | RxPausePkts | Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC |
| 0xB | RxBroadcast | Rx good broadcast packets (not including error broadcast packets or valid multicast packets) |
| 0xC | RxMulticast | Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets) |
| 0xD | RxUnicast | Rx good unicast packets |
| 0xE | Rx64Octets | Total Rx packets (bad packets included) that were 64 octets in length |
| 0xF | Rx65to127Octets | Total Rx packets (bad packets included) that are between 65 and 127 octets in length |
| 0x10 | Rx128to255Octets | Total Rx packets (bad packets included) that are between 128 and 255 octets in length |
| 0x11 | Rx256to511Octets | Total Rx packets (bad packets included) that are between 256 and 511 octets in length |
| 0x12 | Rx512to1023Octets | Total Rx packets (bad packets included) that are between 512 and 1023 octets in length |
| 0x13 | Rx1024to1522Octets | Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting) |
| 0x14 | TxLoPriorityByte | Tx lo-priority good octet count, including PAUSE packets |
| 0x15 | TxHiPriorityByte | Tx hi-priority good octet count, including PAUSE packets |
| 0x16 | TxLateCollision | The number of times a collision is detected later than 512 bit-times into the Tx of a packet |
| 0x17 | TxPausePkts | Number of PAUSE frames transmitted by a port |
| 0x18 | TxBroadcastPkts | Tx good broadcast packets (not including error broadcast or valid multicast packets) |
| 0x19 | TxMulticastPkts | Tx good multicast packets (not including error multicast packets or valid broadcast packets) |
| 0x1A | TxUnicastPkts | Tx good unicast packets |
| 0x1B | TxDeferred | Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium |
| 0x1C | TxTotalCollision | Tx total collision, half duplex only |
| 0x1D | TxExcessiveCollision | A count of frames for which Tx fails due to excessive collisions |
| 0x1E | TxSingleCollision | Successfully Tx frames on a port for which Tx is inhibited by exactly one collision |
| 0x1F | TxMultipleCollision | Successfully Tx frames on a port for which Tx is inhibited by more than one collision |

**Table 21. Format of "All Port Dropped Packet" MIB Counters**

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 30-16 | Reserved | N/A | Reserved | N/A |
| 15-0 | Counter Value | RO | Counter Value | 0 |

"All Port Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 22.

**Table 22. "All Port Dropped Packet" MIB Counters**

| Offset | Counter Name | Description |
|---|---|---|
| 0x100 | Port1 TX Drop Packets | TX packets dropped due to lack of resources |
| 0x101 | Port2 TX Drop Packets | TX packets dropped due to lack of resources |
| 0x102 | Port3 TX Drop Packets | TX packets dropped due to lack of resources |
| 0x103 | Port1 RX Drop Packets | RX packets dropped due to lack of resources |
| 0x104 | Port2 RX Drop Packets | RX packets dropped due to lack of resources |
| 0x105 | Port3 RX Drop Packets | RX packets dropped due to lack of resources |

**Examples:**

**1. MIB Counter Read (Read port 1 "Rx64Octets" Counter)**

Write to reg. 121 (0x79) with 0x1c // Read MIB counters selected

Write to reg. 122 (0x7A) with 0x0e // Trigger the read operation

Then,

Read reg. 128 (0x80), overflow bit [31] // If bit 31 = 1, there was a counter overflow valid bit [30] // If bit 30 = 0, restart (reread) from this register counter bits [29:24]

Read reg. 129 (0x81), counter bits [23:16]

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

**2. MIB Counter Read (Read port 2 "Rx64Octets" Counter)**

Write to reg. 121 (0x79) with 0x1c // Read MIB counter selected

Write to reg. 122 (0x7A) with 0x2e // Trigger the read operation

Then,

Read reg. 128 (0x80), overflow bit [31] // If bit 31 = 1, there was a counter overflow valid bit [30] // If bit 30 = 0, restart (reread) from this register counter bits [29:24]

Read reg. 129 (0x81), counter bits [23:16]

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

**3. MIB Counter Read (Read "Port1 TX Drop Packets" Counter)**

Write to reg. 121 (0x79) with 0x1d // Read MIB counter selected

Write to reg. 122 (0x7A) with 0x00 // Trigger the read operation

Then,

Read reg. 130 (0x82), counter bits [15:8]

Read reg. 131 (0x83), counter bits [7:0]

***Additional MIB Counter Information***

"Per Port" MIB counters are designed as "read clear." These counters will be cleared after they are read.

"All Port Dropped Packet" MIB counters are not cleared after they are accessed and do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

To read out all the counters, the best performance over the SPI bus is (160+3)*8*200 = 260ms, where there are 160 registers, 3 overheads, 8 clocks per access, at 5MHz. In the heaviest condition, the counters will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

A high-performance SPI master is also recommended to prevent counters overflow.

## Absolute Maximum Ratings[6]

Supply Voltage
- $V_{DDA\_1.8}$, $V_{DDC}$ ..... –0.5V to +2.4V
- $V_{DDA\_3.3}$, $V_{DDIO}$ ..... –0.5V to +4.0V

Input Voltage ..... –0.5V to +4.0V
Output Voltage ..... –0.5V to +4.0V
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (Ts) ..... –55°C to +150°C
ESD Rating[8] ..... ±3kV

## Operating Ratings[7]

Supply Voltage
- $V_{DDA\_1.8}$, $V_{DDC}$ ..... +1.66V to +1.94V
- $V_{DDA\_3.3}$ ..... +2.5V to +3.465V
- $V_{DDIO}$ ..... +1.71V to +3.465V

Ambient Temperature ($T_A$)
- Commercial ..... 0°C to +70°C
- Industrial ..... –40°C to +85°C

Junction Temperature ($T_J$) ..... +125°C
Junction Thermal Resistance[9]
- LQFP ($\theta_{JA}$) ..... 47.24°C/W
- LQFP ($\theta_{JC}$) ..... 19.37°C/W

## Electrical Characteristics[10]

Current consumption is for the single 3.3V supply device only, and includes the 1.8V supply voltages ($V_{DDA}$, $V_{DDC}$) that are provided via power output Pin 56($V_{DDCO}$). Each PHY port's transformer consumes an additional 45mA @ 3.3V for 100BASE-TX and 70mA @ 3.3V for 10BASE-T at fully traffic.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **100BASE-TX Operation (All Ports @ 100% Utilization)** | | | | | | |
| $I_{ddxio}$ | 100BASE-TX (analog core + digital core + transceiver + digital I/O) | $V_{DDA\_3.3}$, $V_{DDIO}$ = 3.3V<br>Core power is provided from the internal 1.8V LDO with input voltage $V_{DDIO}$ | | 115 | | mA |
| **10BASE-T Operation (All Ports @ 100% Utilization)** | | | | | | |
| $I_{ddxio}$ | 10BASE-T (analog core + digital core + transceiver + digital I/O) | $V_{DDA\_3.3}$, $V_{DDIO}$ = 3.3V<br>Core power is provided from the internal 1.8V LDO with input voltage $V_{DDIO}$ | | 86 | | mA |
| **Power Management Mode (with MII/RMII in Default PHY Mode)** | | | | | | |
| $I_{dd3}$ | Power-Saving Mode | $V_{DDA\_3.3}$, $V_{DDIO}$ = 3.3V<br>Unplug Port 1 and Port 2<br>Set Register 195 Bit[1,0] = [1,1] | | 96 | | mA |
| $I_{dd4}$ | Soft Power-Down Mode | $V_{DDA\_3.3}$, $V_{DDIO}$ = 3.3V<br>Set Register 195 Bit[1,0] = [1,0] | | 5 | | mA |
| $I_{dd5}$ | Energy-Detect Mode | $V_{DDA\_3.3}$, $V_{DDIO}$ = 3.3V<br>Unplug Port 1 and Port 2<br>Set Register 195 Bit[7,0] = 0x05 with Port 3 PHY mode and by-pass mode. | | 15 | | mA |

**Notes:**

6. Exceeding the absolute maximum ratings may damage the device.
7. The device is not guaranteed to function outside its operating ratings.
8. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k in series with 100pF.
9. No heat spreader (HS) in this package.
10. $T_A$ = +25°C. Specification for packaged product only.

## Electrical Characteristics[10] (Continued)

Current consumption is for the single 3.3V supply device only, and includes the 1.8V supply voltages ($V_{DDA}$, $V_{DDC}$) that are provided via power output Pin 56($V_{DDCO}$). Each PHY port's transformer consumes an additional 45mA @ 3.3V for 100BASE-TX and 70mA @ 3.3V for 10BASE-T at fully traffic.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **CMOS Inputs (VDD_IO = 3.3V/2.5V/1.8V)** | | | | | | |
| $V_{IH}$ | Input High Voltage | | 2.0/1.8/1.3 | | | V |
| $V_{IL}$ | Input Low Voltage | | | | 0.8/0.7/0.5 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = GND ~ $V_{DD\_IO}$ | –10 | | 10 | µA |
| **CMOS Outputs (VDD_IO = 3.3V/2.5V/1.8V)** | | | | | | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -8mA | 2.4/2.0/1.5 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA | | | 0.4/0.4/0.3 | V |
| \|IOZ\| | Output Tri-State Leakage | | | | 10 | µA |
| **100BASE-TX Transmit (Measured Differentially After 1:1 Transformer)** | | | | | | |
| $V_O$ | Peak Differential Output Voltage | 100Ω termination across differential output | 0.95 | | 1.05 | V |
| $V_{IMB}$ | Output Voltage Imbalance | 100Ω termination across differential output | | | 2 | % |
| $T_r/T_f$ | Rise/Fall Time | | 3 | | 5 | ns |
| | Rise/Fall Time Imbalance | | 0 | | 0.5 | ns |
| | Duty Cycle Distortion | | | | ±0.5 | ns |
| | Overshoot | | | | 5 | % |
| | Output Jitter | Peak-to-peak | | 0.7 | 1.4 | ns |
| **10BASE-T Receive** | | | | | | |
| $V_{SQ}$ | Squelch Threshold | 5MHz square wave | | 400 | | mV |
| **10BASE-T Transmit (Measured Differentially After 1:1 Transformer)** | | | | | | |
| $V_P$ | Peak Differential Output Voltage | 100Ω termination across differential output | | 2.4 | | V |
| | Output Jitter | Peak-to-peak | | 1.4 | 11 | ns |

# Timing Specifications

## EEPROM Timing

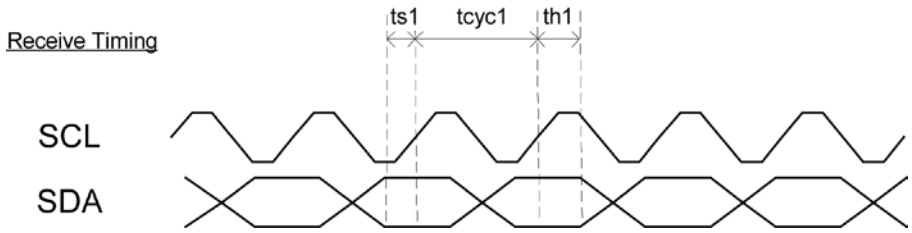



**Figure 15. EEPROM Interface Input Timing Diagram**

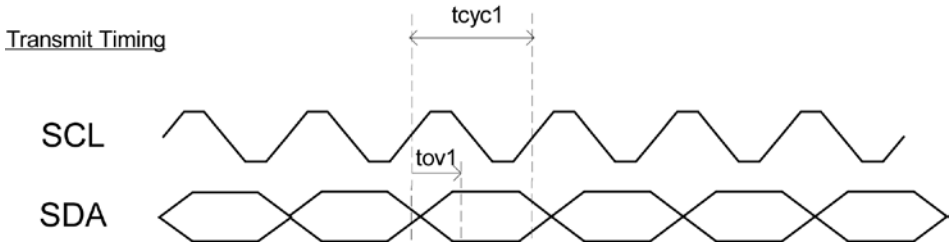



**Figure 16. EEPROM Interface Output Timing Diagram**

**Table 23. EEPROM Timing Parameters**

| Symbols | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{cyc1}$ | Clock Cycle | | 16384 | | ns |
| $t_{s1}$ | Setup Time | 20 | | | ns |
| $t_{h1}$ | Hold Time | 20 | | | ns |
| $t_{ov1}$ | Output Valid | 4096 | 4112 | 4128 | ns |

**MII Timing**

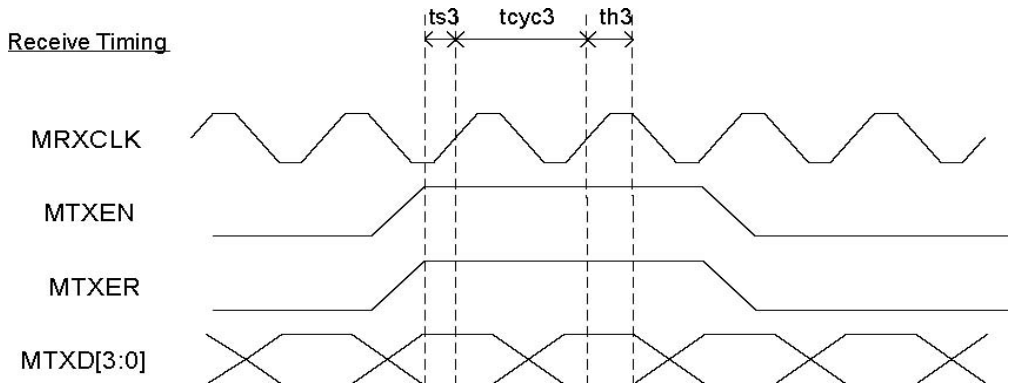



**Figure 17. MAC Mode MII Timing – Data Received from MII**

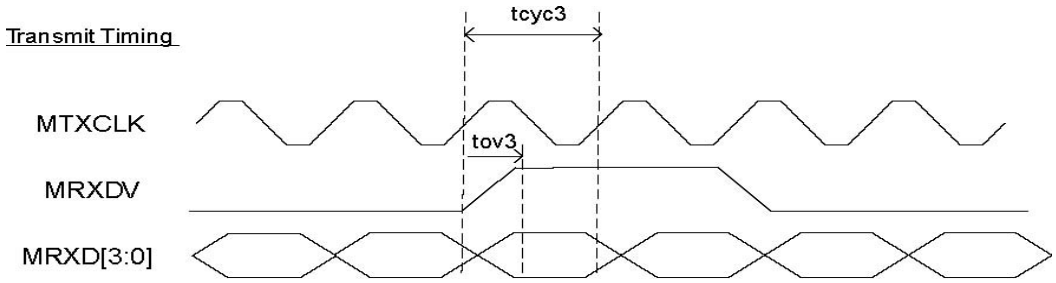



**Figure 18. MAC Mode MII Timing – Data Transmitted to MII**

**Table 24. MAC Mode MII Timing Parameters**

| Symbol | Parameter | 10Base-T/100Base-TX | | | |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units |
| $t_{CYC3}$ | Clock Cycle | | 400/40 | | ns |
| $t_{S3}$ | Set-Up Time | 4 | | | ns |
| $t_{H3}$ | Hold Time | 2 | | | ns |
| $t_{OV3}$ | Output Valid | 7 | 11 | 16 | ns |

**MII Timing (Continued)**

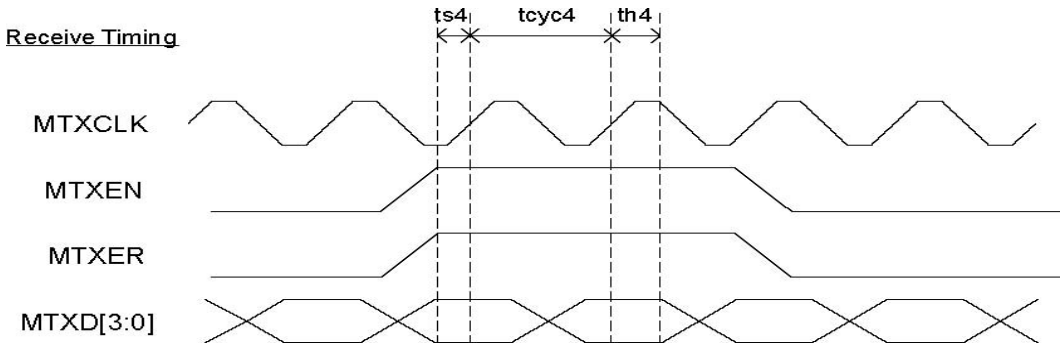



**Figure 19. PHY Mode MII Timing – Data Received from MII**

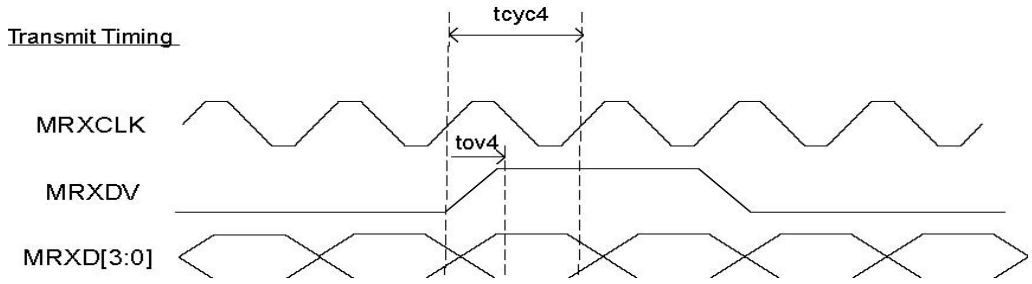



**Figure 20. PHY Mode MII Timing – Data Transmitted to MII**

**Table 25. PHY Mode MII Timing Parameters**

| Symbol | Parameter | 10BaseT/100BaseT | | | |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units |
| $t_{CYC4}$ | Clock Cycle | | 400/40 | | ns |
| $t_{S4}$ | Set-Up Time | 10 | | | ns |
| $t_{H4}$ | Hold Time | 0 | | | ns |
| $t_{OV4}$ | Output Valid | 18 | | 19 | ns |

### RMII Timing

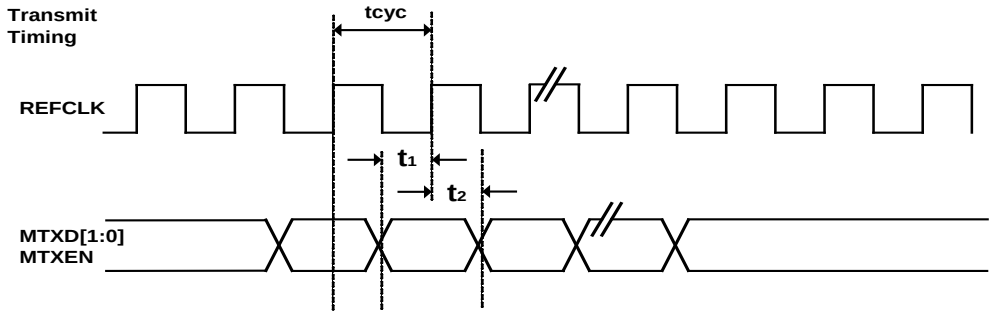



**Figure 21. RMII Timing – Data Received from RMII**

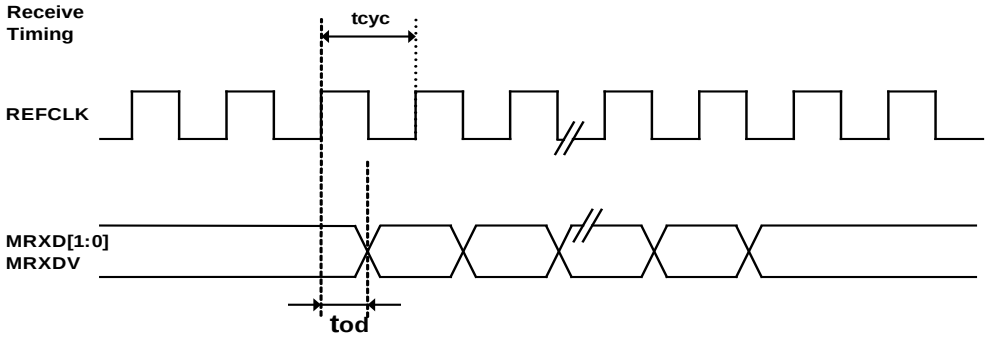



**Figure 22. RMII Timing Parameters**

**Table 26. RMII Timing Parameters**

| Symbols | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{CYC}$ | Clock Cycle | | 20 | | ns |
| $t_1$ | Setup Time | 4 | | | ns |
| $t_2$ | Hold Time | 2 | | | ns |
| $t_{OD}$ | Output Delay | 6 | | 16 | ns |

## I²C Slave Mode Timing

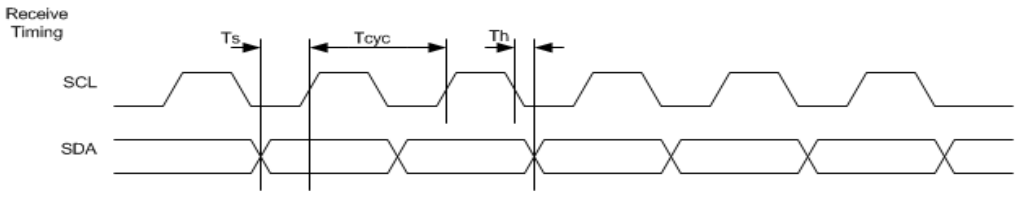



**Figure 23. I²C Input Timing**

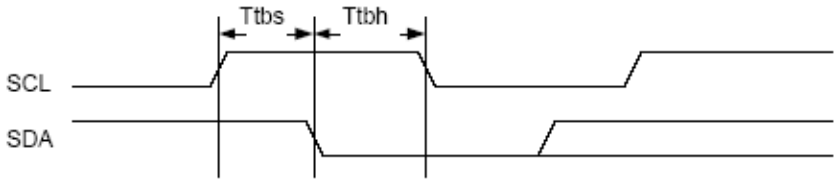



**Figure 24. I²C Start Bit Timing**

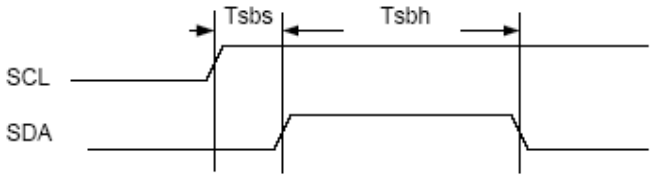



**Figure 25. I²C Stop Bit Timing**

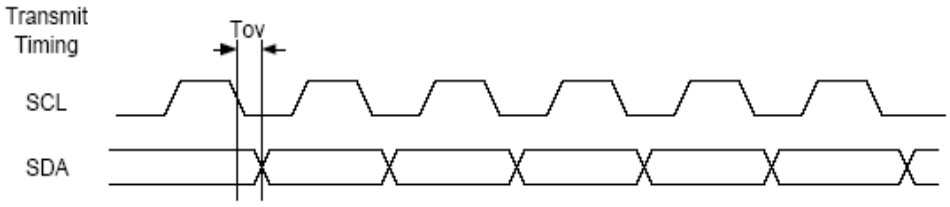



**Figure 26. I²C Output Timing**

## I²C Slave Mode Timing (Continued)

**Table 27. I²C Timing Parameters**

| Symbols | Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{CYC}$ | Clock Cycle | 400 | | | ns |
| $t_S$ | Setup Time | 33 | | Half-cycle | ns |
| $t_H$ | Hold Time | 0 | | | ns |
| $t_{TBS}$ | Start Bit Setup Time | 33 | | | ns |
| $t_{TBH}$ | Start Bit Hold Time | 33 | | | ns |
| $t_{SBS}$ | Stop Bit Setup Time | 2 | | | ns |
| $t_{SBH}$ | Stop Bit Hold Time | 33 | | | ns |
| $t_{OV}$ | Output Valid | 64 | | 96 | ns |

**Note:**

Data is only allowed to change during SCL low time except start and stop bits.

**SPI Timing**

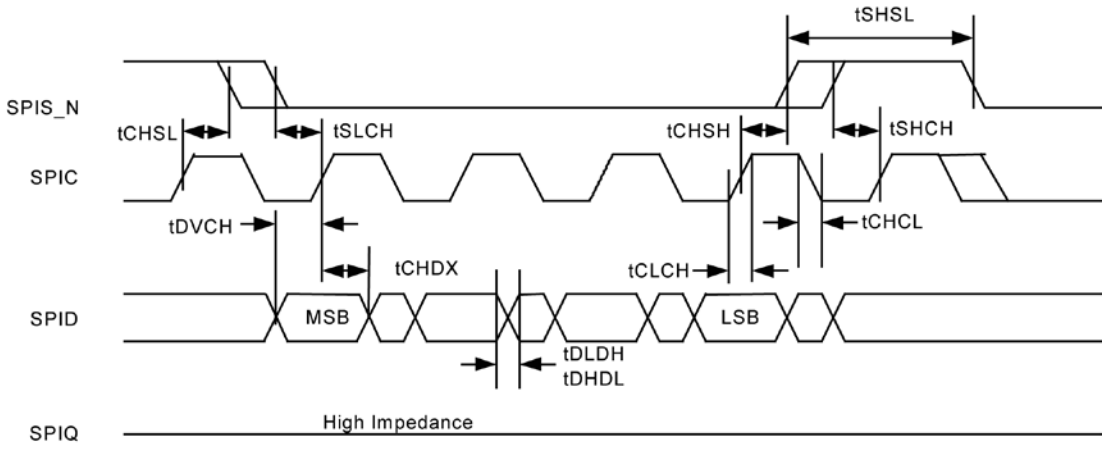



**Figure 27. SPI Input Timing**

**Table 28. SPI Input Timing Parameters**

| Symbols | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $f_C$ | Clock Frequency | | 5 | MHz |
| $t_{CHSL}$ | SPISN Inactive Hold Time | 90 | | ns |
| $t_{SLCH}$ | SPISN Active Setup Time | 90 | | ns |
| $t_{CHSH}$ | SPISN Active Old Time | 90 | | ns |
| $t_{SHCH}$ | SPISN Inactive Setup Time | 90 | | ns |
| $t_{SHSL}$ | SPISN Deselect Time | 100 | | ns |
| $t_{DVCH}$ | Data Input Setup Time | 20 | | ns |
| $t_{CHDX}$ | Data Input Hold Time | 30 | | ns |
| $t_{CLCH}$ | Clock Rise Time | | 1 | µs |
| $t_{CHCL}$ | Clock Fall Time | | 1 | µs |
| $t_{DLDH}$ | Data input rise Time | | 1 | µs |
| $t_{DHDL}$ | Data input fall Time | | 1 | µs |

**SPI Timing (Continued)**

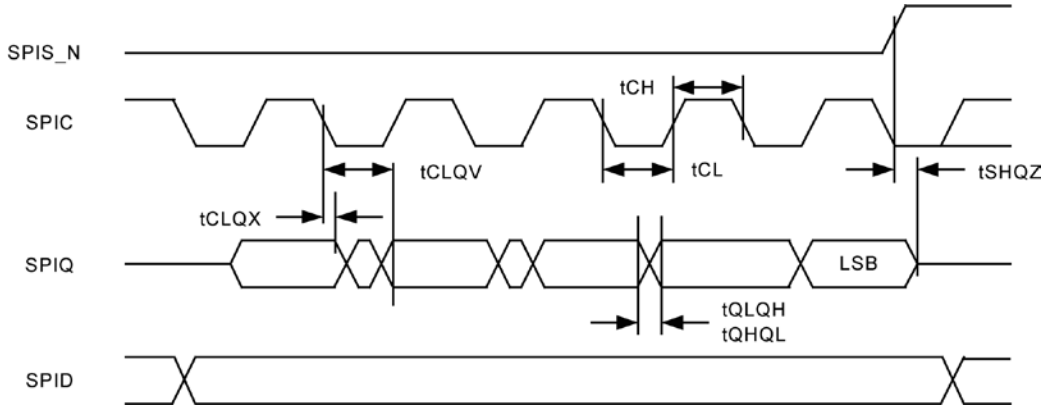



**Figure 28. SPI Output Timing**

**Table 29. SPI Output Timing Parameters**

| Symbols | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $f_C$ | Clock Frequency | | 5 | MHz |
| $t_{CLQX}$ | SPIQ Hold Time | 0 | 0 | ns |
| $t_{CLQV}$ | Clock Low to SPIQ Valid | | 60 | ns |
| $t_{CH}$ | Clock High Time | 90 | | ns |
| $t_{CL}$ | Clock Low Time | 90 | | |
| $t_{QLQH}$ | SPIQ Rise Time | | 50 | ns |
| $t_{QHQL}$ | SPIQ Fall Time | | 50 | ns |
| $t_{SHQZ}$ | SPIQ Disable Time | | 100 | ns |

**Auto-Negotiation Timing**

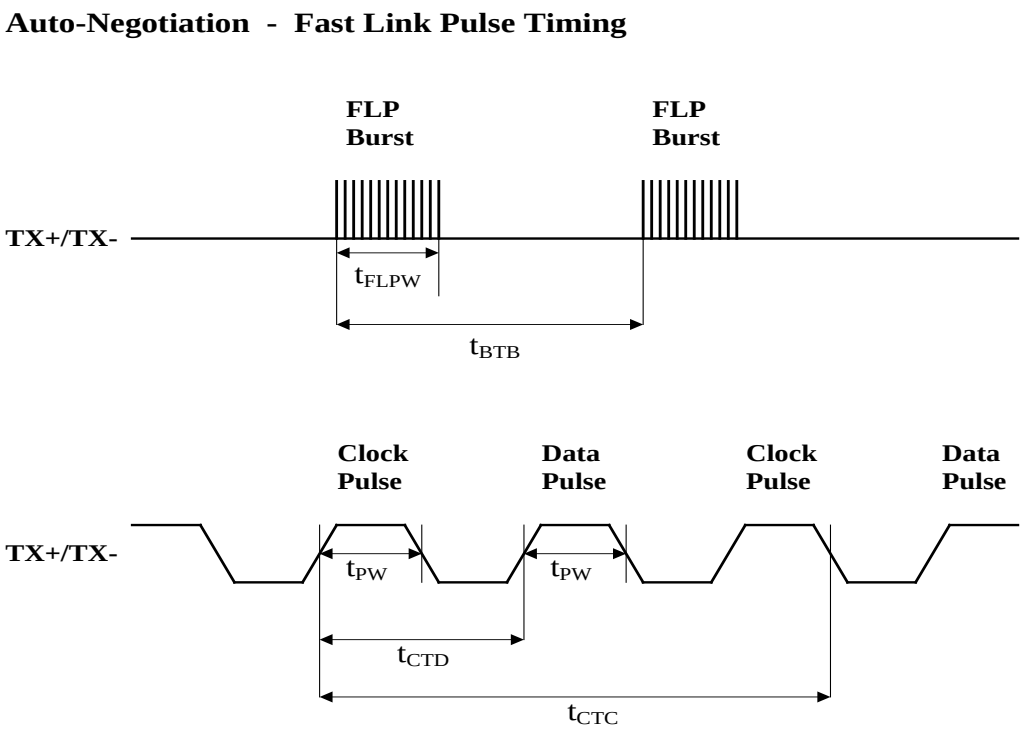



**Figure 29. Auto-Negotiation Timing**

**Table 30. Auto-Negotiation Timing Parameters**

| Symbols | Parameters | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{BTB}$ | FLP Burst to FLP Burst | 8 | 16 | 24 | ms |
| $t_{FLPW}$ | FLP Burst Width | | 2 | | ms |
| $t_{PW}$ | Clock/Data Pulse Width | | 100 | | ns |
| $t_{CTD}$ | Clock pulse to Data Pulse | 55.5 | 64 | 69.5 | µs |
| $t_{CTC}$ | Clock pulse to Clock Pulse | 111 | 128 | 139 | µs |
| | Number of Clock/Data Pulse per Burst | 17 | | 33 | |

**MDC/MDIO Timing**

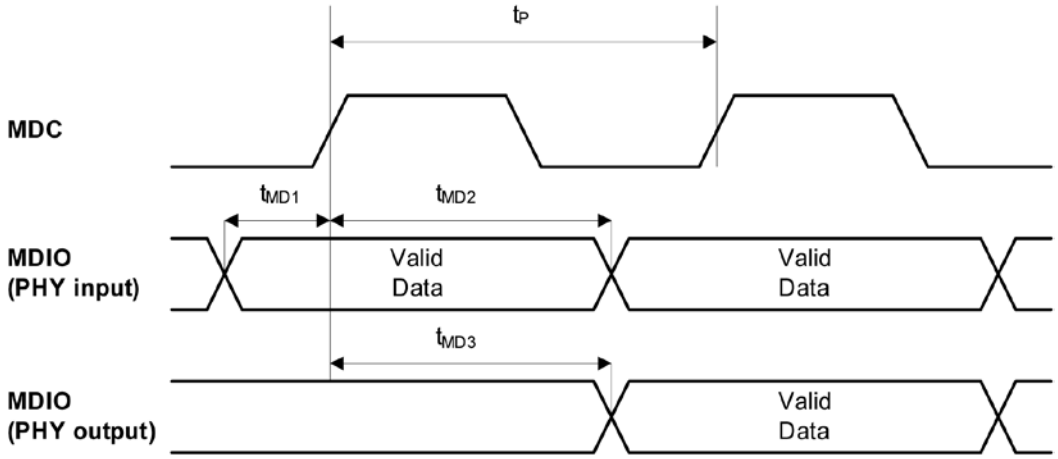



**Figure 30. MDC/MDIO Timing**

**Table 31. MDC/MDIO Timing Parameters**

| Timing Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_P$ | MDC period | | 400 | | ns |
| $t_{1MD1}$ | MDIO (PHY Input) Setup to Rising Edge of MDC | 10 | | | ns |
| $t_{MD2}$ | MDIO (PHY Input) Hold from Rising Edge of MDC | 4 | | | ns |
| $t_{MD3}$ | MDIO (PHY Output) Delay from Rising Edge of MDC | | 222 | | ns |

**Reset Timing**

The KSZ8873MLL/FLL/RLL reset timing requirement is summarized in Figure 31 and Table 32.

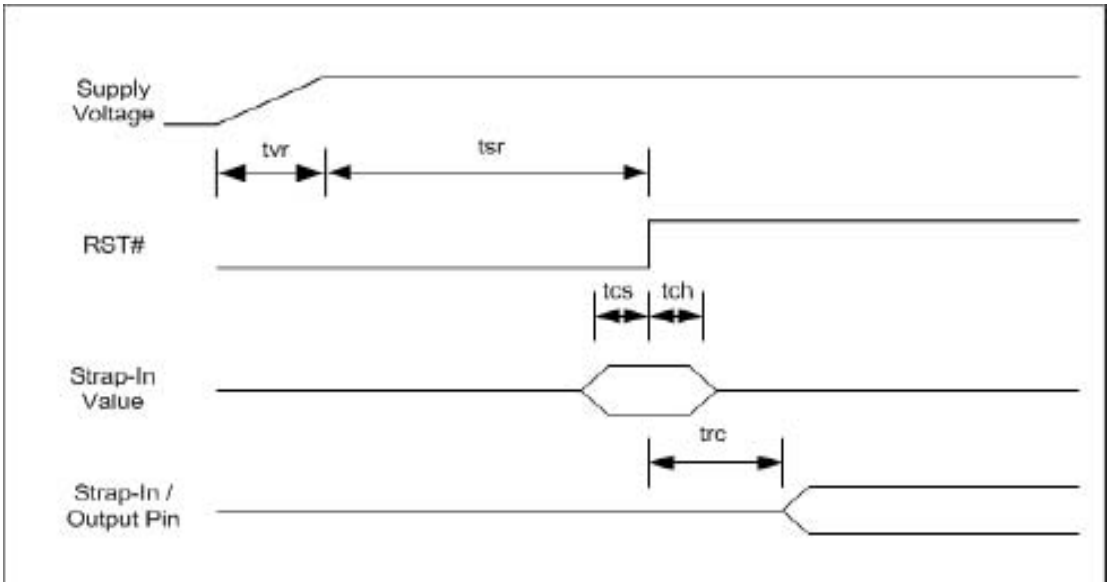



**Figure 31. Reset Timing**

**Table 32. Reset Timing Parameters**

| Symbols | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{SR}$ | Stable Supply Voltages to Reset High | 10 | | ms |
| $t_{CS}$ | Configuration Setup Time | 50 | | ns |
| $t_{OH}$ | Configuration Hold Time | 50 | | ns |
| $t_{RC}$ | Reset to Strap-In Pin Output | 50 | | µs |
| $t_{VR}$ | 3.3V Rise Time | 100 | | µs |

**Note:**

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the managed interface ($I^2C$ slave, SPI slave, SMI, MIIM).

**Reset Circuit**

The reset circuit in Figure 32 is recommended for powering up the KSZ8873MLL/FLL/RLL if reset is triggered only by the power supply.

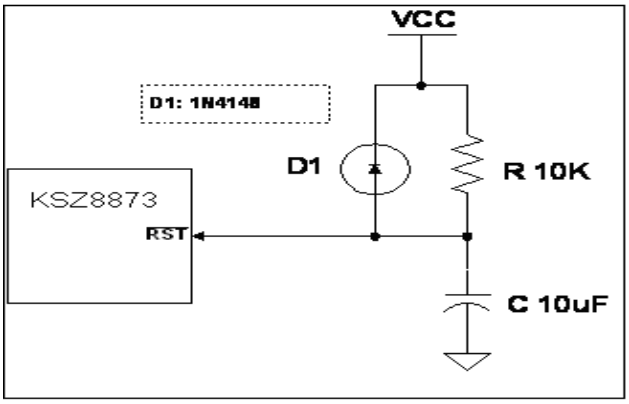



**Figure 32. Recommended Reset Circuit**

The reset circuit in Figure 33 is recommended for applications where reset is driven by another device (e.g., CPU, FPGA, etc),. At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8873MLL/FLL/RLL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power-up.

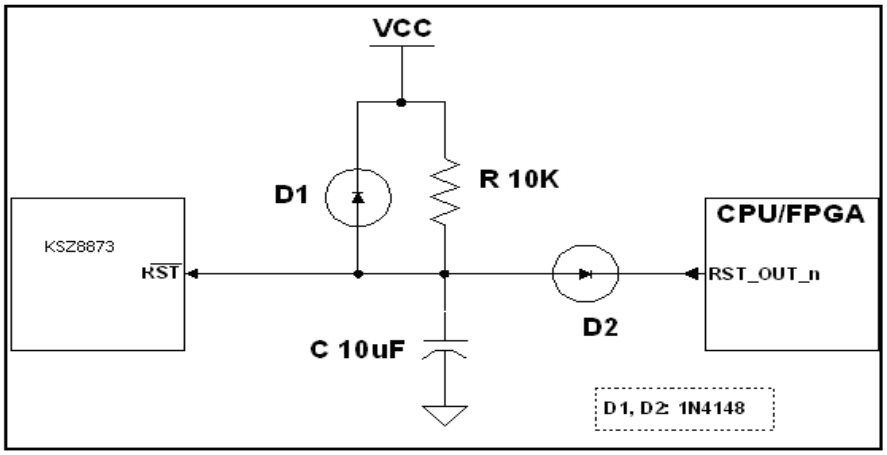



**Figure 33. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output**

## Selection of Isolation Transformers

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 33 gives recommended transformer characteristics.

**Table 33. Transformer Selection Criteria**

| Parameter | Value | Test Condition |
|---|---|---|
| Turns Ratio | 1 CT : 1 CT | |
| Open-Circuit Inductance (minimum) | 350µH | 100mV, 100kHz, 8mA |
| Leakage Inductance (maximum) | 0.4µH | 1MHz (minimum) |
| Inter-Winding Capacitance (maximum) | 12pF | |
| D.C. Resistance (maximum) | 0.9Ω | |
| Insertion Loss (maximum) | 1.0dB | 0MHz – 65MHz |
| HIPOT (minimum) | 1500Vrms | |

**Table 34. Qualified Single-Port Magnetics**

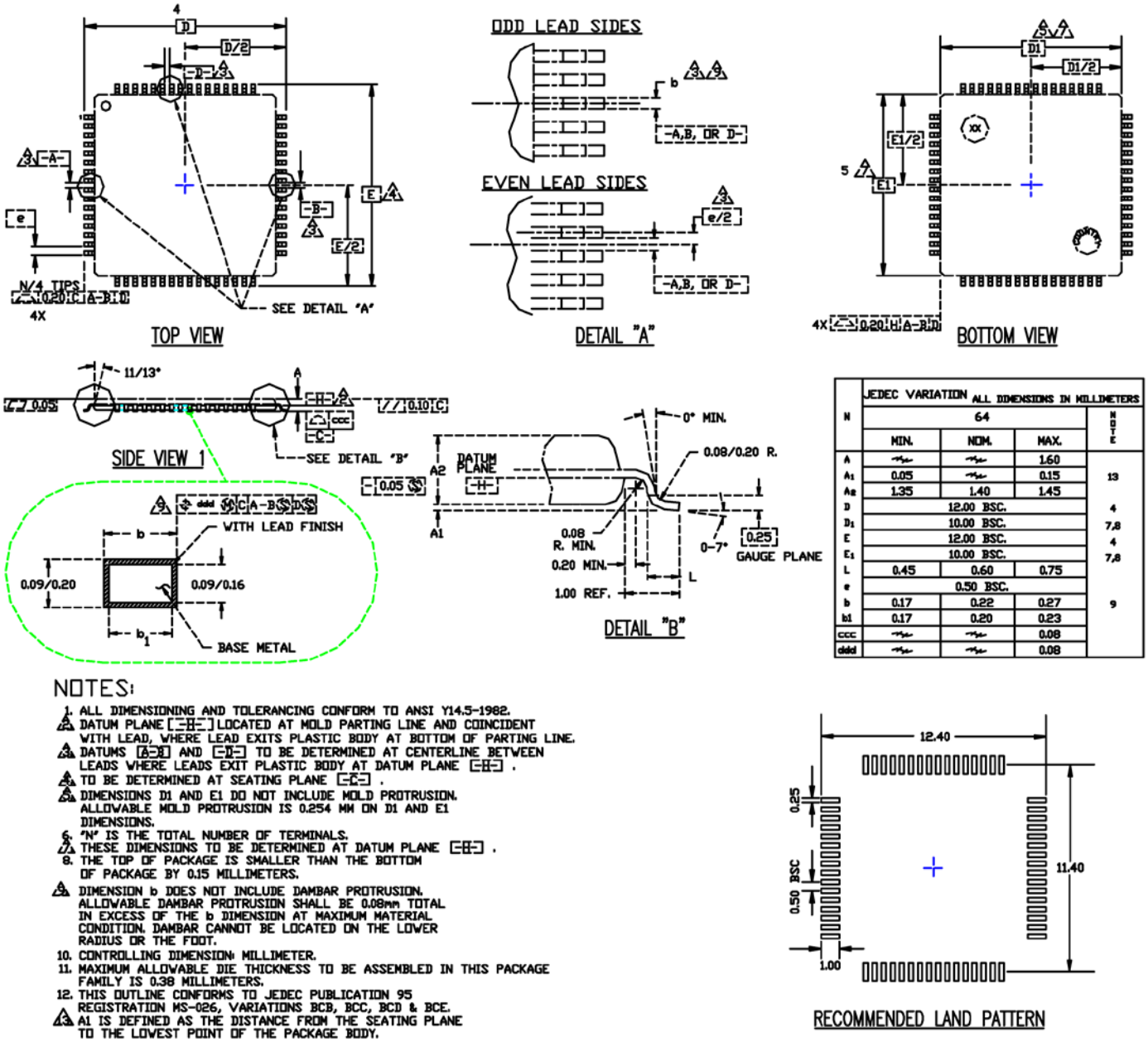
| Magnetic Manufacturer | Part Number | Auto MDI-X | Number of Port |
|---|---|---|---|
| Bel Fuse | S558-5999-U7 | Yes | 1 |
| Bel Fuse (MagJack) | SI-46001 | Yes | 1 |
| Bel Fuse (MagJack) | SI-50170 | Yes | 1 |
| Delta | LF8505 | Yes | 1 |
| LanKom | LF-H41S | Yes | 1 |
| Pulse | H1102 | Yes | 1 |
| Pulse (low cost) | H1260 | Yes | 1 |
| Datatronic | NT79075 | Yes | 1 |
| Transpower | HB726 | Yes | 1 |
| YCL | LF-H41S | Yes | 1 |
| TDK (Mag Jack) | TLA-6T718 | Yes | 1 |

## Selection of Reference Crystal

**Table 35. Typical Reference Crystal Characteristics**

| Chacteristics | Value | Units |
|---|---|---|
| Frequency | 25.00000 | MHz |
| Frequency Tolerance (maximum) | ±50 | ppm |
| Load capacitance (maximum) | 20 | pF |
| Series Resistance | 40 | Ω |

## Package Information[11] and Recommended Landing Pattern




| N | JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|---|---|---|---|---|
| | 64 | | | NOTE |
| | MIN. | NOM. | MAX. | |
| A | --- | --- | 1.60 | |
| A1 | 0.05 | --- | 0.15 | 13 |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | | 12.00 BSC. | | 4 |
| D1 | | 10.00 BSC. | | 7,8 |
| E | | 12.00 BSC. | | 4 |
| E1 | | 10.00 BSC. | | 7,8 |
| L | 0.45 | 0.60 | 0.75 | |
| e | | 0.50 BSC. | | |
| b | 0.17 | 0.22 | 0.27 | 9 |
| b1 | 0.17 | 0.20 | 0.23 | |
| ccc | --- | --- | 0.08 | |
| ddd | --- | --- | 0.08 | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS [-A-] AND [-B-] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE [-H-].
4. TO BE DETERMINED AT SEATING PLANE [-C-].
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [-H-].
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS BCB, BCC, BCD & BCE.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.




**64-Pin LQFP Package**

**Note:**

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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