LM27341,LM27342

LM27341/LM27342/LM27341Q/LM27342Q 2 MHz 1.5A/2A Wide Input Range Step-Down DC-DC Regulator with Frequency Synchronization

Literature Number: SNVS497D

National Semiconductor

LM27341/LM27342/ LM27341Q/LM27342Q

February 9, 2010

2 MHz 1.5A/2A Wide Input Range Step-Down DC-DC Regulator with Frequency Synchronization

General Description

The LM27341 and LM27342 regulators are monolithic, high frequency, PWM step-down DC-DC converters in 10-pin LLP and 10-pin eMSOP packages. They contain all the active functions to provide local DC-DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

With a minimum of external components the LM27341 and LM27342 are easy to use. The ability to drive 1.5A or 2A loads respectively, with an internal 150 mΩ NMOS switch results in the best power density available. The world-class control circuitry allows for on-times as low as 65 ns, thus supporting exceptionally high frequency conversion. Switching frequency is internally set to 2 MHz and synchronizable from 1 to 2.35 MHz, which allows the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequency is very high, efficiencies up to 90% are easy to achieve. External shutdown is included featuring an ultra-low shutdown current of 70 nA. The LM27341and LM27342 utilize peak current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output over-voltage protection.

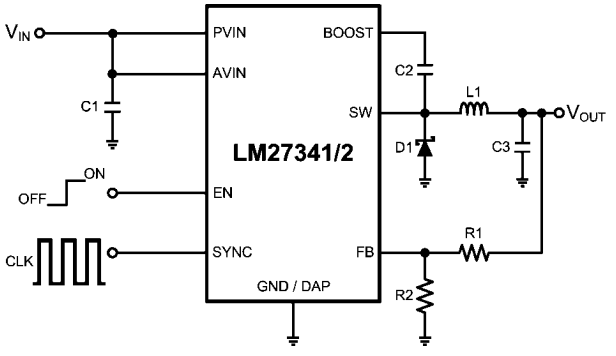
Features

- Space saving 3 x 3 mm LLP-10 & eMSOP-10 package
- Wide input voltage range 3V to 20V
- Wide output voltage range 1V to 18V
- LM27341 delivers 1.5A maximum output current
- LM27342 delivers 2A maximum output current
- High switching frequency 2 MHz
- Frequency synchronization 1.00 MHz < f_{SW} < 2.35 MHz
- 150 mΩ NMOS switch with internal bootstrap supply
- 70 nA shutdown current
- Internal voltage reference accuracy of 1%
- Peak Current-Mode, PWM operation
- Thermal shutdown
- LM27341Q and LM27342Q are AEC-Q100 Grade 1 qualified and are manufactured on an Automotive Grade Flow

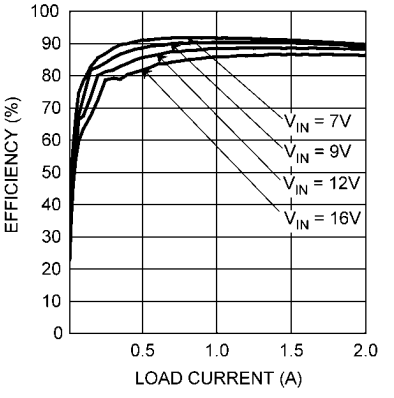
Applications

- Local 12V to Vcore Step-Down Converters
- Radio Power Supply
- Core Power in HDDs
- Set-Top Boxes
- Automotive
- USB Powered Devices
- DSL Modems

Typical Application Circuit



30005674



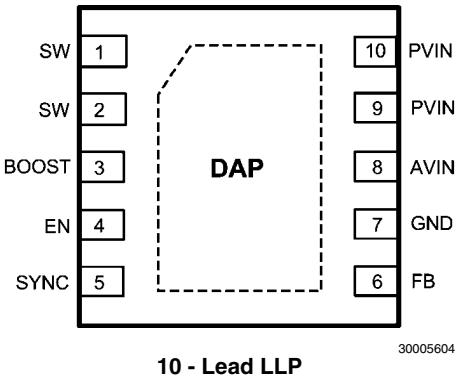
30005676

Efficiency vs Load Current
V_{OUT} = 5V, f_{sw} = 2 MHz

LM27341/LM27342/LM27341Q/LM27342Q 2 MHz 1.5/2A Wide Input Range Step-Down DC-DC Regulator with Frequency Synchronization

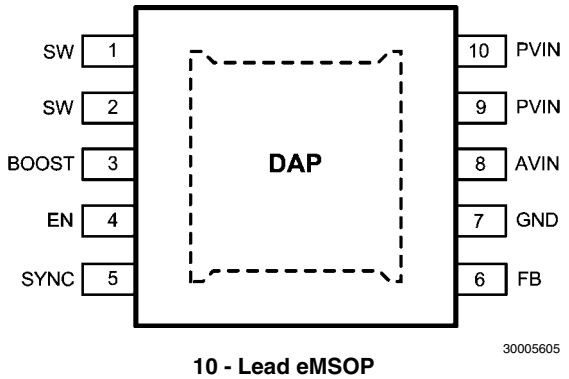
Connection Diagrams

Top View



10 - Lead LLP

Top View



10 - Lead eMSOP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As	Feature
LM27341MY	eMSOP -10	MUC10A	SSCB	1000 Units on Tape and Reel	
LM27341MYX	eMSOP -10	MUC10A	SSCB	3500 Units on Tape and Reel	
LM27342MY	eMSOP -10	MUC10A	SSCA	1000 Units on Tape and Reel	
LM27342MYX	eMSOP -10	MUC10A	SSCA	3500 Units on Tape and Reel	
LM27341SD	LLP - 10	SDA10A	L231B	1000 Units on Tape and Reel	
LM27341SDX	LLP - 10	SDA10A	L231B	4500 Units on Tape and Reel	
LM27342SD	LLP - 10	SDA10A	L231A	1000 Units on Tape and Reel	
LM27342SDX	LLP - 10	SDA10A	L231A	4500 Units on Tape and Reel	
LM27341QMY	eMSOP -10	MUC10A	SSJB	1000 Units Per Anti-Static Tube	AEC-Q100 Grade 1 qualified. Automotive Grade Production Flow*
LM27341QMYX	eMSOP -10	MUC10A	SSJB	3500 Units on Tape and Reel	
LM27342QMY	eMSOP -10	MUC10A	SSJA	1000 Units Per Anti-Static Tube	
LM27342QMYX	eMSOP -10	MUC10A	SSJA	3500 Units on Tape and Reel	

*Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard. Automotive grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

Pin Descriptions

Pin	Name	Function
1,2	SW	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.
3	BOOST	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
4	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3V.
5	SYNC	Frequency synchronization input. Drive this pin with an external clock or pulse train. Ground it to use the internal clock.
6	FB	Feedback pin. Connect FB to the external resistor divider to set output voltage.
7	GND	Signal and Power Ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
8	AVIN	Supply voltage for the control circuitry.
9,10	PVIN	Supply voltage for output power stage. Connect a bypass capacitor to this pin.
DAP	GND	Signal / Power Ground and thermal connection. Tie this directly to GND (pin 7). See Application Information regarding optimum thermal layout.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

AVIN, PVIN	-0.5V to 24V
SW Voltage	-0.5V to 24V
Boost Voltage	-0.5V to 28V
Boost to SW Voltage	-0.5V to 6.0V
FB Voltage	-0.5V to 3.0V
SYNC Voltage	-0.5V to 6.0V
EN Voltage	-0.5V to (V_{IN} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Susceptibility (*Note 2*)	2kV
Soldering Information	
Infrared Reflow (5sec)	260°C

Operating Ratings (*Note 1*)

AVIN, PVIN	3V to 20V
SW Voltage	-0.5V to 20V
Boost Voltage	-0.5V to 24V
Boost to SW Voltage	3.0V to 5.5V
Junction Temperature Range	−40°C to +125°C
Thermal Resistance (θ_{JA}) LLP10 (*Note 3*)	33°C/W
Thermal Resistance (θ_{JA}) eMSOP10 (*Note 3*)	45°C/W

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to 125°C). V_{IN} = 12V, and V_{BOOST} - V_{SW} = 4.3V unless otherwise specified. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM PARAMETERS						
V_{FB}	Feedback Voltage	T_J = 0°C to 85°C	0.990	1.0	1.010	V
		T_J = -40°C to 125°C	**0.984**	1.0	**1.014**	
$\Delta V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 20V		0.003		% / V
I_{FB}	Feedback Input Bias Current			20	**100**	nA
OVP	Over Voltage Protection, V_{FB} at which PWM Halts.			1.13		V
UVLO	Undervoltage Lockout	V_{IN} Rising until V_{SW} is Switching	**2.60**	2.75	**2.90**	V
	UVLO Hysteresis	V_{IN} Falling from UVLO	**0.30**	0.47	**0.6**	
SS	Soft Start Time		0.5	1	1.5	ms
I_Q	Quiescent Current, I_Q = I_{Q_AVIN} + I_{Q_PVIN}	V_{FB} = 1.1 (not switching)		2.4		mA
	Quiescent Current, I_Q = I_{Q_AVIN} + I_{Q_PVIN}	V_{EN} = 0V (shutdown)		70		nA
I_{BOOST}	Boost Pin Current	f_{SW}= 2 MHz		8.2	**10**	mA
		f_{SW}= 1 MHz		4.4	6	
OSCILLATOR						
f_{SW}	Switching Frequency	SYNC = GND	**1.75**	2	**2.3**	MHz
V_{FB_FOLD}	FB Pin Voltage where SYNC input is overridden.			0.53		V
f_{FOLD_MIN}	Frequency Foldback Minimum	V_{FB} = 0V		220	250	kHz
LOGIC INPUTS (EN, SYNC)						
f_{SYNC}	SYNC Frequency Range		1		2.35	MHz
V_{IL}	EN, SYNC Logic low threshold	Logic Falling Edge			0.4	V
V_{IH}	EN, SYNC Logic high threshold	Logic Rising Edge	1.8			
t_{SYNC_HIGH}	SYNC, Time Required above V_{IH} to Ensure a Logical High.				100	ns
t_{SYNC_LOW}	SYNC, Time Required below V_{IL} to Ensure a Logical Low.				100	ns
I_{SYNC}	SYNC Pin Current	V_{SYNC} < 5V		20		nA
I_{EN}	Enable Pin Current	V_{EN} = 3V		6	15	µA
		V_{IN} = V_{EN} = 20V		50	100	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INTERNAL MOSFET						
$R_{DS(ON)}$	Switch ON Resistance			150	**320**	mΩ
I_{CL}	Switch Current Limit	LM27342	**2.5**		**4.0**	A
		LM27341	**2.0**		**3.7**	
D_{MAX}	Maximum Duty Cycle	SYNC = GND	**85**	93		%
t_{MIN}	Minimum on time			65		ns
I_{SW}	Switch Leakage Current			40		nA
BOOST LDO						
V_{LDO}	Boost LDO Output Voltage			3.9		V
THERMAL						
T_{SHDN}	Thermal Shutdown Temperature	Junction temperature rising		165		°C
	Thermal Shutdown Hysteresis	Junction temperature falling		15		°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.

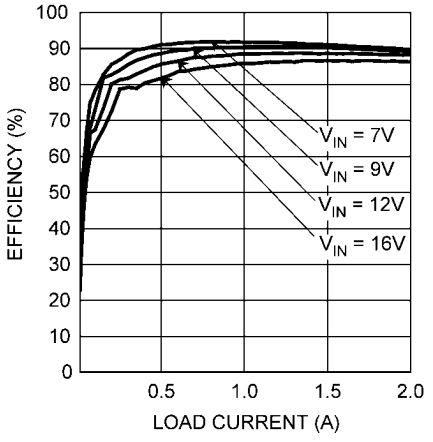
Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Thermal shutdown will occur if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a 3” x 3” PC board with 2oz. copper on 4 layers in still air.

Typical Performance Characteristics

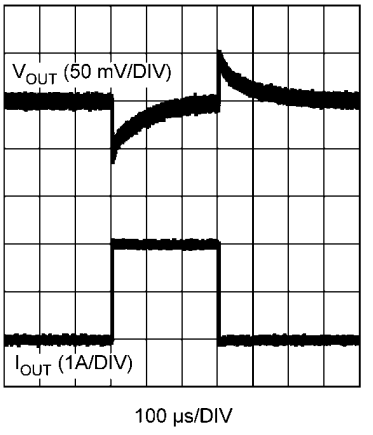
All curves taken at V_{IN} = 12V, V_{BOOST} - V_{SW} = 4.3V and T_A = 25°C, unless specified otherwise.

Efficiency vs Load Current
V_{OUT} = 5V, f_{SW} = 2 MHz
Refer to *Figure 10*



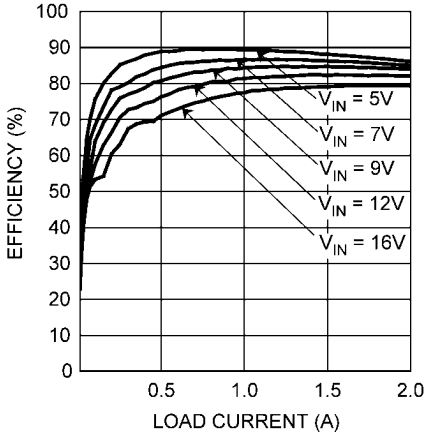
30005676

Load Transient
V_{OUT} = 5V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to *Figure 10*



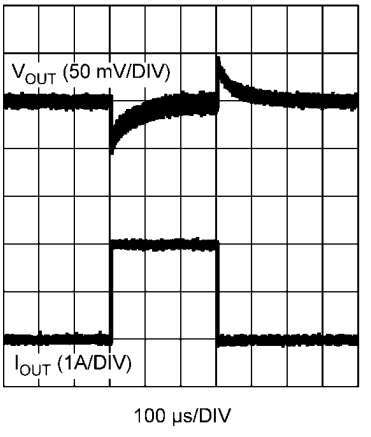
300056100

Efficiency vs Load Current
V_{OUT} = 3.3V, f_{SW} = 2 MHz
Refer to *Figure 12*



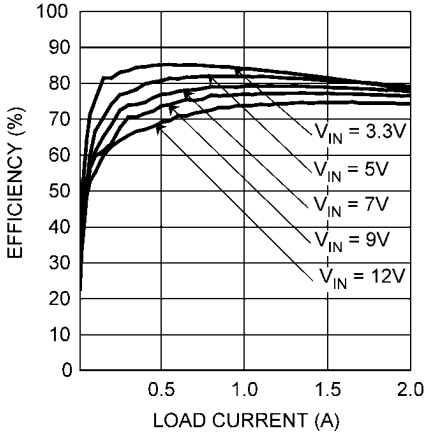
30005680

Load Transient
V_{OUT} = 3.3V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to *Figure 12*



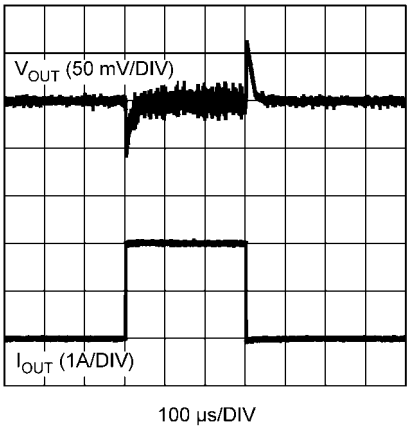
300056102

Efficiency vs Load Current
V_{OUT} = 1.8V, f_{SW} = 2 MHz
Refer to *Figure 15*



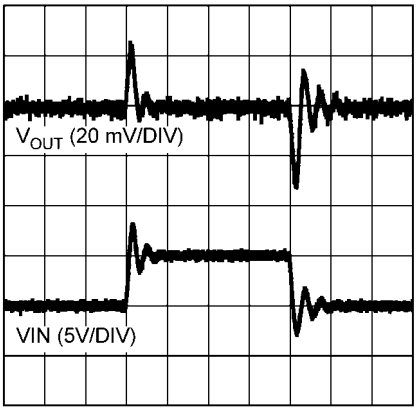
30005684

Load Transient
V_{OUT} = 1.8V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to *Figure 15*



300056105

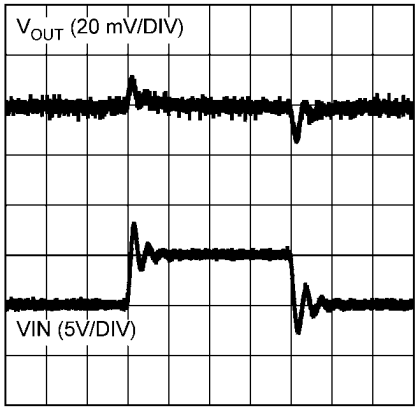
Line Transient
V_{IN} = 10 to 15V, V_{OUT} = 3.3V, no C_{FF}
Refer to *Figure 13*



100 µs/DIV

300056109

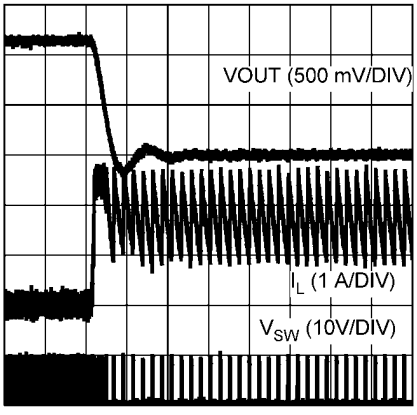
Line Transient
V_{IN} = 10 to 15V, V_{OUT} = 3.3V
Refer to *Figure 12*



100 µs/DIV

300056108

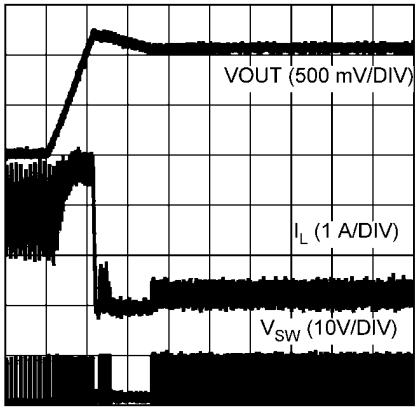
Short Circuit



20 µs/DIV

300056110

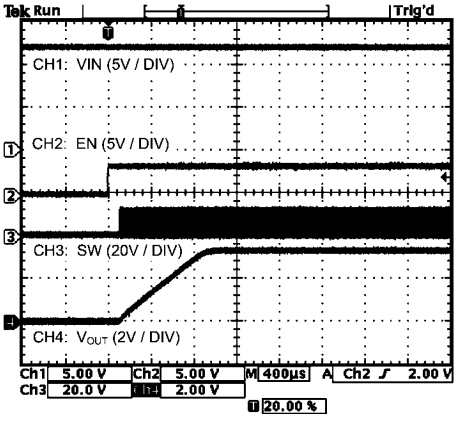
Short Circuit Release



40 µs/DIV

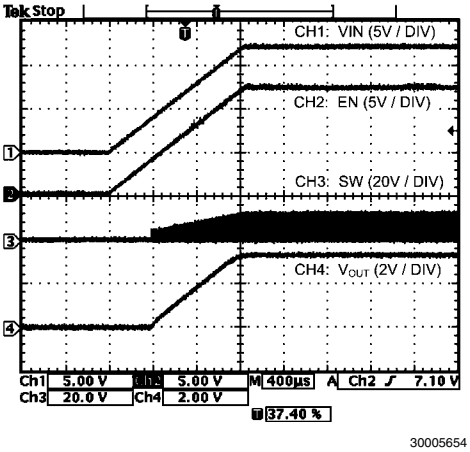
300056111

Soft Start



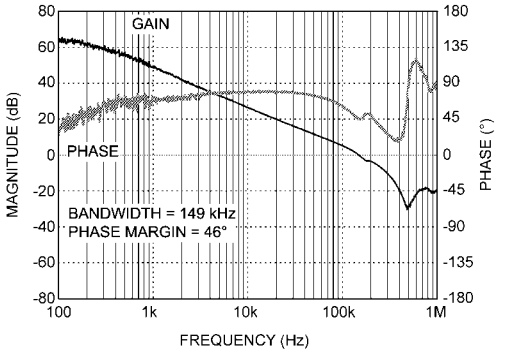
30005653

Soft Start with EN Tied to V_{IN}



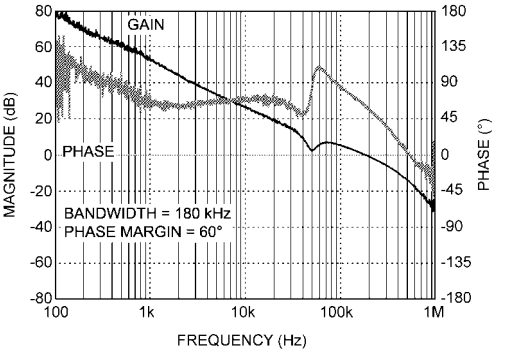
30005654

V_{IN} = 12V, V_{OUT} = 5 V, L = 2.2 µH, C_{OUT} = 44 µF Iout =1A
Refer to *Figure 10*



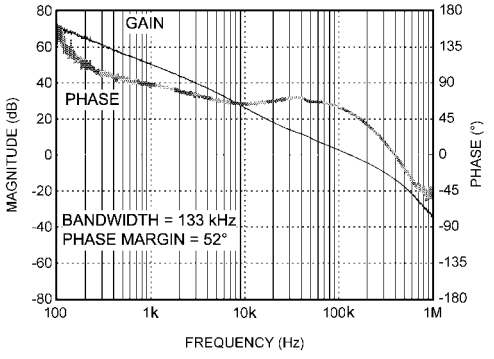
300056112

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5 µH C_{OUT} = 44 µF Iout =1A
Refer to *Figure 12*



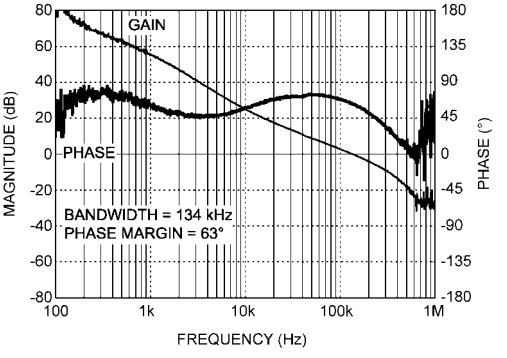
300056113

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0 µH C_{OUT} = 44 µF Iout =1A
Refer to *Figure 15*



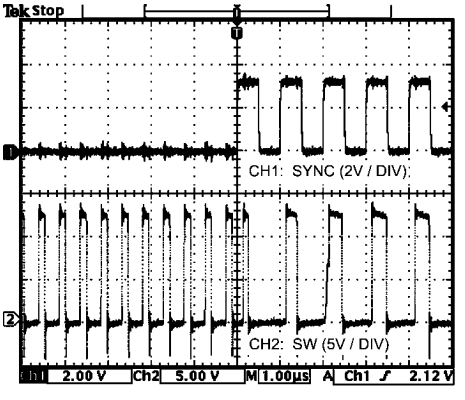
300056114

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.56 µH C_{OUT} = 68 µF Iout =1A
Refer to *Figure 17*



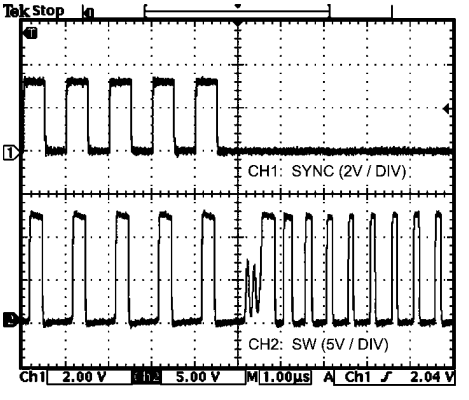
300056115

Sync Functionality



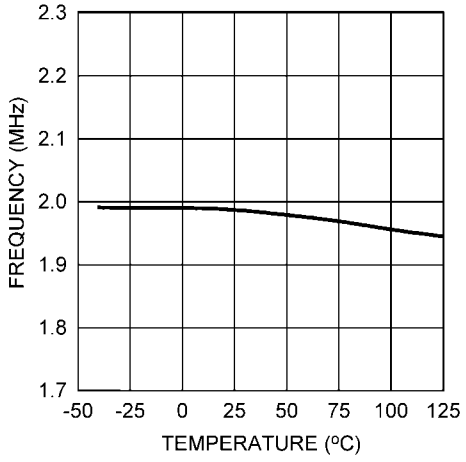
30005655

Loss of Synchronization



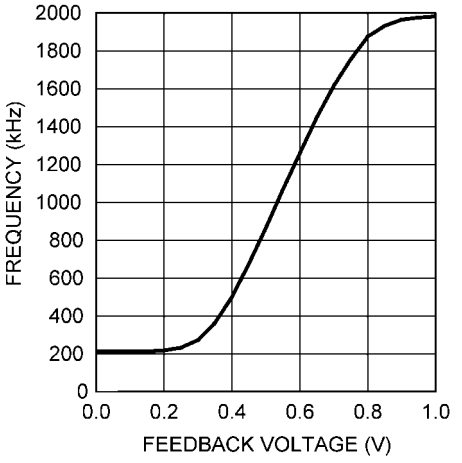
30005656

Oscillator Frequency vs Temperature
V_{SYNC} = GND, f_{SW} = 2 MHz



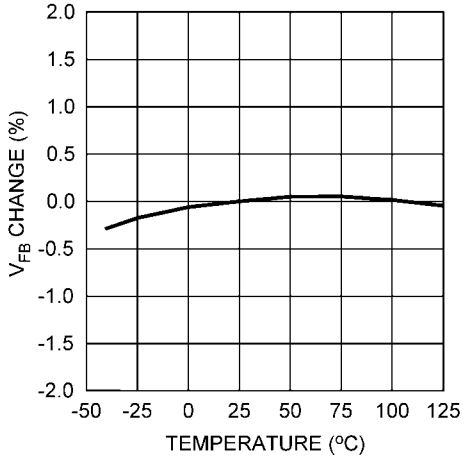
30005628

Oscillator Frequency vs V_{FB}



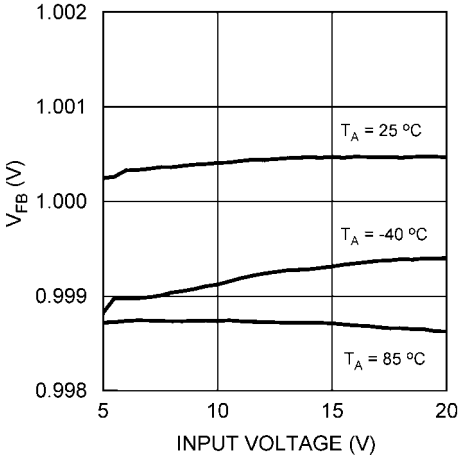
30005629

V_{FB} vs Temperature



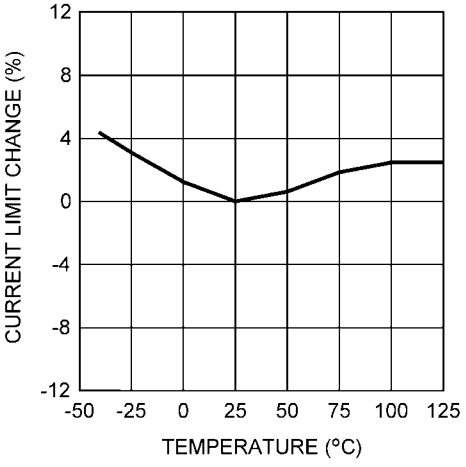
30005630

V_{FB} vs V_{IN}



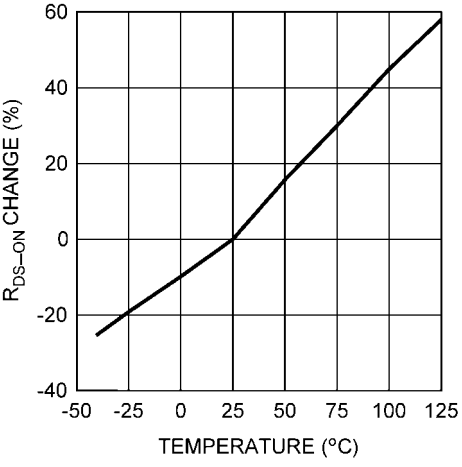
30005631

Current Limit vs Temperature
V_{IN} = 12V



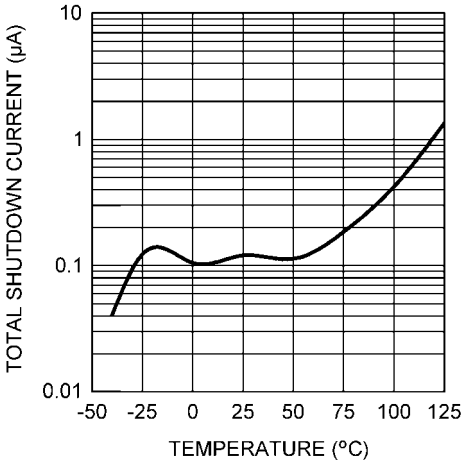
30005632

R_{DSON} vs Temperature



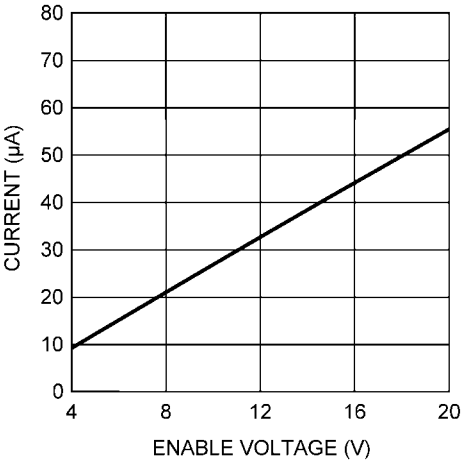
30005633

I_Q (Shutdown) vs Temperature
$I_Q = I_{AVIN} + I_{PVIN}$



30005634

I_{EN} vs V_{EN}



30005635

Block Diagram

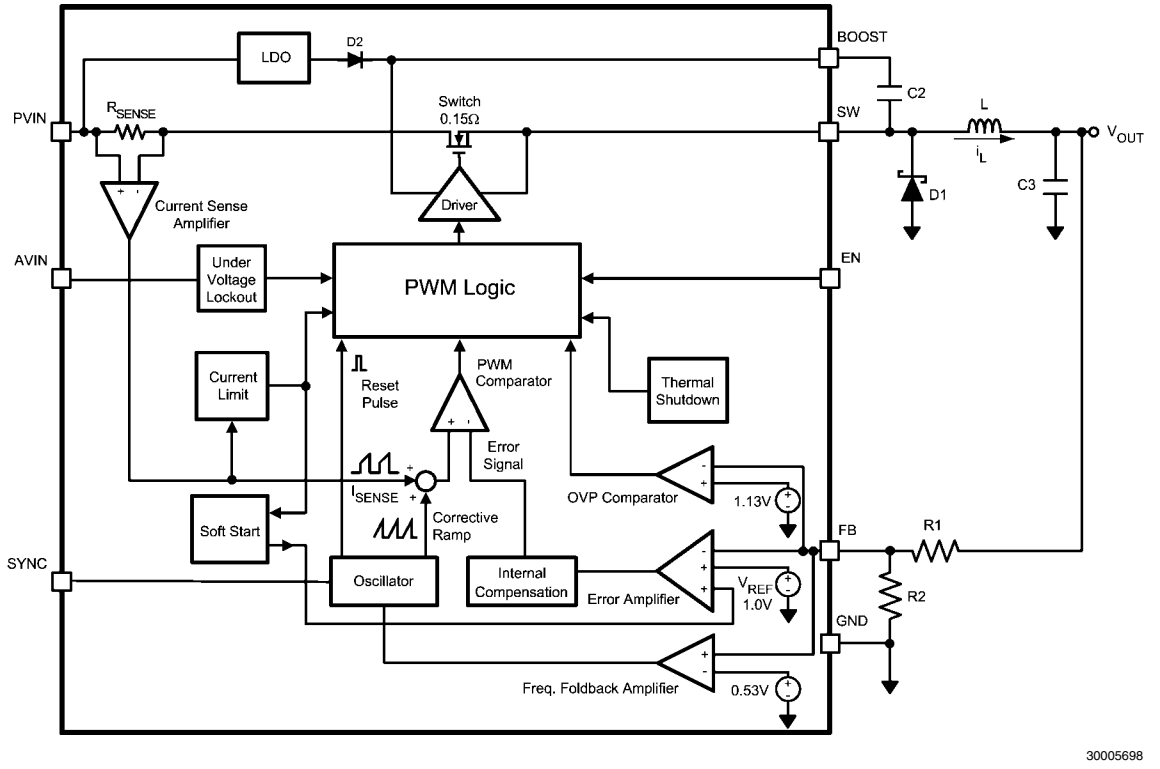


FIGURE 1.

Application Information

THEORY OF OPERATION

The LM27341/LM27342 is a constant-frequency, peak current-mode PWM buck regulator IC that delivers a 1.5 or 2A load current. The regulator has a preset switching frequency of 2 MHz. This high frequency allows the LM27341/LM27342 to operate with small surface mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LM27341/LM27342 is internally compensated, which reduces design time, and requires few external components.

The following operating description of the LM27341/LM27342 will refer to the Block Diagram (*Figure 1*) and to the waveforms in *Figure 2*. The LM27341/LM27342 supplies a regulated output voltage by switching the internal NMOS switch at a constant frequency and varying the duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (i_L) increases with a linear slope. The current-sense amplifier measures i_L, which generates an output proportional to the switch current typically called the sense signal. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage (V_{FB}) and V_{REF}. When the output of the PWM comparator goes high, the switch turns off until the next switching cycle begins. During the switch off-time (t_{OFF}), inductor current discharges through the catch diode D1, which forces the SW pin (V_{SW}) to swing below ground by the forward voltage (V_{D1}) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

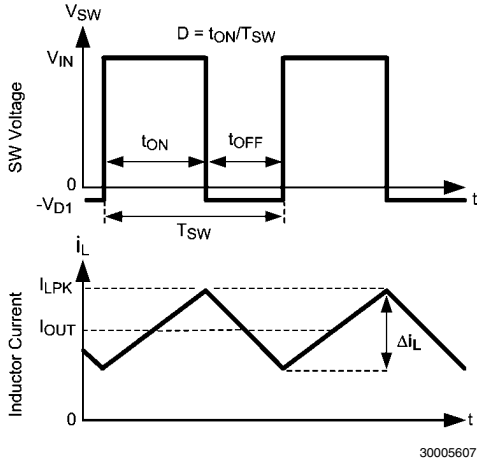


FIGURE 2. LM27341/LM27342 Waveforms of SW Pin Voltage and Inductor Current

BOOST FUNCTION

Capacitor C_2 in *Figure 1*, commonly referred to as C_{BOOST}, is used to store a voltage V_{BOOST}. When the LM27341/LM27342 starts up, an internal LDO charges C_{BOOST} ,via an internal diode, to a voltage sufficient to turn the internal NMOS switch on. The gate drive voltage supplied to the internal NMOS switch is V_{BOOST} - V_{SW}.

During a normal switching cycle, when the internal NMOS control switch is off (t_{OFF}) (refer to *Figure 2*), V_{BOOST} equals V_{LDO} minus the forward voltage of the internal diode (V_{D2}). At the same time the inductor current (i_L) forward biases the catch diode D1 forcing the SW pin to swing below ground by the forward voltage drop of the catch diode (V_{D1}). Therefore, the voltage stored across C_{BOOST} is

$$V_{BOOST} - V_{SW} = V_{LDO} - V_{D2} + V_{D1}$$

Thus,

$$V_{BOOST} = V_{SW} + V_{LDO} - V_{D2} + V_{D1}$$

When the NMOS switch turns on (t_{ON}), the switch pin rises to

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L),$$

reverse biasing D1, and forcing V_{BOOST} to rise. The voltage at V_{BOOST} is then

$$V_{BOOST} = V_{IN} – (R_{DSON} \times I_L) + V_{LDO} – V_{D2} + V_{D1}$$

which is approximately

$$V_{IN} + V_{LDO} - 0.4V$$

V_{BOOST} has pulled itself up by its "bootstraps", or boosted to a higher voltage.

LOW INPUT VOLTAGE CONSIDERATIONS

When the input voltage is below 5V and the duty cycle is greater than 75 percent, the gate drive voltage developed across C_{BOOST} might not be sufficient for proper operation of the NMOS switch. In this case, C_{BOOST} should be charged via an external Schottky diode attached to a 5V voltage rail, see *Figure 3*. This ensures that the gate drive voltage is high enough for proper operation of the NMOS switch in the triode region. Maintain V_{BOOST} - V_{SW} less than the 6V absolute maximum rating.

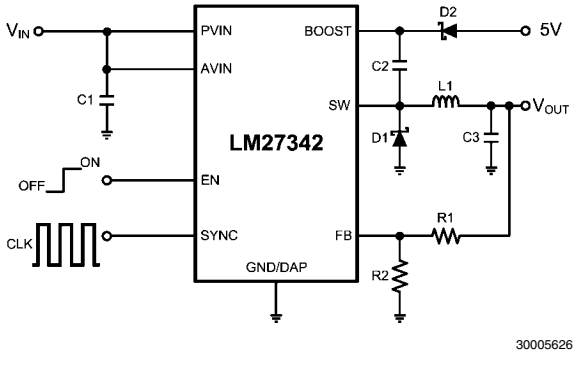


FIGURE 3. External Diode Charges C_{BOOST}

HIGH OUTPUT VOLTAGE CONSIDERATIONS

When the output voltage is greater than 3.3V, a minimum load current is needed to charge C_{BOOST}, see *Figure 4*. The minimum load current forward biases the catch diode D1 forcing the SW pin to swing below ground. This allows C_{BOOST} to charge, ensuring that the gate drive voltage is high enough for proper operation. The minimum load current depends on many factors including the inductor value.

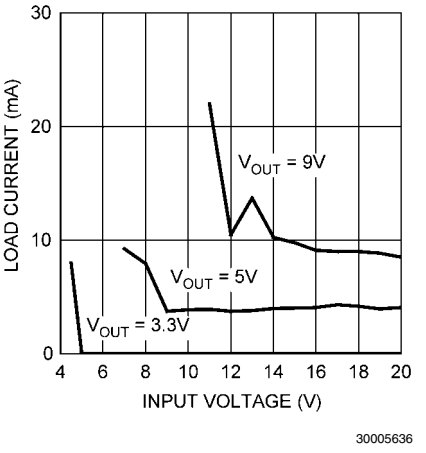


FIGURE 4. Minimum Load Current for L = 1.5 µH

ENABLE PIN / SHUTDOWN MODE

Connect the EN pin to a voltage source greater than 1.8V to enable operation of the LM27341/LM27342. Apply a voltage less than 0.4V to put the part into shutdown mode. In shutdown mode the quiescent current drops to typically 70 nA. Switch leakage adds another 40 nA from the input supply. For proper operation, the LM27341/LM27342 EN pin should never be left floating, and the voltage should never exceed V_{IN} + 0.3V.

The simplest way to enable the operation of the LM27341/LM27342 is to connect the EN pin to AVIN which allows self start-up of the LM27341/LM27342 when the input voltage is applied.

When the rise time of V_{IN} is longer than the soft-start time of the LM27341/LM27342 this method may result in an overshoot in output voltage. In such applications, the EN pin voltage can be controlled by a separate logic signal, or tied to a resistor divider, which reaches 1.8V after V_{IN} is fully established (see *Figure 5*). This will minimize the potential for output voltage overshoot during a slow V_{IN} ramp condition. Use the lowest value of V_{IN} , seen in your application when calculating the resistor network, to ensure that the 1.8V minimum EN threshold is reached.

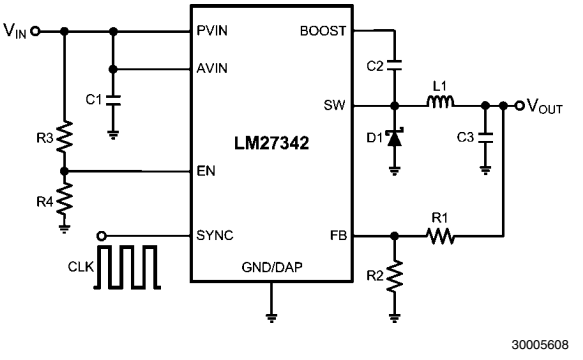


FIGURE 5. Resistor Divider on EN

$$R3 = \left(\frac{V_{IN}}{1.8} - 1\right) \times R4$$

FREQUENCY SYNCHRONIZATION

The LM27341/LM27342 switching frequency can be synchronized to an external clock, between 1.00 and 2.35 MHz, applied at the SYNC pin. At the first rising edge applied to the SYNC pin, the internal oscillator is overridden and subsequent positive edges will initiate switching cycles. If the external SYNC signal is lost during operation, the LM27341/LM27342 will revert to its internal 2 MHz oscillator within 1.5 µs. To disable Frequency Synchronization and utilize the internal 2 MHz oscillator, connect the SYNC pin to GND.

The SYNC pin gives the designer the flexibility to optimize their design. A lower switching frequency can be chosen for higher efficiency. A higher switching frequency can be chosen to keep EMI out of sensitive ranges such as the AM radio band. Synchronization can also be used to eliminate beat frequencies generated by the interaction of multiple switching power converters. Synchronizing multiple switching power converters will result in cleaner power rails.

The selected switching frequency (f_{SYNC}) and the minimum on-time (t_{MIN}) limit the minimum duty cycle (D_{MIN}) of the device.

$$D_{MIN} = t_{MIN} \times f_{SYNC}$$

Operation below D_{MIN} is not reccomended. The LM27341/LM27342 will skip pulses to keep the output voltage in regulation, and the current limit is not guaranteed. The switching is in phase but no longer at the same switching frequency as the SYNC signal.

CURRENT LIMIT

The LM27341 and LM27342 use cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 2.0A min (LM27341) or 2.5A min (LM27342) , and turns off the switch until the next switching cycle begins.

FREQUENCY FOLDBACK

The LM27341/LM27342 employs frequency foldback to protect the device from current run-away during output short-circuit. Once the FB pin voltage falls below regulation, the switch frequency will smoothly reduce with the falling FB voltage until the switch frequency reaches 220 kHz (typ). If the device is synchronized to an external clock, synchronization is disabled until the FB pin voltage exceeds 0.53V

SOFT-START

The LM27341/LM27342 has a fixed internal soft-start of 1 ms (typ). During soft-start, the error amplifier's reference voltage ramps from 0.0 V to its nominal value of 1.0 V in approximately 1 ms. This forces the regulator output to ramp in a controlled fashion, which helps reduce inrush current. Upon soft-start the part will initially be in frequency foldback and the frequency will rise as FB rises. The regulator will gradually rise to 2 MHz. The LM27341/LM27342 will allow synchronization to an external clock at FB > 0.53V.

OUTPUT OVERVOLTAGE PROTECTION

The overvoltage comparator turns off the internal power NFET when the FB pin voltage exceeds the internal reference voltage by 13% ($V_{FB} > 1.13 * V_{REF}$). With the power NFET turned off the output voltage will decrease toward the regulation level.

UNDERVOLTAGE LOCKOUT

Undervoltage lockout (UVLO) prevents the LM27341/LM27342 from operating until the input voltage exceeds 2.75V(typ).

The UVLO threshold has approximately 470 mV of hysteresis, so the part will operate until V_{IN} drops below 2.28V(typ). Hysteresis prevents the part from turning off during power up if V_{IN} has finite impedance.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the internal NMOS switch when the IC junction temperature exceeds 165°C (typ). After thermal shutdown occurs, hysteresis prevents the internal NMOS switch from turning on until the junction temperature drops to approximately 150°C.

Design Guide

INDUCTOR SELECTION

Inductor selection is critical to the performance of the LM27341/LM27342. The selection of the inductor affects stability, transient response and efficiency. A key factor in inductor selection is determining the ripple current (Δi_L) (see *Figure 2*).

The ripple current (Δi_L) is important in many ways.

First, by allowing more ripple current, lower inductance values can be used with a corresponding decrease in physical dimensions and improved transient response. On the other hand, allowing less ripple current will increase the maximum achievable load current and reduce the output voltage ripple (see Output Capacitor section for more details on calculating output voltage ripple). Increasing the maximum load current is achieved by ensuring that the peak inductor current (I_{LPK}) never exceeds the minimum current limit of 2.0A min (LM27341) or 2.5A min (LM27342) .

$$I_{LPK} = I_{OUT} + \Delta i_L / 2$$

Secondly, the slope of the ripple current affects the current control loop. The LM27341/LM27342 has a fixed slope corrective ramp. When the slope of the current ripple becomes significantly less than the converter's corrective ramp (see Figure 1), the inductor pole will move from high frequencies to lower frequencies. This negates one advantage that peak current-mode control has over voltage-mode control, which is, a single low frequency pole in the power stage of the converter. This can reduce the phase margin, crossover frequency and potentially cause instability in the converter. Contrarily, when the slope of the ripple current becomes significantly greater than the converter's corrective ramp, resonant peaking can occur in the control loop. This can also cause instability (Sub-Harmonic Oscillation) in the converter. For the power supply designer this means that for lower switching frequencies the current ripple must be increased to keep the inductor pole well above crossover. It also means that for higher switching frequencies the current ripple must be decreased to avoid resonant peaking.

With all these factors, how is the desired ripple current selected? The ripple ratio (r) is defined as the ratio of inductor ripple current (Δi_L) to output current (I_{OUT}), evaluated at maximum load:

$$r = \frac{\Delta i_L}{I_{OUT}}$$

A good compromise between physical size, transient response and efficiency is achieved when we set the ripple ratio between 0.2 and 0.4. The recommended ripple ratio vs. duty cycle shown below (see *Figure 6*) is based upon this compromise and control loop optimizations. Note that this is just

a guideline. Please see Application note AN-1197 for further considerations.

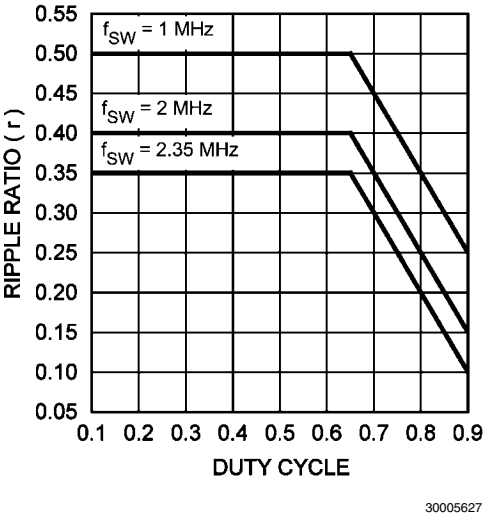


FIGURE 6. Recommended Ripple Ratio Vs. Duty Cycle

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}}$$

The application's lowest input voltage should be used to calculate the ripple ratio. The catch diode forward voltage drop (V_{D1}) and the voltage drop across the internal NFET (V_{DS}) must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}}$$

V_{DS} can be approximated by:

$$V_{DS} = I_{OUT} \times R_{DS(ON)}$$

The diode forward drop (V_{D1}) can range from 0.3V to 0.5V depending on the quality of the diode. The lower V_{D1} is, the higher the operating efficiency of the converter.

Now that the ripple current or ripple ratio is determined, the required inductance is calculated by:

$$L = \frac{V_{OUT} + V_{D1}}{I_{OUT} \times r \times f_{SW}} \times (1\text{-}D_{MIN})$$

where D_{MIN} is the duty cycle calculated with the maximum input voltage, f_{sw} is the switching frequency, and I_{OUT} is the maximum output current of 2A. Using I_{OUT} = 2A will minimize the inductor's physical size.

INDUCTOR CALCULATION EXAMPLE

Operating conditions for the LM27342 are:

V_{IN} = 7 - 16V V_{OUT} = 3.3V I_{OUT} = 2A

f_{SW} = 2 MHz V_{D1} = 0.5V

First the maximum duty cycle is calculated.

$$D_{MAX} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} - V_{DS})$$
$$= (3.3V + 0.5V) / (7V + 0.5V - 0.30V)$$
$$= 0.528$$

Using *Figure 6* gives us a recommended ripple ratio = 0.4.

Now the minimum duty cycle is calculated.

$$D_{MIN} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} - V_{DS})$$
$$= (3.3V + 0.5V) / (16V + 0.5V - 0.30V)$$
$$= 0.235$$

The inductance can now be calculated.

$$L = (1 - D_{MIN}) \times (V_{OUT} + V_{D1}) / (I_{OUT} \times r \times f_{sw})$$
$$= (1 - 0.235) \times (3.3V + .5V) / (2A \times 0.4 \times 2\ MHz)$$
$$= 1.817\ \mu H$$

This is close to the standard inductance value of 1.8 µH. This leads to a 1% deviation from the recommended ripple ratio, which is now 0.4038.

Finally, we check that the peak current does not reach the minimum current limit of 2.5A.

$$I_{LPK} = I_{OUT} \times (1 + r / 2)$$
$$= 2A \times (1 + .4038 / 2)$$
$$= 2.404A$$

The peak current is less than 2.5A, so the DC load specification can be met with this ripple ratio. To design for the LM27341 simply replace I_{OUT} = 1.5A in the equations for I_{LPK} and see that I_{LPK} does not exceed the LM27341's current limit of 2.0A (min).

INDUCTOR MATERIAL SELECTION

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. To prevent the inductor from saturating over the entire -40 °C to 125 °C range, pick an inductor with a saturation current higher than the upper limit of I_{CL} listed in the Electrical Characteristics table.

Ferrite core inductors are recommended to reduce AC loss and fringing magnetic flux. The drawback of ferrite core inductors is their quick saturation characteristic. The current limit circuit has a propagation delay and so is oftentimes not fast enough to stop a saturated inductor from going above the current limit. This has the potential to damage the internal switch. To prevent a ferrite core inductor from getting into saturation, the inductor saturation current rating should be higher than the switch current limit I_{CL}. The LM27341/LM27342 is quite robust in handling short pulses of current that are a few amps above the current limit. Saturation protection is provided by a second current limit which is 30% higher than the cycle by cycle current limit. When the saturation protection is triggered the part will turn off the output switch and attempt to soft-start. (When a compromise has to be made, pick an inductor with a saturation current just above the lower limit of the I_{CL}.) Be sure to validate the short-circuit protection over the intended temperature range.

An inductor's saturation current is usually lower when hot. So consult the inductor vendor if the saturation current rating is only specified at room temperature.

Soft saturation inductors such as the iron powder types can also be used. Such inductors do not saturate suddenly and

therefore are safer when there is a severe overload or even shorted output. Their physical sizes are usually smaller than the Ferrite core inductors. The downside is their fringing flux and higher power dissipation due to relatively high AC loss, especially at high frequencies.

INPUT CAPACITOR

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and Equivalent Series Inductance (ESL). The recommended input capacitance is 10 µF, although 4.7 µF works well for input voltages below 6V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS-IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)}$$

where r is the ripple ratio defined earlier, I_{OUT} is the output current, and D is the duty cycle. It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LM27341/LM27342, certain capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier Low ESR are all good choices for input capacitors and have acceptable ESL. Multilayer ceramic capacitors (MLCC) have very low ESL. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult the capacitor manufacturer's datasheet to see how rated capacitance varies over operating conditions.

OUTPUT CAPACITOR

The output capacitor is selected based upon the desired output ripple and transient response. The LM27341/2's loop compensation is designed for ceramic capacitors. A minimum of 22 µF is required at 2 MHz (33 uF at 1 MHz) while 47 - 100 µF is recommended for improved transient response and higher phase margin. The output voltage ripple of the converter is:

$$\Delta V_{OUT} = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not.

The transient response is determined by the speed of the control loop and the ability of the output capacitor to provide the initial current of a load transient. Capacitance can be increased significantly with little detriment to the regulator stability. However, increasing the capacitance provides diminishing improvement over 100 uF in most applications, because the bandwidth of the control loop decreases as output capacitance increases. If improved transient performance is required, add a feed forward capacitor. This becomes especially important for higher output voltages where the bandwidth of the LM27341/LM27342 is lower. See Feed Forward Capacitor and Frequency Synchronization sections.

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet the following condition:

$$I_{RMS-OUT} = I_{OUT} \times \frac{r}{\sqrt{12}}$$

where I_{OUT} is the output current, and r is the ripple ratio.

CATCH DIODE

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_{OUT} \times (1\text{-}D)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency choose a Schottky diode with a low forward voltage drop.

BOOST DIODE (OPTIONAL)

For circuits with input voltages V_{IN} < 5V and duty cycles (D) >0.75V. a small-signal Schottky diode is recommended. A good choice is the BAT54 small signal diode. The cathode of the diode is connected to the BOOST pin and the anode to a 5V voltage rail.

BOOST CAPACITOR

A ceramic 0.1 µF capacitor with a voltage rating of at least 6.3V is sufficient. The X7R and X5R MLCCs provide the best performance.

OUTPUT VOLTAGE

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good starting value for R2 is 1 kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2$$

FEED FORWARD CAPACITOR (OPTIONAL)

A feed forward capacitor C_{FF} can improve the transient response of the converter. Place C_{FF} in parallel with R1. The value of C_{FF} should place a zero in the loop response at, or above, the pole of the output capacitor and R_{LOAD}. The C_{FF} capacitor will increase the crossover frequency of the design, thus a larger minimum output capacitance is required for designs using C_{FF}. C_{FF} should only be used with an output capacitance greater than or equal to 44 uF.

$$C_{FF} <= \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R1}$$

Calculating Efficiency, and Junction Temperature

The complete LM27341/LM27342 DC-DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D).

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}}$$

V_{DS} is the voltage drop across the internal NFET when it is on, and is equal to:

$$V_{DS} = I_{OUT} \times R_{DSON}$$

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the Electrical Characteristics section of the schottky diode datasheet. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_{D1} + V_{DCR}}{V_{IN} + V_{D1} - V_{DS}}$$

V_{DCR} usually gives only a minor duty cycle change, and has been omitted in the examples for simplicity.

SCHOTTKY DIODE CONDUCTION LOSSES

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_{D1} \times I_{OUT} (1\text{-}D)$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

INDUCTOR CONDUCTION LOSSES

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR}$$

MOSFET CONDUCTION LOSSES

The LM27341/LM27342 conduction loss is mainly associated with the internal NFET:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D$$

MOSFET SWITCHING LOSSES

Switching losses are also associated with the internal NFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node:

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$$

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times f_{SW} \times t_{RISE})$$

$$P_{SW} = P_{SWF} + P_{SWR}$$

Typical Rise and Fall Times vs Input Voltage

V_{IN}	t_{RISE}	t_{FALL}
5V	8ns	8ns
10V	9ns	9ns
15V	10ns	10ns

IC QUIESCENT LOSSES

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN}$$

I_Q is the quiescent operating current, and is typically around 2.4 mA.

MOSFET DRIVER LOSSES

The other operating power that needs to be calculated is that required to drive the internal NFET:

$$P_{BOOST} = I_{BOOST} \times V_{BOOST}$$

V_{BOOST} is normally between 3VDC and 5VDC. The I_{BOOST} rms current is dependant on switching frequency f_{SW}. I_{BOOST} is approximately 8.2 mA at 2 MHz and 4.4 mA at 1 MHz.

TOTAL POWER LOSSES

Total power losses are:

$$P_{LOSS} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST} + P_{DIODE} + P_{IND}$$

Losses internal to the LM27341/LM27342 are:

$$P_{INTERNAL} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST}$$

EFFICIENCY CALCULATION EXAMPLE

Operating conditions are:

V_{IN} = 12V	V_{OUT} = 3.3V	I_{OUT} = 2A
f_{SW} = 2 MHz	V_{D1} = 0.5V	R_{DCR} = 20 mΩ

Internal Power Losses are:

P_{COND}	$= I_{OUT}^2 \times R_{DSON} \times D$	
	$= 2^2 \times 0.15\Omega \times 0.314$	= 188 mW
P_{SW}	$= (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$	
	= (12V x 2A x 2 MHz x 10ns)	= 480 mW
P_Q	$= I_Q \times V_{IN}$	
	= 2.4 mA x 12V	= 29 mW
P_{BOOST}	$= I_{BOOST} \times V_{BOOST}$	
	= 8.2 mA x 4.5V	= 37 mW
$P_{INTERNAL}$	$= P_{COND} + P_{SW} + P_Q + P_{BOOST}$	= 733 mW

Total Power Losses are:

P_{DIODE} = V_{D1} x I_{OUT} (1 - D)
= 0.5V x 2 x (1 - 0.314) = 686 mW

P_{IND} = I_{OUT}^2 x R_{DCR}
= 2^2 x 20 mΩ = 80 mW

P_{LOSS} = $P_{INTERNAL}$ + P_{DIODE} + P_{IND} = 1.499 W

The efficiency can now be estimated as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{6.6\ W}{6.6\ W + 1.499\ W} = 81\ \%$$

With this information we can estimate the junction temperature of the LM27341/LM27342.

CALCULATING THE LM27341/LM27342 JUNCTION TEMPERATURE

Thermal Definitions:

T_J = IC junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from IC junction to device case

$R_{\theta JA}$ = Thermal resistance from IC junction to ambient air

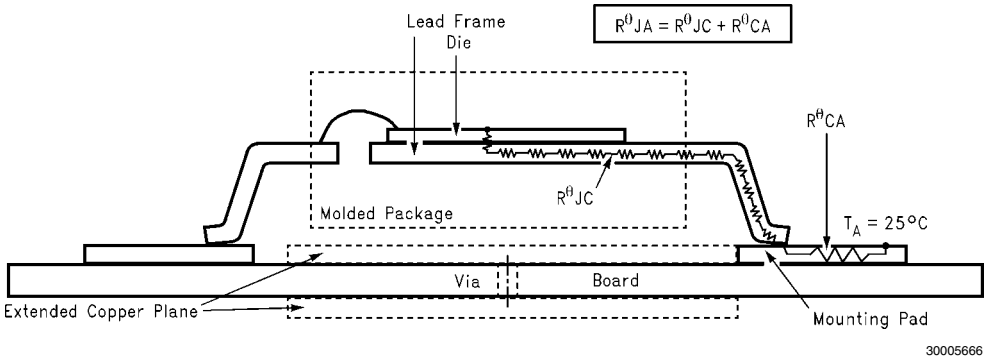


FIGURE 7. Cross-Sectional View of Integrated Circuit Mounted on a Printed Circuit Board.

Heat in the LM27341/LM27342 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs conductor).

Heat Transfer goes as:

Silicon→Lead Frame→PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{Power}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{Power}$$

This impedance can vary depending on the thermal properties of the PCB. This includes PCB size, weight of copper used to route traces , the ground plane, and the number of layers within the PCB. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Six to nine thermal vias should be placed under the exposed pad to the ground plane. Placing more than nine thermal vias results in only a small reduction to $R_{\theta JA}$ for the same copper area. These vias should have 8 mil holes to avoid wicking solder away from the DAP. See AN-1187 and AN-1520 for more information on package thermal performance. If a compromise for cost needs to be made, the thermal vias for the eMSOP package can range from 8-14 mils, this will increase the possibility of solder wicking.

To predict the silicon junction temperature for a given application, three methods can be used. The first is useful before prototyping and the other two can more accurately predict the junction temperature within the application.

Method 1:

The first method predicts the junction temperature by extrapolating a best guess $R_{\theta JA}$ from the table or graph. The tables and graph are for natural convection. The internal dissipation can be calculated using the efficiency calculations. This allows the user to make a rough prediction of the junction temperature in their application. Methods two and three can later be used to determine the junction temperature more accurately.

The two tables below have values of $R_{\theta JA}$ for the LLP and the eMSOP package.

$R_{\theta JA}$ values for the eMSOP @ 1Watt dissipation:

Number of Board Layers	Size of Bottom Layer Copper Connected to DAP	Size of Top Layer Copper Connected to Dap	Number of 10 mil Thermal Vias	$R_{\theta JA}$
2	0.25 in²	0.05 in²	8	80.6 ° C/W
2	0.5625 in²	0.05 in²	8	70.9 ° C/W
2	1 in²	0.05 in²	8	62.1 ° C/W
2	1.3225 in²	0.05 in²	8	54.6 ° C/W
4 (Eval Board)	3.25 in²	2.25 in²	14	35.3 ° C/W

$R_{\theta JA}$ values for the LLP @ 1Watt dissipation:

Number of Board Layers	Size of Bottom Layer Copper Connected to DAP	Size of Top Layer Copper Connected to Dap	Number of 8 mil Thermal Vias	$R_{\theta JA}$
2	0.25 in²	0.05 in²	8	78 °C/W
2	0.5625 in²	0.05 in²	8	65.6 ° C/W
2	1 in²	0.05 in²	8	58.6 ° C/W
2	1.3225 in²	0.05 in²	8	50 °C/W
4 (Eval Board)	3.25 in²	2.25 in²	15	30.7 ° C/W

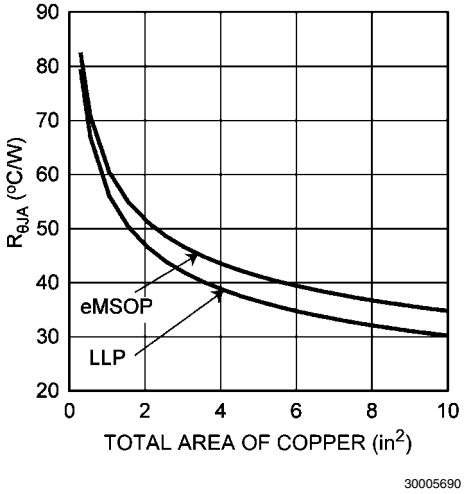


FIGURE 8. Estimate of Thermal Resistance vs. Ground Copper Area
Eight Thermal Vias and Natural Convection

Method 2:

The second method requires the user to know the thermal impedance of the silicon junction to case. ($R_{\theta JC}$) is approximately 9.5°C/W for the eMSOP package or 9.1°C/W for the LLP. The case temperature should be measured on the bottom of the PCB at a thermal via directly under the DAP of the LM27341/LM27342. The solder resist should be removed from this area for temperature testing. The reading will be more accurate if it is taken midway between pins 2 and 9, where the NMOS switch is located. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature (T_C) we have:

$$R_{\theta JC} = \frac{T_J - T_C}{Power}$$

Therefore:

$$T_J = (R_{\theta JC} \times P_{LOSS}) + T_C$$

METHOD 2 EXAMPLE

The operating conditions are the same as the previous Efficiency Calculation:

V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 2A
f_{SW} = 2 MHz V_{D1} = 0.5V R_{DCR} = 20 mΩ

Internal Power Losses are:

P_{COND} = $I_{OUT}^2 \times R_{DSON} \times D$
= $2^2 \times 0.15\Omega \times 0.314$ = 188 mW

P_{SW} = $(V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL})$
= (12V x 2A x 2 MHz x 10ns) = 480 mW

P_Q = $I_Q \times V_{IN}$
= 1.5 mA x 12V = 29 mW

P_{BOOST} = $I_{BOOST} \times V_{BOOST}$
= 7 mA x 4.5V = 37 mW

$P_{INTERNAL}$ = $P_{COND} + P_{SW} + P_Q + P_{BOOST}$ = 733 mW

The junction temperature can now be estimated as:

$$T_J = (R_{\theta JC} \times P_{INTERNAL}) + T_C$$

A National Semiconductor eMSOP evaluation board was used to determine the T_J of the LM27341/LM27342. The four layer PCB is constructed using FR4 with 2oz copper traces. There is a ground plane on the internal layer directly beneath the device, and a ground plane on the bottom layer. The ground plane is accessed by fourteen 10 mil vias. The board measures 2in x 2in (50.8mm x 50.8mm). It was placed in a container with no airflow. The case temperature measured on this LM27342MY Demo Board was 48.7°C. Therefore,

$$T_J = (9.5\ °C/W \times 733\ mW) + 48.7\ °C$$

$$T_J = 55.66\ °C$$

To keep the Junction temperature below 125 °C for this layout, the ambient temperature must stay below 94.33 °C.

$$T_{A\_MAX} = T_{J\_MAX} - T_J + T_A$$

$$T_{A\_MAX} = 125\ °C - 55.66\ °C + 25\ °C$$

$$T_{A\_MAX} = 94.33\ °C$$

Method 3:

The third method can also give a very accurate estimate of silicon junction temperature. The first step is to determine

$R_{\theta JA}$ of the application. The LM27341/LM27342 has over-temperature protection circuitry. When the silicon temperature reaches 165 °C, the device stops switching. The protection circuitry has a hysteresis of 15 °C. Once the silicon temperature has decreased to approximately 150 °C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any PCB can be characterized during the early stages of the design by raising the ambient temperature in the given application until the circuit enters thermal shutdown. If the SW-pin is monitored, it will be obvious when the internal NFET stops switching indicating a junction temperature of 165 °C. We can calculate the internal power dissipation from the above methods. All that is needed for calculation is the estimate of R_{DSON} at 165 °C. This can be extracted from the graph of R_{DSON} vs. Temperature. The value is approximately 0.267 ohms. With this, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165^{o}C - T_A}{P_{INTERNAL}}$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

METHOD 3 EXAMPLE

The operating conditions are the same as the previous Efficiency Calculation:

V_{IN} = 12V	V_{OUT} = 3.3V	I_{OUT} = 2A
f_{SW} = 2 MHz	V_{D1} = 0.5V	R_{DCR} = 20 mΩ

Internal Power Losses are:

P_{COND}	= I_{OUT}^2 x R_{DSON} x D	
	= 2^2 x 0.267Ω x .314	= 335 mW
P_{SW}	= (V_{IN} x I_{OUT} x f_{SW} x t_{FALL})	
	= (12V x 2A x 2 MHz x 10nS)	= 480 mW
P_Q	= I_Q x V_{IN}	
	= 1.5 mA x 12V	= 29 mW
P_{BOOST}	= I_{BOOST} x V_{BOOST}	
	= 7 mA x 4.5V	= 37 mW
$P_{INTERNAL}$	= P_{COND} + P_{SW} + P_Q + P_{BOOST}	= 881 mW

Using a National Semiconductor eMSOP evaluation board to determine the $R_{\theta JA}$ of the board. The four layer PCB is constructed using FR4 with 2oz copper traces. There is a ground plane on the internal layer directly beneath the device, and a ground plane on the bottom layer. The ground plane is accessed by fourteen 10 mil vias. The board measures 2in x 2in (50.8mm x 50.8mm). It was placed in an oven with no forced airflow.

The ambient temperature was raised to 132 °C, and at that temperature, the device went into thermal shutdown. $R_{\theta JA}$ can now be calculated.

$$R_{\theta JA} = \frac{165^{o}C - 132^{o}C}{0.881\ W} = 37.46\ ^{o}C/W$$

To keep the Junction temperature below 125 °C for this layout, the ambient temperature must stay below 92 °C.

$$T_{A\_MAX} = T_{J\_MAX} - (R_{\theta JA} \times P_{INTERNAL})$$

$$T_{A\_MAX} = 125\ °C - (37.46\ °C/W \times 0.881\ W)$$

$$T_{A\_MAX} = 92\ °C$$

This calculation of the maximum ambient temperature is only 2.3 °C different from the calculation using method 2. The methods described above to find the junction temperature in the eMSOP package can also be used to calculate the junction temperature in the LLP package. The 10 pin LLP package has a $R_{\theta JC}$ = 9.1°C/W, while $R_{\theta JA}$ can vary depending on the layout. $R_{\theta JA}$ can be calculated in the same manner as described in method 3.

PCB Layout Considerations

COMPACT LAYOUT

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines will help the user design a circuit with maximum rejection of outside EMI and minimum generation of unwanted EMI.

Parasitic inductance can be reduced by keeping the power path components close together and keeping the area of the loops small, on which high currents travel. Short, thick traces or copper pours (shapes) are best. In particular, the switch node (where L1, D1, and the SW pin connect) should be just large enough to connect all three components without excessive heating from the current it carries. The LM27341/LM27342 operates in two distinct cycles (see *Figure 2*) whose high current paths are shown below in *Figure 9*:

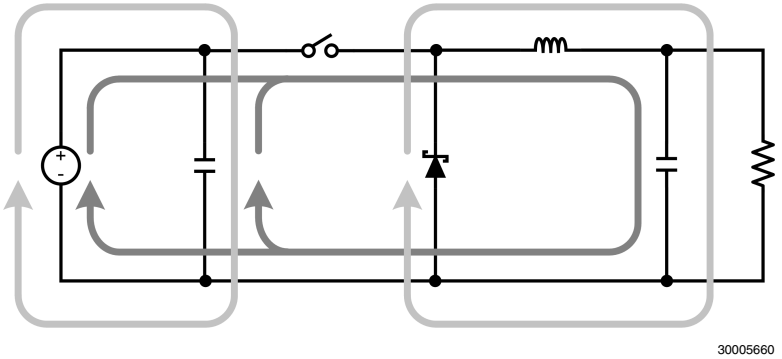


FIGURE 9. Buck Converter Current Loops

The dark grey, inner loop represents the high current path during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

GROUND PLANE AND SHAPE ROUTING

The diagram of *Figure 9* is also useful for analyzing the flow of continuous current vs. the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing should be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just like any other circuit path. The path between the input source and the input capacitor and the path between the catch diode and the load are examples of continuous current paths. In contrast, the path between the catch diode and the input capacitor carries a large pulsating current. This path should be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel should be used right at the pad of the input capacitor to connect the component side shapes to the ground plane. A second pulsating current loop that is often ignored is the gate drive loop formed by the SW and BOOST pins and boost capacitor C_{BOOST}. To minimize this loop and the EMI it generates, keep C_{BOOST} close to the SW and BOOST pins.

FB LOOP

The FB pin is a high-impedance input, and the loop created by R2, the FB pin and ground should be made as small as possible to maximize noise rejection. R2 should therefore be placed as close as possible to the FB and GND pins of the IC.

PCB SUMMARY

1. Minimize the parasitic inductance by keeping the power path components close together and keeping the area of the high-current loops small.
2. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground connections should be immediately adjacent, with multiple vias in parallel at the pad of the input capacitor connected to GND. Place C_{IN} and D1 as close to the IC as possible.
3. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which should be near the GND connections of C_{IN} and D1.
4. There should be a continuous ground plane on the copper layer directly beneath the converter. This will reduce parasitic inductance and EMI.
5. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 should be routed away from the inductor and any other traces that are switching.
6. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the layout designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-1229 for further considerations and the LM27342 demo board as an example of a four-layer layout.

LM27341/LM27342 Circuit Examples

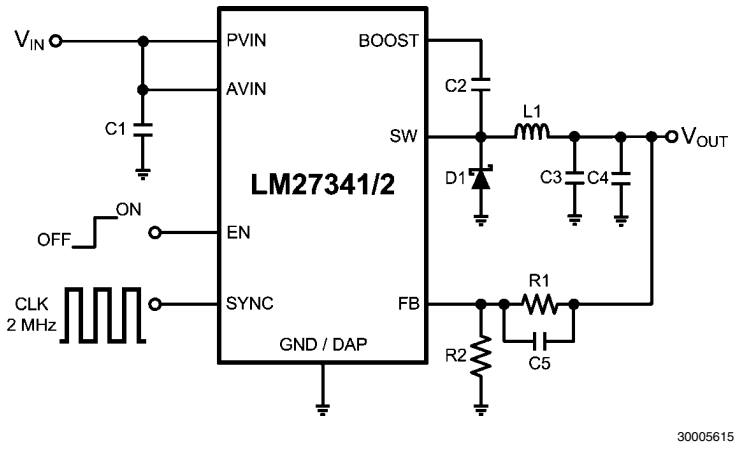
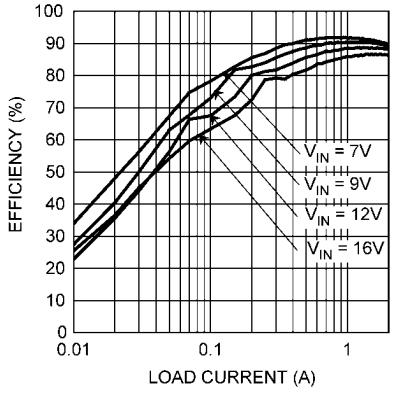
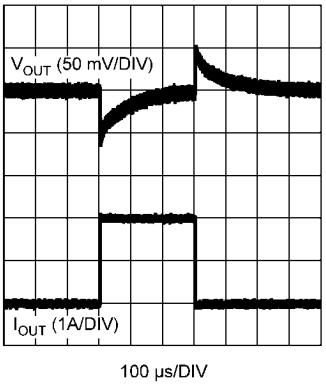


FIGURE 10. V_{IN} = 7 - 16V, V_{OUT} = 5V, f_{SW} = 2 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 10*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	2.2 µH	CDRHD5D28RHPNP	Sumida
Feedback Resistor	R1	560Ω	CRCW0603560RFKEA	Vishay
Feedback Resistor	R2	140Ω	CRCW0603140RFKEA	Vishay

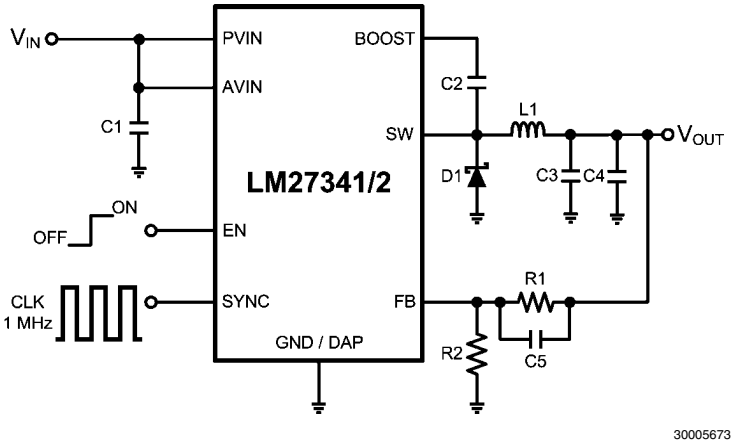
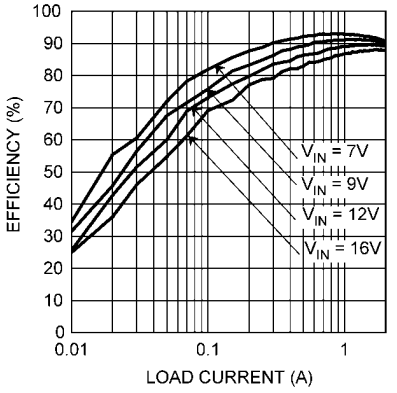
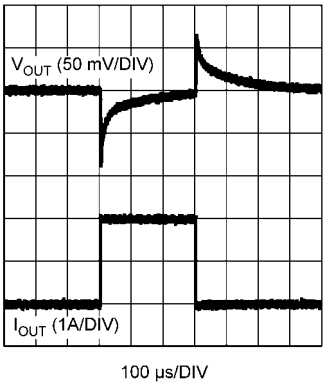


FIGURE 11. V_{IN} = 7 - 16V, V_{OUT} = 5V, f_{SW} = 1 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 11*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0. 27 µF	C0603C274K4RACTU	Kemet
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	3.3 µH	CDRH6D26HPNP	Sumida
Feedback Resistor	R1	560Ω	CRCW0603560RFKEA	Vishay
Feedback Resistor	R2	140Ω	CRCW0603140RFKEA	Vishay

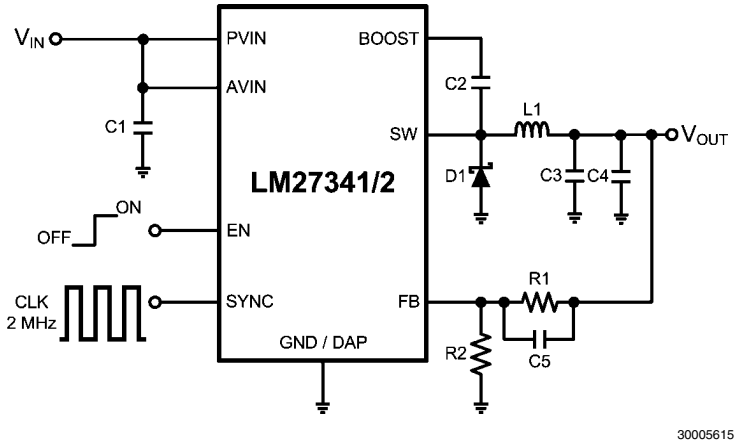
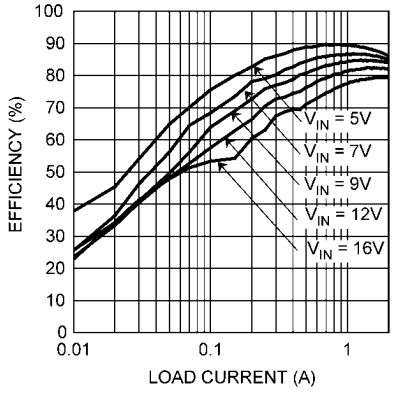
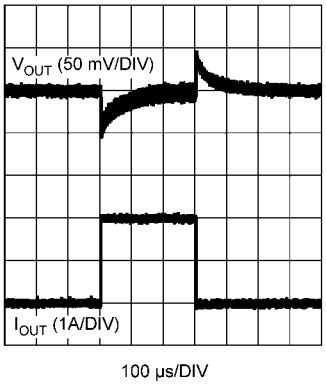


FIGURE 12. V_{IN} = 5 - 16V, V_{OUT} = 3.3V, f_{SW} = 2 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 12*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.5 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback Resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

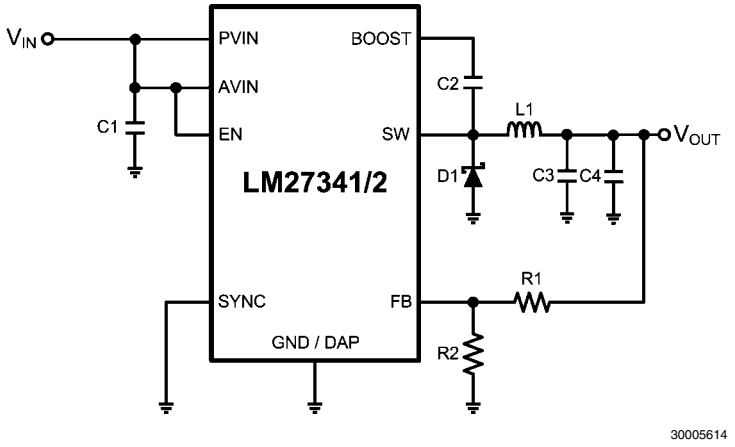
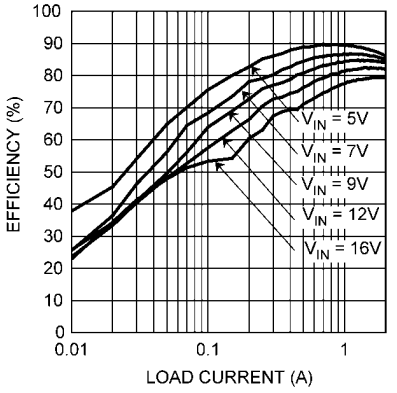
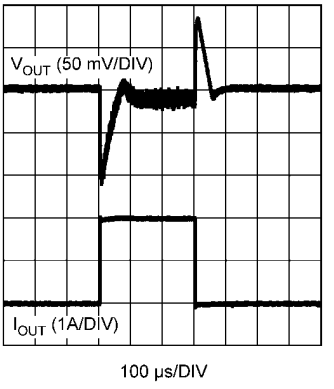


FIGURE 13. V_{IN} = 5 - 16V, V_{OUT} = 3.3V, f_{SW} = 2 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 13*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.5 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback Resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

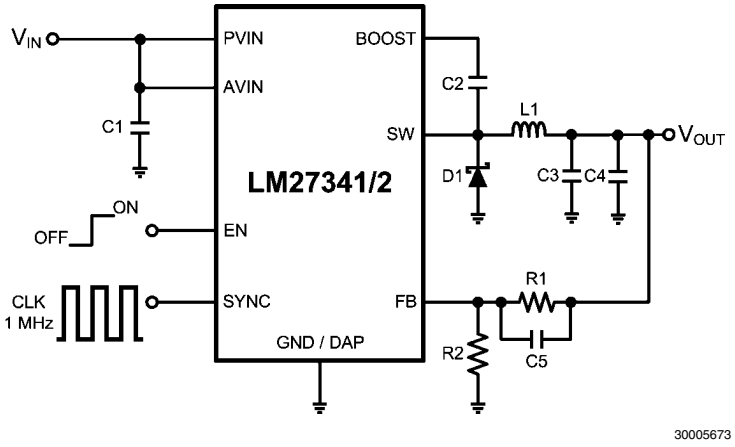
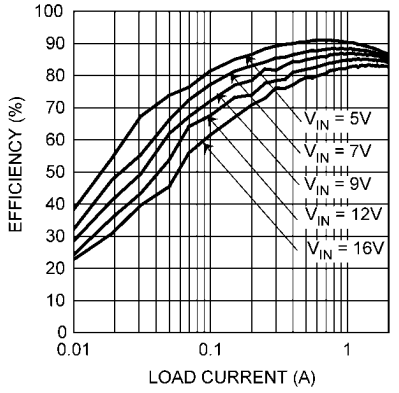
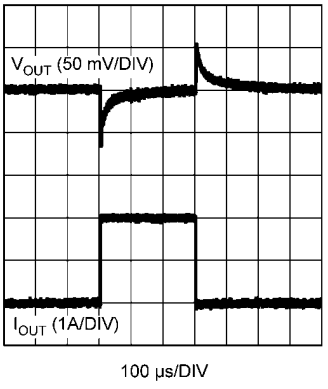


FIGURE 14. V_{IN} = 5 - 16V, V_{OUT} = 3.3V, f_{SW} = 1 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 14*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	0.27 µF	C0603C274K4RACTU	Kemet
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	2.7 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	430 Ω	CRCW0603430RFKEA	Vishay
Feedback Resistor	R2	187 Ω	CRCW0603187RFKEA	Vishay

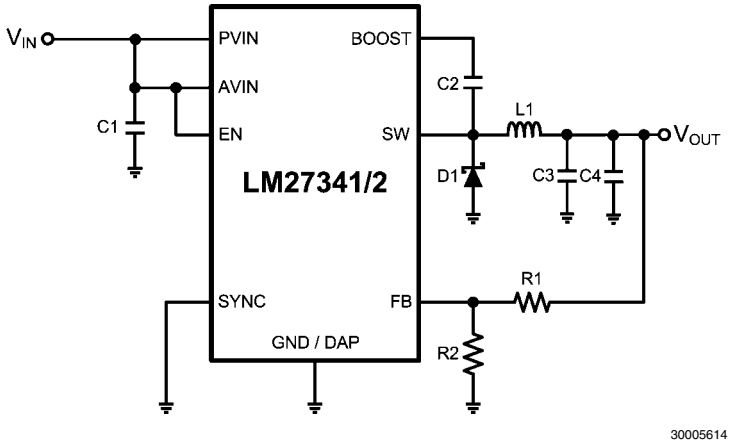
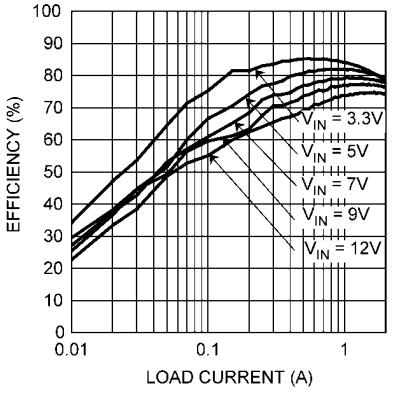
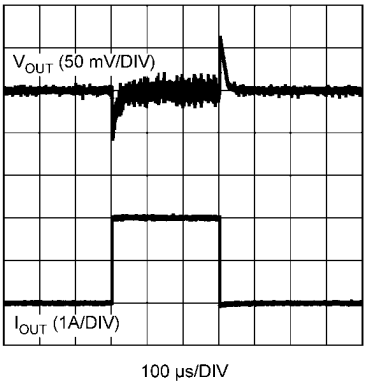


FIGURE 15. V_{IN} = 3.3 - 16V, V_{OUT} = 1.8V, f_{SW} = 2 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 15*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.0 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback Resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

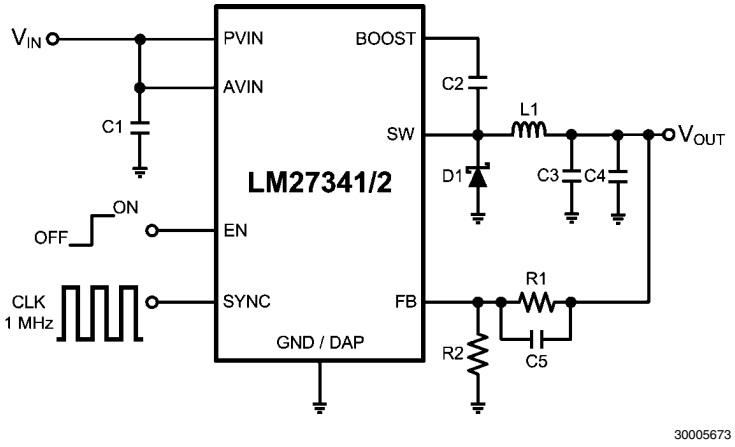
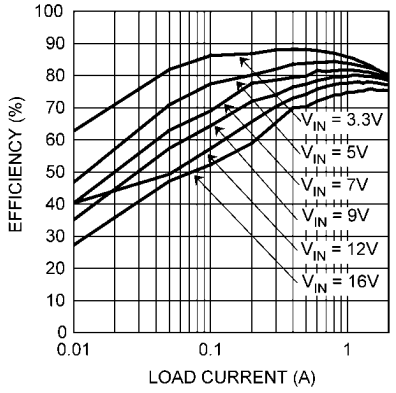
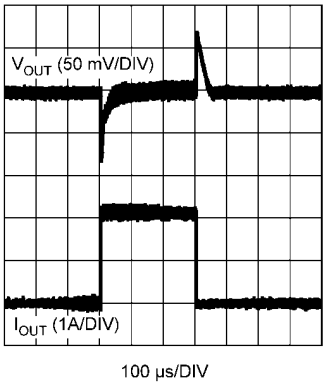


FIGURE 16. V_{IN} = 3.3 - 16V, V_{OUT} = 1.8V, f_{SW} = 1 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current



Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

Bill of Materials for *Figure 16*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 uF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 uF	C3225X7R1C226K	TDK
C_{FF}	C5	3.9 nF	GRM188R71H392KA01D	Murata
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.8 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback Resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

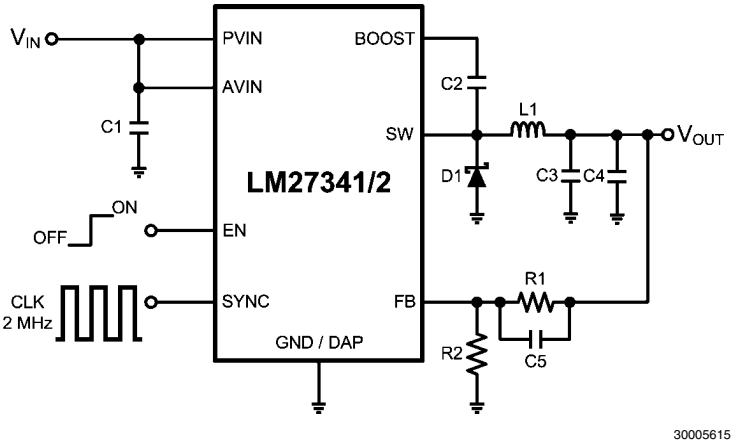
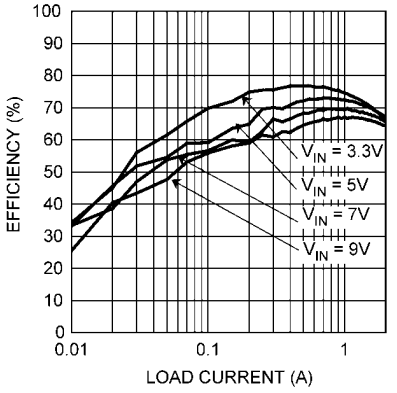
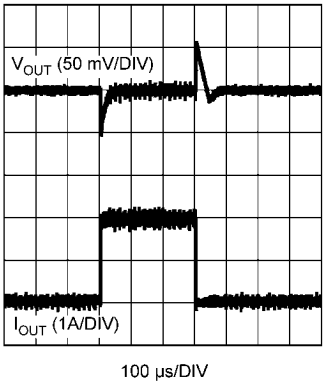


FIGURE 17. V_{IN} = 3.3 - 9V, V_{OUT} = 1.2V, f_{SW} = 2 MHz, I_{OUT} = Full Load



LM27342 Efficiency vs. Load Current

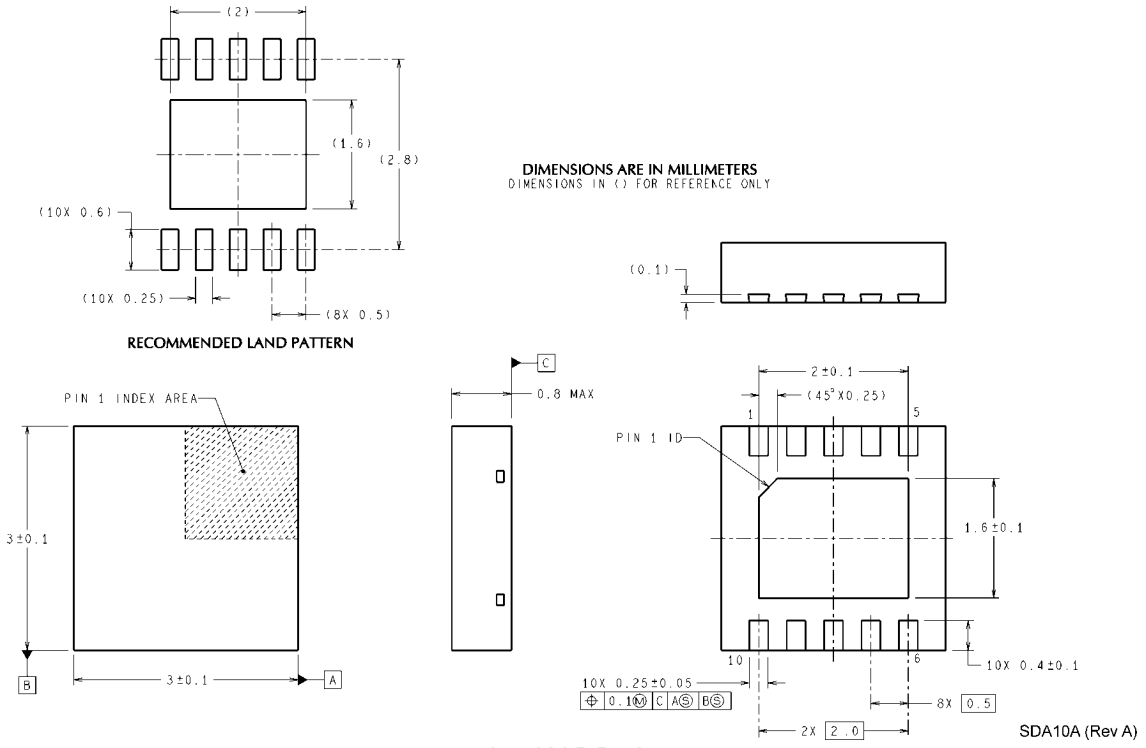


Transient Response
I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs

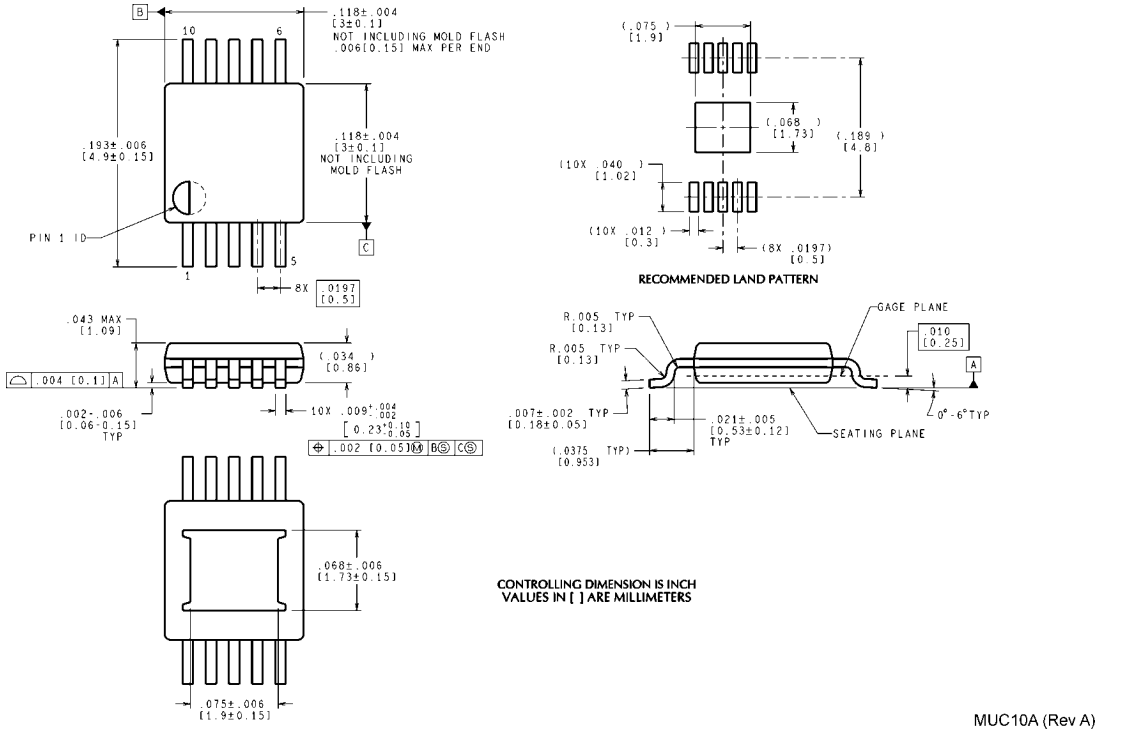
Bill of Materials for *Figure 17*

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LM27341 / LM27342	National Semiconductor
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	NOT MOUNTED		
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	0.56 µH	CDRH2D18/HPNP	Sumida
Feedback Resistor	R1	1.02 kΩ	CRCW06031K02FKEA	Vishay
Feedback Resistor	R2	5.10 kΩ	CRCW06035K10FKEA	Vishay

Physical Dimensions inches (millimeters) unless otherwise noted



10-Lead LLP Package
NS Package Number SDA10A



10-Lead eMSOP Package
NS Package Number MUC10A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265