

8-CHANNEL ANALOGUE MULTIPLEXER/DEMULIPLEXER

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\bar{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\bar{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2 . With $\bar{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2 .

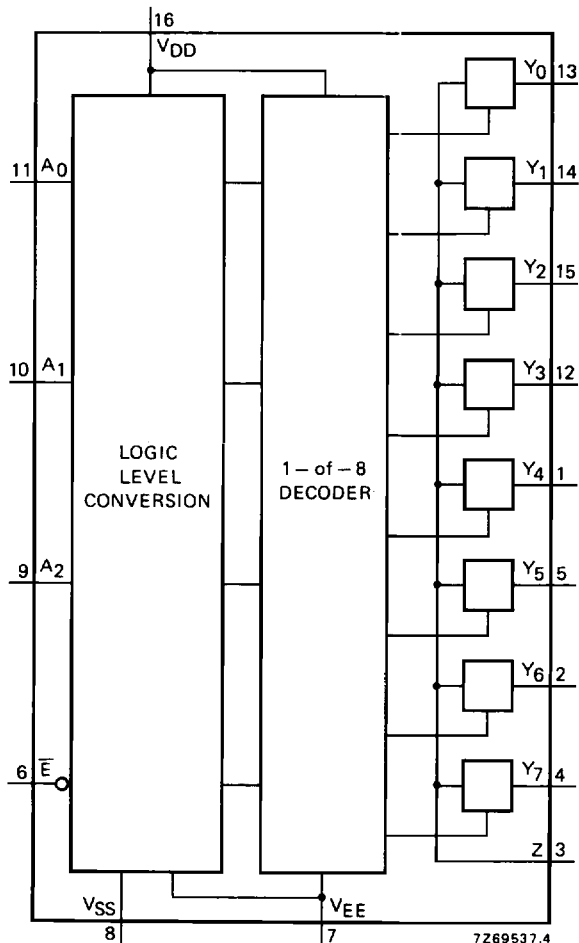
V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2 , and $\bar{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_7 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI
see Family Specifications



HEF4051B

MSI

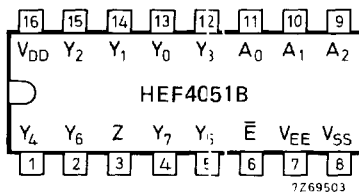


Fig. 2 Pinning diagram.

HEF4051BP(N): 16-lead DIL; plastic (SOT33-1)

HEF4051BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4051BT(D): 16-lead SO; plastic (SOT109-1)

(): Package Designator North America

PINNING

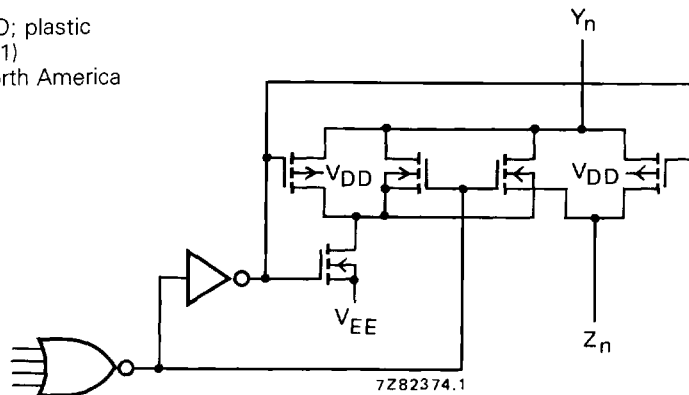
Y_0 to Y_7 independent inputs/outputs

A_0 to A_2 address inputs

$\bar{E}$ enable input (active LOW)

Z common input/output

Fig. 3 Schematic diagram (one switch).



FUNCTION TABLE

$\bar{E}$	inputs			channel ON
	A_2	A_1	A_0	
L	L	L	L	Y_0-Z
L	L	L	H	Y_1-Z
L	L	H	L	Y_2-Z
L	L	H	H	Y_3-Z
L	H	L	L	Y_4-Z
L	H	L	H	Y_5-Z
L	H	H	L	Y_6-Z
L	H	H	H	Y_7-Z
H	X	X	X	none

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD})

V_{EE} -18 to +0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z , when switch current flows into terminals Y , the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z , no V_{DD} current will flow out of terminals Y , in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE} .

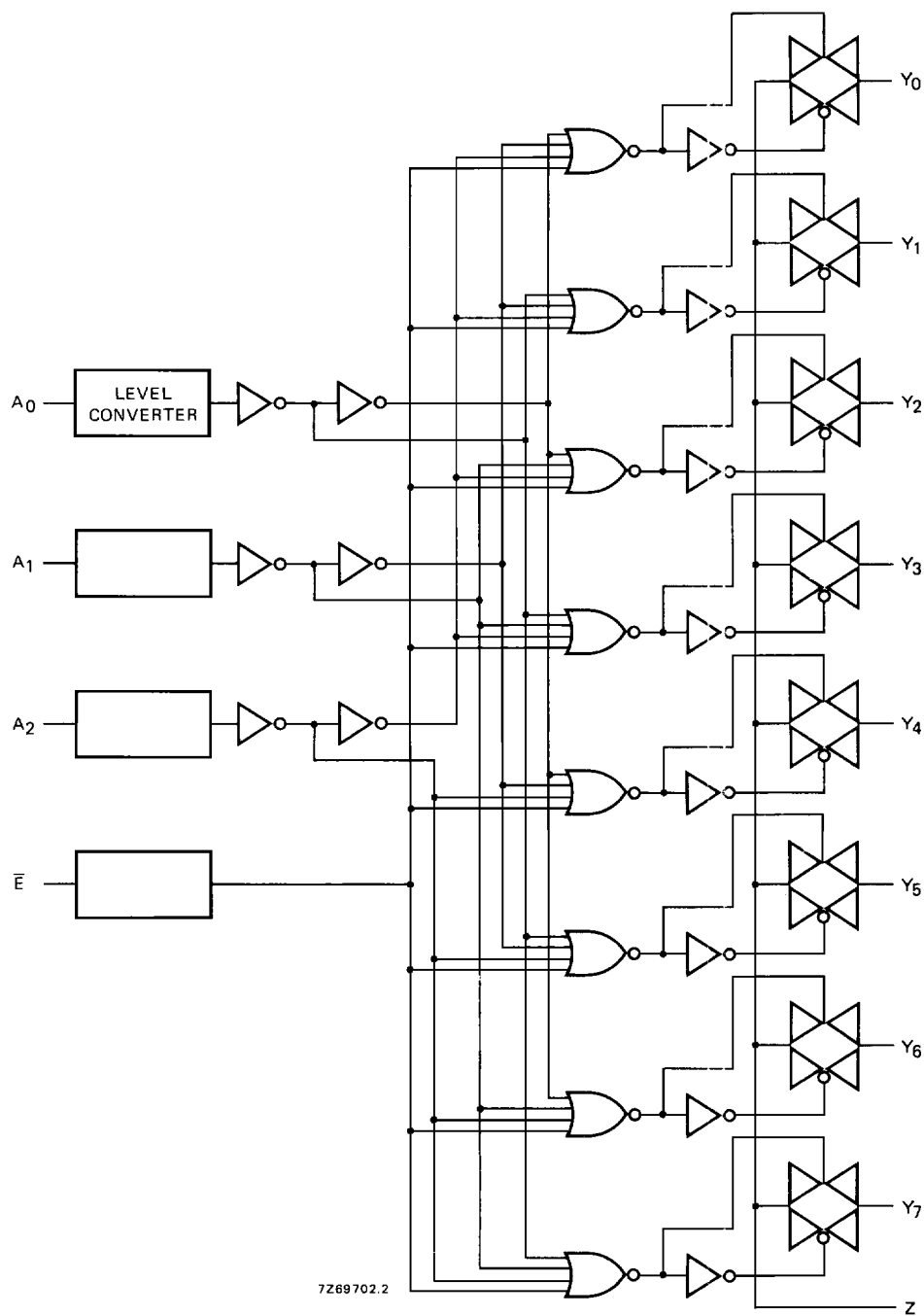


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.	conditions
ON resistance	5	R_{ON}	350	2500 Ω	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245 Ω	
	15		60	175 Ω	
ON resistance	5	R_{ON}	115	340 Ω	$V_{is} = 0$ see Fig. 6
	10		50	160 Ω	
	15		40	115 Ω	
ON resistance	5	R_{ON}	120	365 Ω	$V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200 Ω	
	15		50	155 Ω	
' Δ ' ON resistance between any two channels	5	ΔR_{ON}	25	— Ω	$V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	— Ω	
	15		5	— Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	—	— nA	$\bar{E}$ at V_{DD} $V_{SS} = V_{EE}$
	10		—	— nA	
	15		—	1000 nA	
OFF-state leakage current, any channel	5	I_{OZY}	—	— nA	$\bar{E}$ at V_{SS} $V_{SS} = V_{EE}$
	10		—	— nA	
	15		—	200 nA	

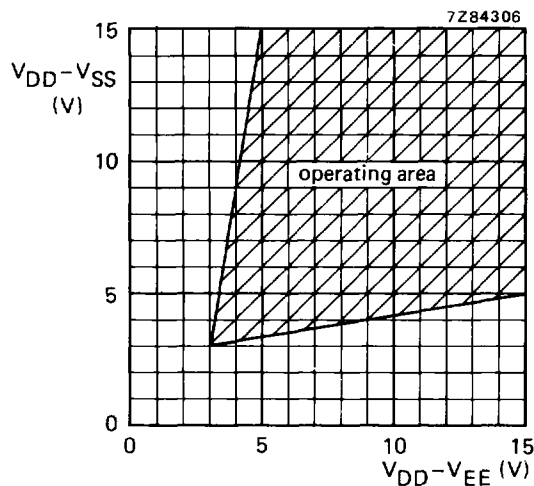
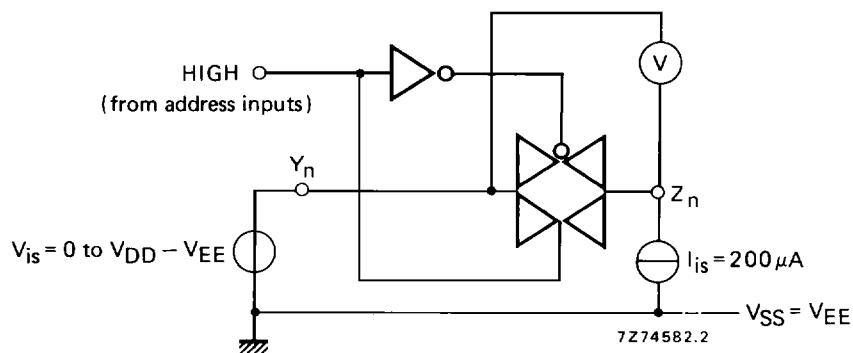
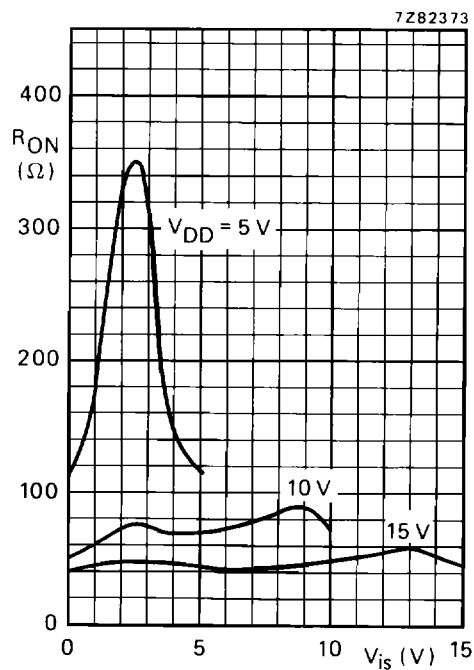


Fig. 5 Operating area as a function of the supply voltages.

Fig. 6 Test set-up for measuring R_{ON} .Fig. 7 Typical R_{ON} as a function of input voltage.

$I_{is} = 200 \mu A$
 $V_{SS} = V_{EE} = 0 V$

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5 10 15	$1\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$ $5\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$ $15\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5 10 15	t_{PHL}	15 5 5	30 10 10	ns note 1
LOW to HIGH	5 10 15	t_{PLH}	15 5 5	30 10 10	ns note 1
$A_n \rightarrow V_{os}$ HIGH to LOW	5 10 15	t_{PHL}	150 60 45	300 120 90	ns note 2
LOW to HIGH	5 10 15	t_{PLH}	150 65 45	300 130 90	ns note 2
Output disable times: $\bar{E} \rightarrow V_{os}$ HIGH	5 10 15	t_{PHZ}	120 90 85	240 180 170	ns note 3
LOW	5 10 15	t_{PLZ}	145 120 115	290 240 230	ns note 3
Output enable times $E \rightarrow V_{os}$ HIGH	5 10 15	t_{PZH}	140 55 40	280 110 80	ns note 3
LOW	5 10 15	t_{PZL}	140 55 40	280 110 80	ns note 3

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5	—		MHz	} note 5
	10	1		MHz	
	15	—		MHz	
Crosstalk; enable or address input to output	5	—		mV	} note 6
	10	50		mV	
	15	—		mV	
OFF-state feed-through	5	—		MHz	} note 7
	10	1		MHz	
	15	—		MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

NOTES

 V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

 V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 10.
- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 15\text{ pF}$ to V_{EE} ; $\bar{E}$ or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 9.

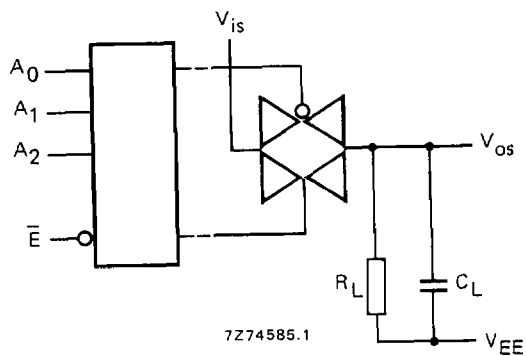


Fig. 8.

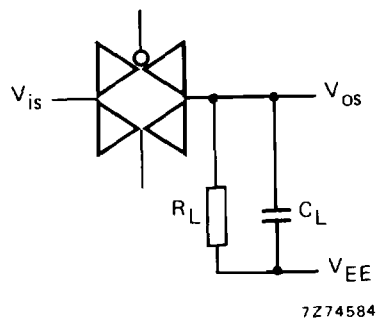


Fig. 9.

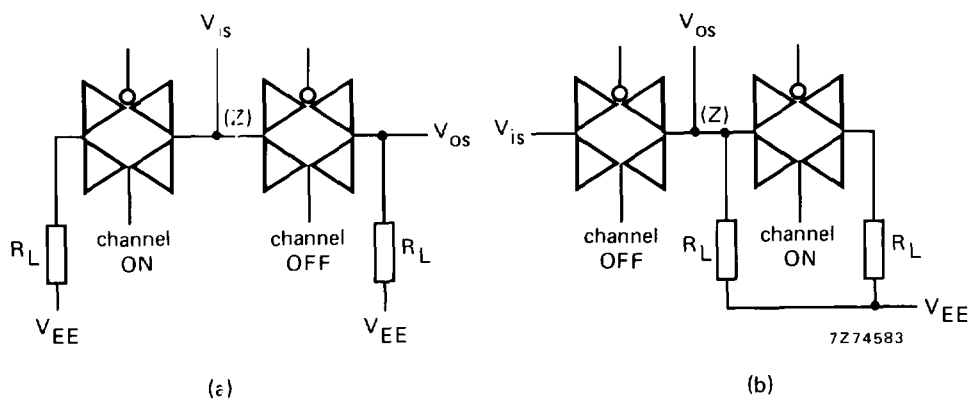


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4051B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.