

FEATURES

1.8 V to 5.5 V operation
Ultralow on resistance
 0.4 Ω typical
 0.6 Ω maximum at 5 V supply
Excellent audio performance, ultralow distortion
 0.07 Ω typical
 0.14 Ω maximum R_{ON} flatness
High current carrying capability
 400 mA continuous
 600 mA peak current at 5 V
Automotive temperature range: -40°C to $+125^{\circ}\text{C}$
Rail-to-rail switching operation
Typical power consumption ($<0.1 \mu\text{W}$)

APPLICATIONS

Cellular phones
 PDAs
 MP3 players
 Power routing
 Battery-powered systems
 PCMCIA cards
 Modems
 Audio and video signal routing
 Communication systems
 Data switching

GENERAL DESCRIPTION

The **ADG888** is a low voltage, dual DPDT (double-pole, double-throw) CMOS device optimized for high performance audio switching. With its low power and small physical size, it is ideal for portable devices.

This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range, making it an ideal solution for applications requiring minimal distortion through the switch. The **ADG888** also has the capability of carrying large amounts of current, typically 400 mA at 5 V operation.

When on, each switch conducts equally well in both directions and has an input signal range that extends to the supplies. The **ADG888** exhibits break-before-make switching action.

FUNCTIONAL BLOCK DIAGRAM

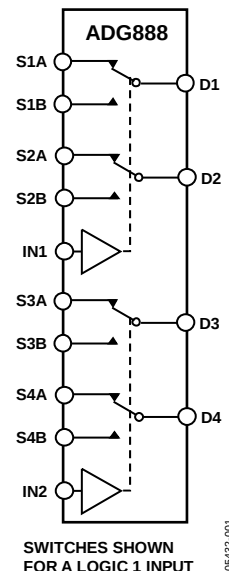


Figure 1.

The **ADG888** is available in a 16-ball WLCSP, 16-lead LFCSP, and a 16-lead TSSOP. These packages make the **ADG888** the ideal solution for space-constrained applications.

PRODUCT HIGHLIGHTS

1. $<0.6 \Omega$ over full temperature range of -40°C to $+125^{\circ}\text{C}$.
2. High current handling capability (400 mA continuous current at 5 V).
3. Low THD + N (0.008% typical).
4. Tiny 16-ball WLCSP, 16-lead LFCSP, and 16-lead TSSOP.

ADG888* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADG888 Evaluation Board

DOCUMENTATION

Data Sheet

- ADG888: 0.4 Ω CMOS, Dual DPDT Switch in WLCSP/LFCSP/TSSOP Data Sheet

User Guides

- UG-429: Evaluation Board for the ADG888 CMOS, Dual DPDT Switch in the WLCSP Package

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

DESIGN RESOURCES

- ADG888 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG888 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

4/16—Rev. A to Rev. B

Changed CB-16 to CB-16-1 and CP-16-4 to CP-16-23	Throughout
Changes to Figure 2 and Table 4.....	6
Moved Figure 4	7
Added Table 5; Renumbered Sequentially	8
Updated Outline Dimensions	13
Changes to Ordering Guide	14

12/06—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Table 2.....	4
Changes to Table 3.....	5
Changes to Ordering Guide	13

7/05—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 4.2 \text{ V}$ to 5.5 V , $GND = 0 \text{ V}$, unless otherwise noted.

Table 1.

Parameter	+25°C	B Version ¹	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	0.4			Ω typ	$V_{DD} = 4.2 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_{DS} = 100 \text{ mA}$
	0.48	0.55	0.6	Ω max	See Figure 16
On Resistance Match Between Channels (ΔR_{ON})	0.04			Ω typ	$V_{DD} = 4.2 \text{ V}$, $V_S = 2.2 \text{ V}$, $I_{DS} = 100 \text{ mA}$
	0.06	0.07	0.075	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.07			Ω typ	$V_{DD} = 4.2 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD}
	0.11	0.13	0.14	Ω max	$I_{DS} = 100 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 5.5 \text{ V}$
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = 1 \text{ V}/4.5 \text{ V}$, $V_D = 4.5 \text{ V}/1 \text{ V}$; see Figure 17
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	22			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	30	33	35	ns max	$V_S = 3 \text{ V}/0 \text{ V}$; see Figure 19
t_{OFF}	13			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	17	18	19	ns max	$V_S = 3 \text{ V}/0 \text{ V}$; see Figure 19
Break-Before-Make Time Delay (t_{BBM})	9			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 3 \text{ V}$; see Figure 20
Charge Injection	70			pC typ	$V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 21
Off Isolation	-67			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 22
Channel-to-Channel Crosstalk	-99			dB typ	Adjacent channel; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 25
	-67			dB typ	Adjacent switch; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 23
Total Harmonic Distortion (THD + N)	0.008			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 3 \text{ V p-p}$
Insertion Loss	-0.03			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 24
-3 dB Bandwidth	29			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 24
C_S (Off)	58			pF typ	
C_D , C_S (On)	110			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 5.5 \text{ V}$
		1	4	μA max	Digital inputs = 0 V or 5.5 V

¹ Temperature range for the Y version is -40°C to $+125^\circ\text{C}$ for the TSSOP and LFCSP; temperature range for the B version is -40°C to $+85^\circ\text{C}$ for the WLCSP.

² Guaranteed by design, not production tested.

$V_{DD} = 2.7\text{ V}$ to 3.6 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	B Version ¹	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
	0.7	0.75	0.8	Ω max	$I_S = 100\text{ mA}$; see Figure 16
On Resistance Match Between Channels (ΔR_{ON})	0.045			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 1\text{ V}$
	0.072	0.077	0.083	Ω max	$I_S = 100\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	0.16			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
			0.262	Ω max	$I_S = 100\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 1\text{ V}/2.6\text{ V}$, $V_D = 2.6\text{ V}/1\text{ V}$; see Figure 17
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = 1\text{ V}$ or 2.6 V ; see Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	28			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$; see Figure 19
	43	47	50	ns max	$V_S = 1.5\text{ V}/0\text{ V}$
t_{OFF}	13			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$; see Figure 19
	20	21	22	ns max	$V_S = 1.5\text{ V}/0\text{ V}$
Break-Before-Make Time Delay (t_{BBM})	14			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 20
Charge Injection	50			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 21
Off Isolation	-67			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 22
Channel-to-Channel Crosstalk	-99			dB typ	Adjacent channel; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
	-67			dB typ	Adjacent switch; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 23
Total Harmonic Distortion (THD + N)	0.01			%	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 1\text{ V p-p}$
Insertion Loss	-0.04			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 24
-3 dB Bandwidth	29			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 24
C_S (Off)	60			pF typ	
C_D , C_S (On)	115			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1	2	μA max	

¹ Temperature range for the Y version is -40°C to $+125^\circ\text{C}$ for the TSSOP and LFCSP; temperature range for the B version is -40°C to $+85^\circ\text{C}$ for the WLCSP.

² Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +6 V
Analog Inputs, Digital Inputs ¹	–0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D 5 V operation	600 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D 5 V operation	400 mA
Operating Temperature Range	
Automotive (Y Version) TSSOP and LFCSP	–40°C to +125°C
Industrial (B version) WLCSP	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance	
16-Lead TSSOP	
θ_{JA} (4-Layer Board)	112°C/W
θ_{JC}	27.6°C/W
16-Lead WLCSP	
θ_{JA} (4-Layer Board)	130°C/W
16-Lead LFCSP	
θ_{JA} (4-Layer Board)	30.4°C/W
Reflow Soldering (RoHS Compliant)	
Peak Temperature	260(+0/–5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

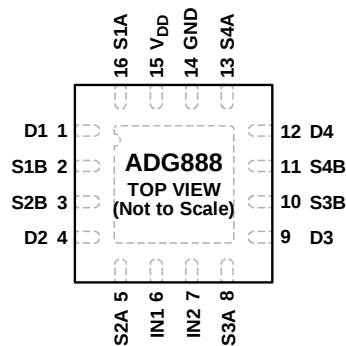
Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 2. 16-Lead LFCSP
Pin Configuration

05432-003

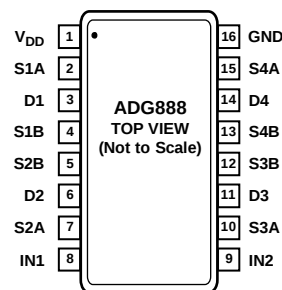


Figure 3. 16-Lead TSSOP
Pin Configuration

05432-004

Table 4. LFCSP and TSSOP Pin Function Descriptions

Pin No.		Mnemonic	Description
LFCSP	TSSOP		
1	3	D1	Drain Terminal 1. Can be an input or output.
2	4	S1B	Source Terminal 1B. Can be an input or output.
3	5	S2B	Source Terminal 2B. Can be an input or output.
4	6	D2	Drain Terminal 2. Can be an input or output.
5	7	S2A	Source Terminal 2A. Can be an input or output.
6	8	IN1	Logic Control Input.
7	9	IN2	Logic Control Input.
8	10	S3A	Source Terminal 3A. Can be an input or output.
9	11	D3	Drain Terminal 3. Can be an input or output.
10	12	S3B	Source Terminal 3B. Can be an input or output.
11	13	S4B	Source Terminal 4B. Can be an input or output.
12	14	D4	Drain Terminal 4. Can be an input or output.
13	15	S4A	Source Terminal 4A. Can be an input or output.
14	16	GND	Ground (0 V) Reference.
15	1	V _{DD}	Most Positive Power Supply Potential.
16	2	S1A	Source Terminal 1A. Can be an input or output.
0	Not applicable	EP	Exposed Pad. The exposed pad must be connected to ground.

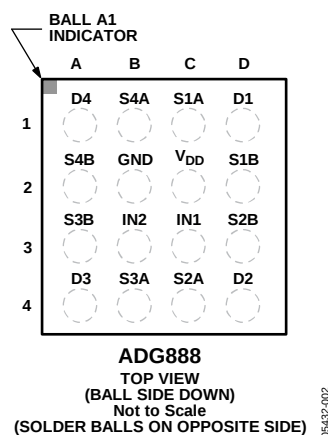


Figure 4. 16-Ball WLCSP Pin Configuration

Table 5. WLCSP Pin Function Descriptions

WLCSP Pin No.	Mnemonic	Description
1A	D4	Drain Terminal 4. Can be an input or output.
1B	S4A	Source Terminal 4A. Can be an input or output.
1C	S1A	Source Terminal 1A. Can be an input or output.
1D	D1	Drain Terminal 1. Can be an input or output.
2A	S4B	Source Terminal 4B. Can be an input or output.
2B	GND	Ground (0 V) Reference.
2C	V _{DD}	Most Positive Power Supply Potential.
2D	S1B	Source Terminal 1B. Can be an input or output.
3A	S3B	Source Terminal 3B. Can be an input or output.
3B	IN2	Logic Control Input.
3C	IN1	Logic Control Input.
3D	S2B	Source Terminal 2B. Can be an input or output.
4A	D3	Drain Terminal 3. Can be an input or output.
4B	S3A	Source Terminal 3A. Can be an input or output.
4C	S2A	Source Terminal 2A. Can be an input or output.
4D	D2	Drain Terminal 2. Can be an input or output.

Table 6. Truth Table

Logic (IN1/IN2)	Switch 1A/2A/3A/4A	Switch 1B/2B/3B/4B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

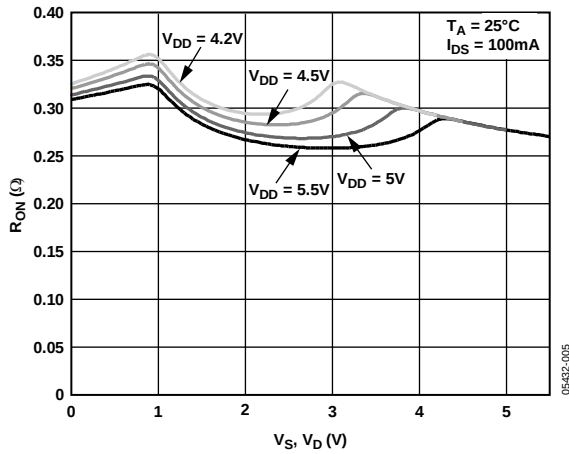


Figure 5. On Resistance vs. V_D (V_S), $V_{DD} = 4.2$ V to 5.5 V

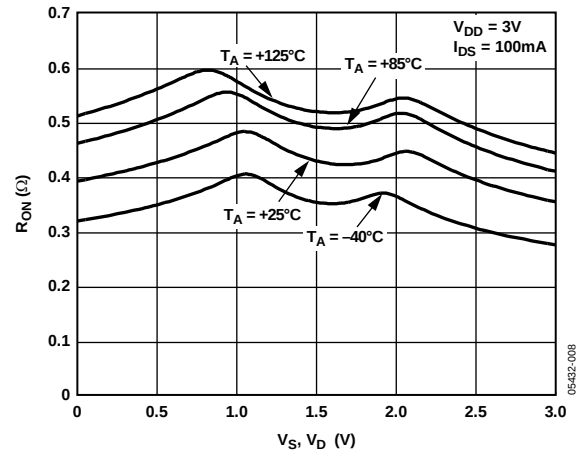


Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3$ V

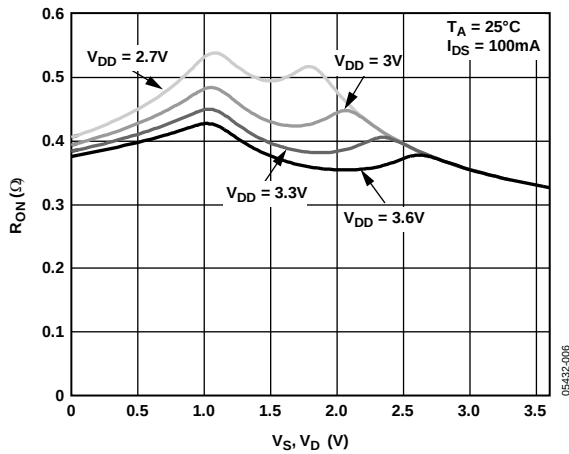


Figure 6. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.6 V

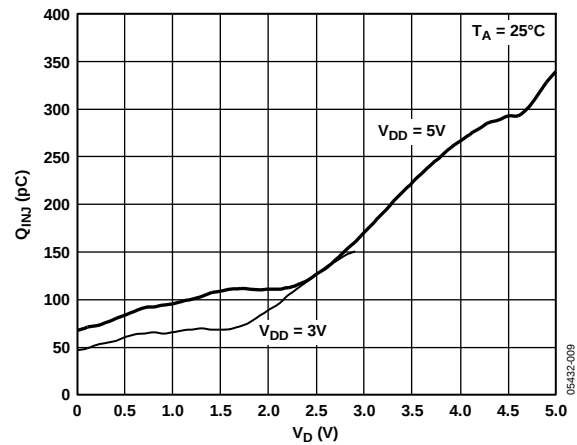


Figure 9. Charge Injection vs. Source Voltage

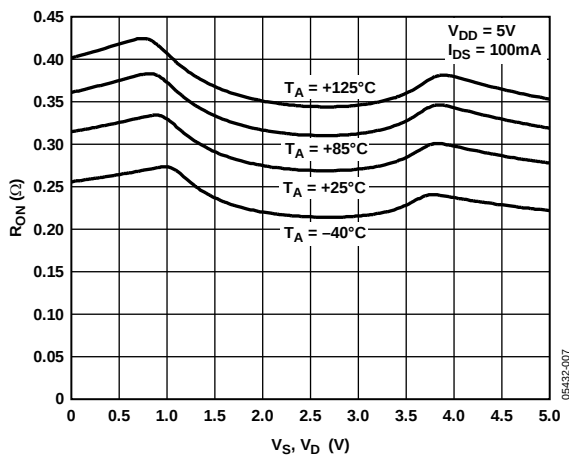


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 5$ V

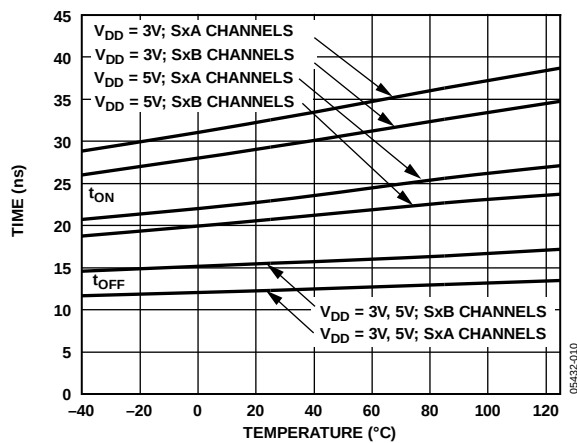


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

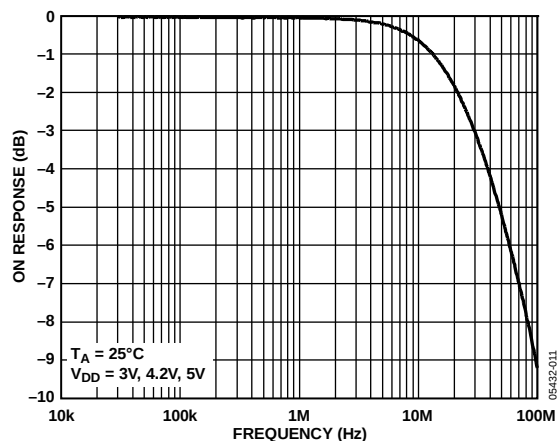


Figure 11. Bandwidth

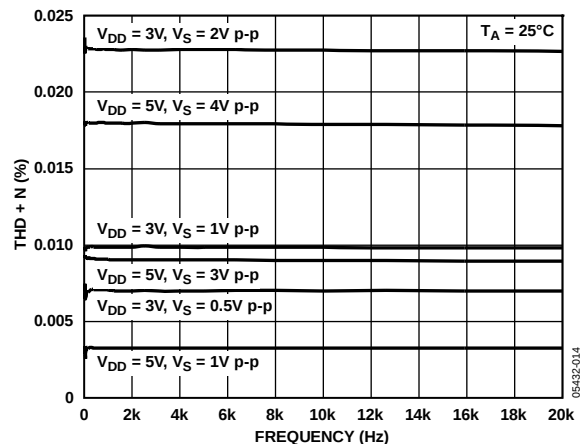


Figure 14. Total Harmonic Distortion + Noise (THD + N)

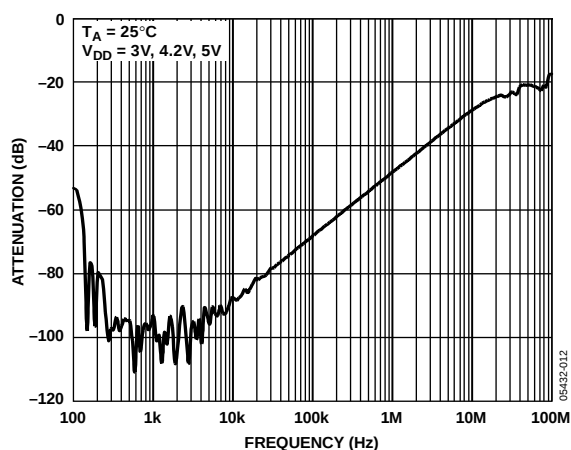


Figure 12. Off Isolation vs. Frequency

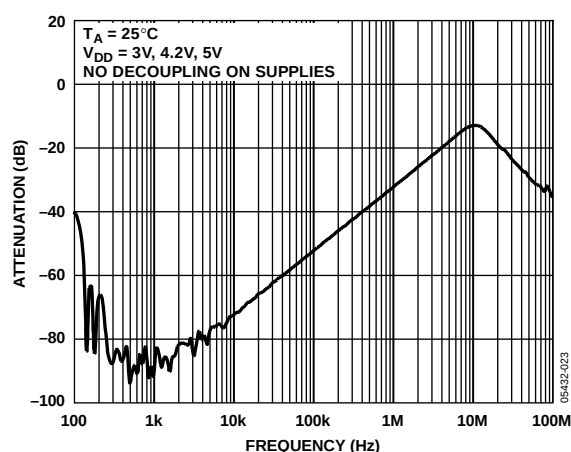


Figure 15. AC PSRR

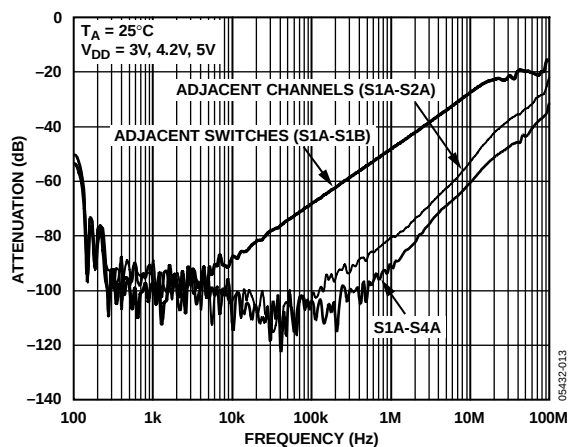


Figure 13. Crosstalk vs. Frequency

TEST CIRCUITS

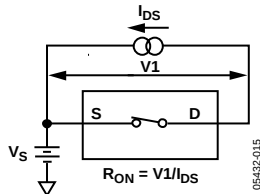


Figure 16. On Resistance

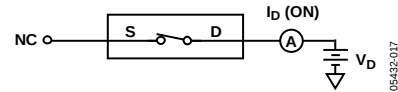


Figure 18. On Leakage

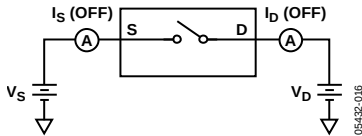


Figure 17. Off Leakage

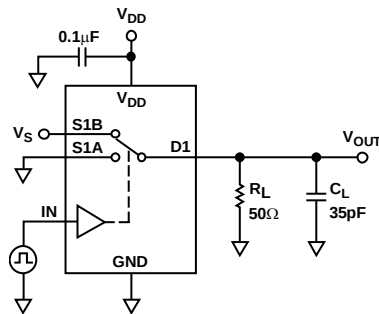
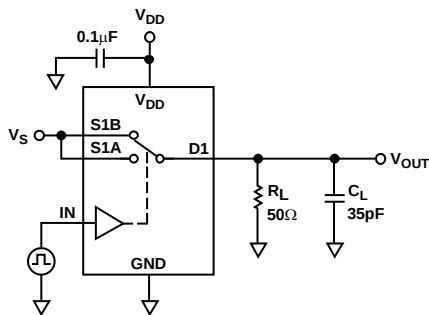
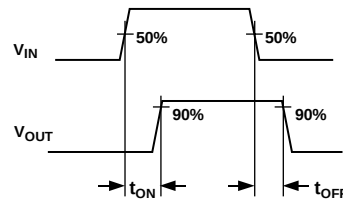
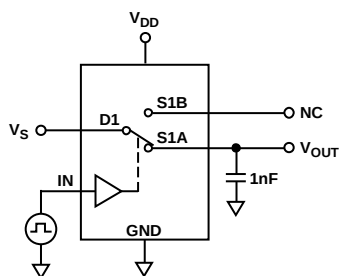
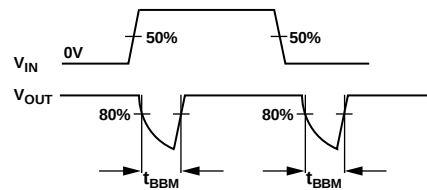
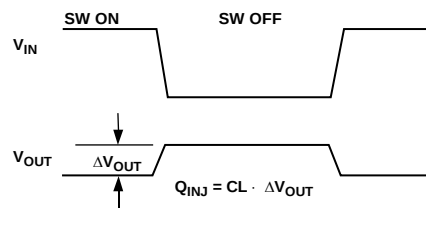
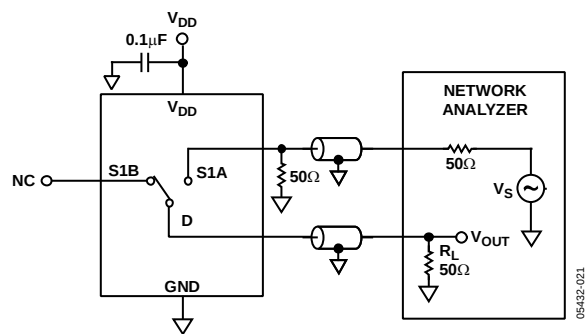
Figure 19. Switching Times, t_{ON} , t_{OFF} Figure 20. Break-Before-Make Time Delay, t_{BBM} 

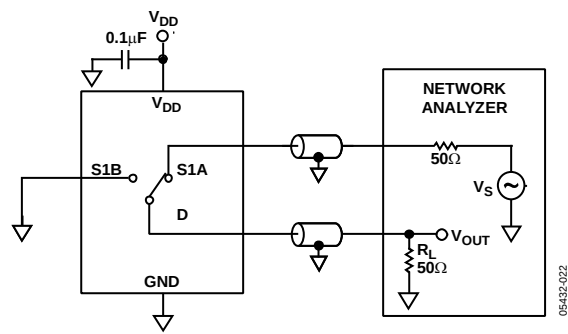
Figure 21. Charge Injection





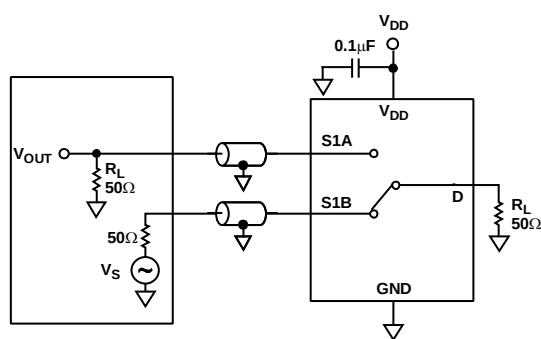
$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 22. Off Isolation



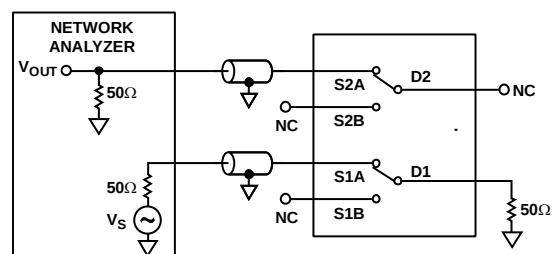
$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 24. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 23. Channel-to-Channel Crosstalk (S1A to S1B)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 25. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (ON)

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}

On resistance match between any two channels.

I_S (OFF)

Source leakage current with the switch off.

I_D , I_S (ON)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (OFF)

Off switch source capacitance. Measured with reference to ground.

C_D , C_S (ON)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. This is specified for two conditions:

- Adjacent channel, that is, S1A to S2A, S1B to S2B, S3A to S4A, or S3B to S4B.
- Adjacent switch, that is, S1A to S1B, S2A to S2B, S3A to S3B, or S4A to S4B.

–3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

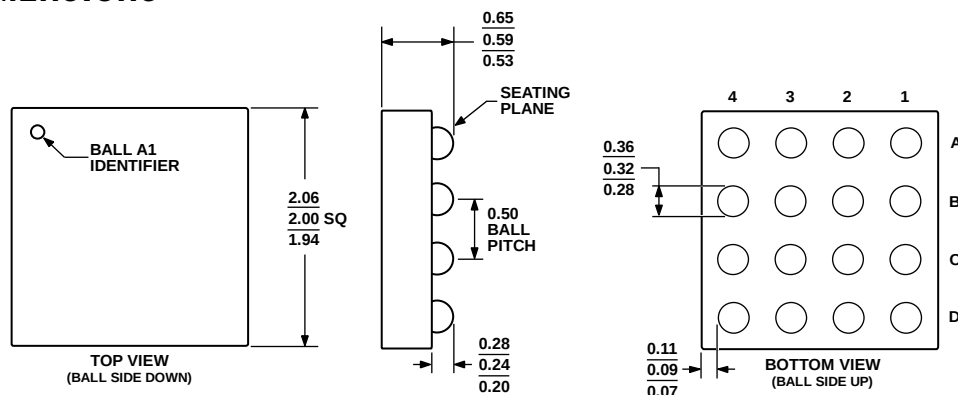
Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitudes plus signal noise to the fundamental.

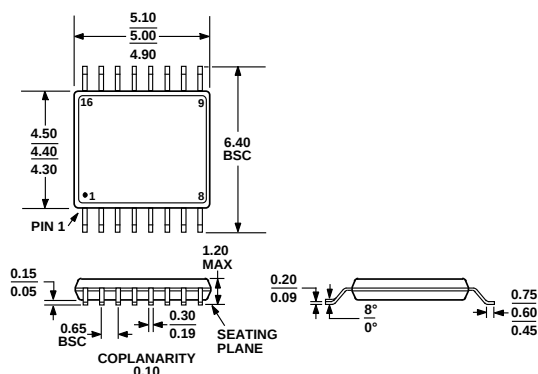
OUTLINE DIMENSIONS



02-03-2012-B

Figure 26. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-1)

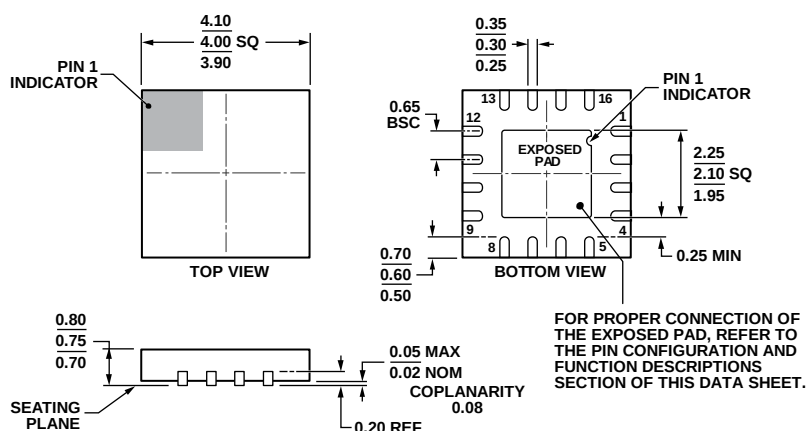
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 27. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 28. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm x 4 mm Body and 0.75 mm Package Height
(CP-16-23)

Dimensions shown in millimeters

111909-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding ²
ADG888YRUZ	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	S0D S02
ADG888YRUZ-REEL	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG888YRUZ-REEL7	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG888YCPZ-REEL7	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23	
ADG888BCBZ-REEL7	–40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-1	

¹ Z = RoHS Compliant Part.

² Branding on these packages is limited to three characters due to space constraints.

NOTES

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Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[EVAL-ADG888EBZ](#) [ADG888YRUZ](#) [ADG888YCPZ-REEL7](#) [ADG888YRUZ-REEL](#) [ADG888YRUZ-REEL7](#)