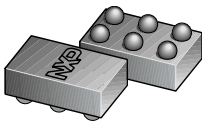


IP3319CX6

Single-channel common-mode filter with integrated ESD protection network

Rev. 2 — 29 May 2013 **Product data sheet**

1. Product profile

1.1 General description

2-lines (one differential channel) common-mode filter with integrated ESD protection up to 15 kV contact discharge, exceeding IEC 61000-4-2, level 4. The device can eliminate efficiently common-mode noise from USB 2.0 and other high-speed interfaces with differential lines. IP3319CX6 attenuates significantly common-mode noise above 800 MHz while differential-mode signal extends out to more than 1 GHz before reaching the −3 dB point.

IP3319CX6 is designed to protect sensitive I/Os, such as USB 2.0, Ethernet, Digital Video Interface (DVI) and Low-Voltage Differential Signaling (LVDS) interfaces from destruction by ElectroStatic Discharge (ESD).

IP3319CX6 is a combination of an integrated copper-coils common-mode filter and a monolithic silicon technology-based ESD protection. It integrates two ultra-low capacitance rail-to-rail diodes plus a separated protection diode in a 0.4 mm pitch Wafer-Level Chip-Size Package (WLCSP). Due to the rail-to-rail concept, the protection is working independently from availability of a supply voltage

1.2 Features and benefits

- 2-lines (one differential mode) common-mode filter
- ESD protection for the USB ID line
- Extremely low clamping voltage
- ESD protection up to ±15 kV on external contact pins
- Ultra low ESD diode capacitance
- WLCSP6 with 0.4 mm pitch

1.3 Applications

- USB 2.0 High-speed lines
- LVDS interfaces
- DVI

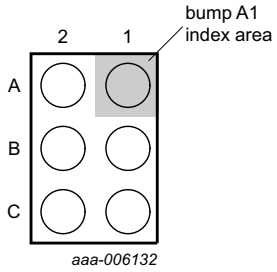
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	single line; input to output		-	6	-	Ω
C_d	diode capacitance	V_I = 0 V; f = 1 MHz; pins A2, B2 to GND	[1]	-	1.5	-	pF

[1] This parameter is guaranteed by design.

2. Pinning information



transparent top view
solder balls facing down

Fig 1. Pin configuration

Table 2. Pinning

Pin	Symbol [1]	Description [1]
A1	D+_OUT	USB data D+ (host side)
A2	D+_IN	USB data D+ (connector side)
B1	D−_OUT	USB data D− (host side)
B2	D−_IN	USB data D− (connector side)
C1	GND	ground
C2	ID	USB identification

[1] D+ and D− are interchangeable.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
IP3319CX6	WLCSP6	wafer level chip-size package; 6 bumps (2 × 3) [1]	IP3319CX6

[1] Size: 1.34 mm × 0.95 mm × 0.57 mm

4. Marking

IP3319CX6 is laser-marked with the following information (see Figure 2):

- A marker indicating the pin A1 position.
- Two lines of characters or numbers:
  - The first line (placeholder <marking code>) indicates the marking code. Mapping of product type number to marking code is given in Table 4.
  - The second line (placeholder <lot ID>) indicates the production lot. This information enables tracking a device down to a particular production date.

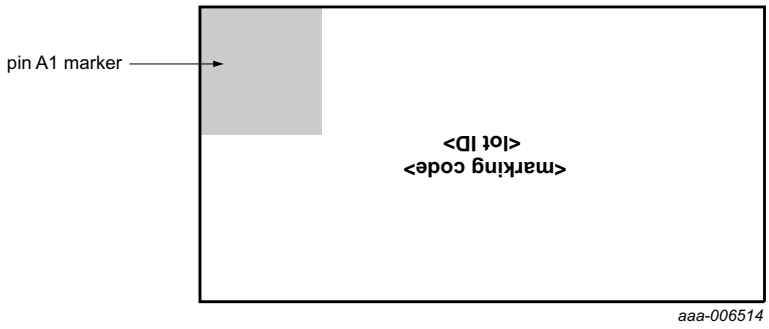
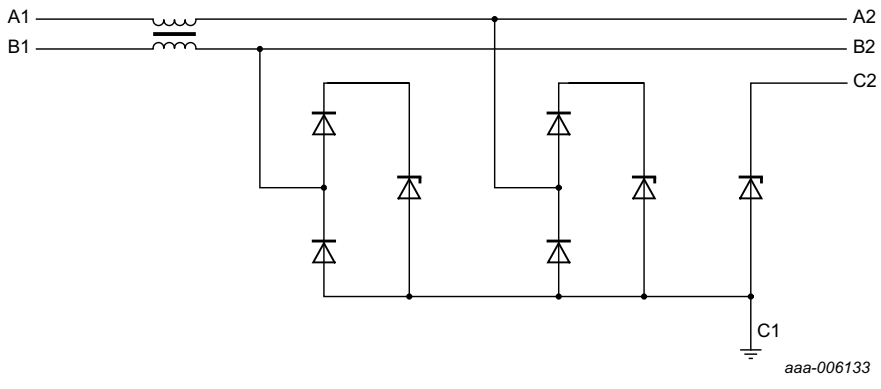


Fig 2. IP3319CX6: outline of the marking

Table 4. Marking codes

Type number	Marking code
IP3319CX6	319

5. Functional diagram



D+ and D- are interchangeable.

Fig 3. Functional diagram

6. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; pins A2, B2, C2 to GND (C1)			
		contact discharge	–15	+15	kV
		air discharge	–15	+15	kV
		IEC 61000-4-2, level 4; pins A1, B1 to GND (C1)			
		contact discharge	–2	+2	kV
		air discharge	–2	+2	kV
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C

7. Characteristics

7.1 Electrical characteristics

Table 6. Electrical characteristics

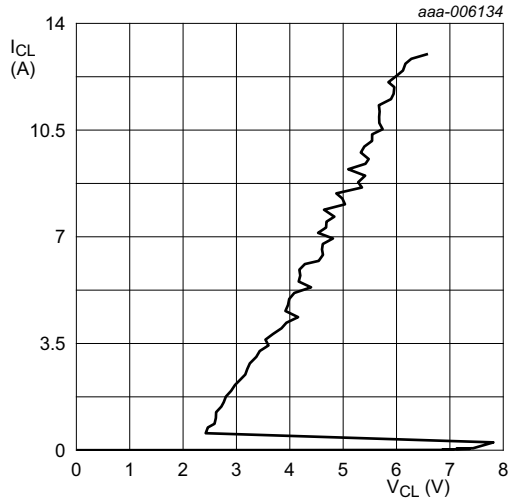
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	single line; input to output		-	6	-	Ω
C_d	diode capacitance	V_I = 0 V; f = 1 MHz; pins A2, B2 to GND	[1]	-	1.5	-	pF
		pin C2 to GND	[1]	-	1.7	-	pF
I_{RM}	reverse leakage current	pins A2, B2, C2 to GND; V_I = 3 V		-	0.01	1	μA
V_{BR}	breakdown voltage	pins A2, B2, C2 to GND; I_R = 10 mA		6	-	10	V
V_F	forward voltage	I_F = 10 mA		-	0.7	-	V
R_{dyn}	dynamic resistance	TLP	[2]				
		positive transient		-	0.25	-	Ω
		negative transient		-	0.20	-	Ω
		surge	[3]				
		positive transient		-	0.20	-	Ω
		negative transient		-	0.14	-	Ω
V_{CL}	clamping voltage	I_{CL} = 6 A	[3]	-	4	-	V
		I_{CL} = –6 A	[3]	-	–2.5	-	V

[1] This parameter is guaranteed by design.

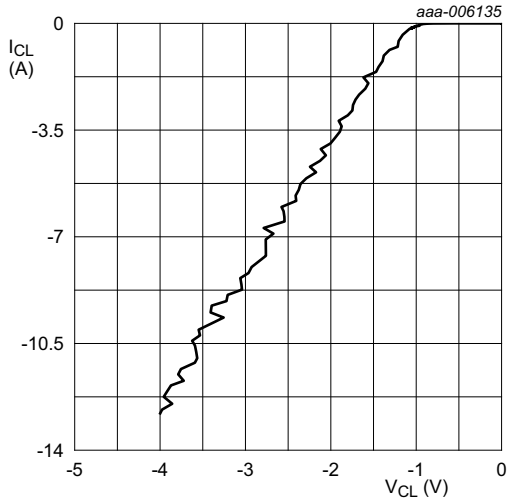
[2] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.

[3] According to IEC 61000-4-5 (8/20 μs).



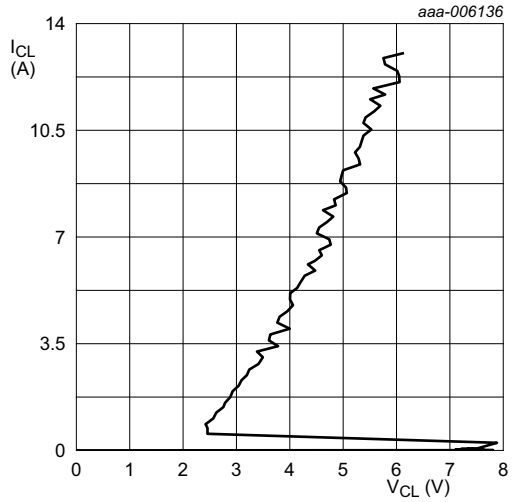
Pin A2; t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 4. Dynamic resistance with positive clamping



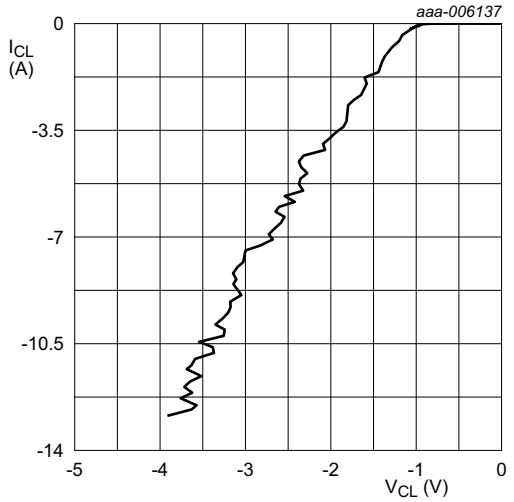
Pin A2; t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 5. Dynamic resistance with negative clamping



Pin C2; t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 6. Dynamic resistance with positive clamping



Pin C2; t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

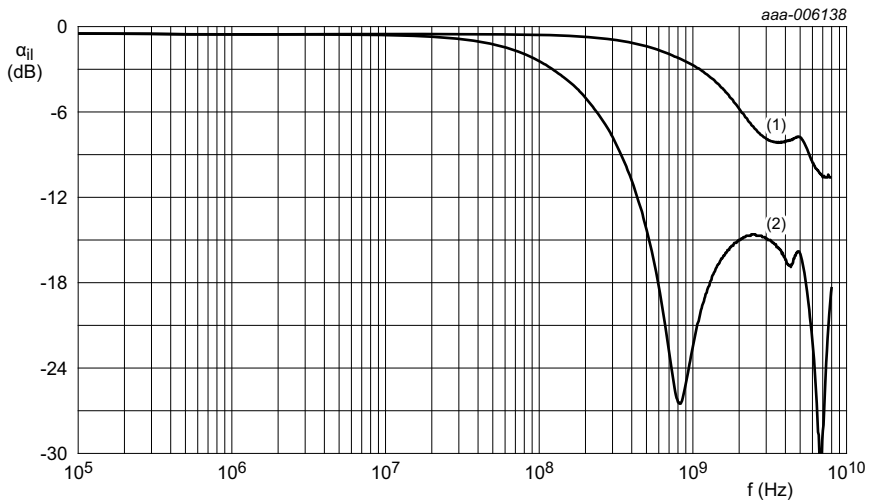
7.2 Frequency characteristics

Table 7. Frequency characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common mode						
α_{il}	insertion loss	S21cc; R_{gen} = 50 Ω; R_L = 50 Ω				
		700 MHz ≤ f ≤ 1.8 GHz	-	-	–13	dB
		f > 1.8 GHz	-	-	–11	dB
Differential mode						
α_{il}	insertion loss	S21dd; R_{gen} = 50 Ω; R_L = 50 Ω				
		f = 500 MHz	–3	-	-	dB
		f = 1 GHz	–5	-	-	dB

Figure 8 shows the common mode and differential mode attenuation measured in a 50 Ω NetWork Analyzer (NWA) system.

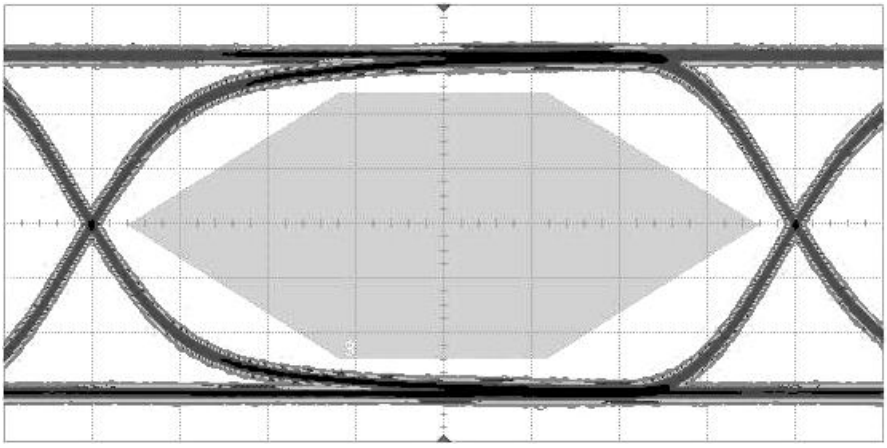
The 3 dB point for the differential-mode signal is above 1 GHz. The common-mode attenuation reaches a typical value of –25 dB in the GSM band.



(1) S21dd: differential mode

(2) S21cc: common mode

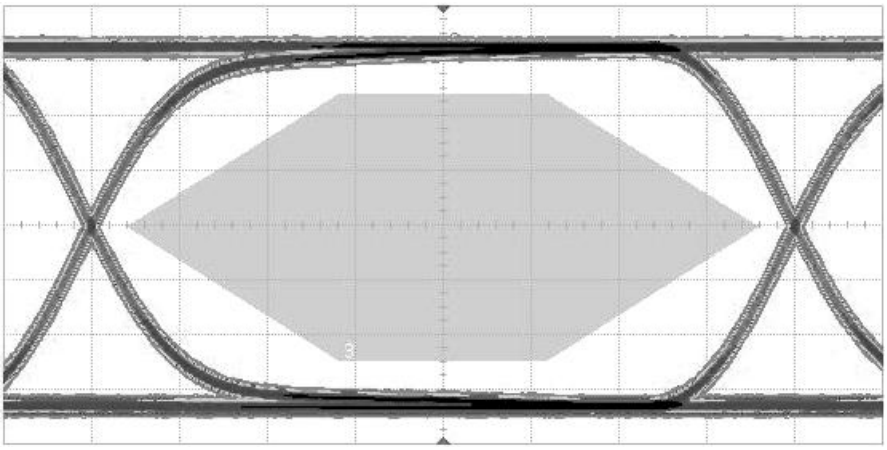
Fig 8. Common-mode and differential-mode insertion loss



aaa-006139

Data rate: 480 Mbit/s (USB 2.0 High-speed)
Vertical scale = 124 mV/div
Horizontal scale = 260 ps/div

Fig 9. USB 2.0 eye diagram Printed-Circuit Board (PCB) with IP3319CX6



aaa-006140

Data rate: 480 Mbit/s (USB 2.0 High-speed)
Vertical scale = 124 mV/div
Horizontal scale = 260 ps/div

Fig 10. USB 2.0 eye diagram PCB without IP3319CX6 (reference)

8. Package outline

WLCSP6: wafer level chip-size package; 6 bumps (2 x 3)

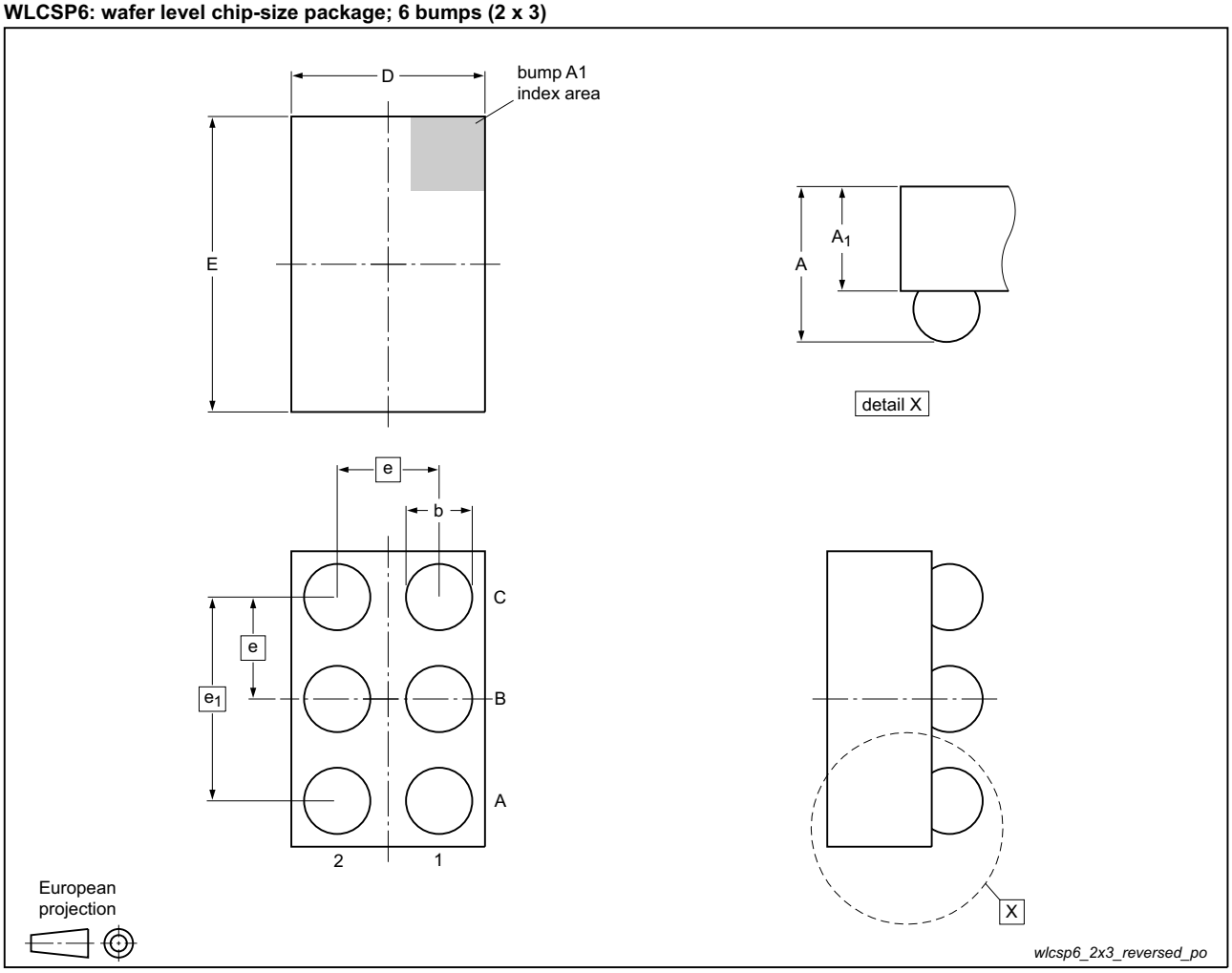


Fig 11. Package outline WLCSP6

Table 8. Package outline dimensions of WLCSP6

Symbol	Min	Typ	Max	Unit
A	0.54	0.57	0.60	mm
A_1	0.36	0.37	0.38	mm
b	0.21	0.26	0.31	mm
D	0.90	0.95	1.00	mm
E	1.29	1.34	1.39	mm
e	0.38	0.40	0.42	mm
e_1	0.76	0.80	0.84	mm

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			4 500
IP3319CX6	WLCSP6	4 mm pitch, 8 mm tape and reel	-135

[1] For further information and the availability of packing methods, see Section 14.

10. Soldering

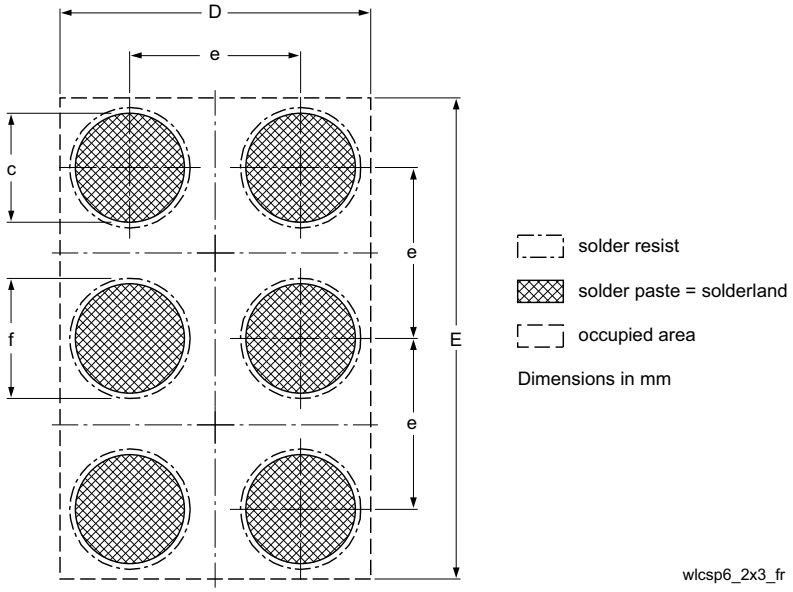


Fig 12. Reflow soldering footprint WLCSP6

Table 10. Reflow soldering dimensions of WLCSP6

Symbol	Min	Typ	Max	Unit
c	-	0.25	-	mm
D	0.91	0.96	1.01	mm
E	1.31	1.36	1.41	mm
e	-	0.40	-	mm
f	-	0.325	-	mm

11. Design and assembly recommendations

11.1 PCB design guidelines

For optimum performance, use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 11 for the recommended Printed-Circuit Board (PCB) design parameters.

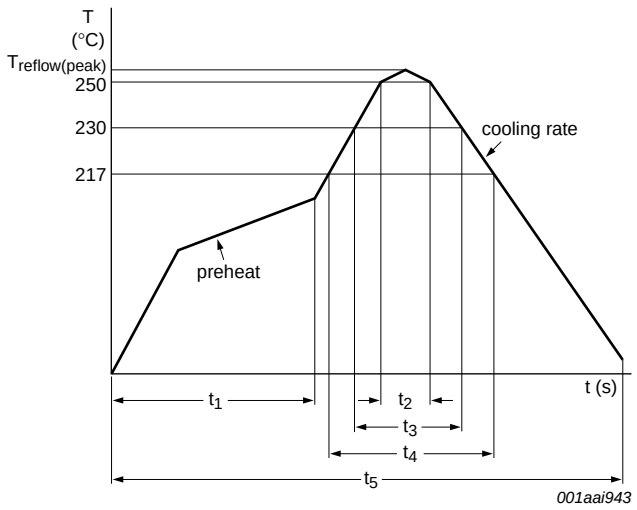
Table 11. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

11.2 PCB assembly guidelines for Pb-free soldering

Table 12. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	290 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 13



The device can withstand at least three reflows of this profile.

Fig 13. Pb-free solder reflow profile

Table 13. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

12. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3319CX6 v.2	20130529	Product data sheet	-	IP3319CX6 v.1
Modifications:	• Section 1.1 “General description”: corrected • Table 5: V_I and V_{ESD} updated • Table 6: $R_{s(ch)}$, C_d and V_{BR} updated • Section 13 “Legal information”: updated			
IP3319CX6 v.1	20130130	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

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