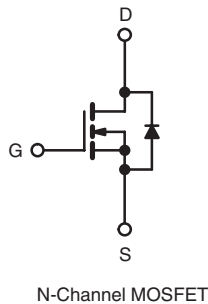
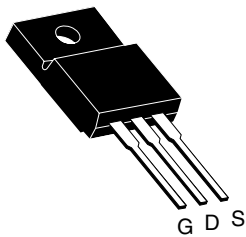


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.52
Q_g (Max.) (nC)	52	
Q_{gs} (nC)	13	
Q_{gd} (nC)	18	
Configuration	Single	

TO-220 FULLPAK



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Compliant to RoHS directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5 kV_{RMS} ($t = 60$ s, $f = 60$ Hz)

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half and Full Bridge Convertors
- Power Factor Correction Boost

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB7N50APbF
	SiHFIB7N50A-E3
SnPb	IRFIB7N50A
	SiHFIB7N50A

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ^f	I_D	$T_C = 25$ °C	A
Continuous Drain Current		$T_C = 100$ °C	
Pulsed Drain Current ^{a, e}	I_{DM}	44	
Linear Derating Factor		0.48	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	275	mJ
Repetitive Avalanche Current ^{a, e}	I_{AR}	11	A
Repetitive Avalanche Energy ^a	E_{AR}	6.0	mJ
Maximum Power Dissipation	P_D	60	W
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	6.9	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 4.5$ mH, $R_G = 25$ Ω , $I_{AS} = 11$ A (see fig. 12).
- $I_{SD} \leq 11$ A, $dI/dt \leq 140$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- Uses IRFB11N50A, SiHFB11N50A data and test conditions.
- Drain current limited by maximum junction temperature.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.1	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	610	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.0 A ^b	-	-	0.52	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 6.6 A ^d		6.1	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d		-	1423	-	pF
Output Capacitance	C _{oss}			-	208	-	
Reverse Transfer Capacitance	C _{rss}			-	8.1	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	2000	-	nC
Effective Output Capacitance	C _{oss eff.}		V _{DS} = 400 V, f = 1.0 MHz	-	55	-	
			V _{DS} = 0 V to 400 V ^{c, d}	-	97	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 11 A, V _{DS} = 400 V see fig. 6 and 13 ^{b, d}	-	-	52	nC
Gate-Source Charge	Q _{gs}			-	-	13	
Gate-Drain Charge	Q _{gd}			-	-	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 11 A R _G = 9.1 Ω, R _D = 22 Ω, see fig. 10 ^{b, d}		-	14	-	ns
Rise Time	t _r			-	35	-	
Turn-Off Delay Time	t _{d(off)}			-	32	-	
Fall Time	t _f			-	28	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.6	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	44	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 11 A, dI/dt = 100 A/μs ^{b, d}		-	510	770	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.4	5.1	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- Uses IRFB11N50A, SiHFB11N50A data and test conditions.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

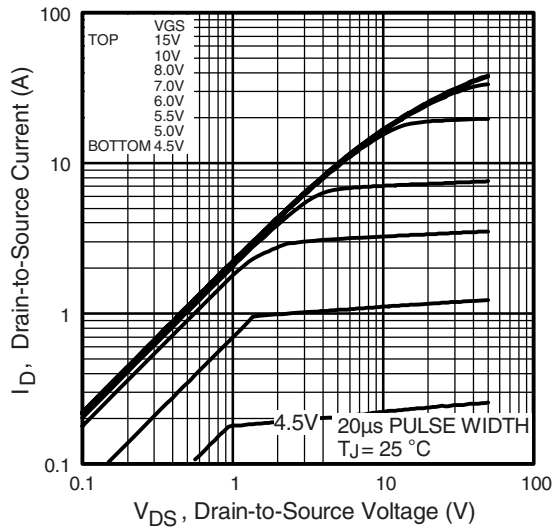


Fig. 1 - Typical Output Characteristics

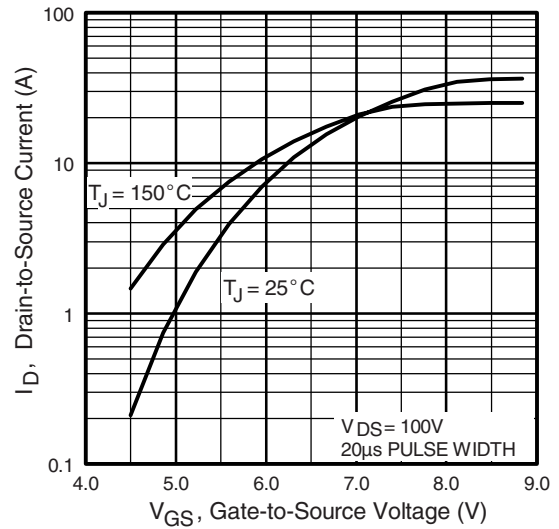


Fig. 3 - Typical Transfer Characteristics

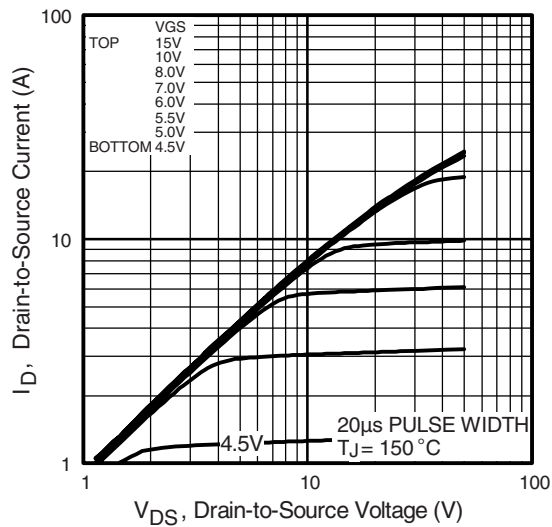


Fig. 2 - Typical Output Characteristics

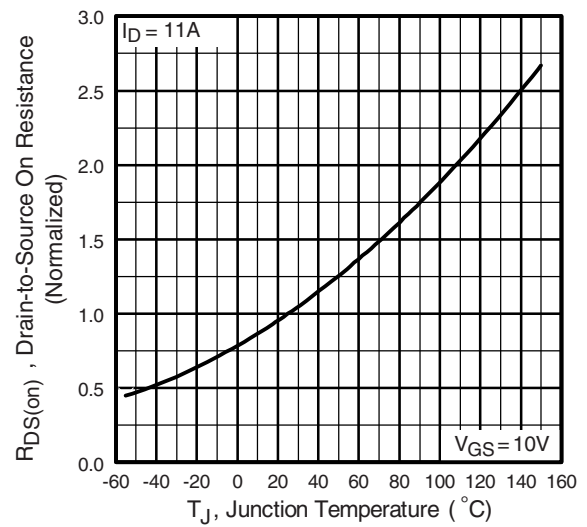


Fig. 4 - Normalized On-Resistance vs. Temperature

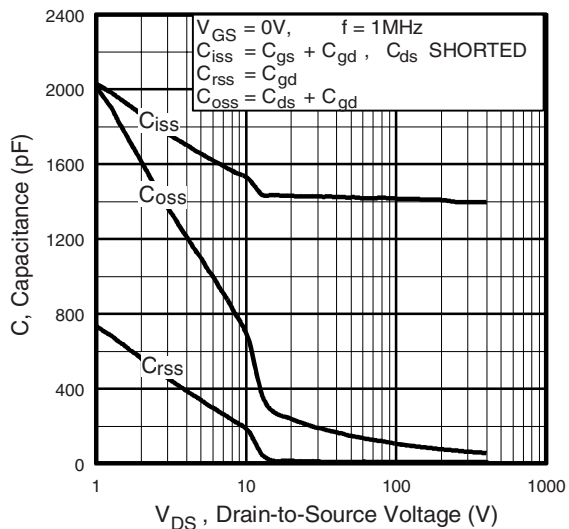


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

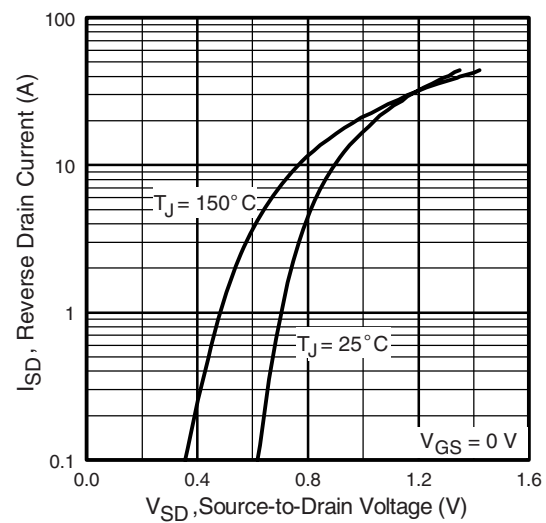


Fig. 7 - Typical Source-Drain Diode Forward Voltage

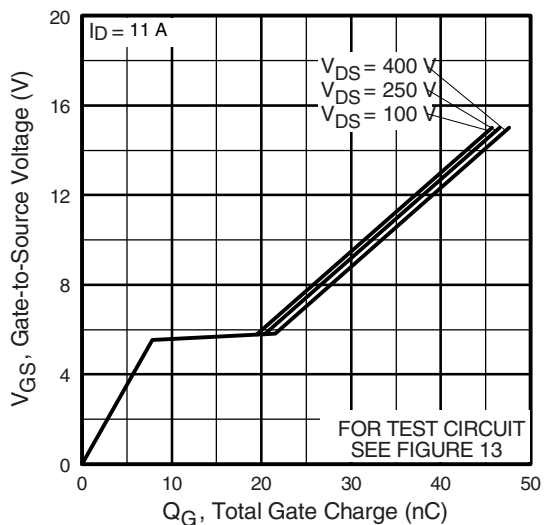


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

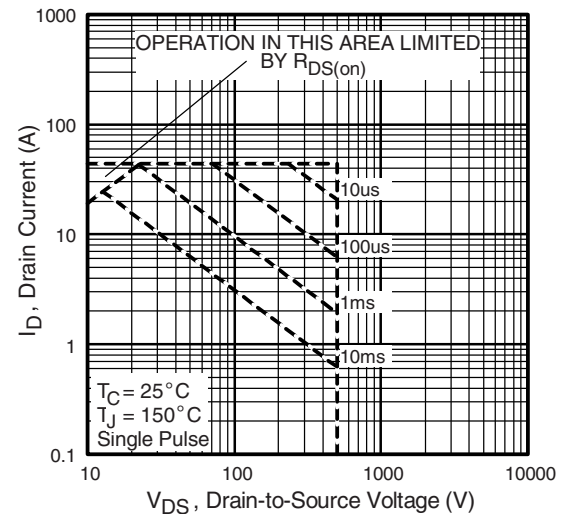


Fig. 8 - Maximum Safe Operating Area

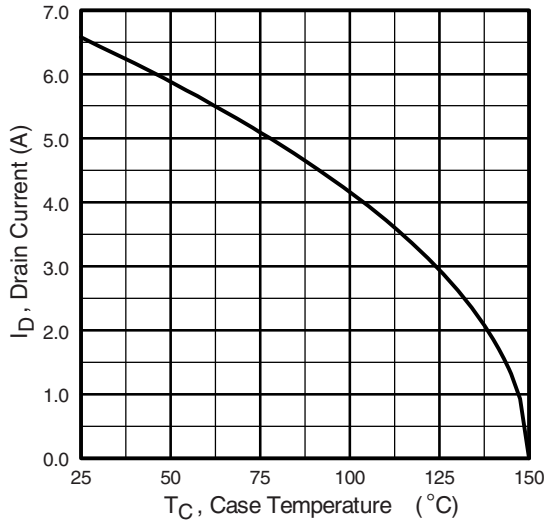


Fig. 9 - Maximum Drain Current vs. Case Temperature

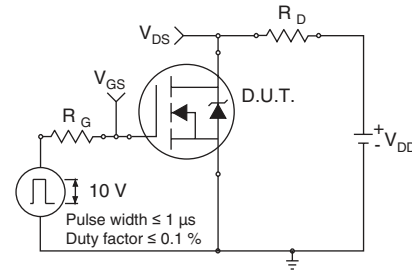


Fig. 10a - Switching Time Test Circuit

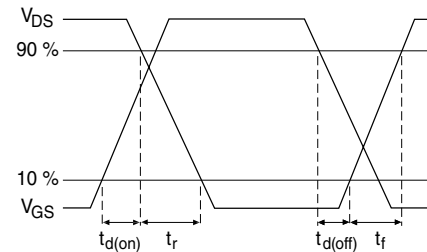


Fig. 10b - Switching Time Waveforms

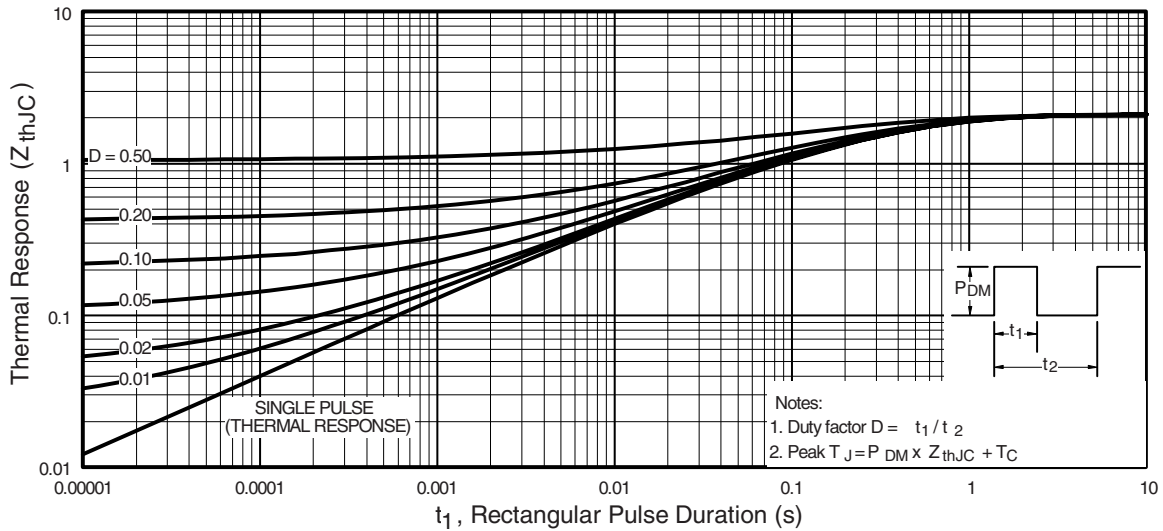


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

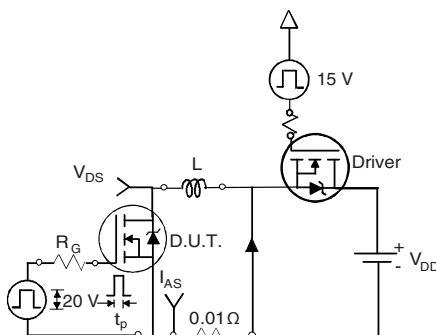


Fig. 12a - Unclamped Inductive Test Circuit

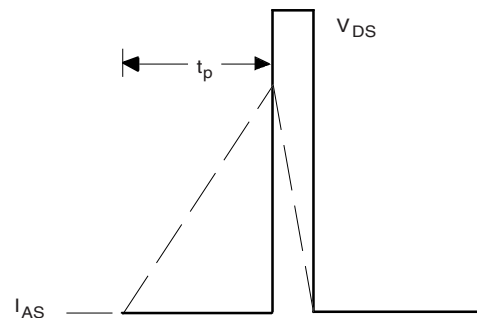


Fig. 12b - Unclamped Inductive Waveforms

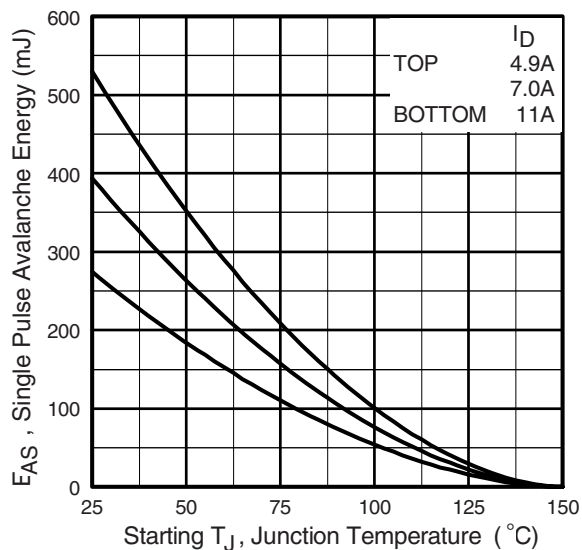


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

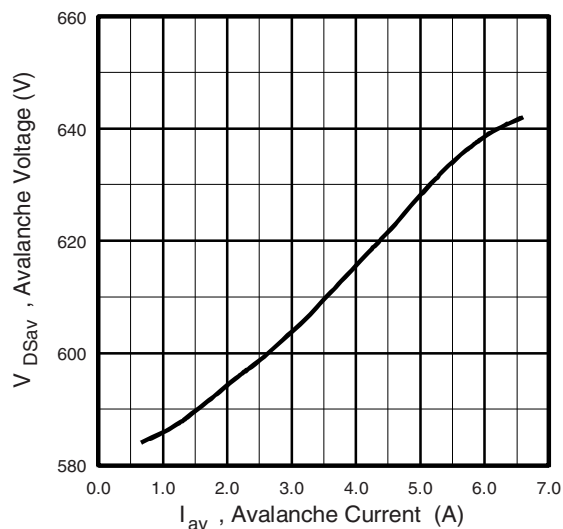


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

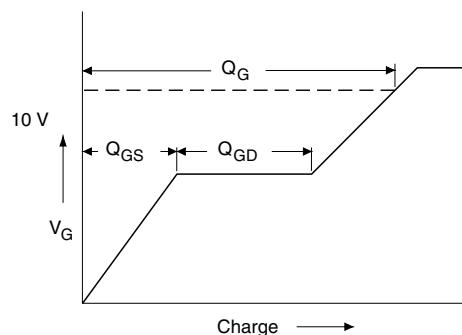


Fig. 13a - Basic Gate Charge Waveform

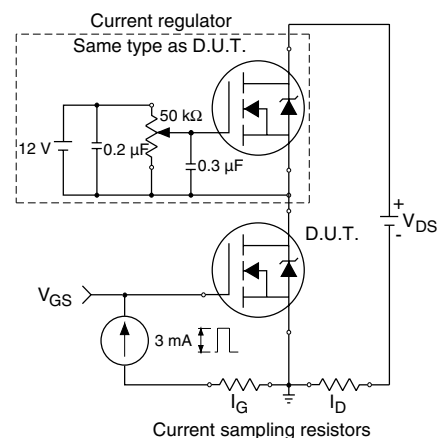
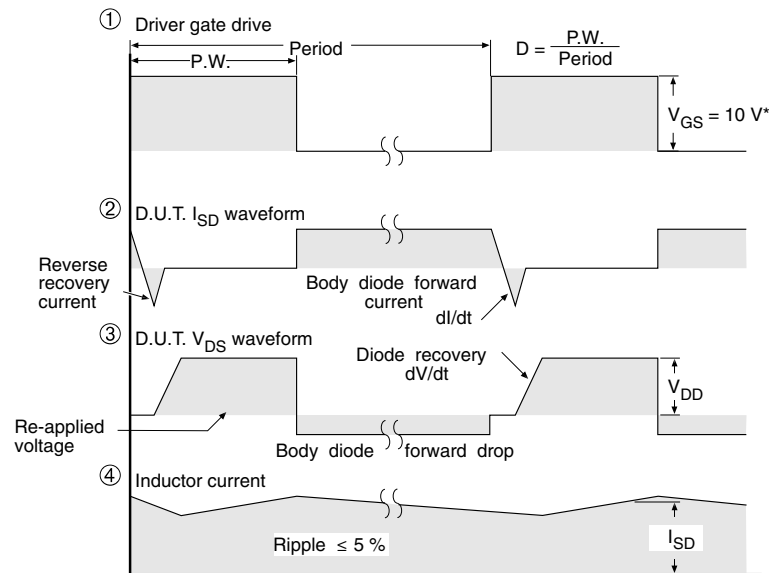
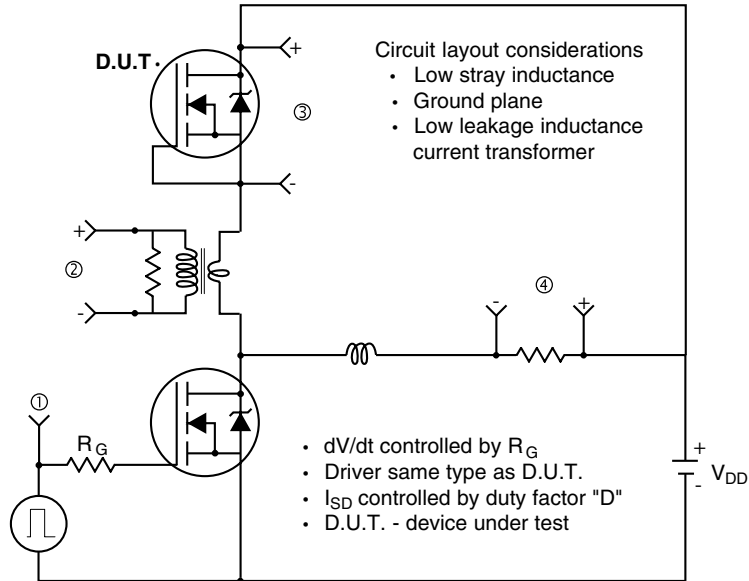


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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