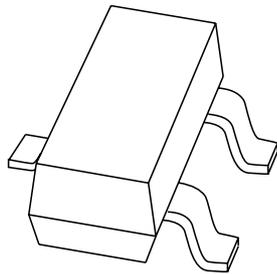


DATA SHEET



PBSS5240T

40 V, 2 A

PNP low V_{CEsat} (BISS) transistor

Product specification
Supersedes data of 2001 Oct 31

2004 Jan 15

40 V, 2 A
PNP low V_{CEsat} (BISS) transistor

PBSS5240T

FEATURES

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation
- Replacement for SOT89/SOT223 standard packaged transistor.

APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

DESCRIPTION

PNP low V_{CEsat} transistor in a SOT23 plastic package.
 NPN complement: PBSS4240T.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS5240T	ZF*

Note

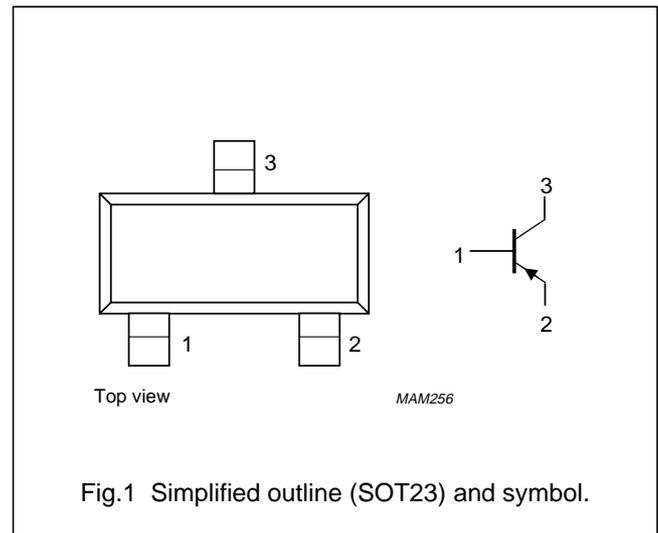
- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-40	V
I_C	collector current (DC)	-2	A
I_{CM}	peak collector current	-3	A
R_{CEsat}	equivalent on-resistance	<220	mΩ

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5240T	-	plastic surface mounted package; 3 leads	SOT23

40 V, 2 A
PNP low V_{CEsat} (BISS) transistor

PBSS5240T

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–40	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–2	A
I_{CM}	peak collector current		–	–3	A
I_{BM}	peak base current		–	–300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	300	mW
		$T_{amb} \leq 25\text{ °C}$; note 2	–	480	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tin plated, mounting pad for collector 1 cm².

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	417	K/W
		in free air; note 2	260	K/W

Notes

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tin plated, mounting pad for collector 1 cm².

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PBSS5240T

CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

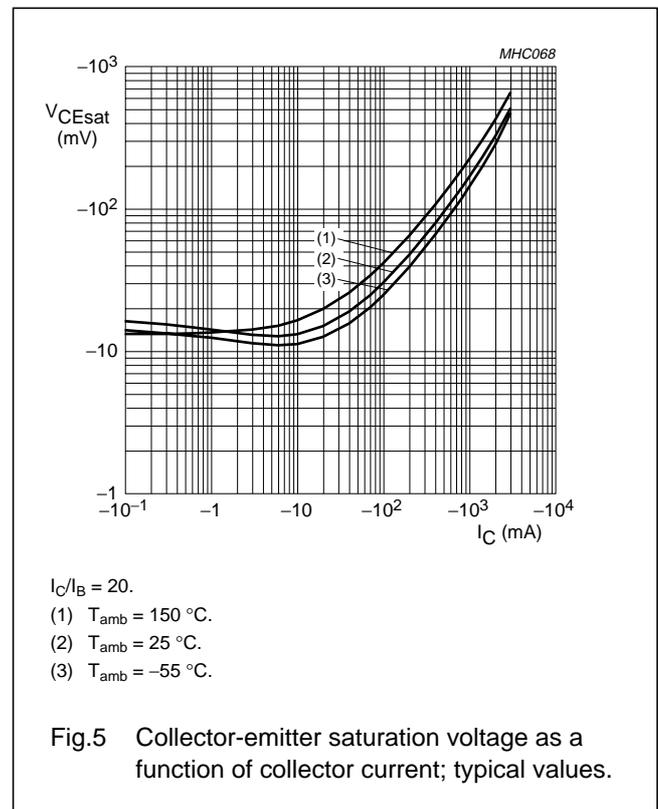
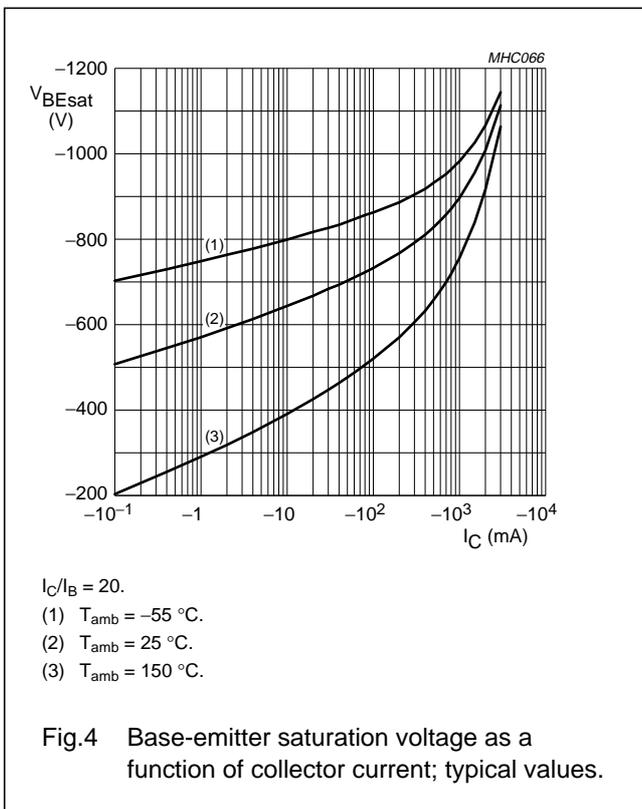
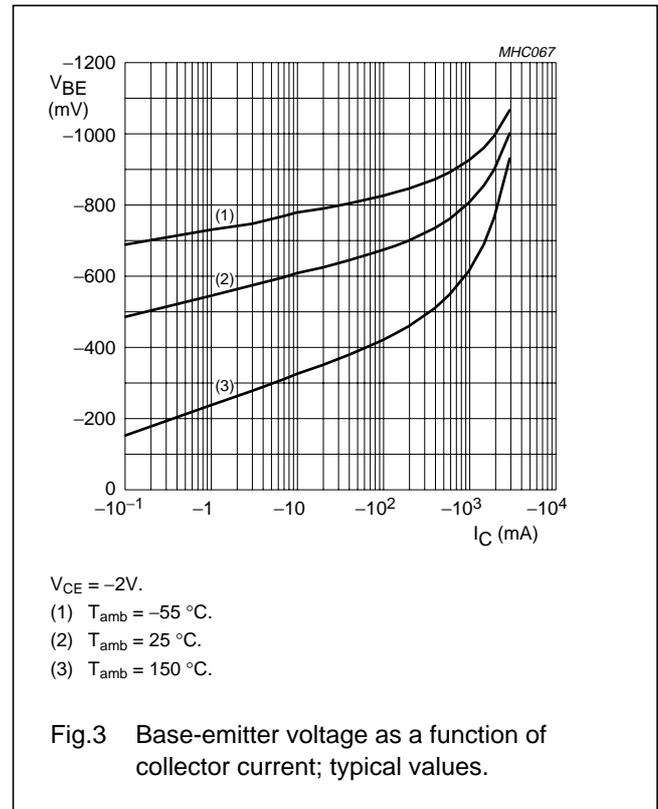
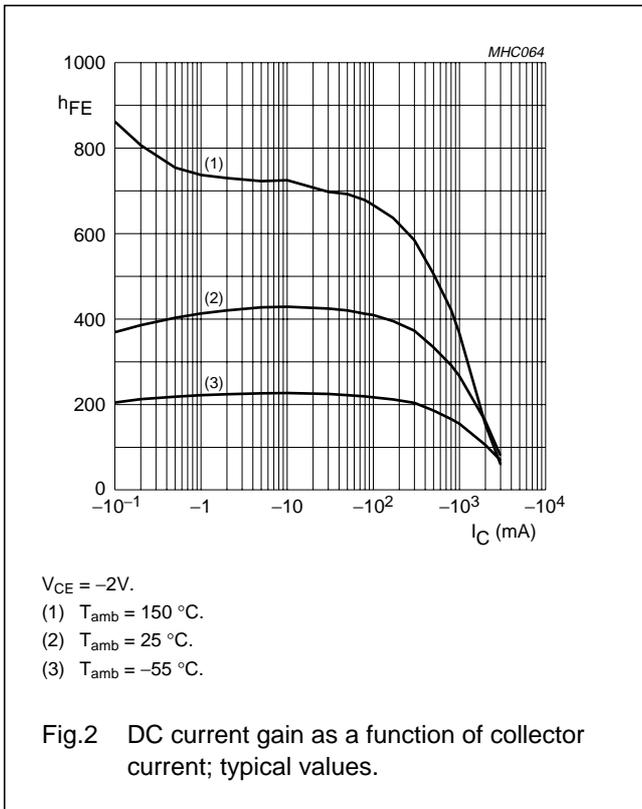
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	μA
I_{BEO}	emitter-base cut-off current	$V_{EB} = -4\text{ V}; I_C = 0$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}$ $I_C = -100\text{ mA}$ $I_C = -500\text{ mA}$ $I_C = -1\text{ A}$ $I_C = -2\text{ A}$	300 260 210 100	450 350 290 180	– – – –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	–55	–100	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–70	–110	mV
		$I_C = -750\text{ mA}; I_B = -15\text{ mA}$	–	–140	–225	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–140	–225	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–240	–350	mV
R_{CEsat}	equivalent on-resistance	$I_C = -500\text{ mA}; I_B = -50\text{ mA};$ note 1	–	160	<220	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–	–1.1	V
$V_{BE(on)}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	–	–	–0.75	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	100	200	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0;$ $f = 1\text{ MHz}$	–	23	28	pF

Note

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.

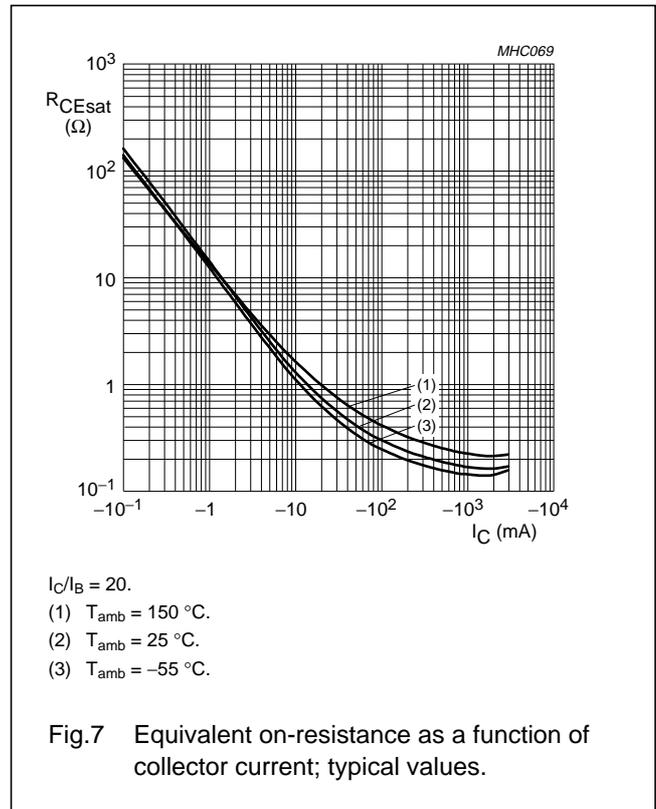
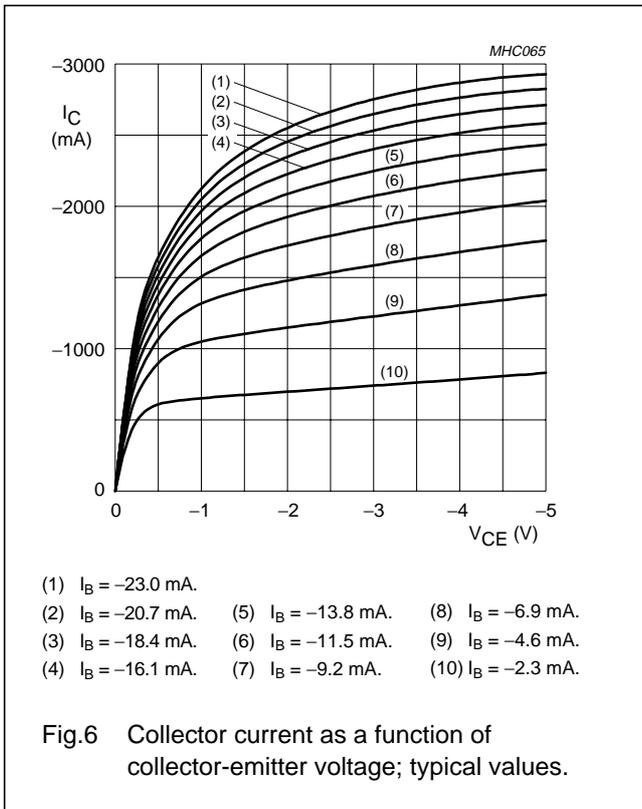
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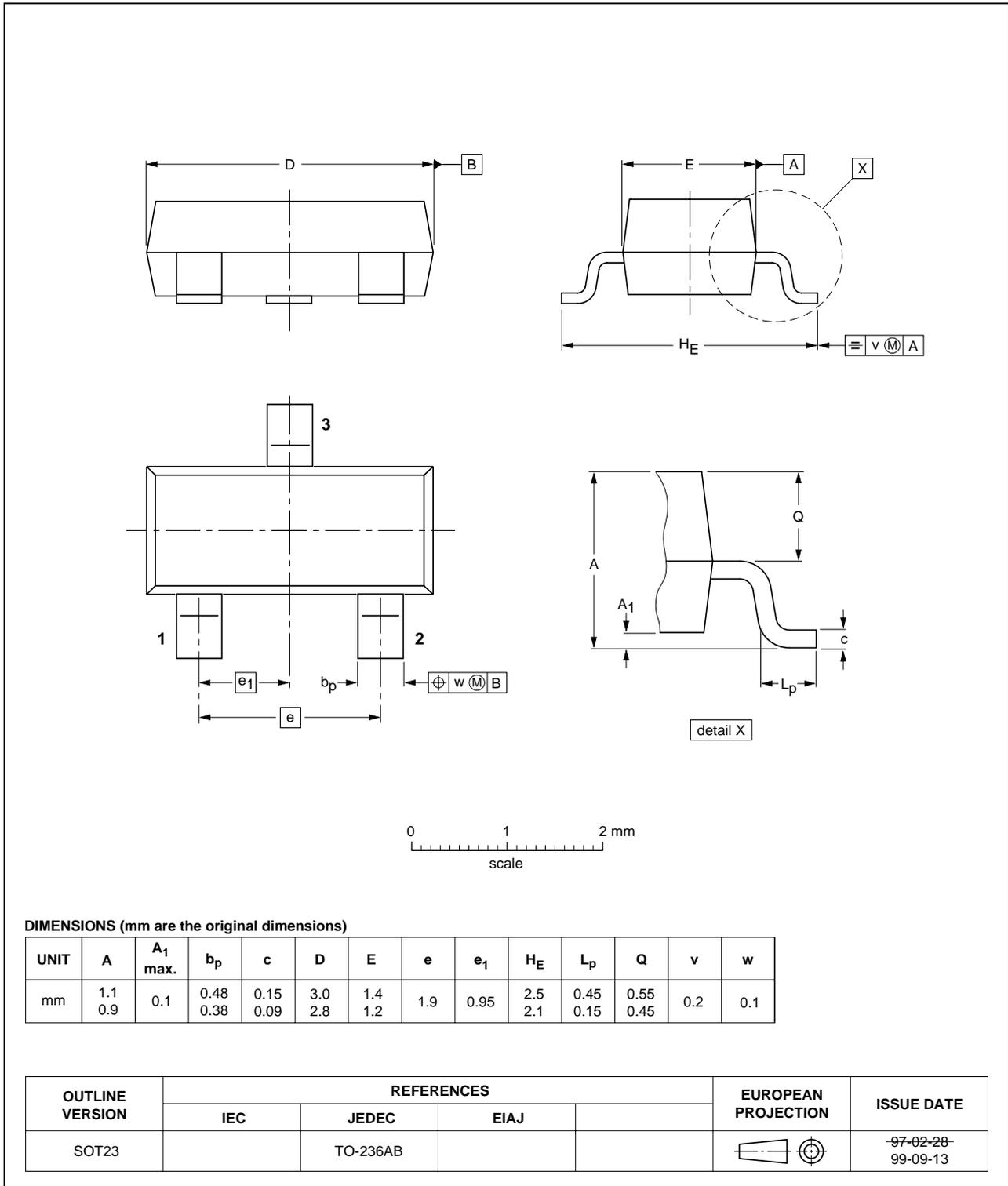
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



40 V, 2 A
PNP low V_{CEsat} (BISS) transistor

PBSS5240T

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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