



PMZ1200UPE

30 V, P-channel Trench MOSFET

25 March 2015

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Leadless ultra small SMD package: 1.0 x 0.6 x 0.48 mm

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

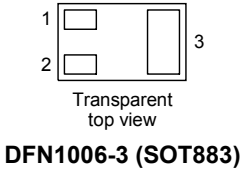
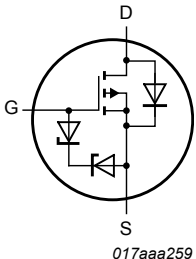
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ }^{\circ}\text{C}$		-	-	-30	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	-410	mA
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -410\text{ mA}; T_J = 25\text{ }^{\circ}\text{C}$		-	1.2	1.4	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1006-3 (SOT883)	 017aaa259
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ1200UPE	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

7. Marking

Table 4. Marking codes

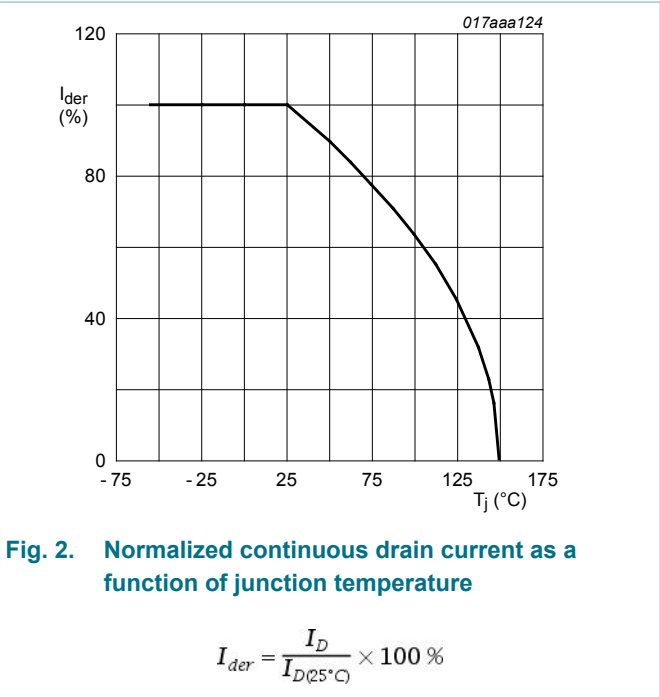
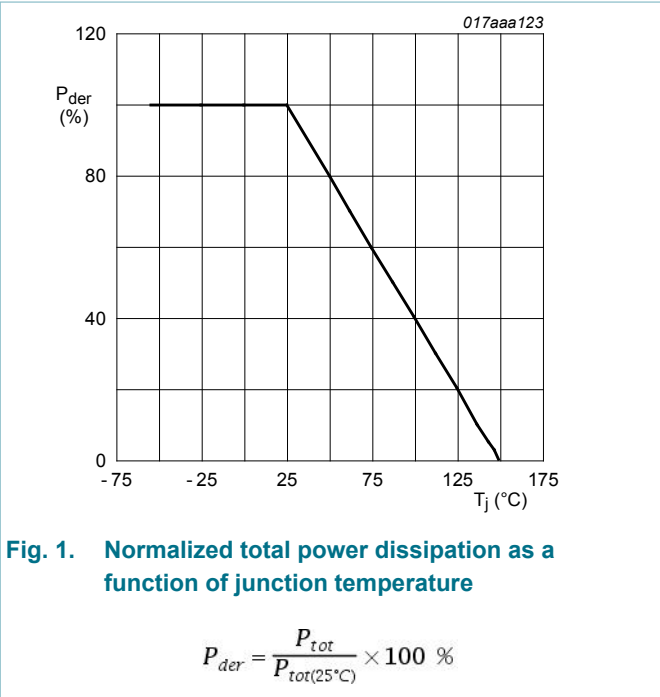
Type number	Marking code
PMZ1200UPE	ZL

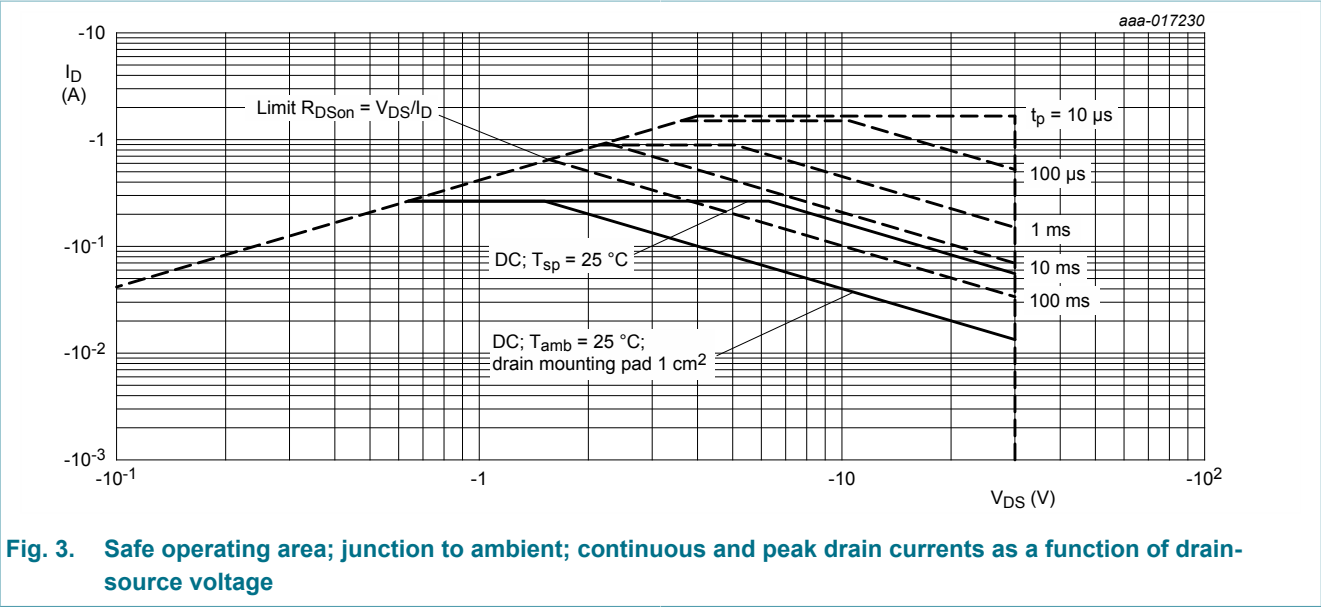
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-410	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-260	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-1.7	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	310	mW
			[1]	-	400	mW
		T _{sp} = 25 °C		-	1670	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-410	mA

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



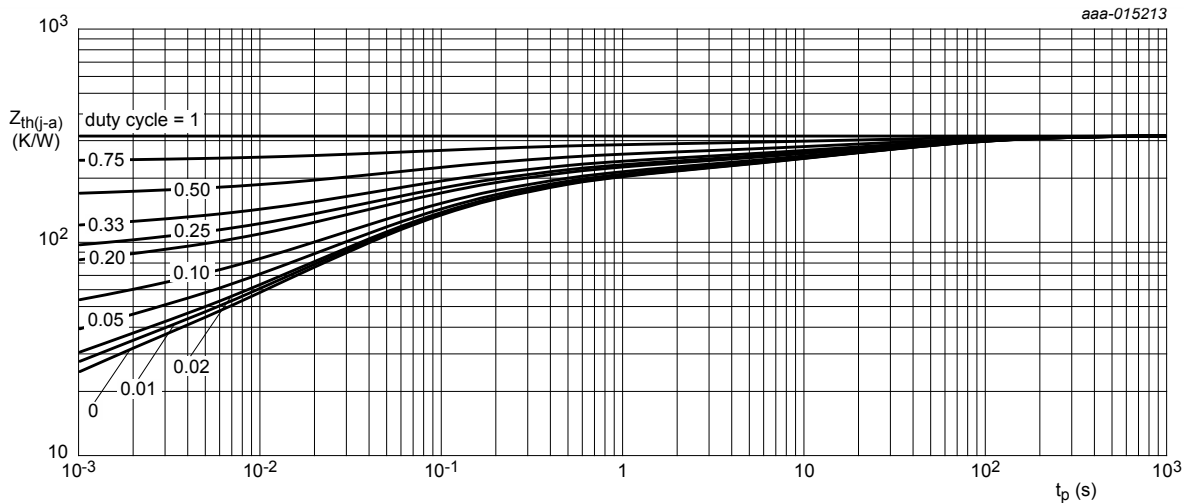


9. Thermal characteristics

Table 6. Thermal characteristics

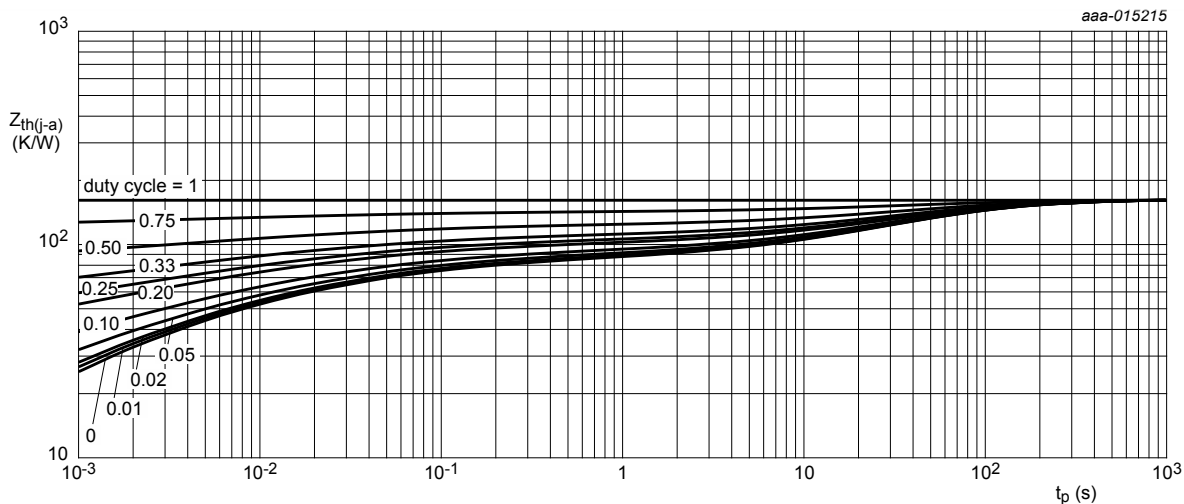
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	350	405	K/W
			[2]	-	270	310	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	65	75	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$		-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$		-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -30 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$		-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	5	μA
		$V_{GS} = -8 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	-5	μA
		$V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	1	μA
		$V_{GS} = -4.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	-1	μA
		$V_{GS} = 2.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	100	nA
		$V_{GS} = -2.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V$; $I_D = -410 mA$; $T_j = 25 ^\circ C$		-	1.2	1.4	Ω
		$V_{GS} = -4.5 V$; $I_D = -410 mA$; $T_j = 150 ^\circ C$		-	2	2.4	Ω
		$V_{GS} = -2.5 V$; $I_D = -320 mA$; $T_j = 25 ^\circ C$		-	1.7	2.3	Ω
		$V_{GS} = -1.8 V$; $I_D = -80 mA$; $T_j = 25 ^\circ C$		-	2.1	3.1	Ω
		$V_{GS} = -1.5 V$; $I_D = -10 mA$; $T_j = 25 ^\circ C$		-	3	5.1	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V$; $I_D = -410 mA$; $T_j = 25 ^\circ C$		-	820	-	mS
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V$; $I_D = -410 mA$; $V_{GS} = -4.5 V$; $T_j = 25 ^\circ C$		-	0.7	1.2	nC
Q_{GS}	gate-source charge			-	0.2	-	nC
Q_{GD}	gate-drain charge			-	0.2	-	nC
C_{iss}	input capacitance	$V_{DS} = -15 V$; $f = 1 MHz$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$		-	43.2	-	pF
C_{oss}	output capacitance			-	5.9	-	pF
C_{rss}	reverse transfer capacitance			-	4.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V$; $I_D = -410 mA$; $V_{GS} = -4.5 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 ^\circ C$		-	3	-	ns
t_r	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	14	-	ns
t_f	fall time			-	5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = -410 mA$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$		-	-0.95	-1.2	V

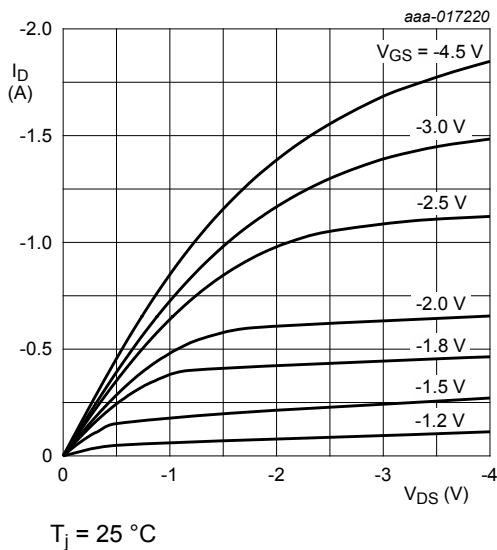


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

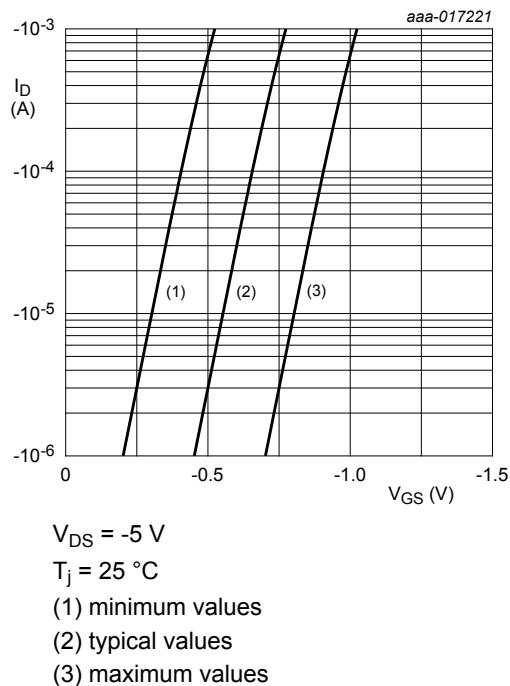


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

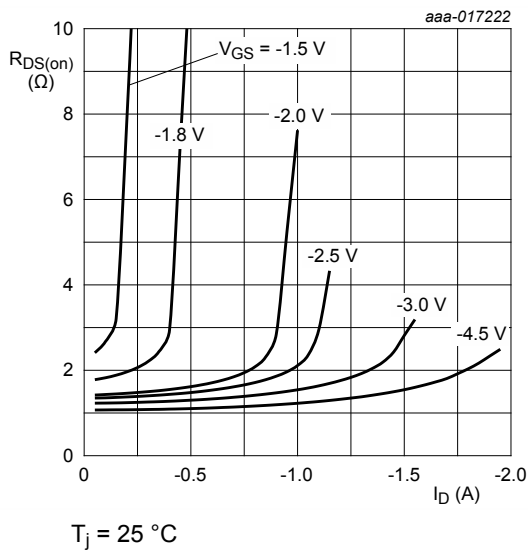


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

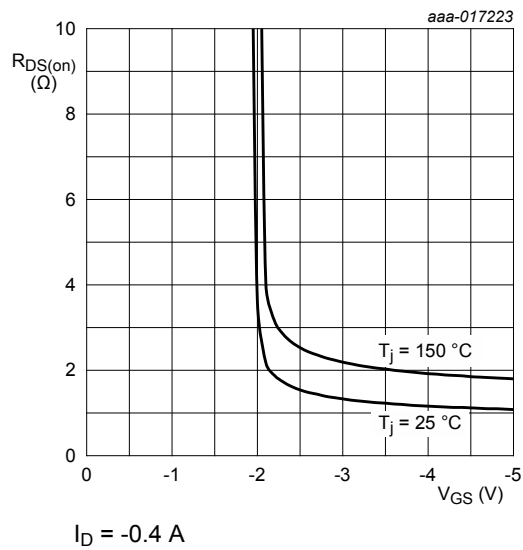


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

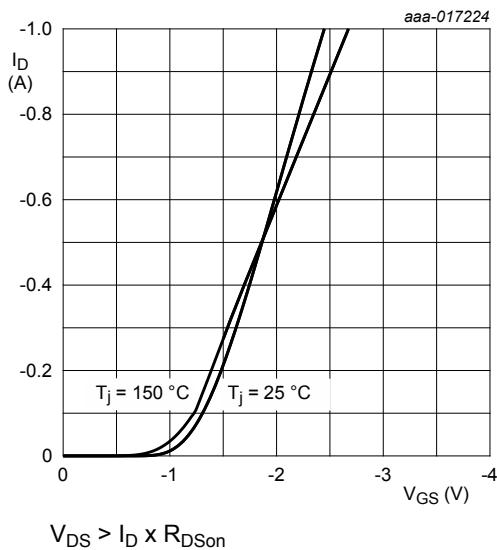


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

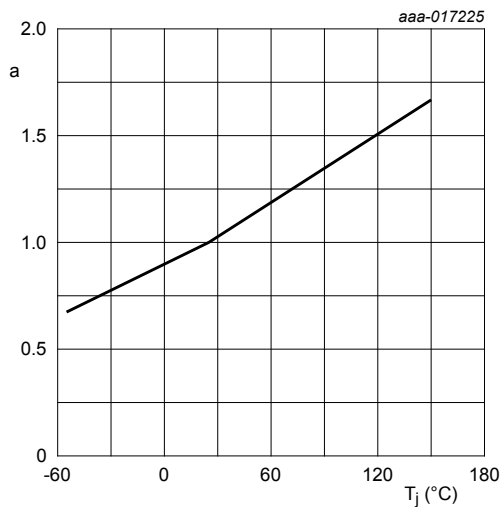


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)25\text{ °C}}}$$

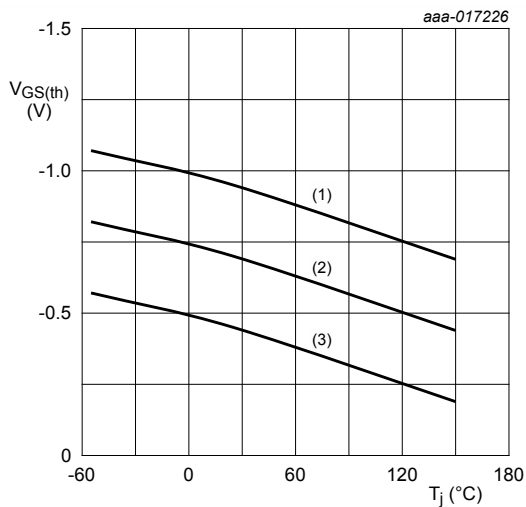


Fig. 12. Gate-source threshold voltage as a function of junction temperature

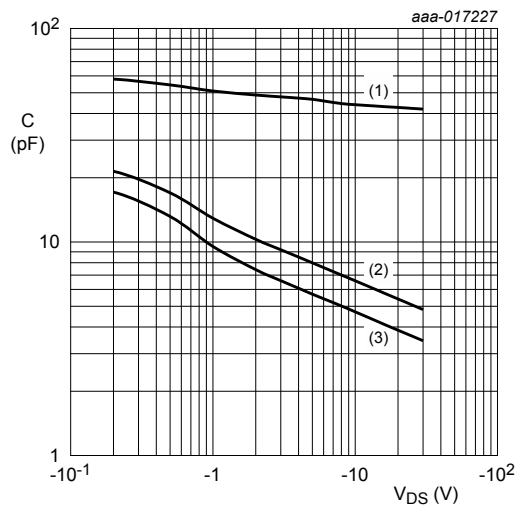


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

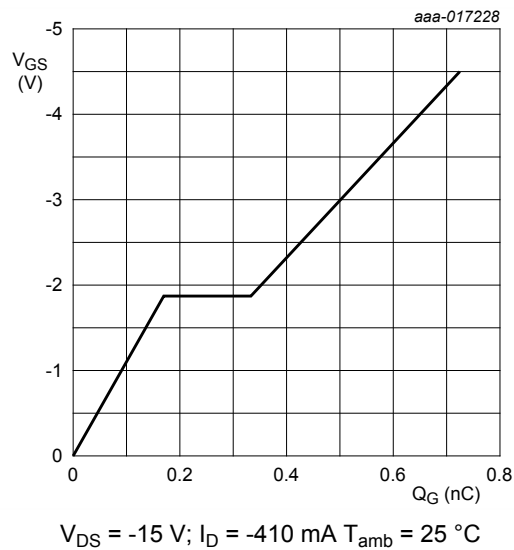


Fig. 14. Gate-source voltage as a function of gate charge; typical values



Fig. 15. Gate charge waveform definitions

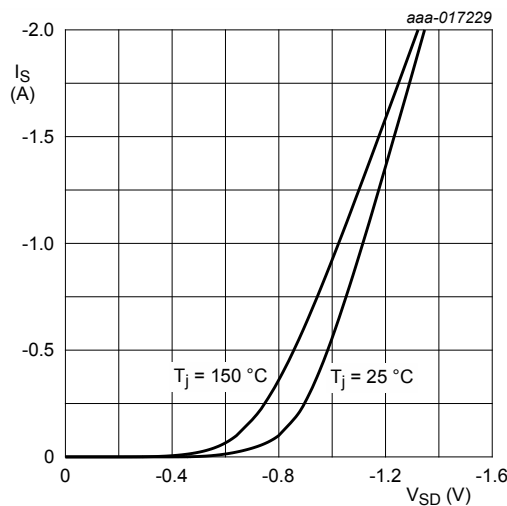


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

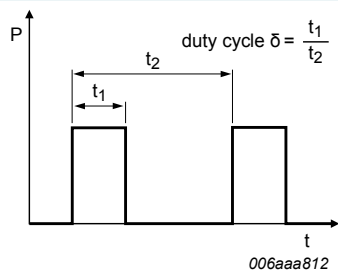


Fig. 17. Duty cycle definition

12. Package outline

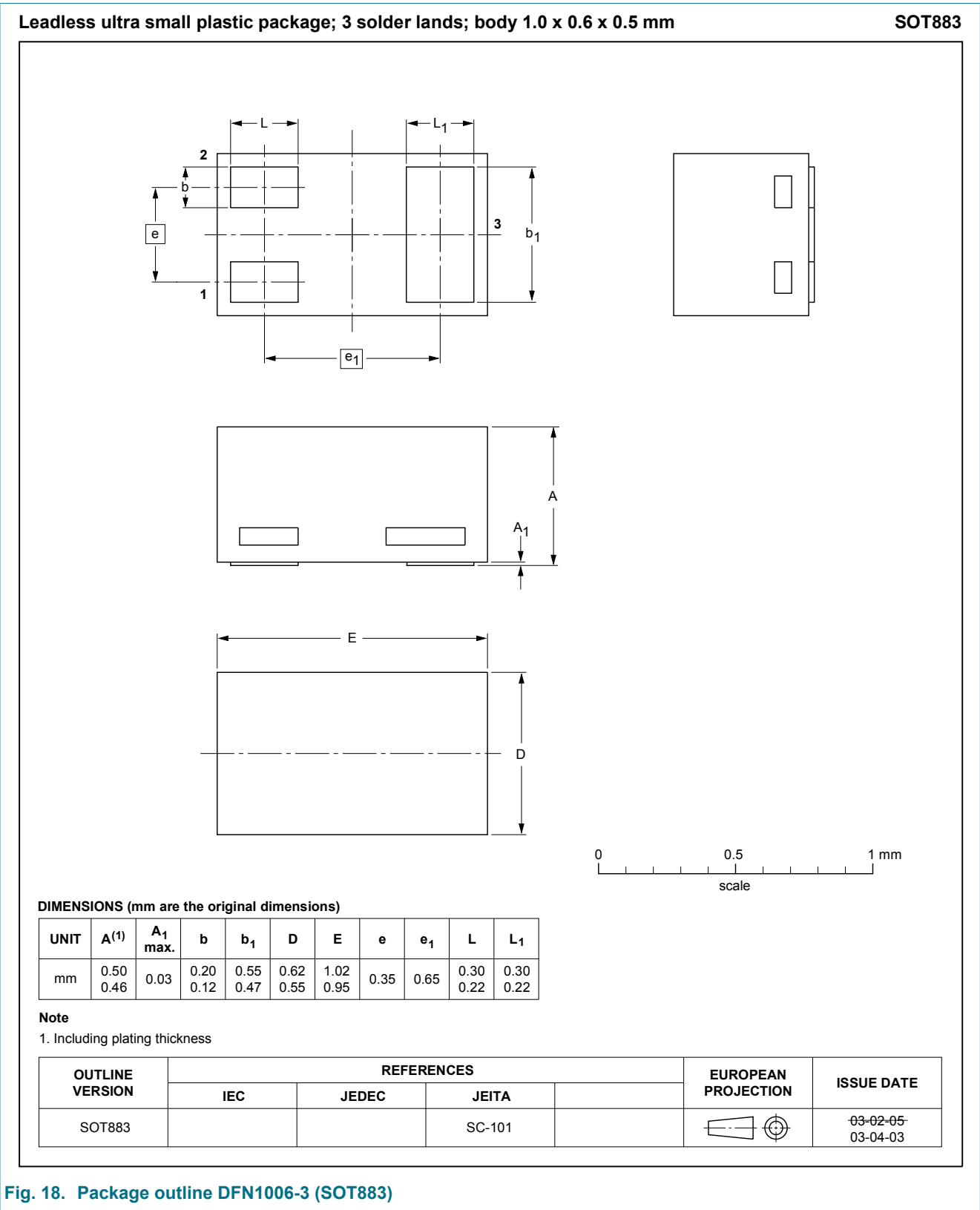


Fig. 18. Package outline DFN1006-3 (SOT883)

13. Soldering

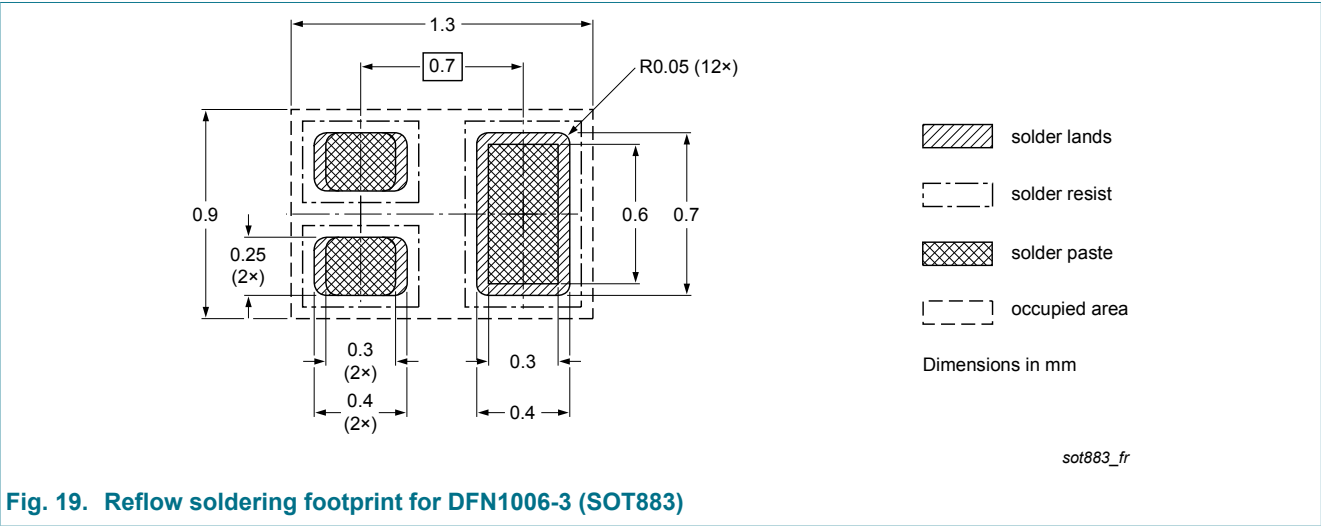


Fig. 19. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZ1200UPE v.1	20150325	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 25 March 2015

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