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# AR8035 Integrated 10/100/1000 Mbps Ethernet Transceiver

## Data Sheet

*80-Y0618-3 Rev A*

*October 25, 2012*

**Confidential and Proprietary - Qualcomm Atheros, Inc.**



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# Revision history

| Revision | Date | Description |
|---|---|---|
| 1.0 | April 2011 | Initial release |
| 2.0 | November 2011 | Electrical Characteristics<br>■ 3.2 Recommended Operation Conditions: delete DVDDL/AVDDL, $\Psi_{JA}$; add VDDH_REG, $\Psi_{JT}$, AVDDL/DVDDL (industrial and commercial); add thermal conditions<br>■ 3.6 change title from MDIO DC Characteristics to MDIO/MDC DC...; change $V_{IH}$ min value and $V_{IL}$ max value<br>■ 3.7 table 3-14: change $Jitter_{pk-pk}$ max value to 100<br>■ 3.11 Digital pin design guide (new)<br>Registers<br>■ 4.2.3 Status Register – Copper page, change bit[8] reset value to always 1<br>■ 4.3.4 Hib control and auto-neg test register: change bit[12], [6:5] to reserved<br>■ 4.3.5 External loopback selection, change bit[0] to R/W<br>■ 4.3.7 Power saving control (new) |

| Revision | Date | Description |
|---|---|---|
| A | October 2012 | System change from SharePoint to Agile. Based on SharePoint document system MKG-15827.<br>Introduction<br>■ Update Features<br>■ Update figure functional block diagram<br>Pin Description<br>■ Update Table Mode definition<br>■ Update Table Signal to pin descriptions<br>Function Descriptioin<br>■ Update Auto-negotiation<br>■ Update Function Wake on LAN<br>Electrical Characteristics<br>■ Absolute maximum ratings: add symbol Vmin<br>■ Update RGMII characteristics:<br>□ Table RGMII DC characteristics — 2.5/3/3V I/O supply: add GND - 0.3 to Min of symbol $V_{IL}$<br>□ Table RGMII DC characteristics — 1.8V I/O supply: add 2.1 to Max for symbol $V_{IH}$, add GND - 0.3 to Min for symbol $V_{IL}$, and add 1.9 to Max for symbol $V_{OH}$<br>□ Table RGMII DC characteristics — 1.5V I/O supply: add 1.8 to Max for symbol $V_{IH}$, add GND - 0.3 to Min for symbol $V_{IL}$, and add 1.57 to Max for symbol $V_{OH}$<br>□ Update RGMII characteristics and AC timing diagrams<br>■ MDIO timing: change Min from 10 to 0, add Typ 4, and remove Max of symbol tmdelay in Table MDIO AC characteristic<br>■ Clock characteristics: remove symbol Fs and Fo in table Recommended crystal parameters<br>■ Power pin current consumption: update the voltage range from “3.3V ±10%” to “3.3V ±5%” for symbol AVDD33 in table Power pin consumption<br>Update Registers<br>■ Add a note to table Register summary<br>■ Control register<br>■ Status register<br>■ Auto-negotiation advertisement register<br>■ 1000BASE-T status register<br>■ Extended status register<br>■ Function control register<br>■ Smart speed register: add bit[8]: GIGA_DIS_QUAL<br>■ Remove registers Auto-negotiation status, Auto-negotiation XNP transmit, Auto-negotiation XNP transmit1, Auto-negotiation XNP transmit2, Auto-negotiation LP XNP ability, Auto-negotiation LP XNP ability1, Auto-negotiation LP XNP ability2<br>■ Add registers PHY control debug register 0, Green feature configure 2, AZ control2, Cld control3, |

# Contents

# Tables

# Figures

# 1 Introduction

The AR8035 Ethernet transceiver is a single port, 10/100/1000 Mbps tri-speed Ethernet PHY. The AR8035 Ethernet transceiver supports RGMII to the MAC. The AR8035 Ethernet transceiver belongs to the Arctic™ PHY family which provides a low power, low BOM cost solution for comprehensive applications including enterprise, carrier and home networks such as CPE, home gateway, enterprise switch, carrier switch/router, mobile base station and base station controller, optical module and media converter, industrial automation and measurement.

The AR8035 Ethernet transceiver integrates Green ETHOS® power saving technologies which significantly save power in both active operation and idle condition. Green ETHOS power saving schemes include ultra-low power in cable unplugged mode or port power down mode, as well as automatically optimized power saving based on cable length. The AR8035 Ethernet transceiver supports standard IEEE 802.3az Energy Efficient Ethernet (EEE) and Qualcomm Atheros proprietary SmartEEE™. SmartEEE allows legacy MAC and SoC devices without IEEE 802.3az support to cowork with AR8035 to provide full IEEE 802.3az support. Furthermore, the AR8035 Ethernet transceiver supports Wake-on-LAN (WoL) feature to manage and regulate total system power requirements.

The AR8035 Ethernet transceiver embeds Cable Diagnostics Test (CDT) technology for measuring cable length, detecting the cable status, and identifying remote and local PHY malfunctions, bad or marginal patch cord segments or connectors.

The AR8035 Ethernet transceiver requires only a single 3.3 V power supply. Embedded regulators are used to generate other required voltages. The AR8035 Ethernet transceiver integrates the termination circuitry at the line side.

The AR8035 Ethernet transceiver supports IEEE 802.3az standard. The key features include:

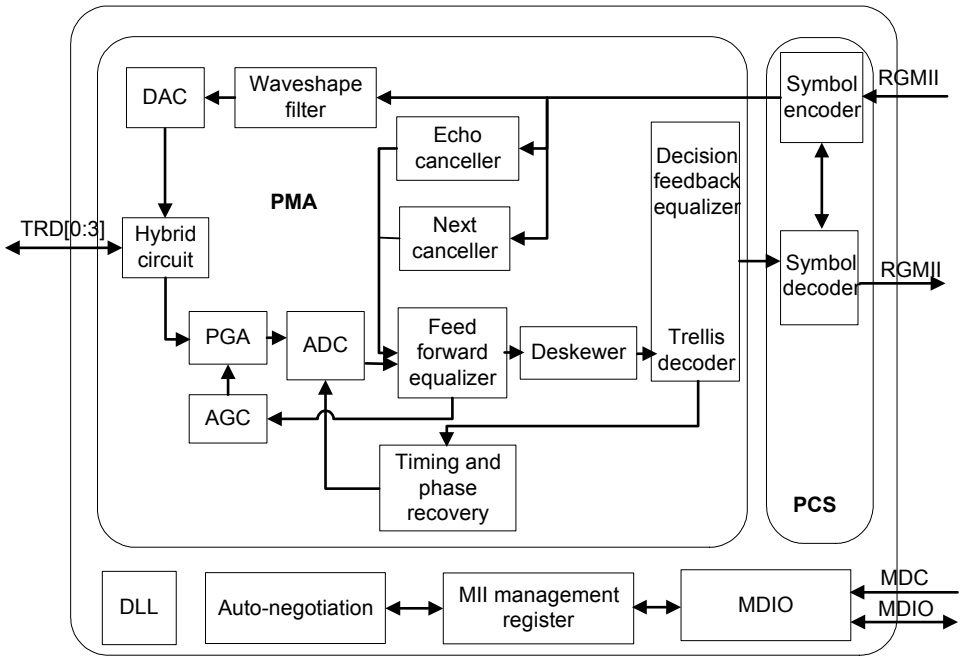
- 10BASE-Te PHY uses reduced transmit amplitude.
- 100BASE-TX and 1000BASE-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power when data traffic is idle.

## 1.1 Features

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- RGMII to MAC devices
- RGMII timing modes support internal delay and external delay on Rx path
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE

- SmartEEE which allows legacy MAC and SoC devices without IEEE 802.3az support to cowork with AR8035 to provide full IEEE 802.3az support
- Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant auto-negotiation
- Jumbo frame support up to 10 KB (full-duplex)
- Multiple loopback modes for diagnostics
- Robust surge protection with ±750 V/line-to-line mode and ±4 kV/line-to-ground mode IEC61000-4-5(2001)
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3 V, optional for external regulator for core voltage
- 6 mm × 6 mm, 48-pin QFN package
- Industry temperature (I-temp) option available

## 1.2 Functional block diagram



# 2 Pin Descriptions

This section includes a package pinout and signal descriptions.

### Nomenclatures for signal names

| | |
|---|---|
| **NC** | No signal connection from this pin |
| **_n** | Signal name suffix indicating active low signals |
| **_P** | Signal name suffix indicating the positive side of a differential signal |
| **_N** | Signal name suffix indicating the negative side of a differential signal |

### Nomenclatures for signal types

| | |
|---|---|
| **D** | Open drain |
| **IA** | Analog input signal |
| **I** | Digital input signal |
| **I/O** | Digital bidirectional signal |
| **OA** | Analog output signal |
| **O** | Digital output signal |
| **P** | Power or ground signal |
| **PD** | Internal pull-down for input |
| **PU** | Internal pull-up for input |

## 2.1 Pinout diagram

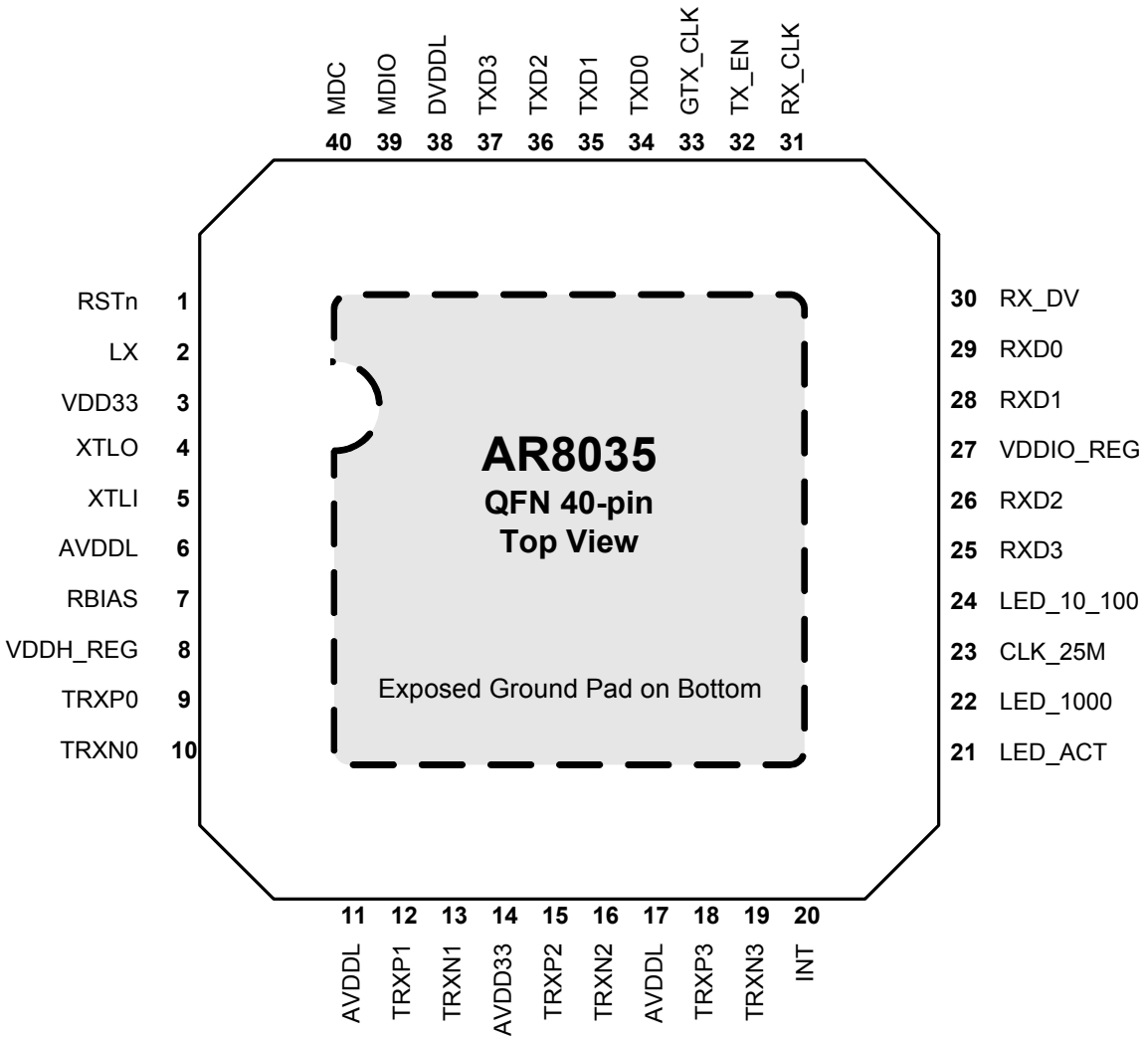



**Figure 2-1 AR8035 48-pin QFN pinout (top view)**

**NOTE** An exposed ground pad is on the back side of the package.

## 2.2 Pin descriptions

**Table 2-1 Signal to pin descriptions**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| ***MDI*** | | | |
| TRXP0 | 9 | IA, OA | Media-dependent interface 0, differential 100 Ω transmission line |
| TRXN0 | 10 | | |

**Table 2-1 Signal to pin descriptions** (cont.)

| Symbol | Pin | Type | Description |
|---|---|---|---|
| TRXP1 | 12 | IA, OA | Media-dependent interface 1, differential 100 Ω transmission line |
| TRXN1 | 13 | | |
| TRXP2 | 15 | IA, OA | Media-dependent interface 2, differential 100 Ω transmission line |
| TRXN2 | 16 | | |
| TRXP3 | 18 | IA, OA | Media-dependent interface 3, differential 100 Ω transmission line |
| TRXN3 | 19 | | |
| ***RGMII*** | | | |
| GTX_CLK | 33 | I, PD | RGMII transmit clock, 125 MHz @ 1000 Mbps, 25 MHz @ 100 Mbps, and 2.5 MHz @ 10 Mbps digital clock input. Adding a 22 Ω damping resistor is recommended near MAC side. |
| RX_CLK | 31 | I/O, PD | RGMII receive clock, 125 MHz @1000 Mbps, 25 MHz @ 100 Mbps, and 2.5 MHz @ 10 Mbps digital clock output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| RX_DV | 30 | I/O, PD | RGMII receive data valid, RGMII output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| RXD0 | 29 | I/O, PD | RGMII receive data 0, RGMII output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| RXD1 | 28 | I/O, PD | RGMII receive data 1, RGMII output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| RXD2 | 26 | I/O, PD | RGMII receive data 2, RGMII output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| RXD3 | 25 | I/O, PD | RGMII receive data 3, RGMII output. Adding a 22 Ω damping resistor is recommended near PHY side.<br>Power-on strapping input |
| TX_EN | 32 | I, PD | RGMII transmit enable, RGMII input |
| TXD0 | 34 | I, PD | RGMII transmit data 0, RGMII input |
| TXD1 | 35 | I, PD | RGMII transmit data 1, RGMII input |
| TXD2 | 36 | I, PD | RGMII transmit data 2, RGMII input |
| TXD3 | 37 | I, PD | RGMII transmit data 3, RGMII input |
| ***Management interface*** | | | |
| MDC | 40 | I, PU | Management data clock reference |
| MDIO | 39 | I/O, D, PU | Management data, 1.5 kΩ pull-up resistor to 3.3 V/2.5 V |
| ***LED*** | | | |

**Table 2-1 Signal to pin descriptions** (cont.)

| Symbol | Pin | Type | Description | | |
|---|---|---|---|---|---|
| LED_ACT | 21 | I/O, PU | Parallel LED output for 10BASE-Te/100BASE-TX/1000BASE-T activity; LED active based on power-on strapping.<br>If pulled up, active low; if pulled down, active high. | | |
| LED_1000 | 22 | I/O, PU | Parallel LED output for 1000BASE-T link; LED active based on power-on strapping.<br>If pulled up, active low; if pulled down, active high. | | |
| LED_10_100 | 24 | I/O, PU | Parallel LED output for 10BASE-Te/100BASE-TX link. LED active based on power-on strapping of LED_1000.<br>If LED_1000 is pulled up, this pin is active low; if LED_1000 is pulled down, this pin is active high. | | |
| | | | External PU | High | 10 Mbps |
| | | | | Low | 100 Mbps |
| | | | External PD | Low | 10 Mbps |
| | | | | High | 100 Mbps |
| For detailed information of LED, see “LED interface” on page 25. | | | | | |
| ***System signal group/reference*** | | | | | |
| CLK_25M | 23 | O, PD | .The clock output that references the local clock. The frequency, configured by the register, can be 25 MHz, 50 MHz, 62.5 MHz or 125 MHz. | | |
| RSTn | 1 | I | System reset, active low. This pin requires an external pull-up resistor to 2.5 V or 3.3 V. | | |
| XTLI | 5 | IA | Crystal oscillator input; typical 27 pF capacitor to GND. Support external 25 MHz 1.2 V swing clock input through this pin. | | |
| XTLO | 4 | OA | Crystal oscillator output; typical 27 pF capacitor to GND | | |
| RBIAS | 7 | OA | External 2.37 kΩ 1% resistor to GND to set bias current | | |
| INT | 20 | I/O, D, PD | System interrupt output. This pin is OD-gate by default and requires external 10 kΩ pull-up resistor, active low. | | |
| ***Power*** | | | | | |
| LX | 2 | OA | Power inductor pin. Add an external 4.7 µH/500 mA power inductor to this pin directly. | | |
| VDDH_REG | 8 | OA | 2.5 V internal regulator output. Adding a 1 µF capacitor parallel with this pin and GND is recommended. | | |
| VDDIO_REG | 27 | OA | Regulator output for the RGMII I/O voltage. It can be either 1.5 V (default) or 1.8 V. If 2.5 V is intended for the RGMII I/O, connect this pin with the 2.5 V regulator output at pin 10 (VDDH_REG). | | |
| AVDDL | 6, 11, 17 | P | 1.1 V analog input. Connect to pin 38 through a bead. | | |
| DVDDL | 38 | P | 1.1 V digital core power input. Connect to power inductor directly and 10 µF+0.1 µF ceramic capacitors to GND. | | |
| VDD33 | 3 | P | 3.3 V input for internal switching regulator | | |

**Table 2-1 Signal to pin descriptions** (cont.)

| Symbol | Pin | Type | Description |
|---|---|---|---|
| AVDD33 | 14 | P | 3.3 V input for PHY, from VDD33 through a bead |
| In the Type column, PU and PD indicates the pin includes internal weak pull-up and pull-down resistor respectively. | | | |

# 2.3 Power-on strapping

Table 2-2 lists the pin-to-PHY core power-on strapping configurations.

**Table 2-2 Power-on strapping pins**

| PHY pin | PHY core configuration signal | Description | Default internal weak pull-up/down |
|---|---|---|---|
| RXD0 | PHYADDRESS0 | LED_ACT and RXD[1:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00. | 0 |
| RXD1 | PHYADDRESS1 | | 0 |
| LED_ACT | PHYADDRESS2 | | 1 |
| RX_DV | MODE[0] | Mode select bit 0 | 0 |
| RXD2 | MODE[1] | Mode select bit 1 | 0 |
| LED_1000 | MODE[2] | Mode select bit 2 | 1 |
| RXD3 | MODE[3] | Mode select bit 3 | 0 |
| RX_CLK | 1.8V/1.5V | Select the RGMII I/O voltage level<br>1 = 1.8 V I/O<br>0 = 1.5 V I/O | 0 |

1. 0 = Pull-down, 1 = Pull-up.
2. Power-on strapping pins are latched during power-up reset or warm hardware reset.
3. Because the MAC device input pins can be driven high or low during power-up or reset, PHY power-on strapping status can be affected by the MAC side. In this case, an external 10 kΩ pull-down or pull-up resistor is required to ensure stable status.
4. When using 2.5 V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

## 2.3.1 Mode definition

Table 2-3 lists the mode definition.

**Table 2-3 Mode definition**

| Mode [3:0] | Description |
|---|---|
| 1100 | RGMII, PLL OFF, INT |
| 1110 | RGMII, PLL ON, INT |

**Table 2-3 Mode definition** (cont.)

| Mode [3:0] | Description |
|---|---|
| Others | Reserved |
| PLLOFF indicates that AR8035 can shut down internal PLL in power saving mode. In PLL OFF mode, when AR8035 enters power saving mode (hibernation), CLK_25M output drops periodically, which saves more power. In PLL ON mode, CLK_25M outputs continuously. | |

# 3 Function Description

The AR8035 Ethernet transceiver is an low cost GbE PHY. The highly integrated Analog Front End (AFE) and Digital Signal Processing (DSP) architecture ensures robust performance combined with substantial cost reduction. The AR8035 Ethernet transceiver provides physical layer functions for half/full-duplex 10BASE-Te, 100BASE-TX and full-duplex 1000BASE-T Ethernet to transmit and receive high-speed data over standard Category 5 (CAT5) un-shielded twisted pair cable.

The AR8035 10/100/1000 PHY is fully IEEE 802.3ab compliant, and supports Reduced Gigabit Media-Independent Interface (RGMII) to connect to a Gigabit-capable MAC.

The AR8035 Ethernet transceiver combines echo canceller, Near End Cross Talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

Table 3-1 lists feature comparison among the AR8031, AR8033, and AR8035 family.

**Table 3-1 AR8031, AR8033, and AR8035 comparison**

| Feature | AR8031 | AR8033 | AR8035 |
|---|---|---|---|
| RGMII | Yes | Yes | Yes |
| SGMII | Yes | Yes | – |
| Cu Ethernet(2) | Yes | Yes | Yes |
| EEE (IEEE 802.3az) | Yes | Yes | Yes |
| Wake-on-LAN | Yes | Yes | Yes |
| SerDes/Fiber(3) | Yes | Yes | – |
| 1588v2 | Yes | – | – |
| Sync-E | Yes | Yes | – |
| Packaging | 48-pin | 48-pin | 40-pin |

1. AR8031 and AR8033 are pin-to-pin compatible.
2. 10BASE-Te, 100BASE-TX, and 1000BASE-T are supported.
3. 100BASE-FX and 1000BASE-X are supported.

## 3.1 Transmit functions

Table 3-2 lists the transmit function encoder modes.

**Table 3-2 Transmit function encoder modes**

| Mode | Description |
|---|---|
| 1000BASE-T | In 1000BASE-T mode, AR8035 scrambles Tx data bytes from the MAC interfaces and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable. |
| 100BASE-TX | In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a 3-level MLT3 sequence transmitted by the PMA. |
| 10BASE-Te | In 10BASE-Te mode, AR8035 transmits and receives Manchester-encoded data. |

# 3.2 Receive functions

## 3.2.1 Decoder modes

Table 3-3 lists the receive function decoder modes.

**Table 3-3 Receive function decoder mode**

| Mode | Description |
|---|---|
| 1000BASE-T | In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces. |
| 100BASE-TX | In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated. |
| 10BASE-Te | In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned. |

## 3.2.2 Analog-to-Digital converter

Each Rx channel includes an advanced high speed ADC with high resolution for better Signal-to-Noise Ratio (SNR) and lower error rates.

## 3.2.3 Echo canceller

Because hybrid circuit is used to transmit and receive simultaneously on each pair, echo occurs when the transmitter is not perfectly matched to the line. Connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, can also result in drastic SNR degradation on the Rx signal.

The adaptive digital echo canceller is used to compensate for the varied channel conditions that result in SNR degradation on the Rx signal.

### 3.2.4 NEXT canceller

The 1000BASE-T physical layer uses all four twisted pairs to transmit data which incurs significant high frequency crosstalk occurs between adjacent pairs.

Three parallel NEXT cancellers are thus integrated on each Rx channel to cancel high frequency crosstalk by subtracting an estimate noise signals from the equalizer output.

### 3.2.5 Baseline wander canceller

Baseline wander occurs on Ethernet links AC-coupled to the transceiver. When the AC-coupling cannot maintain voltage levels for a specific time, the transmitted pulses are distorted which results in erroneous sampled values for affected pulses.

The baseline wander cancellation circuit continuously monitors and compensates for this issue, minimizing the impact of DC baseline shift on the overall error rate.

### 3.2.6 Digital adaptive equalizer

The digital adaptive equalizer, using a combination of Feedforward Equalizer (FFE) and Decision Feedback Equalizer (DFE), removes inter-symbol interference at the receiver by filtering unequalized signals from ADC output for optimized SNR.

### 3.2.7 Auto-negotiation

The auto-negotiation function for 10BASE-Te/100BASE-TX/1000BASE-T Copper complies with IEEE 802.3 clauses 28 and 40.

Auto-negotiation provides a mechanism to exchange information between a pair of link partners to choose the optimized mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-on reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- Link down

When auto-negotiation is disabled, the operation speed mode can be manually selected using the IEEE MII register 0.

**NOTE** In 10BASE-Te/100BASE-TX, when one end disables auto-negotiation (force mode) and the other end enables auto-negotiation (advertise half-duplex), the link can be established and the end with auto-negotiation enabled works in half-duplex mode. So if the end in force mode is in half-duplex mode, the information transmission between the two link partners works normally; if the end in force mode is in full-duplex mode,

mismatch occurs between the two link partners. The link cannot be established in 1000BASE-T under similar situation.

## 3.2.8 Smartspeed

The Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8035 device to downgrade in speed based on cabling conditions. With Smartspeed enabled, after a configurable number (MII Register 14.4:2) of failed attempts, the PHY automatically downgrades the highest ability it advertises to the next lower speed: from 1000 to 100 to 10.

The Smartspeed feature is enabled by default. See “Smart speed register” on page 65 for detailed information.

- Bit[5]: SMARTSPEED_EN
  - 1 = Enables Smartspeed (default)
  - 0 = Disables Smartspeed
- Bits[4:2]: SMARTSPEED_RETRY_LIMIT

  Sets the number of link attempts before adjusting
- Bit[1]: BYPASS_SMARTSPEED_TIMER

  Timer to determine the stable link condition

**NOTE** The Smartspeed enable bit requires a software reset to take effect after writing bit[15] in Control register (0x0) to 1. When Smartspeed function is disabled, write bit[8] in Smart speed register (0x14) to 1, rather than change bit[9] in 1000BASE-T control register (0x9), to disable 1000BASE-T full-duplex link ability.

## 3.2.9 Automatic MDI/MDIX crossover

During auto-negotiation, the automatic MDI/MDIX crossover function automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable.

The algorithm described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover when the remote device implements automatic MDI crossover as well.

For 1000BASE-T, swap can happen only between pair A and pair B, or pair C and pair D. See Table 3-4.

**Table 3-4 Supported MDI pair combinations**

| | | | | |
|---|---|---|---|---|
| A (1, 2) | B (3, 6) | C (4, 5) | D (7, 8) | Normal MDI |
| B (3, 6) | A (1, 2) | D (7, 8) | C (4, 5) | Normal MDI-X |
| A (1, 2) | B (3, 6) | D (7, 8) | C (4, 5) | Normal MDI with pair swap on C and D pair |
| B (3, 6) | A (1, 2) | C (4, 5) | D (7, 8) | Normal MDI-X with pair swap on C and D pair |

### 3.2.10 Polarity correction

If cable polarity is incorrectly wired, the polarity correction function automatically corrects polarity errors on the receive pairs in 1000BASE-T, 100BASE-TX, and 10BASE-Te modes.

## 3.3 Loopback modes

### 3.3.1 Digital loopback

Digital loopback loops transmitted data back to the receiver using digital circuit in the AR8035 device. Figure 3-1 shows the block diagram for the digital loopback.

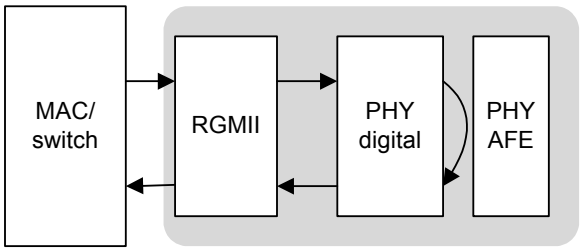



**Figure 3-1 Digital loopback**

#### Configuring internal loopback

MII register settings for PHY internal digital loopback mode selection:

- 1000M loopback: register 0x0 = 0x4140
- 100M loopback: register 0x0 = 0x6100
- 10M loopback: register 0x0 = 0x4100

### 3.3.2 External cable loopback

External cable loopback loops RGMII Tx to RGMII Rx through complete digital and analog path and an external cable. This function is used to test the digital data paths and the analog circuits. Figure 3-2 shows a block diagram of external cable loopback.

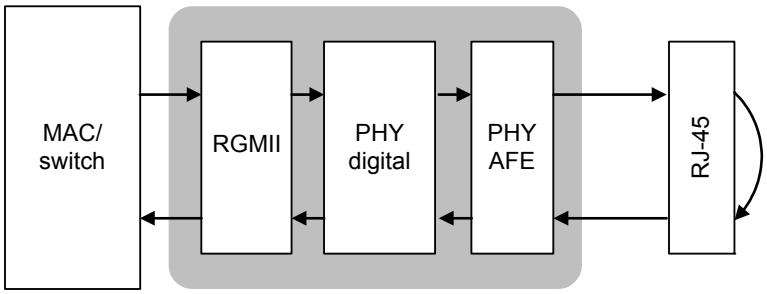



**Figure 3-2 External cable loopback**

### Configuring external cable loopback

To configure external cable loopback:

1. Plug in an external loopback cable (1 wiring 3, 2 wiring 6, 4 wiring 7, and 5 wiring 8).
2. Set bit[15] PS_HIB_EN of External loopback selection register (Debug Register offset 0xB) to 0 to disable hibernate (power saving) mode.
3. Set bit[0] EXT_LPBK of External loopback selection register (Debug Register offset 0x11) to 1 to enable external loopback.
4. Set MII Register 0x0 to select loopback modes:
   - 1000M loopback: register 0x0 = 0x8140
   - 100M loopback: register 0x0 = 0xA100
   - 10M loopback: register 0x0 = 0x8100

**NOTE** When cable is removed and reconnected to 1000M mode, the register 0x0 must be configured to 0x8140 again to establish PHY link.

## 3.3.3 Remote PHY loopback

In remote PHY loopback mode, the data from MDI Rx is looped back to MDI Tx to enable the remote link partner to detect the connectivity in the loop.

Figure 3-3 shows the block diagram of the remote PHY loopback.

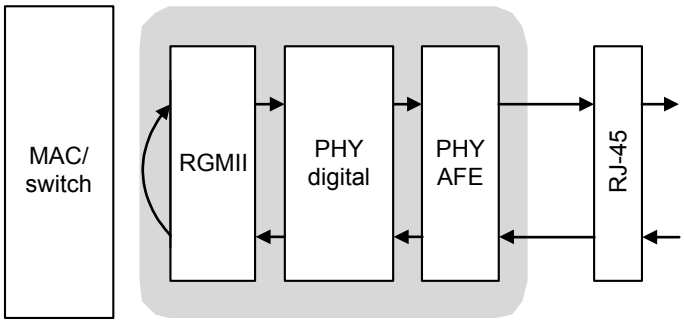



**Figure 3-3 Remote PHY loopback**

### Configuring remote PHY loopback

To enable remote PHY loopback, set bit[0] of MMD3 — RemotePHY loopback register (MMD3 Register offset 0x805A) to 1.

**NOTE** When remote loopback is enabled, packets from link partner still appear at RGMII.

## 3.4 Cable diagnostic test

The Cable Diagnostic Test (CDT) feature uses Time Domain Reflectometry (TDR) technology to identify malfunctions in remote and local PHYs, bad or marginal cable, patch cord segments and connectors.

The following are the problems that can be possibly diagnosed using CDT:

- Open
- Short
- Cable impedance mismatch
- Bad connector
- Termination mismatch
- Bad magnetic

The CDT can be performed when no link partner is present or the link partner is auto-negotiating.

### Configuring CDT

To perform the cable diagnostic test:

1. Set bits[9:8] MDI PAIR SELECT of Cable diagnostic test control register (offset 0x16) to select the MDI pair to be tested.
2. Set bit[0] ENABLE TEST of Cable diagnostic test control register (offset 0x16) to 1 to enable CDT.
3. Check bits[9:8] STATUS of Cable diagnostic test status register (offset 0x1C) for cable status.

4. Check bits[7:0] DELTA_TIME of Cable diagnostic test status register (offset 0x1C) for delta time. The distance between the faulty point and PHY is [delta time] × 0.824.

## 3.5 LED interface

The LED interface can be controlled by the PHY or manually, independent of the state of the PHY. The LED pins can be programmed to indicate the following status:

- Operation speed
- Traffic mode
- Link

Figure 3-4 and Figure 3-5 show the reference designs for the LED interface.

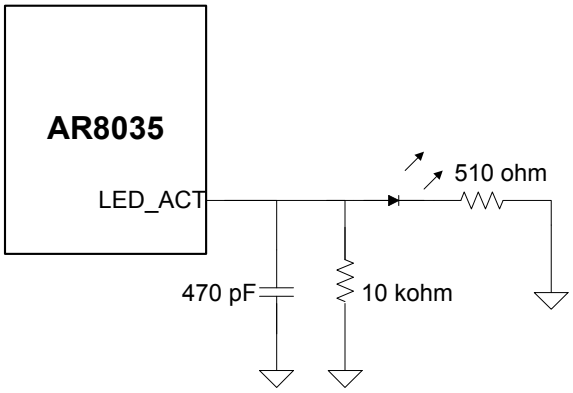



**Figure 3-4 Reference design for LED, active high**

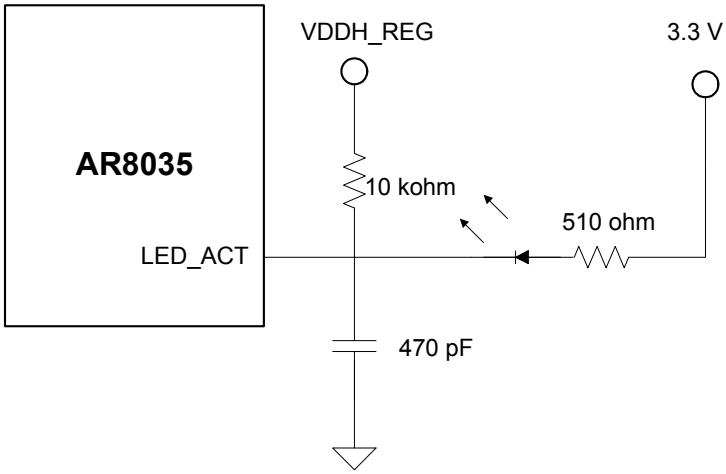



**Figure 3-5 Reference design for LED, active low**

The active status of LED_ACT and LED_1000 depends on power-on strapping mode. When the interface is strapped high, the LED interface is active low; when strapped low, the LED interface is active high.

The active status of LED_10_100 depends on LED_1000 power-on strapping mode and thus LED_10_100 and LED_1000 use the same LED reference design.

The default LED functions are listed in Table 3-5.

**Table 3-5 Default LED status**

| Symbol | 10M link | 10M active | 100M link | 100M active | 1000M link | 1000M active |
|---|---|---|---|---|---|---|
| LED_10_100 | OFF | OFF | ON | ON | OFF | OFF |
| LED_1000 | OFF | OFF | OFF | OFF | ON | ON |
| LED_ACT | ON | BLINK | ON | BLINK | ON | BLINK |
| ON = active; OFF = inactive | | | | | | |

## 3.6 Power supplies

One external power supply is required:

- 3.3 V

Internal power rails are:

- 3.3 V
- 2.5 V
- 1.1 V
- 1.8/1.5 V

AR8035 integrates a switch regulator to convert 3.3 V to 1.1 V with high efficiency for core power rail.

Two embedded LDOs are integrated to support 2.5, 1.5/1.8 V RGMII I/O voltages. When working at 2.5 V RGMII I/O, connect the VDDH_REG pin to VDDIO_REG pin directly. The 2.5 V to 1.5/1.8 V regulator can be set to any mode because the output voltage is same as input which causes regulator shutdown. When working at 2.5 V RGMII I/O, AR8035 can connect with 3.3 V RGMII I/O. Because the input can bear 3.3 V logic signal, the output logic VoH and VoL can satisfy the 3.3 V LVCMOS/LVTTL requirements. See “Electrical Characteristics” on page 34 for parameter details.

Figure 3-6 shows the reference design for 2.5/3.3 V RGMII voltage level.

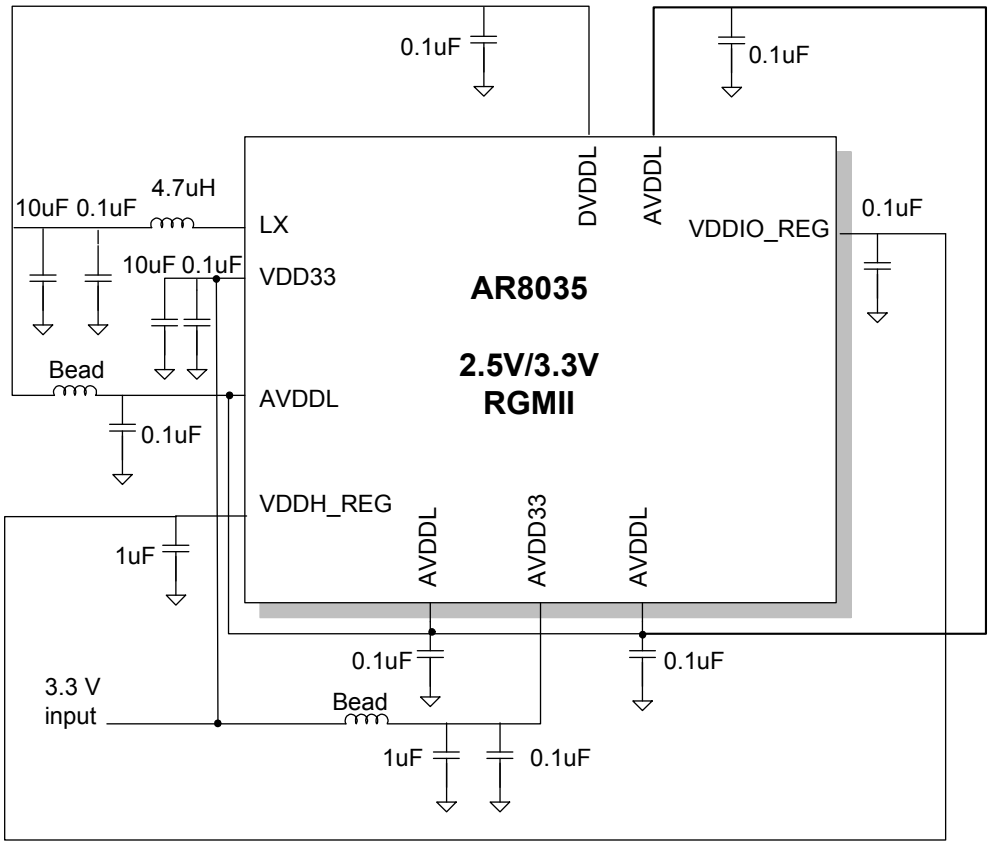



**Figure 3-6 Reference design, 2.5/3.3 V RGMII I/O**

When working at 1.5/1.8 V RGMII I/O, disconnect VDDH_REG and VDDIO_REG and set the internal LDO to output the right voltage. The 1.5 V or 1.8 V selection is configured by bit[3] in PHY control debug register 0 (debug register 0x1F).

Figure 3-7 shows the reference design for 1.5/1.8 V RGMII voltage level.

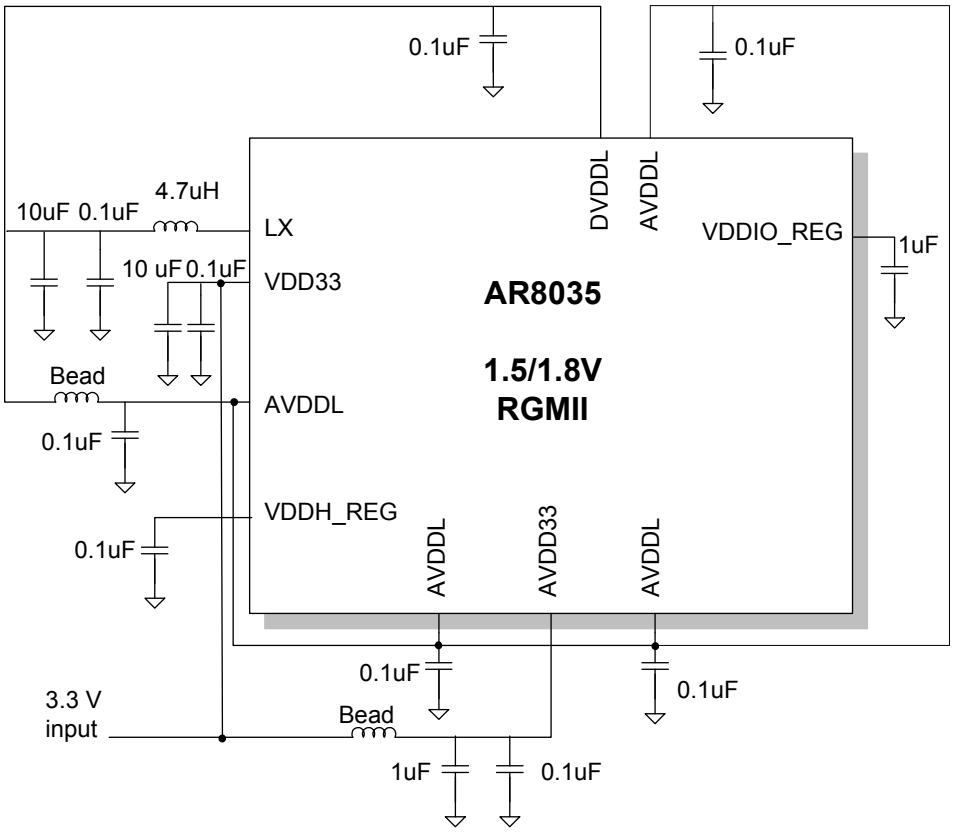



**Figure 3-7 Reference design, 1.5/1.8 V RGMII I/O**

## 3.7 Management interface

The management interface, compliance with IEEE 802.3u clause 22, provides access to the internal registers of PHYs via the MDC and MDIO pins. MDC is sourced by the station management entity to the PHY as the timing reference for transfer of information on the MDIO signal.

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO is an open-drain I/O and requires an external 1.5 kΩ pull-up resistor.

Table 3-6 and Table 3-7 describe the management interface format.

**Table 3-6 Management interface frame fields**

| | PRE | ST | OP | PHYAD | REGAD | TA | DATA | IDLE |
|---|---|---|---|---|---|---|---|---|

**Table 3-6 Management interface frame fields** (cont.)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| READ | 1...1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| WRITE | 1...1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

**Table 3-7 Management interface field definitions**

| Field | Definition |
|---|---|
| PRE | A sequence of 32 contiguous single logic bits on MDIO with corresponding cycles on MDC to provide PHY with a pattern for synchronization. |
| ST | 2-bit start of frame |
| OP | 2-bit operation code. 10 = read transaction, 01 = write transaction |
| PHYAD | 5-bit PHY device address. The bits[2:0] in the PHY address are configured by power-on strapping, thus eight PHYs can be connected to a single management interface. The PHYs connected to the same bus have unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. |
| REGAD | 5-bit register address. The 5-bit register address allows 32 registers to be addressed at each PHY. The first register address bit transmitted and received is the MSB of the address. |
| TA | 2-bit field to avoid contention during a read operation.<br>In read operation, both MAC and PHY are at high-impedance state for the first bit time. The PHY drives a zero during the second bit time of the turnaround.<br>In write operation, the MAC must drive 10. |
| DATA | 16-bit data from accessed register. MSB is transmitted first. |
| IDLE | High-impedance without driving state of the MDIO. At least one clocked idle state is required between frames. |

# 3.8 Green ETHOS feature

## 3.8.1 Low power modes

The AR8035 device supports the low power mode with software power-down.

To enter the standard IEEE power-down mode, set the bit[11] POWER_DOWN of Control register to 1. In this mode, AR8035 ignores all MAC interface signals except the MDC/MDIO and does not respond to any activity on the media side.

AR8035 cannot wake up on its own and is only waken up by setting the POWER_DOWN bit to 0.

## 3.8.2 Short cable power mode

Given cable length of less than 30 meters, Qualcomm Atheros proprietary Green ETHOS power saving technology saves 25% power consumption over standard consumption on 100-meter CAT5 cable.

### 3.8.3 Hibernation mode

Hibernation mode yields very low power consumption compared with normal operation mode.

When cable is unplugged, AR8035 enters hibernation mode in about 10 seconds. When cable is reconnected, AR8035 wakes up to restore normal function.

## 3.9 IEEE 802.3az

IEEE 802.3az provides a mechanism to reduce power consumption between data packets bursts. Two operating states are supported: active state for normal data transfer, and Low Power Idle (LPI) state for power saving between the data packet bursts.

The link partners enter LPI state by sending short refresh signals to maintain the link. In the low-power state, PHY shuts down most of the analog and digital blocks. In Ethernet network where systems stay in non-burst mode most of time, therefore over 90% power can be saved with LPI enabled.

During link establishment, both link partners exchange information through auto-negotiation to determine if both parties are LPI-capable.

Legacy Ethernet products are supported.

The link states for IEEE 802.3az include:

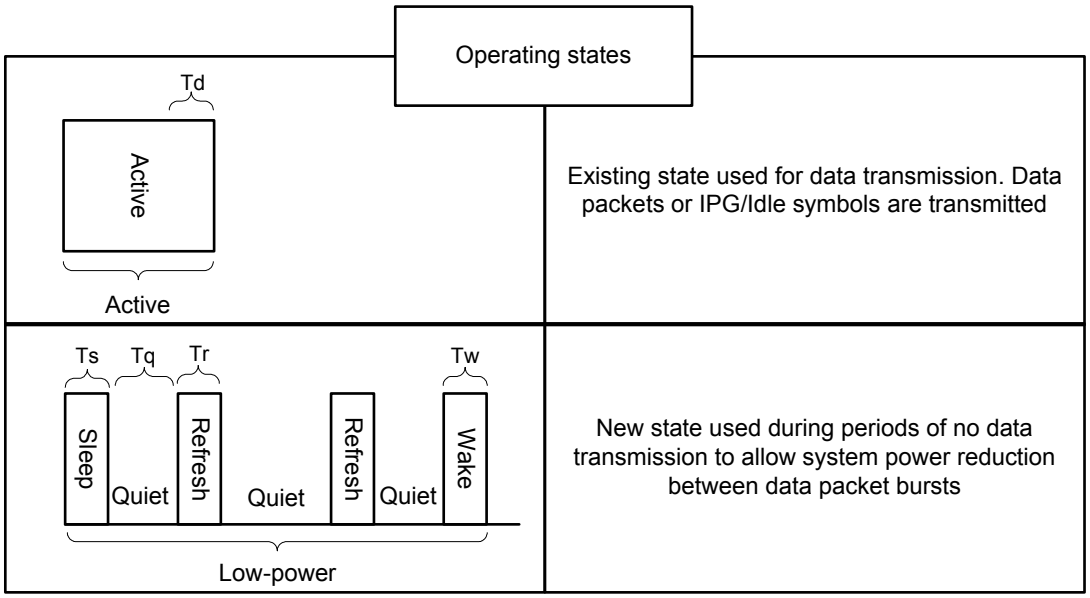
- Active: Act in regular mode for transmitting or receiving data.
- Sleep: Send specific signal to inform remote link partner of entering low-power state.
- Quiet: No signal transmitted on media. Most of the analog and digital blocks are shut down.
- Refresh: Periodically send specific training signal to maintain timing recovery and equalizer coefficients.
- Wake: Send specific wake-up signal to remote link partner to inform of entering Active state.

IEEE 802.3az LPI is supported on 100BASE-TX and 1000BASE-T.

100BASE-TX EEE allows asymmetrical operation that allows Tx or Rx to enter the LPI mode independently.

1000BASE-T EEE requires symmetrical operation that both Tx and Rx must enter the LPI mode simultaneously.

Figure 3-8 shows the IEEE 802.3az operating states for AR8035.




Td: Decision time, higher-layer control policy timing
Ts: Sleep time, Min. duration Sleep symbols sent before going to Quiet
Tq: Quiet duration, Max. duration PHY remains Quiet before Refresh
Tr: Refresh duration, Min. duration HY sends Refresh symbols
Tw: Wake time, Max. period to permit the receiving system to wake up

**Figure 3-8 Operating states — 802.3az LPI mode**

Figure 3-9 shows the IEEE 802.3az operating power modes for AR8035.

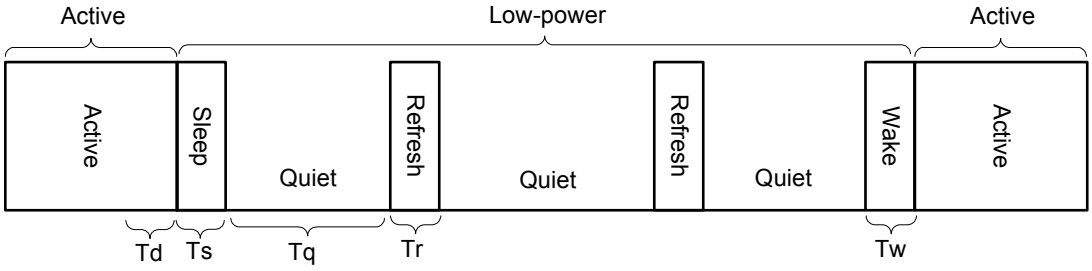



**Figure 3-9 Operating power modes — 802.3az LPI mode**

## 3.10 SmartEEE

Qualcomm Atheros proprietary SmartEEE is compatible with IEEE 802.3az and allows legacy MAC devices (without IEEE 802.az support) into systems providing full IEEE 802.3az support. SmartEEE is enabled by default after power-on or hardware reset.

SmartEEE checks egress data flow at a specific interval to see if any packets being transmitted. If no packet is detected, SmartEEE enters LPI mode. When packets come while the PHY is at LPI mode, AR8035 takes 16.5 µs (typical) to wake up (as defined by IEEE 802.3az) and sends out the

data after the time configured in the register. AR8035 provides internal buffer for caching egress data to ensure no packet loss before wakeup.

In SmartEEE mode, the RGMII Rx direction does not generate LPI pattern, thus only normal packets and idle packets can appear on the RGMII. No Tx LPI pattern is generated for MACs without EEE capability because LPI is generated inside PHY according to SmartEEE mechanism. For MACs with EEE capability, SmartEEE control registers can be set to bypass SmartEEE function MMD3 Register 0x805D[8].

**NOTE**

- For typical application, adjusting the default register setting is not recommended.
- The wait time before entering LPI mode is configured by MMD3 — SmartEEE control 2 register and bits[7:0] LPI_TIMER of MMD3 — SmartEEE control 3 register.
- The wakeup time from LPI mode to sending out data can be configured by MMD3 — SmartEEE control 1 register. This setting is used for collaboration with link partner for customized purpose.

## 3.11 Wake-on-LAN

Wake-on-LAN (WoL) is a mechanism to manage and regulate the total network power consumption. AR8035 supports the following WoL features:

- Supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waken up. The 48-bit MAC address is written in MMD3 0x804A, 0x804B, 0x804C registers.

  For example, to write a specific MAC address (0xAAAABBBBCCCC) to PHY, write MMD3 0x804A = 0xAAAA, 0x804B = 0xBBBB, and 0x804C = 0xCCCC. The PHY internal MAC address can be set to any value.

  **NOTE** The MAC address is not a real MAC address and is only a symbol to indicate the content of the frame.

  Figure 3-10 shows the WoL system application structure.

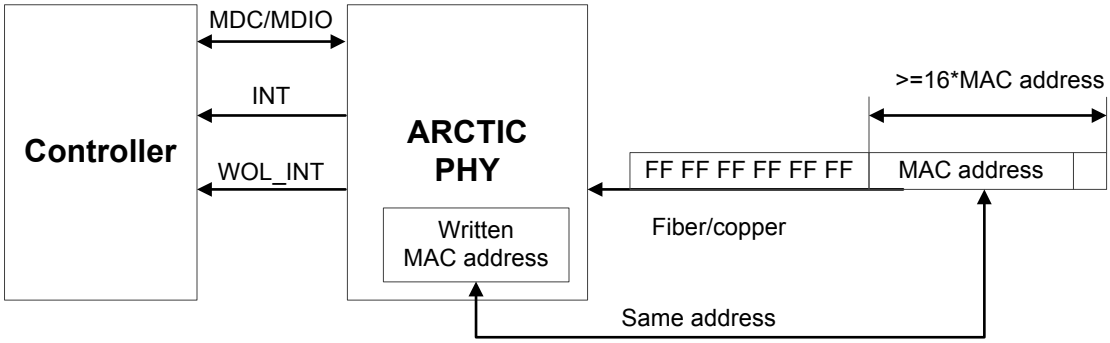



**Figure 3-10 WoL system application structure**

- One hardware pin can be used for triggering WoL interrupt:
  - Active low signal through the INT pin. When the interrupt bit in register 0x12[0] is set to 1, AR8035 generates interrupt at the reception of WoL packet.

When WoL interrupt occurs, the bit[0] INT_WOL_PTP in Interrupt status register (MII Register 0x13) is set to 1. This bit is cleared after read operation.

When the bit[0] INT_WOL_PTP in Interrupt enable register is set to 1, the external INT pin is triggered when interrupt occurs.

**NOTE**

- Because PHY requires to receive packets from the line side, PHY cannot be powered down. If the link partner supports Energy Efficient Ethernet function, both ends can use EEE mode to save more power.
- In LPI mode, the controller can use WoL function to turn off unused circuits to save power. When receiving WoL interrupt from PHY, the controller can wake up to work.
  - Control register (MII Register 0x0)
    - Bit[10] ISOLATE: When this bit is set to 1, the RGMII output pins are tri-stated. The RGMII inputs are ignored. This bit can be used to save more power of PHY in system power saving mode. When receiving WoL packet, this bit is cleared automatically.
- The bit[5] WOL_EN in MMD3 — PTP1588 control register (MMD3 0x8012) is used to enable or disable WoL function.
- Write MMD7 0x801A[13] = 0 to set interrupt active high (by default the value is 1, active low).

# 4 Electrical Characteristics

## 4.1 Absolute maximum ratings

Table 4-1 summarizes the absolute maximum ratings for the AR8035 Ethernet transceiver. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

**Table 4-1 Absolute maximum ratings**

| Symbol | Parameter | Max rating | Unit |
|---|---|---|---|
| VDD33/AVDD33 | 3.3 V supply voltage | 3.8 | V |
| AVDDL | 1.1 V analog supply voltage | 1.6 | V |
| DVDDL | 1.1 V digital core supply voltage | 1.6 | V |
| $T_{store}$ | Storage temperature | -65 to 150 | °C |
| HBM | Electrostatic discharge tolerance — human body model | ±2000 | V |
| MM | Machine model | ±200 | V |
| Vmin | Supply voltage min | -0.3 | V |

## 4.2 Recommended operating conditions

Table 4-2 lists the recommended operating conditions for the AR8035 Ethernet transceiver.

**Table 4-2 Recommended operating conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD33/AVDD33 | 3.3 V supply voltage | 3.15 | 3.3 | 3.45 | V |
| VDDH_REG | 2.5 V analog/digital | 2.4 | 2.62 | 2.75 | V |
| AVDDL/DVDDL | 1.1 V analog/digital with on-chip regulator | 1.04 | 1.1 | 1.17 | V |
| $T_{ambient}$ | Ambient temperature for normal operation — Commercial chip version AR8035-AL1A | 0 | – | 70 | °C |
| | Ambient temperature for normal operation — Industrial chip version AR8035-AL1B | -40 | – | 85 | °C |

**Table 4-2 Recommended operating conditions** (cont.)

| | | | | | |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | -40 | – | 125 | °C |
| $\Psi_{JT}$ | Thermal Dissipation Coefficient | – | 3.8 | – | °C/W |

**NOTE** External regulators are optional for supplying AVDDL/DVDDL. For industrial version, external AVDDL/DVDDL inputs must be within the range of 1.2 V ± 5%. For commercial version, external AVDDL/DVDDL inputs must be within the range of 1.1 V - 5% and 1.2 V + 5%.

**NOTE** The following condition must be satisfied:

$$T_{Jmax} > T_{Cmax} + \Psi_{JT} \times P_{Typical}$$

Where:

$T_{Jmax}$ = Maximum allowable junction temperature

$T_{Cmax}$ = Maximum allowable case temperature

$\Psi_{JT}$ = Thermal dissipation coefficient

$P_{Typical}$ = Typical power dissipation

## 4.3 RGMII characteristics

Table 4-3 shows the RGMII DC characteristics with 2.5/3.3V I/O supply.

**Table 4-3 RGMII DC characteristics — 2.5/3.3V I/O supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $I_{IH}$ | Input high current | – | 15 | µA |
| $I_{IL}$ | Input low current | -15 | – | µA |
| $V_{IH}$ | Input high voltage | 1.7 | 3.5 | V |
| $V_{IL}$ | Input low voltage | GND - 0.3 | 0.7 | V |
| $V_{OH}$ | Output high voltage | 2.4 | 2.8 | V |
| $V_{OL}$ | Output low voltage | GND - 0.3 | 0.4 | V |

Table 4-4 shows the RGMII DC characteristics with 1.8 V I/O supply.

**Table 4-4 RGMII DC characteristics — 1.8V I/O supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.4 | 2.1 | V |
| $V_{IL}$ | Input low voltage | GND - 0.3 | 0.4 | V |

**Table 4-4 RGMII DC characteristics — 1.8V I/O supply** (cont.)

| | | | | |
|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | 1.5 | 1.9 | V |
| $V_{OL}$ | Output low voltage | – | 0.3 | V |

Table 4-5 shows the RGMII DC characteristics with 1.5 V I/O supply.

**Table 4-5 RGMII DC characteristics — 1.5 I/O supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.2 | 1.8 | V |
| $V_{IL}$ | Input low voltage | GND - 0.3 | 0.3 | V |
| $V_{OH}$ | Output high voltage | 1.3 | 1.57 | V |
| $V_{OL}$ | Output low voltage | – | 0.2 | V |

Figure 4-1 shows the RGMII input AC timing diagram.

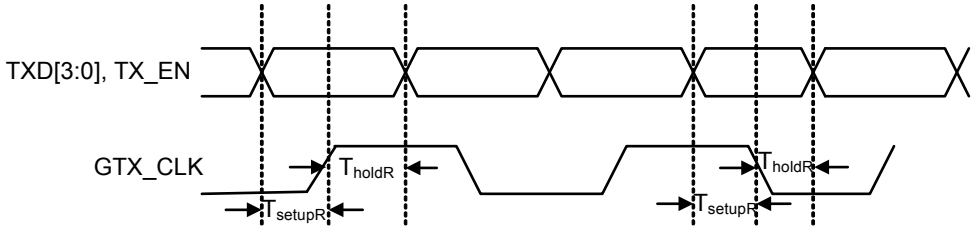



**Figure 4-1 RGMII input timing diagram**

Table 4-6 shows the RGMII input AC characteristics.

**Table 4-6 RGMII AC characteristics — no internal delay**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{setupR}$ | Data to clock input setup time (at receiver) | 1.0 | 2.0 | – | ns |
| $T_{holdR}$ | Data to clock input hold time (at receiver) | 1.0 | 2.0 | – | ns |

1. If the transmitter side (MAC) does not add internal delay or PCB trace delay for GTX_CLK, the input setup and hold time minimum must be within ±0.5 ns. GTX_CLK precise 2.4 ns delay can be added in PHY internal by setting bit[8] RGMII_TX_CLK_DLY = 1 in SerDes test and system mode control register (Debug Register 0x5).
2. For 1000BASE-T, both the rising and falling edges are used to sample the data.
3. For 10BASE-Te/100BASE-TX, only the rising edge is used to sample the data.

RX_CLK hardware reset adds typical 2 ns delay internally by default, so the MAC side has sufficient setup and hold time for sampling. Figure 4-2 shows the RGMII output AC timing with internal delay added diagram.

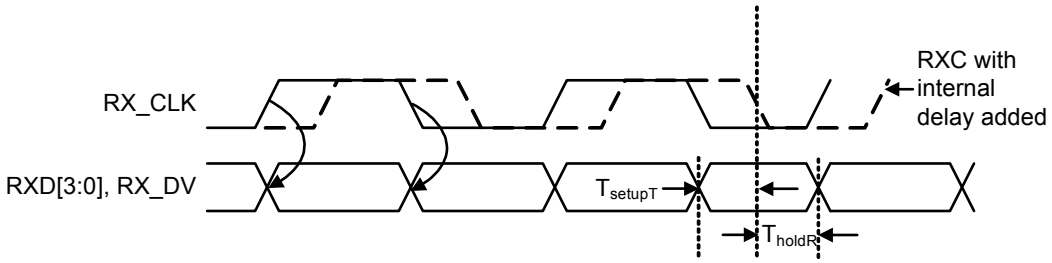



**Figure 4-2 RGMII output AC timing diagram with internal delay added**

Table 4-7 shows the RGMII AC characteristics with delay added.

**Table 4-7 RGMII AC characteristics — with internal delay added (default)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{setupT}$ | Data to clock output setup (at transmitter — integrated delay) | 1.2 | 2.0 | – | ns |
| $T_{holdT}$ | Clock to data output hold (at transmitter — integrated delay) | 1.2 | 2.0 | – | ns |

1. RX_CLK delay can be disabled by setting bit[15] SEL_CLK125M_DSP = 0 in Analog test control register (Debug Register 0x0).
2. If RX_CLK delay is disabled in PHY, the RX_CLK to RXD edge delay is within ±500 ps requiring the MAC side to add internal delay or PCB trace delay.

## 4.4 MDIO timing

Figure 4-3 shows the MDIO AC timing diagram.

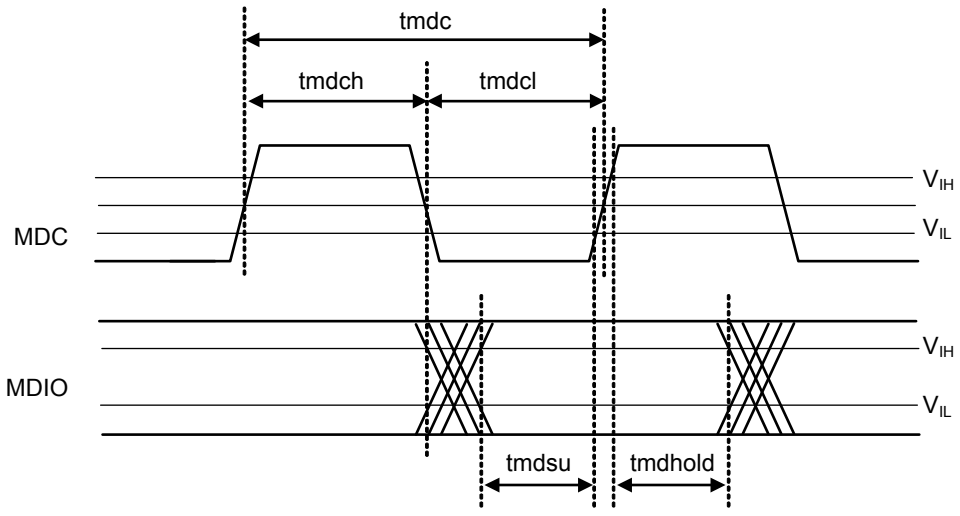



**Figure 4-3 MDIO AC timing diagram**

**Table 4-8 MDIO AC characteristic**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tmdc | MDC period | 40 | – | – | ns |
| tmdcl | MDC low period | 16 | – | – | ns |
| tmdch | MDC high period | 16 | – | – | ns |
| tmdsu | MDIO to MDC rising setup time | 10 | – | – | ns |
| tmdhold | MDIO to MDC rising hold time | 10 | – | – | ns |
| tmdelay | MDC to MDIO output delay | 0 | 4 | – | ns |

## 4.5 MDIO/MDC DC characteristic

**Table 4-9 MDIO/MDC DC characteristic**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | 2.4 | – | V |
| $V_{OL}$ | Output low voltage | – | 0.4 | V |
| $V_{IH}$ | Input high voltage | 1.7 | – | V |
| $V_{IL}$ | Input low voltage | – | 0.7 | V |
| $I_{IH}$ | Input high current | – | 0.4 | mA |
| $I_{IL}$ | Input low current | -0.4 | – | mA |

## 4.6 Clock characteristics

AR8035 supports both crystal and external clock input as reference. The basic principle for selecting crystal and load capacitance is to make the oscillation stable at 25 MHz ± 50 ppm. Crystal with 25 MHz ± 30 ppm frequency tolerance is preferred with two 27 pF NPO ceramic capacitors. The capacitors can be changed according to actual crystal selection and board level test results under full application temperature and voltage ranges.

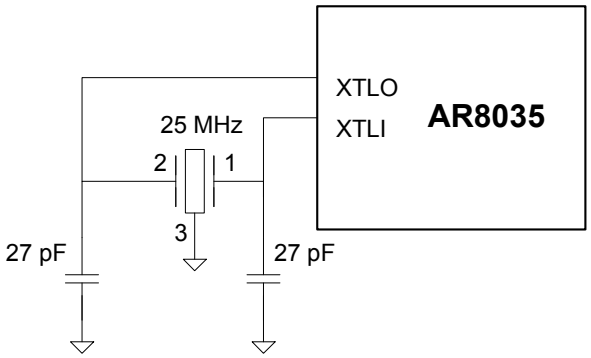



**Figure 4-4 External crystal**

**Table 4-10 Recommended crystal parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ff | Crystal fundamental frequency | – | 25 | – | MHz |
| Ft | Frequency tolerance | -30ppm | – | +30ppm | MHz |
| Cs | Shunt capacitance | – | 7 | – | pF |
| Cl | Load capacitance | – | 15 | – | pF |
| Vo | I/O voltage level (for drive level evaluation) | – | 1.2 | – | V |
| DL | Drive level | – | 300 | – | µW |
| ESR | Equivalent series resistance | – | 30 | 50 | Ω |

**Table 4-11 External clock input characteristic**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T_XI_PER | XI Clock Period | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns |
| T_XI_HI | XI Clock High | 14 | 20.0 | – | ns |
| T_XI_LO | XI Clock Low | 14 | 20.0 | – | ns |
| T_XI_RISE | XI Clock Rise Time, VIL (max) to VIH (min) | – | – | 4 | ns |
| T_XI_FALL | XI Clock Fall time, VIL (max) TO VIH (min) | – | – | 4 | ns |
| V_IH_XI | The XI input high level | 0.8 | 1.2 | 1.5 | V |
| V_IL_XI | The XI input low level voltage | -0.3 | 0 | 0.15 | V |
| $C_{IN}$ | Load capacitance | – | 1 | 2 | pF |
| $Jitter_{RMS}$ | Period broadband RMS jitter | – | – | 15 | ps |
| $Jitter_{pk-pk}$ | Period broadband peak to peak jitter | – | – | 100 | ps |

**Table 4-12 CLK_25M output characteristics**

| Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency | -50ppm | 25, 50, 62.5, 125 | +50ppm | MHz |
| Output high voltage | 2.3 | 2.62 | 2.8 | V |
| Output low voltage | GND - 0.3 | – | 0.4 | V |
| Clock period jitter (peak-to-peak)[1)] | – | 680 | – | ps |
| Clock cycle to cycle period jitter (peak-to-peak)[1)] | – | 400 | – | ps |

1. Jitter characteristics is for 125 MHz output.
2. Jitter is broadband period jitter with 1000000 samples.
3. Output frequency stability depends on the crystal circuit oscillation frequency or input clock frequency stability.
4. If CLK_25M is not used, it can be left floated. If it is used, external 22 Ω serial resistor is required for signal integrity.
5. If it is used as a chip reference clock, pay attention to the input requirement, especially the jitter. For reliable application such as Giga switch/PHY reference clock, a jitter attenuation circuit is required.

## 4.7 Power pin current consumption

Table 4-13 shows the current consumption for the power pins.

**Table 4-13 Power pin consumption**

| Symbol | Voltage range | Current (max) |
|---|---|---|
| AVDDL | 1.1 V ± 5% | 50.8 mA |
| DVDDL | 1.1 V ± 5% | 113.7 mA |
| AVDD33 | 3.3 V ± 5% | 63.8 mA |
| VDDIO_REG | Connect VDDH_REG 2.5 V | 20.9 mA |

## 4.8 Typical power consumption parameters

The following conditions apply to the typical characteristics unless otherwise specified:

VCC = 3.3 V (1.1 V switching regulator integrated and 50 mW RGMII power included).

**Table 4-14 Total system power**

| Symbol | Condition | Total current (mA) | LED consumption (mA) | Total power consumption without LED (mW) |
|---|---|---|---|---|
| $P_{LDPS}$ | Link down, power saving mode | 3 | 0 | 9.9 |
| $P_{PWD}$ | Power down mode | 2.5 | 0 | 8.25 |
| $P_{1000F}$ | 1000BASE-T full-duplex line speed | 119 | 2.7 | 392.7 |
| $P_{1000idle}$ | 1000BASE-T idle | 109 | 4 | 359.5 |

**Table 4-14 Total system power** (cont.)

| Symbol | Condition | Total current (mA) | LED consumption (mA) | Total power consumption without LED (mW) |
|---|---|---|---|---|
| $P_{100F}$ | 100BASE-TX full-duplex line speed | 33.9 | 3.5 | 111.9 |
| $P_{100idle}$ | 100BASE-TX idle | 32.6 | 4 | 107.6 |
| $P_{10F}$ | 10BASE-Te full-duplex line speed | 31.5 | 1 | 104.0 |
| $P_{10idle}$ | 10BASE-Te idle | 9.4 | 1.5 | 31.0 |
| ***802.az enabled*** | | | | |
| $P_{1000idle}$ | 1000BASE-T idle | 20.0 | 4 | 66.0 |
| $P_{100idle}$ | 100BASE-TX idle | 14.7 | 4 | 48.5 |
| ***Qualcomm Atheros Proprietary Green ETHOS® Power Savings Per Cable Length*** | | | | |
| $P_{1000F\ 20m}$ | 1000BASE-T full-duplex 20m cable | 92 | 2.7 | 303.6 |
| $P_{1000idle\ 20m}$ | 1000BASE-T idle 20m cable | 85 | 4 | 280.5 |
| $P_{1000F\ 100m}$ | 1000BASE-T full-duplex 100m cable | 119 | 2.7 | 392.7 |
| $P_{1000idle\ 100m}$ | 1000BASE-T idle 100m cable | 109 | 4 | 359.7 |
| $P_{1000F\ 140m}$ | 1000BASE-T full-duplex 140m cable | 137 | 2.7 | 452.1 |
| $P_{1000idle\ 140m}$ | 1000BASE-T idle 140m cable | 128 | 4 | 422.4 |

**NOTE** Power consumption test results are based on the demo board.

# 4.9 Power-on sequence, reset and clock

## 4.9.1 Power-on sequence

AR8035 only requires a single 3.3 V power supply input. The 1.1 V core and 2.5 V, 1.8/1.5 V voltages are generated by AR8035 internal regulators. So the AR8035 power-on sequence to establish the power rails stability is met internally.

## 4.9.2 Reset and clock timing

The AR8035 hardware reset requires the clock to take effect. Input clock including the crystal and external input clock must be stable for at least 1 ms before RESET can be de-asserted. For chip reliability, an external clock must be input after the power-on sequence.

Figure 4-5 shows the reset timing diagram.

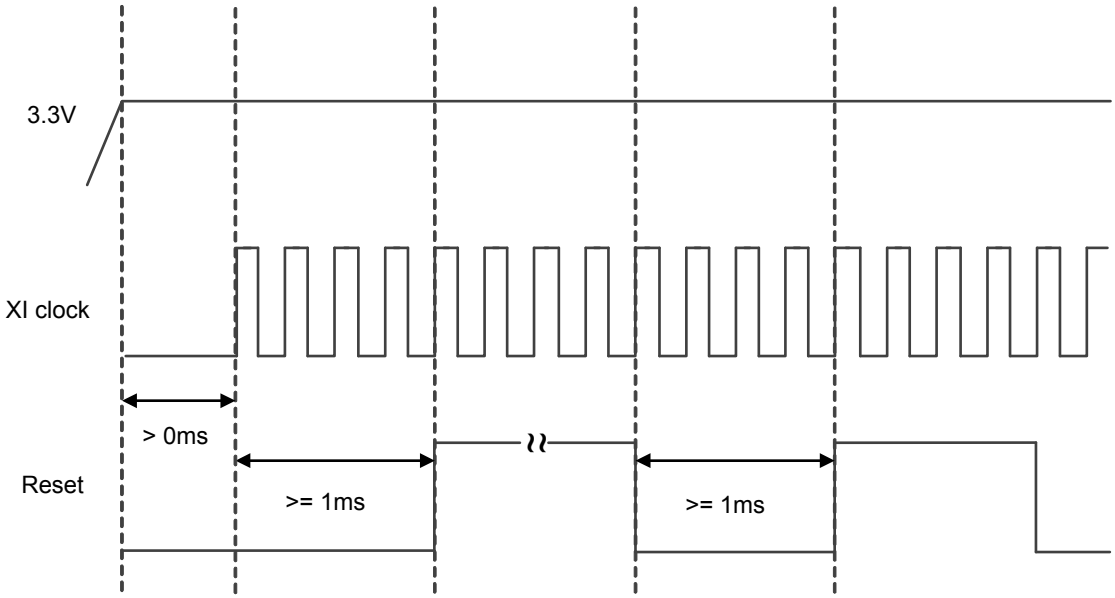



**Figure 4-5 Reset timing diagram**

**NOTE** When using crystal, clock is generated internally after the power is stable. To get reliable power-on reset, keep asserting the reset low signal long enough to ensure that the clock is stable and clock-to-reset (1 ms) requirement is satisfied.

## 4.10 Digital pin design guide

**Table 4-15 Digital pin designs**

| Pin type | Pin description | Reset asserted | Reset de-asserted (Normal working level) |
|---|---|---|---|
| Input | TXD[3:0]<br>TX_EN<br>GTX_CLK | Input, internal weak PD | Input, based on RGMII I/O voltage level set |
| I/O | RXD[3:0]<br>RX_DV<br>RX_CLK | Input, internal weak PD | Output, based on RGMII I/O voltage level set |
| I/O | LED_1000<br>LED_ACT<br>LED_10_100 | Input, internal weak PU | Output, 2.5 V (VDDH_REG) |
| Input | MDC | Input, internal weak PU | Input, 2.5 V (3.3 V tolerant) |
| I/O | MDIO | Input, internal weak PU | I/O, 2.5 V (3.3 V tolerant) |
| Input | RSTn | Input, no weak PU | Input, 2.5 V (3.3 V tolerant) |

**Table 4-15 Digital pin designs** (cont.)

| Pin type | Pin description | Reset asserted | Reset de-asserted (Normal working level) |
|---|---|---|---|
| Output | INT | Output, kept driving low | Open drain output (default), based on external PU voltage level |

1. When MDC/MDIO/RESET acts as an input, $V_{IH}$ min is 1.7 V, $V_{IL}$ max is 0.7 V, thus the chip supports 2.5/3.3 V LVTTL/LVCMOS level signal input.
2. Power-on strapping pins are input when reset is asserted. They are output during normal operation. External pull-up to VDDIO_REG for RGMII signal, and to 2.5 V (VDDH_REG) for LED are recommended.
3. RESET and MDIO can be pulled up to 2.5 V (VDDH_REG) or 3.3 V.

# 5 Registers

Three types of registers are present on AR8035:

- IEEE defined 32 MII registers, referred to as “MII Registers” in this document
  - MII registers are accessed directly through the management frame.
- Debug registers defined by Qualcomm Atheros, referred to as “Debug Registers” in this document
  - Write the offset address of debug register to 0x1D.
  - Read/write the data from/to 0x1E.
- IEEE defined MDIO Manageable Device (MMD) register, referred to as “MDIO Interface (MMD3/MMD7) Registers” in this document
  - MMD registers are accessed by reading/writing MMD access control register (MII register 0xD) and MMD access data register (MII register 0xE).

**Example: Writing 0x8000 to register 0x0 of MMD3**

1. Write 0x3 to MII register 0xD to set the device address of the MMD register.
2. Write 0x0 to MII register 0xE to set the offset address of the MMD register.
3. Write 0x4003 to MII register 0xD to keep the device address.
4. Read MII register 0xE to check the data from register 0x0 of MMD3.
5. Write 0x8000 to MII register 0xE, that is register 0x0 of MMD3.

**NOTE** Read operation follows the process 1 to 4.

## 5.1 Register bit type

Table 5-1 shows the register bit types.

**Table 5-1 Register bit types**

| Type | Description |
|---|---|
| LH | Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs. |
| LL | Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs. |

**Table 5-1 Register bit types** (cont.)

| Type | Description |
|---|---|
| Retain | Value written to a register field takes effect without a software reset. |
| SC | Self-clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete. |
| Update | The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written. |

# 5.2 MII registers

**Table 5-2 Register summary**

| Offset | Register |
|---|---|
| 0x00 | “Control register” on page 46 |
| 0x01 | “Status register” on page 47 |
| 0x02 | “PHY identifier 1 register” on page 49 |
| 0x03 | “PHY identifier 2 register” on page 49 |
| 0x04 | “Auto-negotiation advertisement register” on page 50 |
| 0x05 | “Auto-negotiation link partner ability register” on page 52 |
| 0x06 | “Auto-negotiation expansion register” on page 54 |
| 0x07 | “Auto-negotiation next page transmit register” on page 54 |
| 0x08 | “Auto-negotiation link partner next page register” on page 55 |
| 0x09 | “1000BASE-T control register” on page 56 |
| 0x0A | “1000BASE-T status register” on page 58 |
| 0x0B | Reserved |
| 0x0C | Reserved |
| 0x0D | “MMD access control register” on page 59 |
| 0x0E | “MMD access data register” on page 59 |
| 0x0F | “Extended status register” on page 59 |
| 0x10 | “PHY specific function control register” on page 60 |
| 0x11 | “PHY specific status register” on page 61 |
| 0x12 | “Interrupt enable register” on page 63 |
| 0x13 | “Interrupt status register” on page 64 |
| 0x14 | “Smart speed register” on page 65 |
| 0x15 | Reserved |
| 0x16 | “Cable diagnostic test control register” on page 66 |
| 0x17 | Reserved |
| 0x18 | “LED control register” on page 67 |

**Table 5-2 Register summary** (cont.)

| Offset | Register |
|---|---|
| 0x19 | “Manual LED override register” on page 68 |
| 0x1A | Reserved |
| 0x1B | “Cable diagnostic test status register” on page 69 |
| 0x1C | “Cable diagnostic test status register” on page 69 |
| 0x1D | “Debug port — address offset register” on page 69 |
| 0x1E | “Debug port — dataport register” on page 70 |
| 0x1F | “Debug registers” on page 70 |
| For typical application, poll the PHY specific status register to get link/speed/duplex information and then configure MAC before sending and receiving packets. | |

## 5.2.1 Control register

Offset: 0x00

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | RESET | Mode | R/W | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. When the operation is done, this bit is cleared automatically.<br>1 = PHY reset<br>0 = Normal operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | SC | |
| 14 | LOOPBACK | Mode | R/W | When loopback is activated, the transmitter data on TXD is looped back to RXD internally.<br>1 = Enable loopback<br>0 = Disable loopback |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | SPEED SELECTION (LSB) | Mode | R/W | Force speed = {bit[6] SPEED SELECTION (MSB), bit[13] SPEED SELECTION (LSB)}<br>00 = 10 Mbps<br>01 = 100 Mbps<br>10 = 1000 Mbps<br>11 = Reserved |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 12 | AUTO-NEGOTIATION | Mode | R/W | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 11 | POWER DOWN | Mode | R/W | When the port is switched from power down to normal operation, software reset and restart Auto-negotiation are performed even when bit[15] RESET and bit[9] RESTART AUTO-NEGOTIATION are not set.<br>1 = Power-down<br>0 = Normal operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 10 | ISOLATE | Mode | R/W | The RGMII output pins are tri-stated when this bit is 1. The RGMII inputs are ignored.<br>1 = Isolate<br>0 = Normal operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9 | RESTART AUTO-NEGOTIATION | Mode | R/W, SC | Auto-negotiation automatically restarts after hardware or software reset regardless of whether this bit is set or not.<br>1 = Restart auto-negotiation process<br>0 = Normal operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | DUPLEX MODE | Mode | R/W | 1 = Full-duplex<br>0 = Half-duplex |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 7 | COLLISION TEST | Mode | R/W | Setting this bit to 1 asserts the COL pin whenever the TX_EN pin is asserted.<br>1 = Enable COL signal test<br>0 = Disable COL signal test |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 6 | SPEED SELECTION (MSB) | Mode | R/W | See bit[13] SPEED SELECTION (LSB) |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 5:0 | RESERVED | Mode | R/O | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.2 Status register

Offset: 0x01

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | 100BASE-T4 | Mode | RO | 100BASE-T4<br>Always 0<br>This protocol is not available.<br>1 = PHY supports 100BASE-T4.<br>0 = PHY does not support 100BASE-T4. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | 100BASE-TX FULL-DUPLEX | Mode | RO | Always 1<br>1 = PHY supports 100BASE-TX full-duplex.<br>0 = PHY does not support 100BASE-TX full-duplex. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 13 | 100BASE-TX HALF-DUPLEX | Mode | RO | Always 1<br>1 = PHY supports 100BASE-TX half-duplex.<br>0 = PHY does not support 100BASE-TX half-duplex. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 12 | 10BASE-T FULL-DUPLEX | Mode | RO | Always 1<br>1 = PHY supports 10BASE-T full-duplex.<br>0 = PHY does not support 10BASE-T full-duplex. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 11 | 10BASE-T HALF-DUPLEX | Mode | RO | Always 1<br>1 = PHY supports 10BASE-T half-duplex.<br>0 = PHY does not support 10BASE-T half-duplex. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 10 | 100BASE-T2 FULL-DUPLEX | Mode | RO | Always 0<br>1 = PHY supports 100BASE-T2.<br>0 = PHY does not support 100BASE-T2. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9 | 100BASE-T2 HALF-DUPLEX | Mode | RO | Always 0<br>1 = PHY supports 100BASE-T2.<br>0 = PHY does not support 100BASE-T2. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | EXTENDED STATUS | Mode | RO | Always 1<br>Extended status information in Extended status register |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 7 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 6 | MF PREAMBLE SUPPRESSION | Mode | RO | Always 1<br>1 = PHY accepts management frames with preamble suppressed.<br>0 = PHY does not accept management frames with preamble suppressed. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 5 | AUTO-NEGOTIATION COMPLETE | Mode | RO | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 4 | REMOTE FAULT | Mode | RO, LH | 1 = Remote fault condition detected<br>0 = Remote fault condition not detected |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 3 | AUTO-NEGOTIATION ABILITY | Mode | RO | 1 = PHY supports auto-negotiation.<br>0 = PHY does not support auto-negotiation. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 2 | LINK STATUS | Mode | RO, LL | This bit indicates whether the link was lost since the last read. For the current link status, see bit[10] LINK (REAL-TIME) of register PHY specific status register.<br>1 = Link is up<br>0 = Link is down |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 1 | JABBER DETECT | Mode | RO, LH | 1 = Jabber condition detected<br>0 = Jabber condition not detected |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 0 | EXTENDED CAPABILITY | Mode | RO | Always 1<br>1 = Extended register capabilities |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

### 5.2.3 PHY identifier 1 register

Offset: 0x02

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | ORGANIZATIONALLY UNIQUE IDENTIFIER BIT 3:18 | Mode | RO | Always 0x004D<br>Organizationally unique identifier bits[18:3] |
| | | HW Rst. | 0x004D | |
| | | SW Rst. | 0x004D | |

### 5.2.4 PHY identifier 2 register

Offset: 0x03

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | ORGANIZATIONALLY UNIQUE IDENTIFIER LSB. MODEL NUMBER REVISION NUMBER | Mode | RO | Always 0xD072<br>Organizationally unique identifier bits[19:24] |
| | | HW Rst. | 0xD072 | |
| | | SW Rst. | 0xD072 | |

## 5.2.5 Auto-negotiation advertisement register

Offset: 0x04

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | NEXT PAGE | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>If 1000BASE-T is advertised, the required next pages are automatically transmitted. Bit[15] NEXT PAGE of Auto-negotiation advertisement register must be set to 0 if no additional next pages are required.<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 14 | ACK | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | REMOTE FAULT | Mode | R/W | 1 = Set Remote Fault bit<br>0 = Do not set Remote Fault bit |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 12 | XNP_ABLE | Mode | R/W | Extended next page enable control bit:<br>1 = Local device supports transmission of extended next pages.<br>0 = Local device does not support transmission of extended next pages. |
| | | HW Rst. | Always 1 | |
| | | SW Rst. | Retain | |
| 11 | ASYMMETRIC PAUSE | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Asymmetric pause<br>0 = No asymmetric pause |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 10 | PAUSE | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = MAC PAUSE implemented<br>0 = MAC PAUSE not implemented |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 9 | 100BASE-T4 | Mode | RO | Always 0<br>1 = PHY supports 100BASE-T4.<br>0 = PHY does not support 100BASE-T4. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | 100BASE-TX FULL DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 7 | 100BASE-TX HALF DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 6 | 10BASE-T FULL DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 5 | 10BASE-T HALF DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 4:0 | SELECTOR FIELD | Mode | RO | Selector field mode<br>Always 1<br>1 = IEEE 802.3 |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

## 5.2.6 Auto-negotiation link partner ability register

Offset: 0x05

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | NEXT PAGE | Mode | RO | Received code word bit[15]<br>1 = Link partner supports Next Page<br>0 = Link partner does not support Next Page |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | ACK | Mode | RO | Acknowledge<br>Received code word bit[14]<br>1 = Link partner successfully received link code word<br>0 = Link partner failed to receive link code word |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 13 | REMOTE FAULT | Mode | RO | Remote fault<br>Received code word bit[13]<br>1 = Link partner detects remote fault<br>0 = Link partner does not detect remote fault |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 12 | RESERVED | Mode | RO | Technology ability field<br>Received code word bit[12] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 11 | ASYMMETRIC PAUSE | Mode | RO | Technology ability field<br>Received code word bit[11]<br>1 = Link partner requests asymmetric pause<br>0 = Link partner does not request asymmetric pause |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10 | PAUSE | Mode | RO | Technology ability field<br>Received code word bit[10]<br>1 = Link partner supports pause operation<br>0 = Link partner does not support pause operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9 | 100BASE-T4 | Mode | RO | Technology ability field<br>Received code word bit[9]<br>1 = Link partner supports 100BASE-T4<br>0 = Link partner does not support 100BASE-T4 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | 100BASE-TX FULL DUPLEX | Mode | RO | Technology ability field<br>Received code word bit[8]<br>1 = Link partner supports 100BASE-TX full-duplex<br>0 = Link partner does not support 100BASE-TX full-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7 | 100BASE-TX HALF DUPLEX | Mode | RO | Technology ability field<br>Received code word bit[7]<br>1 = Link partner supports 100BASE-TX half-duplex<br>0 = Link partner does not support 100BASE-TX half-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 6 | 10BASE-T FULL DUPLEX | Mode | RO | Technology ability field<br>Received code word bit[6]<br>1 = Link partner support 10BASE-T full-duplex<br>0 = Link partner does not support 10BASE-T full-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 5 | 10BASE-T HALF DUPLEX | Mode | RO | Technology ability field<br>Received code word bit[5]<br>1 = Link partner supports 10BASE-T half-duplex<br>0 = Link partner does not support 10BASE-T half-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 4:0 | SELECTOR FIELD | Mode | RO | Selector field<br>Received code word bit[4:0] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.7 Auto-negotiation expansion register

Offset: 0x06

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:5 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 4 | PARALLEL DETECTION FAULT | Mode | RO | 1 = A fault is detected<br>0 = No fault is detected |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 3 | LINK PARTNER NEXT PAGE ABLE | Mode | RO | 1 = Link partner supports Next Page<br>0 = Link partner does not support Next Page |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 2 | LOCAL NEXT PAGE ABLE | Mode | RO | 1 = Local device supports Next Page<br>0 = Local device does not support Next Page |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 1 | PAGE RECEIVED | Mode | RO, LH | 1 = A new page is received<br>0 = No new page is received |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 0 | LINK PARTNER AUTO-NEGOTIATION ABLE | Mode | RO | 1 = Link partner supports auto-negotiation<br>0 = Link partner does not support auto-negotiation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.8 Auto-negotiation next page transmit register

Offset: 0x07

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | NEXT PAGE | Mode | R/W | Transmit code word bit[15] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | RESERVED | Mode | R/W | Transmit code word bit[14] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | MESSAGE PAGE MODE | Mode | R/W | Transmit code word bit[13] |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 12 | ACK2 | Mode | R/W | Transmit code word bit[12] |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 11 | TOGGLE | Mode | RO | Transmit code word bit[11] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10:0 | MESSAGE/UNFORMATTED FIELD | Mode | R/W | Transmit code word bits[10:0] |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

## 5.2.9 Auto-negotiation link partner next page register

Offset: 0x08

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | NEXT PAGE | Mode | RO | Received code word bit[15] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | RESERVED | Mode | RO | Received code word bit[14] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | MESSAGE PAGE MODE | Mode | RO | Received code word bit[13] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 12 | ACK2 | Mode | RO | Received code word bit[12] |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 11 | TOGGLE | Mode | RO | Received code word bit[11] |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 10:0 | MESSAGE/UNFORMATTED FIELD | Mode | RO | Received code word bits[10:0] |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.10 1000BASE-T control register

Offset: 0x09

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:13 | TEST MODE | Mode | R/W | After exiting the test mode, hardware reset or software reset (bit[15] RESET of Control register) must be issued to ensure normal operation.<br>000 = Normal Mode<br>001 = Test mode 1 – Transmit waveform test<br>010 = Test mode 2 – Transmit jitter test (master mode)<br>011 = Test mode 3 – Transmit jitter test (slave mode)<br>100 = Test mode 4 – Transmit distortion test<br>101, 110, 111 = Reserved |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 12 | MASTER/SLAVE MANUAL CONFIGURATION ENABLE | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART_AUTO_NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER_DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Manual master/slave configuration<br>0 = Automatic master/slave configuration |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 11 | MASTER/SLAVE CONFIGURATION | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART_AUTO_NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER_DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>Bit[11] MASTER/SLAVE CONFIGURATION is ignored if bit[12] MASTER/SLAVE MANUAL CONFIGURATION ENABLE = 0.<br>1 = Manual configure as master<br>0 = Manual configure as slave |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 10 | PORT TYPE | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART_AUTO_NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER_DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>Bit[10] PORT TYPE is ignored if bit[12] MASTER/SLAVE MANUAL CONFIGURATION ENABLE = 1.<br>1 = Prefer multi-port device (master)<br>0 = Prefer single-port device (slave) |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 9 | 1000BASE-T FULL DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART_AUTO_NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER_DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 8 | 1000BASE-T HALF-DUPLEX | Mode | R/W | The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART_AUTO_NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER_DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down<br>1 = Advertise<br>0 = Not advertised<br>Note: The 1000BASE-T/half-duplex is not advertised by default. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 7:0 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.11 1000BASE-T status register

Offset: 0x0A

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | MASTER/SLAVE CONFIGURATION FAULT | Mode | RO, LH | This bit is cleared on a read operation.<br>1 = Master/Slave configuration fault detected<br>0 = No fault detected |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | MASTER/SLAVE CONFIGURATION RESOLUTION | Mode | RO | This bit is valid only when bit[1] PAGE RECEIVED of Auto-negotiation expansion register = 1.<br>1 = Local PHY configuration resolved to master<br>0 = Local PHY configuration resolved to slave |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | LOCAL RECEIVER STATUS | Mode | RO | 1 = Local receiver OK<br>0 = Local receiver not OK |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 12 | REMOTE RECEIVER STATUS | Mode | RO | 1 = Remote receiver OK<br>0 = Remote receiver not OK |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 11 | LINK PARTNER 1000 BASE-T FULL DUPLEX CAPABILITY | Mode | RO | This bit is valid only when bit[1] PAGE RECEIVED of Auto-negotiation expansion register = 1.<br>1 = Link partner supports 1000BASE-T full-duplex<br>0 = Link partner does not support 1000BASE-T full-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10 | LINK PARTNER 1000 BASE-T HALF DUPLEX CAPABILITY | Mode | R/W | This bit is valid only when bit[1] PAGE RECEIVED of Auto-negotiation expansion register = 1.<br>1 = Link partner supports 1000 BASE-T half-duplex<br>0 = Link partner does not support 1000 BASE-T half-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9:8 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7:0 | IDLE ERROR COUNT | Mode | RO, SC | MSB of idle error counter<br>Report the idle error count since the last time this register was read. The counter counts up to 11111111 and does roll over. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.12 MMD access control register

Offset: 0x0D

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:14 | FUNCTION | Mode | R/W | 00 = Address<br>01 = Data, no post increment<br>10 = Data, post increment on read and write operations<br>11 = Data, post increment on write operation only |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13:5 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 4:0 | DEVAD | Mode | R/W | Device address |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |

## 5.2.13 MMD access data register

Offset: 0x0E

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:14 | ADDRESS DATA | Mode | R/W | If bits[15:14] FUNCTION = 00 in MMD access control register, MMD DEVAD is address register.<br>Otherwise, MMD DEVAD is data register indicated by the contents of its address register.<br>See “MII registers” on page 45 for detailed information of accessing MMD registers. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 13:0 | RESERVED | – | | – |

## 5.2.14 Extended status register

Offset: 0x0F

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | RESERVED | Mode | RO | Always 1 |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 14 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 13 | 1000BASE-T FULL-DUPLEX | Mode | RO | Always 1<br>1 = PHY supports 1000BASE-T full-duplex.<br>0 = PHY does not support 1000BASE-T full-duplex. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 12 | 1000BASE-T HALF-DUPLEX | Mode | R/W | Always 0<br>1 = PHY supports 1000BASE-T half-duplex.<br>0 = PHY does not support 1000BASE-T half-duplex. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 11:0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.15 PHY specific function control register

Offset: 0x10

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:12 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 11 | ASSERT CRS ON TRANSMIT | Mode | R/W | This bit is valid only in 10BASE-T half-duplex mode:<br>1 = Assert on Transmitting or receiving<br>0 = Never assert on transmitting, only assert on receiving |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 10 | FORCE_LINK | Mode | R/W | 1 = When bit[12] AUTO-NEGOTIATION of Control register = 1, force 10BASE-T link up<br>0 = Normal mode |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 9:7 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 6:5 | MDI CROSSOVER MODE | Mode | R/W | Changes to these bits are disruptive to the normal operation, therefore any changes to these registers must be followed by a software reset to take effect.<br>00 = Manual MDI configuration<br>01 = Manual MDIX configuration<br>10 = Reserved<br>11 = Enable automatic crossover for all modes |
| | | HW Rst. | 11 | |
| | | SW Rst. | Update | |
| 4:3 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 2 | SQE TEST | Mode | R/W | SQE Test is automatically disabled in full-duplex mode regardless of the state of this bit.<br>1 = SQE test enabled<br>0 = SQE test disabled |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 1 | POLARITY REVERSAL | Mode | R/W | If polarity is disabled, the polarity is forced to be normal in 10BASE-T.<br>1 = Polarity auto reversal enabled:<br>To set this bit to 1, write 0.<br>To set this bit to 0, write 1.<br>0 = Polarity auto reversal disabled. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 0 | DISABLE JABBER | Mode | RO | Jabber is available in 10BASE-T half-duplex mode only.<br>1 = Disable jabber function<br>0 = Enable jabber function |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.16 PHY specific status register

Offset: 0x11

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:14 | SPEED | Mode | RO | These status bits are valid only when bit[11] SPEED AND DUPLEX RESOLVED = 1. Bit[11] is set when Auto-negotiation is completed or Auto-negotiation is disabled.<br>11 = Reserved<br>10 = 1000 Mbps<br>01 = 100 Mbps<br>00 = 10 Mbps |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 13 | DUPLEX | Mode | RO | This status bit is valid only when bit[11] SPEED AND DUPLEX RESOLVED = 1. Bit[11] is set when Auto-negotiation is completed or Auto-negotiation is disabled.<br>1 = Full-duplex<br>0 = Half-duplex |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 12 | PAGE RECEIVED (REAL-TIME) | Mode | RO | 1 = Page received<br>0 = Page not received |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 11 | SPEED AND DUPLEX RESOLVED | Mode | RO | When Auto-negotiation is not enabled, set this bit = 1 for force speed mode.<br>1 = Resolved<br>0 = Not resolved |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10 | LINK (REAL-TIME) | Mode | RO | 1 = Link up<br>0 = Link down |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 9:7 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 6 | MDI CROSSOVER STATUS | Mode | RO | This status bit is valid only when bit[11] SPEED AND DUPLEX RESOLVED = 1. Bit[11] is set when Auto-Negotiation is completed or Auto-negotiation is disabled.<br>The value of this bit depends on what is written to bits[6:5] MDI CROSSOVER MODE of PHY specific function control register in manual configuration mode. Bits[6:5] MDI CROSSOVER MODE of PHY specific function control register are updated with software reset.<br>1 = MDIX<br>0 = MDI |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 5 | WIRESPEED DOWNGRADE | Mode | RO | When Smartspeed function is enable:<br>1 = Downgrade<br>0 = No Downgrade |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 4 | RESERVED | Mode | RO | – |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 3 | TRANSMIT PAUSE ENABLED | Mode | RO | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device.<br>This status bit is valid only when bit[11] SPEED AND DUPLEX RESOLVED = 1. Bit[11] is set when Auto-negotiation is completed; while in force mode, this bit is set to 0.<br>1 = Transmit pause enabled<br>0 = Transmit pause disabled |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 2 | RECEIVE PAUSE ENABLED | Mode | RO | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device.<br>This status bit is valid only when bit[11] SPEED AND DUPLEX RESOLVED = 1. Bit[11] is set when Auto-negotiation is completed; while in force mode, this bit is set to 0.<br>1 = Receive pause enabled<br>0 = Receive pause disabled |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 1 | POLARITY (REAL-TIME) | Mode | RO | 1 = Reverted.<br>0 = Normal |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 0 | JABBER (REAL-TIME) | Mode | RO | 1 = Jabber<br>0 = No jabber |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.17 Interrupt enable register

Offset: 0x12

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | AUTO-NEGOTIATION ERROR | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14 | SPEED CHANGED | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 13 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 12 | PAGE RECEIVED | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 11 | LINK FAIL INTERRUPT | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 10 | LINK SUCCESS INTERRUPT | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 9 | FAST LINK DOWN[1] | Mode | R/W | 1 = Interrupt enable, must be enabled with bit[6] FAST LINK DOWN[0] together<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 8 | LINK_FAIL_BX | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 7 | LINK_SUCCESS_BX | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 6 | FAST LINK DOWN[0] | Mode | R/W | Must be enabled together with bit[9] FAST LINK DOWN[1]<br>1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 5 | WIRESPEED-DOWNGRADE INTERRUPT | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 4 | INT_10MS_PTP | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 3 | INT_RX_PTP | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 2 | INT_TX_PTP | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 1 | POLARITY CHANGED | Mode | R/W | 1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 0 | INT_WOL_PTP | Mode | R/W | Wake-on-LAN interrupt<br>1 = Interrupt enable<br>0 = Interrupt disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.18 Interrupt status register

Offset: 0x13

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | AUTO-NEGOTIATION ERROR | Mode | RO, LH | An error can occur if either MASTER/SLAVE does not resolve, or no common HCD, or link does not come up after negotiation is completed.<br>1 = Auto-negotiation error<br>0 = No auto-negotiation error |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14 | SPEED CHANGED | Mode | RO, LH | 1 = Speed changed<br>0 = Speed unchanged |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 13 | RESERVED | Mode | RO, LH | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 12 | PAGE RECEIVED | Mode | RO, LH | 1 = Page received<br>0 = Page not received |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 11 | LINK FAIL INTERRUPT | Mode | RO, LH | 1 = BASE-T Link down occurs.<br>0 = No link is down. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 10 | LINK SUCCESS INTERRUPT | Mode | RO, LH | 1 = BASE-T Link up occurs.<br>0 = No link is up. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 9 | FAST LINK DOWN[1] | Mode | RO, LH | Cooperate with bit[6] to show different speed interrupt |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 8:7 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 6 | FAST LINK DOWN[0] | Mode | RO, LH | Work with bit[9] to show fast link down interrupt [bit9, bit6]<br>00 = Without fast link down<br>01 = 10BASE-T fast link down occurs<br>01 = 100BASE-T fast link down occurs<br>10 = 1000BASE-T fast link down occurs |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 5 | WIRESPEED-DOWNGRADE INTERRUPT | Mode | RO, LH | 1 = Wirespeed-downgrade detected<br>0 = No Wirespeed-downgrade detected |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 4:2 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 1 | POLARITY CHANGED | Mode | RO, LH | 1 = Polarity changed<br>0 = Polarity not changed |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 0 | INT_WOL_PTP | Mode | RO, LH | 1 = Wake-on-LAN packet received<br>0 = No Wake-on-LAN packet received |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.19 Smart speed register

Offset: 0x14

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:9 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 8 | GIGA_DIS_QUAL | Mode | RO | Make PHY to disable GIGA mode. After writing this bit to 1, bit[9] 1000BASE-T FULL DUPLEX of 1000BASE-T control register = 0. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7:6 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 5 | SMARTSPEED_EN | Mode | R/W | The default value is 1.<br>When this bit is set to 1, the PHY enables smartspeed function.<br>Writing this bit requires a software reset to update. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Update | |
| 4:2 | SMARTSPEED_ RETRY_LIMIT | Mode | R/W | The default value is 3.<br>If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. |
| | | HW Rst. | 011 | |
| | | SW Rst. | Update | |
| 1 | BYPASS_ SMARTSPEED_ TIMER | Mode | R/W | The default value is 0.<br>If this bit is set to 1, the Smartspeed FSM bypasses the timer used for stability. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Update | |
| 0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.20 Cable diagnostic test control register

Offset: 0x16

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:10 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9:8 | MDI PAIR SELECT | Mode | R/W | CDT control registers.<br>Use the CDT control registers to select which MDI pair is shown in the CDT status register.<br>00 = MDI[0] pair<br>01 = MDI[1] pair<br>10 = MDI[2] pair<br>11 = MDI[3] pair |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |
| 7:1 | RESERVED | Mode | R/W | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 0 | ENABLE TEST | Mode | R/W | When set, hardware automatically disables this bit when CDT is done.<br>1 = Enable CDT Test<br>0 = Disable CDT Test |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.21 LED control register

Offset: 0x018

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | DISABLE LED | Mode | R/W | Control LED_10_100, LED_ACT<br>0 = Enable<br>1 = Disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14:12 | LED ON TIME | Mode | R/W | LED_ACT active duty cycle.<br>000 = 5 ms<br>001 = 10 ms<br>010 = 21 ms<br>011 = 42 ms<br>100 = 84 ms<br>101 = 168 ms<br>110 to 111 = 42 ms |
| | | HW Rst. | 011 | |
| | | SW Rst. | Retain | |
| 11 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10:8 | LED OFF TIME | Mode | R/W | LED_ACT active duty cycle.<br>000 = 21 ms<br>001 = 42 ms<br>010 = 84 ms<br>011 = 168 ms<br>100 = 330 ms<br>101 = 670 ms<br>110 to 111 = 168 ms |
| | | HW Rst. | 010 | |
| | | SW Rst. | Retain | |
| 7:5 | RESERVED | Mode | RO | – |
| | | HW Rst. | 000 | |
| | | SW Rst. | Always 0 | |
| 4:3 | LED_LINK CONTROL | Mode | R/W | 00 = Direct LED mode (default)<br>11 = Disable LED_10_100 only<br>01, 10 = Reserved |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 2 | LED_ACT CONTROL | Mode | R/W | 0 = Normal<br>1 = LED_ACT blinks when linked |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 1 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 0 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.2.22 Manual LED override register

Offset: 0x19

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:13 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 001 | |
| | | SW Rst. | Retain | |
| 12 | LED_ACT CONTROL | Mode | R/W | 1 = link/active. When link is established, LED_ACT is on. When link is active, LED_ACT blinks.<br>0 = active. When link is established, LED_ACT is off. When link is active, LED_ACT blinks.<br>The blink duty cycle is controlled by LED control register. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 11:8 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 7:6 | LED_LINK10_100 CONTROL | Mode | R/W | 00 = normal<br>01 = LED_ACT blinks<br>10 = LED off<br>11 = LED on<br>LED_ACT can be turned off by bits[3:0] of Manual LED override register. |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |
| 5:4 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 3:2 | LED_RX | Mode | R/W | 00 = Normal<br>01 = Blink<br>10 = LED off<br>11 = LED on<br>LED_ACT status = LED_TX\|LED_RX<br>When both LED_RX and LED_TX are set to 10, LED_ACT is turned off; when either is set to 01, LED_ACT blinks; when either is set to 11, LED_ACT is on. |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |
| 1:0 | LED_TX | Mode | R/W | 00 = Normal<br>01 = Blink<br>10 = LED off<br>11 = LED on<br>When both LED_RX and LED_TX are set to 10, LED_ACT is turned off; when either is set to 01, LED_ACT blinks; when either is set to 11, LED_ACT is on. |
| | | HW Rst. | 00 | |
| | | SW Rst. | Retain | |

## 5.2.23 Cable diagnostic test status register

Offset: 0x1C

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:10 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9:8 | STATUS | Mode | RO | The content of the CDT status registers applies to the cable pair selected in the CDT control registers.<br>11 = Test fail<br>00 = Valid test, normal cable (no short or open in cable)<br>10 = Valid test, open in cable (impedance > 333 Ω)<br>01 = Valid test, short in cable (impedance < 33 Ω) |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7:0 | DELTA_TIME | Mode | RO | Delta time to indicate distance |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.2.24 Debug port — address offset register

Offset: 0x1D

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:6 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 5:0 | ADDRESS OFFSET | Mode | R/W | The address index of the register to be written or read. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

### 5.2.25 Debug port — dataport register

Offset: 0x1E

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | DEBUG DATA PORT | Mode | R/W | The data port of debug register.<br>Set the address offset in register “Debug port — address offset register” on page 69 before accessing this register. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.3 Debug registers

**Table 5-3 Debug register summary**

| Offset | Register |
|---|---|
| 0x00 | “Analog test control register” on page 70 |
| 0x05 | “SerDes test and system mode control register” on page 71 |
| 0xB | “Hibernate control register” on page 71 |
| 0x10 | “100BASE-TX test mode select register” on page 72 |
| 0x11 | “External loopback selection register” on page 73 |
| 0x12 | “10BASE-Tetest mode select register” on page 73 |
| 0x1F | “PHY control debug register 0” on page 74 |
| 0x29 | “Power saving control register” on page 74 |
| 0x3D | “Green feature configure 2 register” on page 75 |

### 5.3.1 Analog test control register

Offset: 0x00

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | SEL_CLK125M_DSP | Mode | R/W | Control bit for RGMII interface Rx clock delay:<br>1 = RGMII Rx clock delay enable<br>0 = RGMII Rx clock delay disable |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 14:0 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0x2EE | |
| | | SW Rst. | Retain | |

## 5.3.2 SerDes test and system mode control register

Offset: 0x05

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | RESERVED | Mode | R/W | Always 0 |
| | | HW Rst. | See Desc. | |
| | | SW Rst. | Retain | |
| 14:9 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | RGMII_TX_CLK_DLY | Mode | R/W | RGMII Tx clock delay control bit:<br>1 = RGMII Tx clock delay enable<br>0 = RGMII Tx clock delay disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7:0 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.3.3 Hibernate control register

Offset: 0x0B

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | PS_HIB_EN | Mode | R/W | Power hibernate control bit for copper interface only<br>1 = Hibernate enable<br>0 = Hibernate disable |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 14:13 | RESERVED | Mode | RO | – |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 12 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 11:7 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0x18 | |
| | | SW Rst. | Retain | |
| 6:5 | RESERVED | Mode | RO | – |
| | | HW Rst. | 10 | |
| | | SW Rst. | Retain | |
| 4:0 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.3.4 100BASE-TX test mode select register

Offset: 0x10

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:8 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 7 | JITTER_TEST | Mode | R/W | 100BASE-TX jitter test |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 6 | OS_TEST | Mode | R/W | 100BASE-TX over shoot test |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 5 | DCD_TEST | Mode | R/W | 100BASE-TX DCD test |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 4:0 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

### 5.3.5 External loopback selection register

Offset: 0x11

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:1 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0x3AA9 | |
| | | SW Rst. | Retain | |
| 0 | EXT_LPBK | Mode | R/W | 1 = Enable the PHY's external loopback, namely channel 0<-> channel 1, channel 2 <-> channel 3.<br>0 = Disable the PHY's external loopback. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.3.6 10BASE-Tetest mode select register

Offset: 0x12

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:6 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0100110000 | |
| | | SW Rst. | Retain | |
| 5 | TEST_MODE[2] | Mode | RO | Bit[2] of TEST_MODE, used together with TEST_MODE[1:0] |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 4 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 3 | RGMII_MODE | Mode | RO | Upon hardware reset, this bit depends on CHIP_SEL and MODE_CFG:<br>1 = select RGMII interface with MAC.<br>0 = select GMII/MII interface with MAC. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 2 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 1:0 | TEST_MODE[1:0] | Mode | R/W | Bit[0] and bit[1] of TEST_MODE, used together with TEST_MODE[2]<br>001= Packet with all 1, 10 MHz sine wave, for harmonic test.<br>010 = Pseudo random, for TP_ IDLE/Jitter/Differential voltage test<br>011 = Normal link pulse only<br>100 = 5 MHz sine wave<br>Others: Normal mode |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.3.7 PHY control debug register 0

Offset: 0x1F

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:4 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 3:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

## 5.3.8 Power saving control register

Offset: 0x29

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | TOP_PS_EN | Mode | R/W | 1 = Top level power saving enable<br>0 = Top level power saving disable |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14:0 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 36DD | |
| | | SW Rst. | Retain | |

### 5.3.9 Green feature configure 2 register

Offset: 0x3D

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | BP_GREEN | Mode | R/W | 1 = Bypass green feature, all ec/nc/dfe blocks are enabled.<br>0 = Enable green feature |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14:8 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 7 | GATE_DFSE_EN | Mode | R/W | 1 = When cable is very short, shut down Decision-Feedback Sequence Estimation (DFSE).<br>0 = Always open DFSE. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 6:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

## 5.4 MDIO interface registers

MDIO interface registers are categorized to two groups:

- MMD3 – MDIO Manageable Device Address 3 for PCS
- MMD7 – MDIO Manageable Device Address 7 for auto-negotiation

**Table 5-4 MMD3 register summary**

| Bit | Name |
|---|---|
| 0x0 | “MMD3 — PCS control register” on page 76 |
| 0x1 | “MMD3 — PCS status register” on page 77 |
| 0x14 | “MMD3 — EEE capability register” on page 77 |
| 0x16 | “MMD3 — EEE wake error counter register” on page 78 |
| 0x8003 | “MMD3 — Cld control 3 register” on page 78 |
| 0x8009 | “MMD3 — AZ control 2 register” on page 79 |
| 0x8012 | “MMD3 — PTP1588 control register” on page 79 |
| 0x804A | “MMD3 — Internal MAC address 1 register” on page 79 |
| 0x804B | “MMD3 — Internal MAC address 2 register” on page 80 |
| 0x804C | “MMD3 — Internal MAC address 3 register” on page 80 |
| 0x805A | “MMD3 — RemotePHY loopback register” on page 80 |
| 0x805B | “MMD3 — SmartEEE control 1 register” on page 80 |

**Table 5-4 MMD3 register summary** (cont.)

| Bit | Name |
|---|---|
| 0x805C | “MMD3 — SmartEEE control 2 register” on page 81 |
| 0x805D | “MMD3 — SmartEEE control 3 register” on page 81 |

**Table 5-5 MMD7 register summary**

| Bit | Name |
|---|---|
| 0x0 | “MMD7 — Auto-negotiation control register” on page 82 |
| 0x1 | “MMD7 — EEE advertisement register” on page 82 |
| 0x16 | “MMD7 — EEE advertisement register” on page 82 |
| 0x17 | “MMD7 — EEE advertisement register” on page 82 |
| 0x18 | “MMD7 — EEE advertisement register” on page 82 |
| 0x19 | “MMD7 — EEE advertisement register” on page 82 |
| 0x1A | “MMD7 — EEE advertisement register” on page 82 |
| 0x1B | “MMD7 — EEE advertisement register” on page 82 |
| 0x3C | “MMD7 — EEE advertisement register” on page 82 |
| 0x3D | “MMD7 — EEE LP advertisement register” on page 83 |
| 0x8000 | “MMD7 — EEE ability auto-negotiation result register” on page 84 |
| 0x8016 | “MMD7 — CLK_25M clock select register” on page 84 |

## 5.4.1 MMD3 — PCS control register

Device Address = 3; Offset = 0x0

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | PCS_RST | Mode | R/W | Reset bit, self-clears.<br>When this bit = 1:<br>Non-vendor specific registers in MMD3/MMD7 are reset.<br>Software reset in MII register 0 bit[15]. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14:11 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10 | CLOCK_ STOPPABLE | Mode | R/W | Not implement. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 9.0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.2 MMD3 — PCS status register

Device Address = 3; Offset = 0x1

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:12 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 11 | TX LP IDLE RECEIVED | Mode | RO | 1 = The transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 10 | RX LP IDLE RECEIVED | Mode | RO | 1 = The receive PCS has received low power idle signaling one or more times since the register was last read. Latch High. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 9 | TX LP IDLE INDICATION | Mode | RO | 1 = The transmit PCS is currently receiving low power idle signals. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | RX LP IDLE INDICATION | Mode | RO | 1 = The receive PCS is currently receiving low power idle signals. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 7:0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.3 MMD3 — EEE capability register

Device address = 3; Offset = 0x14

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:3 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 2 | 1000BT EEE | Mode | RO | EEE is supported for 1000 BASE-T. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 1 | 100BT EEE | Mode | RO | EEE is supported for 100 BASE-T. |
| | | HW Rst. | 1 | |
| | | SW Rst. | 1 | |
| 0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.4 MMD3 — EEE wake error counter register

Device address = 3; Offset = 0x16

| Bit | Name | | | Description |
|---|---|---|---|---|
| 15:0 | EEE WAKE ERROR COUNTER | Mode | RO | Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.<br>This counter is cleared after read operation, and held at all 1 in the case of overflow. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.5 MMD3 — Cld control 3 register

Device address = 3; Offset = 0x8003

| Bit | Name | | | Description |
|---|---|---|---|---|
| 15 | BP_CABLE_ LTH_DET_GT | Mode | RO | In 1000BASE-T mode, cable length detect to analog:<br>1 = Bypass cable length detect.<br>0 = Enable cable length detect. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 14:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

### 5.4.6 MMD3 — AZ control 2 register

Device address = 3; Offset = 0x8009

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:8 | WAKE_TRAINING_ DEBUG | Mode | RO | Wake training timer. The default value is 0x20 (4.096 µs). |
| | | HW Rst. | 0x20 | |
| | | SW Rst. | Retain | |
| 7:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

### 5.4.7 MMD3 — PTP1588 control register

Device Address = 3; Offset = 0x8012

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:7 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 6 | RESERVED | Mode | R/W | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |
| 5 | WOL_EN | Mode | R/W | 0 = Disable wake-on-Lan function.<br>1 = Enable wake-on-Lan function. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 4:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

### 5.4.8 MMD3 — Internal MAC address 1 register

Device Address = 3; Offset = 0x804A

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | LOC_MAC_ ADDR[47:32] | Mode | R/W | Bits[47:32] of internal address, used in Wake-on-LAN. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.4.9 MMD3 — Internal MAC address 2 register

Device Address = 3; Offset = 0x804B

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | LOC_MAC_ ADDR[31:16] | Mode | R/W | Bits[31:16] of internal address, used in Wake-on-LAN. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.4.10 MMD3 — Internal MAC address 3 register

Device Address = 3; Offset = 0x804C

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | LOC_MAC_ ADDR[15:0] | Mode | R/W | Bits[15:0] of internal address, used in Wake-on-LAN. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.4.11 MMD3 — RemotePHY loopback register

Device Address = 3; Offset = 0x805A

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:1 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 0 | REM_PHY_LPBK | Mode | R/W | Loopback received data packets to link partner |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

### 5.4.12 MMD3 — SmartEEE control 1 register

Device Address = 3; Offset = 0x805B

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:8 | LPI_WT | Mode | R/W | 1000BASE-T Tw timer. Buffered data is sent after time out.<br>LSB vs time: 1 µs<br>Default value: 17 µs |
| | | HW Rst. | 0x11 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 7:0 | LPI_WT | Mode | R/W | 100BASE-T Tw timer. Buffered data is sent after timeout.<br>LSB vs time: 1 µs<br>Default value: 17 µs |
| | | HW Rst. | 0x17 | |
| | | SW Rst. | Retain | |

## 5.4.13 MMD3 — SmartEEE control 2 register

Device Address = 3; Offset = 0x805C

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:0 | LPI_TIMER | Mode | R/W | LPI_TIMER[15:0]<br>The LPI_TIMER configures the duration from when no data is being transmitted to entering LPI mode. At timeout, PHY enters LPI mode.<br>LSB vs time: 163.84 µs<br>Default value: 335.544 ms |
| | | HW Rst. | 0x800 | |
| | | SW Rst. | Retain | |

## 5.4.14 MMD3 — SmartEEE control 3 register

Device Address = 3; Offset = 0x805D

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13:12 | LPI_TX_DELAY_SEL | Mode | R/W | Select IPG length inserted between packets (for debug use). |
| | | HW Rst. | 01 | |
| | | SW Rst. | Retain | |
| 11:9 | RESERVED | Mode | RO | – |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 8 | LPI_EN | Mode | R/W | Enables or disables SmartEEE<br>1 = Enable<br>0 = Disable<br>If MMD7 register (0x3C) bits[2:1] = 2'b00, this bit is internally disabled automatically even it is set to 1. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 7:0 | LPI_TIMER | Mode | R/W | LPI_TIMER[23:16]<br>The LPI_TIMER configures the duration from when no data is being transmitted to entering LPI mode. At timeout, PHY enters LPI mode. |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

## 5.4.15 MMD7 — Auto-negotiation control register

Device Address = 7; Offset = 0x0

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15 | AN_RST | Mode | R/W, SC | This bit restores the MMD3/MMD7 registers to default states and triggers a software reset.<br>1 = Augo-negotiation reset<br>0 = Normal operation |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 14 | RESERVED | Mode | RO | Always 0. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 13 | XNP_CTRL | Mode | R/W | If MII register 4 bit[12] is set to 0, setting of this bit has no effect.<br>1 = Local device intends to enable the exchange of extended next page.<br>0 = Local device does not intend to enable the exchange of extended next page. |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 12:0 | RESERVED | Mode | RO | Always 0. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.16 MMD7 — EEE advertisement register

Device Address = 7; Offset = 0x3C

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:3 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 2 | EEE_1000BT | Mode | R/W | If Local device supports EEE operation for 1000BASE-T, and EEE operation is required, this bit must be set to 1.<br>The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 1 | EEE_100BT | Mode | R/W | If Local device supports EEE operation for 100BASE-T, and EEE operation is required, this bit must be set to 1.<br>The value of this bit is updated immediately after writing this register. The value written to this bit takes effect only when any one of the following occurs:<br>■ Software reset is asserted (bit[15] RESET of Control register)<br>■ Restart Auto-Negotiation is asserted (bit[9] RESTART AUTO-NEGOTIATION of Control register)<br>■ Power-down (bit[11] POWER DOWN of Control register) transitions from power down to normal operation<br>■ Link goes down |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.17 MMD7 — EEE LP advertisement register

Device Address = 7; Offset = 0x3D

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:3 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 2 | EEE_1000BT | Mode | RO | 1 = Link partner supports EEE operation for 1000BASE-T, and EEE operation is desired.<br>0 = Link partner does not support EEE operation for 1000BASE-T, or EEE operation is not desired. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 1 | EEE_100BT | Mode | RO | 1 = Link partner supports EEE operation for 100BASE-T, and EEE operation is desired.<br>0 = Link partner does not support EEE operation for 100BASE-T, or EEE operation is not desired. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.18 MMD7 — EEE ability auto-negotiation result register

Device Address = 7; Offset = 0x8000

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:3 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 2 | EEE_1000BT_EN | Mode | RO | 1 = 1000BASE-T 802.3az enabled. Both sides support EEE operation for 1000BASE-T and EEE operation is preferred.<br>0 = 1000BASE-T 802.3az disabled. Either side does not support EEE operation for 1000BASE-T or EEE operation is not preferred. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 1 | EEE_100BT_EN | Mode | RO | 1 = 100BASE-T 802.3az enabled. Both sides support EEE operation for 100BASE-T and EEE operation is preferred.<br>0 = 100BASE-T 802.3az disabled. Either side does not support EEE operation for 100BASE-T or EEE operation is not preferred. |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |
| 0 | RESERVED | Mode | RO | Always 0 |
| | | HW Rst. | 0 | |
| | | SW Rst. | 0 | |

## 5.4.19 MMD7 — CLK_25M clock select register

Device Address = 7; Offset = 0x8016

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 15:9 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 8:7 | DR[0] | Mode | R/W | Driver strength<br>00 = Full<br>01 = Half<br>10/11 = One quarter |
| | | HW Rst. | 1 | |
| | | SW Rst. | Retain | |
| 6:5 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |
| 4:3 | SELECT_CLK25M | Mode | R/W | CLK_25M outputs clock select bits.<br>00 = 25 MHz from crystal XOUT pad<br>01 = 25 MHz divided down from DSP 1G clock<br>10 = 50 MHz from local PLL source<br>01 = 50 MHz from DSP source |
| | | HW Rst. | 0 | |
| | | SW Rst. | Retain | |

| Bit | Name | Type | | Description |
|---|---|---|---|---|
| 2:0 | RESERVED | Mode | – | – |
| | | HW Rst. | – | |
| | | SW Rst. | – | |

# 6 Package Dimensions

The AR8035 is packaged in a 48-pin 6 × 6 mm QFN package. See Figure 6-1 and Table 6-1 for the package drawings and dimensions.

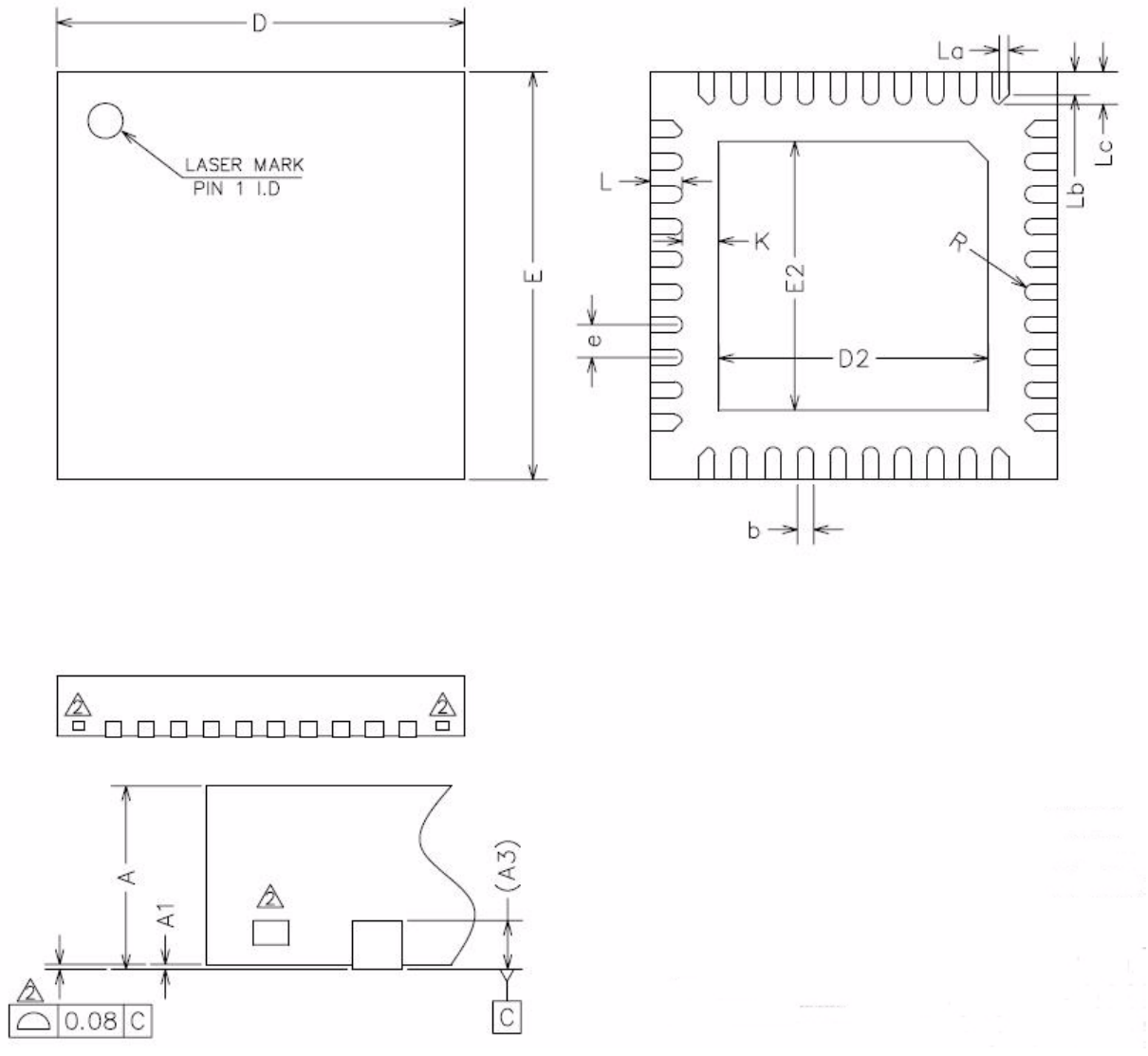



**Figure 6-1 Packag view**

**Table 6-1 Package dimensions**

| Dimension label | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | mm |
| A1 | 0.00 | 0.02 | 0.05 | mm |
| A3 | 0.20 REF | | | |
| b | 0.15 | 0.20 | 0.25 | mm |
| D | 4.90 | 5.00 | 5.10 | mm |
| E | 4.90 | 5.00 | 5.10 | mm |
| D2 | 3.15 | 3.30 | 3.50 | mm |
| E2 | 3.15 | 3.30 | 3.50 | mm |
| e | 0.35 | 0.40 | 0.45 | mm |
| K | 0.20 | – | – | mm |
| L | 0.30 | 0.40 | 0.50 | mm |
| R | 0.09 | – | – | mm |
| La | 0.12 | 0.15 | 0.18 | mm |
| Lb | 0.23 | 0.26 | 0.29 | mm |
| Lc | 0.30 | 0.39 | 0.50 | mm |

# 7 Ordering Information

**Table 7-1 Ordering information**

| Ordering number | Version | Default ordering unit |
|---|---|---|
| AR8035-AL1A | Commercial | Tray pack |
| AR8035-AL1A-R | Commercial | Tape and reel |
| AR8035-AL1B-R | Industrial | Tape and reel |

# 8 Top-side Marking

**Table 8-1 Top-side markings**

| Ordering number | Marking |
|---|---|
| AR8035-AL1A<br>AR8035-AL1A-R | AR8035-A |
| AR8035-AL1B-R | 8035-AL1B |

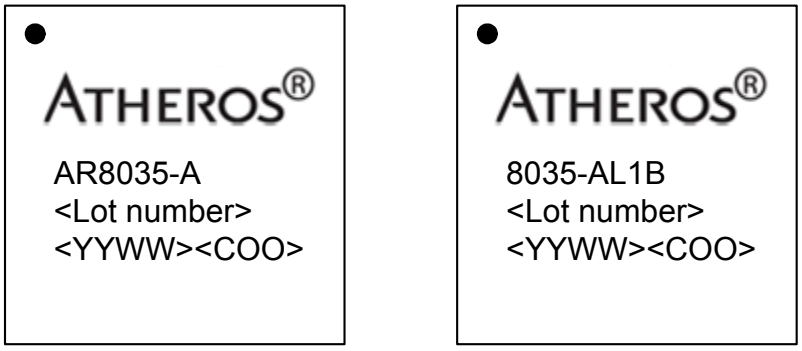



**Figure 8-1 Top-side markings**