



STD16NF06

N-Channel 60V - 0.060Ω - 16A - DPAK
STripFET™ II Power MOSFET

General features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|-----------|------------------|---------------------|----------------|
| STD16NF06 | 60V | <0.070Ω | 16A |

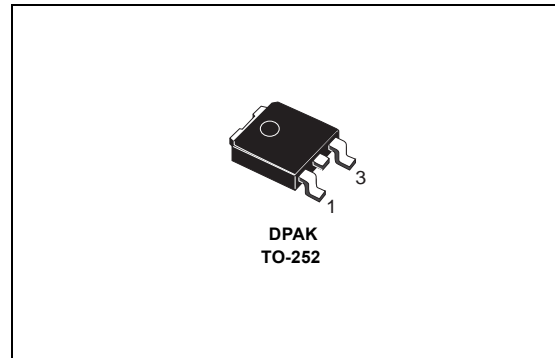
- Typical R_{DS(on)} = 0.060Ω
- Exceptional dv/dt Capability
- 100% Avalanche Tested
- Application Oriented Characterization

Description

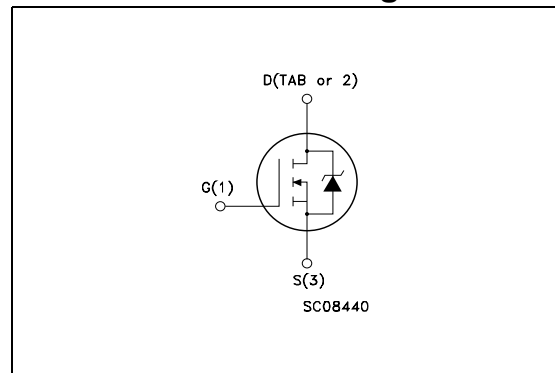
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility

Applications

- Audio Amplifiers
- Power Tools
- Automotive Environment



Internal schematic diagram



Order codes

| Part Number | Marking | Package | Packaging |
|-------------|---------|---------|-------------|
| STD16NF06T4 | D16NF06 | TO-252 | TAPE & REEL |

January 2006

Rev 1
1/11

www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------------|---|------------|---------------------|
| V_{DS} | Drain-source Voltage ($V_{GS} = 0V$) | 60 | V |
| V_{DGR} | Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$) | 60 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| I_D | Drain Current (continuous) at $T_C = 25^\circ\text{C}$ | 16 | A |
| I_D | Drain Current (continuous) at $T_C = 100^\circ\text{C}$ | 11 | A |
| I_{DM} <i>Note 4</i> | Drain Current (pulsed) | 64 | A |
| P_{TOT} | Total Dissipation at $T_C = 25^\circ\text{C}$ | 40 | W |
| | Derating Factor | 0.27 | W/ $^\circ\text{C}$ |
| dv/dt | Peak Diode Recovery voltage slope | 10.5 | V/ns |
| EAS | Single Pulse Avalanche Energy | 178 | mJ |
| T_J T_{stg} | Operating Junction Temperature Storage Temperature | -55 to 175 | $^\circ\text{C}$ |

Table 2. Thermal data

| | | | |
|------------|--|------|--------------------|
| R_{thJC} | Thermal Resistance Junction-case Max | 3.75 | $^\circ\text{C/W}$ |
| R_{thJA} | Thermal Resistance Junction-amb Max | 100 | $^\circ\text{C/W}$ |
| T_I | Maximum Lead Temperature For Soldering Purpose | 275 | $^\circ\text{C}$ |

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|-------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $I_D = 250\mu\text{A}$ $V_{GS} = 0$ | 60 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current ($V_{GS} = 0$) | $V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_C = 125^{\circ}\text{C}$ | | | 1 10 | μA μA |
| I_{GSS} | Gate Body Leakage Current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{V}$ | | | ± 100 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$ $I_D = 250\mu\text{A}$ | 2 | | | V |
| $R_{DS(on)}$ | Static Drain-Source On Resistance | $V_{GS} = 10\text{V}$ $I_D = 8\text{A}$ | | 0.060 | 0.070 | Ω |

Table 4. Dynamic

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------------|---|--|------|--------------------|------|----------------|
| g_{fs} Note 5 | Forward Transconductance | $V_{DS} = 25\text{V}$ $I_D = 8\text{A}$ | | 6 | | S |
| C_{iss} C_{oss} C_{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | $V_{DS} = 15\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$ | | 400 103 41.5 | | pF pF pF |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 30$ $I_D = 16\text{A}$ $V_{GS} = 10\text{V}$ Figure 14 on page 7 | | 14.1 2.8 5.4 | | nC nC nC |

Table 5. Switching times

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------------------------|---|------|-----------|------|----------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 30\text{V}$, $I_D = 8\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ Figure 13 on page 7 | | 4 15 | | ns ns |
| $t_{d(off)}$ t_f | Off voltage Rise Time FallTime | $V_{DD} = 30\text{V}$, $I_D = 8\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ Figure 15 on page 7 | | 16 5.5 | | ns ns |

Table 6. Source drain diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------------------------|---|------|------|------|---------|
| I_{SD} | Source-drain Current | | | | 16 | A |
| I_{SDM} Note 4 | Source-drain Current (pulsed) | | | | 64 | A |
| V_{SD} Note 5 | Forward on Voltage | $I_{SD} = 8A$ $V_{GS} = 0$ | | | 1.5 | V |
| t_{rr} | Reverse Recovery Time | $I_{SD} = 16A$, $di/dt = 100A/\mu s$, | | 49 | | ns |
| Q_{rr} | Reverse Recovery Charge | $V_{DD} = 20V$, $T_J = 150^\circ C$ | | 78 | | μC |
| I_{RRM} | Reverse Recovery Current | Figure 15 on page 7 | | 3.2 | | A |

Note: 1 Value limited by wire bonding

2 Garanted when external $R_g = 4.7 \Omega$ and $t_f < t_{fmax}$.

3 Starting $T_J = 25^\circ C$, $I_D = 19A$, $V_{DD} = 18V$

4 Pulse width limited by safe operating area

5 Pulsed: pulse duration = $300\mu s$, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area

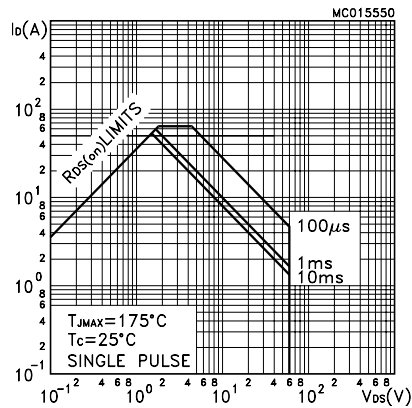


Figure 2. Thermal Impedance

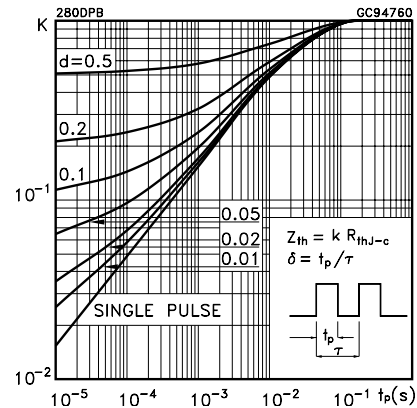


Figure 3. Output Characteristics

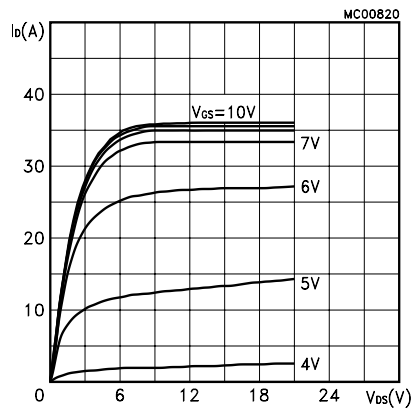


Figure 4. Transfer Characteristics

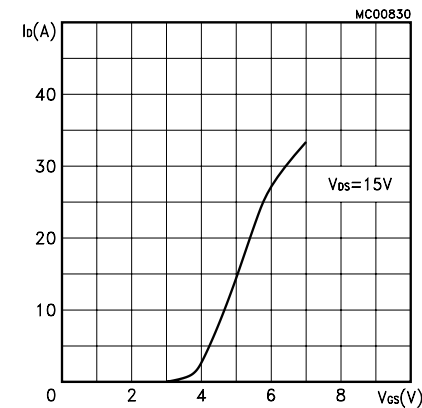


Figure 5. Transconductance

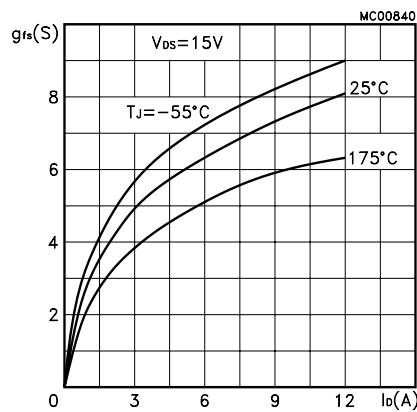


Figure 6. Static Drain-Source on Resistance

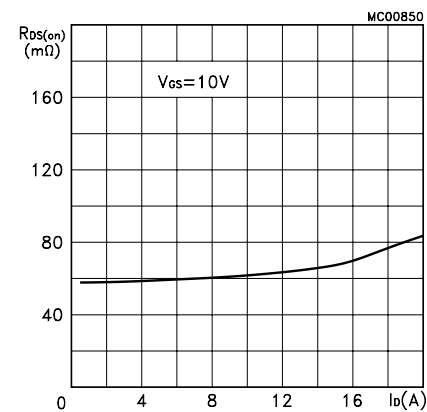
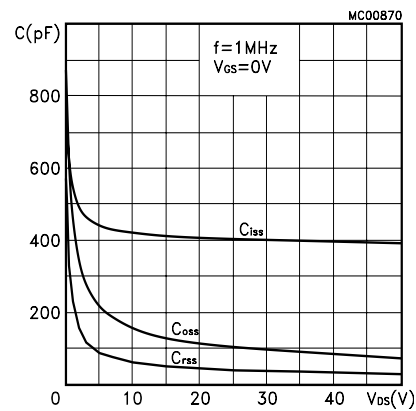
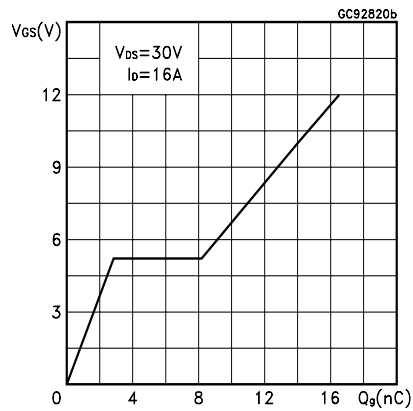
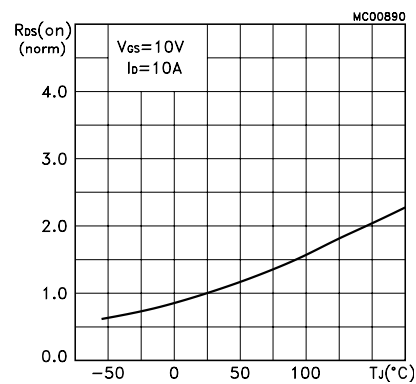
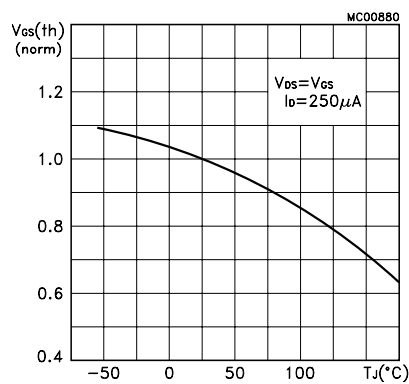
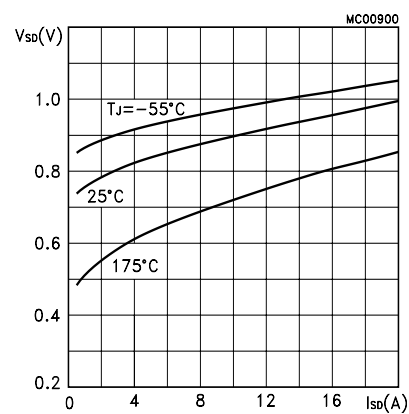
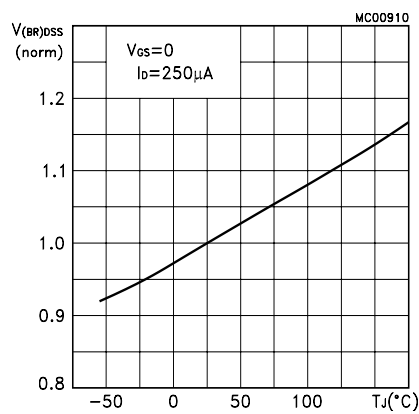


Figure 7. Gate Charge vs Gate-Source Voltage **Figure 8. Capacitance Variations****Figure 9. Normalized Gate Threshold Voltage vs Temperature** **Figure 10. Normalized on Resistance vs Temperature****Figure 11. Source-drain Diode Forward Characteristics****Figure 12. Normalized Breakdown Voltage vs Temperature**

3 Test circuits

Figure 13. Switching Times Test Circuit For Resistive Load

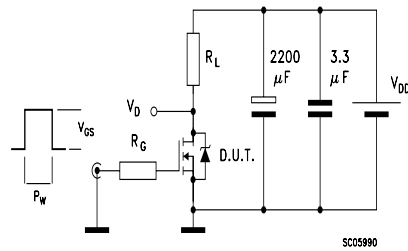


Figure 14. Gate Charge Test Circuit

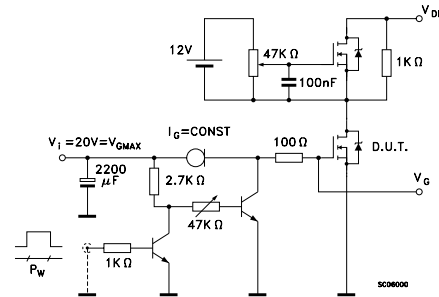


Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times

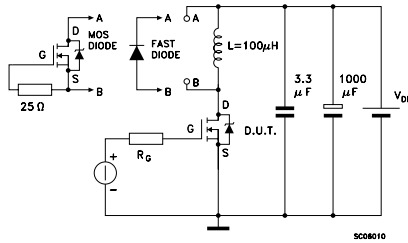


Figure 17. Unclamped Inductive Load Test Circuit

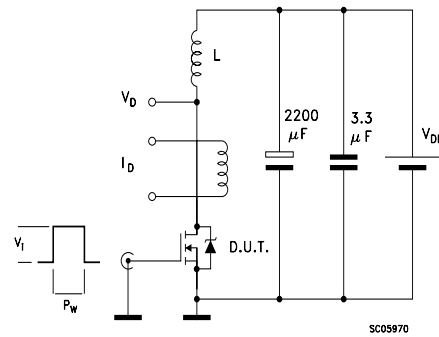
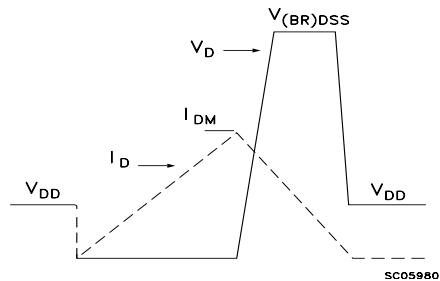


Figure 16. Unclamped Inductive Waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

| TO-252 (DPAK) MECHANICAL DATA | | | | | | |
|-------------------------------|------|------|------|-------|-------|-------|
| DIM. | mm | | | inch | | |
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |

0068772-B

5 Revision History

| Date | Revision | Description of changes |
|-------------|----------|------------------------|
| 10-Jan-2006 | 1 | First release |

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