Jameco Part Number 763999

IEEE 1394-1995 and P1394a Compliant General-Purpose Link-Layer Controller for Computer Peripherals and Consumer Audio/Video Electronics

FEATURES

- Compliant With IEEE 1394-1995 Standards and 1394a-2000 Supplement for High Performance Serial Bus[1]
- Supports Transfer Rates of 400, 200, or 100 Mbps
- Compatible With Texas Instruments Physical Layer Controllers (Phys)
- Supports the Texas Instruments Bus Holder Galvanic Isolation Barrier
- Glueless Interface to 68000 and ColdFire Microcontrollers/Microprocessors
- Supports ColdFire Burst Transfers
- 2-Kbyte General Receive FIFO (GRF) Accessed Through Microcontroller Interface Supports Asynchronous and Isochronous Receive.
- 2-Kbyte Asynchronous Transmit FIFO (ATF) Accessed Through Microcontroller Interface Supports Asynchronous Transmissions.

- Programmable Microcontroller Interface With 8-Bit or 16-Bit Data Bus, Multiple Modes of Operation Including Burst Mode, and Clock Frequency to 60 MHz
- 8-Bit or 16-Bit Data-Mover Port (DM Port) Supports Isochronous, Asynchronous, and Asynchronous Streaming Transmit/Receive From an Unbuffered Port at a Clock Frequency of 25 MHz.
- Backward Compatible With All TSB12LV31(GPLynx) Microcontroller and Data-Mover Functionality in Hardware
- Two-Channel Support for Isochronous Receive to Unbuffered 8/16 Data-Mover Port
- Four-Channel Support for Isochronous Transmit From Unbuffered 8/16 Bit Data-Mover Port
- Single 3.3-V Supply Operation With 5-V Tolerance Using 5-V Bias Terminals
- High Performance 100-Pin PZ Package

NOTE: Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thomson, Limited.

DESCRIPTION

The TSB12LV32 (GP2Lynx) is a high-performance general-purpose IEEE 1394a-2000 link-layer controller (LLC) with the capability of transferring data between the 1394 Phy-link interface, an external host controller, and an external device connected to the data-mover port (local bus interface). The 1394 Phy-link interface provides the connection to a 1394 physical layer device and is supported by the LLC. The LLC provides the control for transmitting and receiving 1394 packet data between the microcontroller interface and the Phy-link interface via internal 2-Kbyte FIFOs at rates up to 400 Mbps. The TSB12LV32 transmits and receives correctly formatted 1394 packets, generates and detects the 1394 cycle start packets, communicates transaction layer transmit requests to the Phy, and generates and inspects the 32-bit cyclic redundancy check (CRC).

The TSB12LV32 is capable of being 1394 cycle master (CM), 1394 bus manager, 1394 isochronous resource manager (IRM) if additional control status registers (CSRs) are added via the external host controller, and supports reception of 1394 isochronous data on two channels and transmission of 1394 isochronous data on four channels.

The TSB12LV32 supports a direct interface to many microprocessors/microcontrollers by including programmable endian swapping. TSB12LV32 has a generic 16-/8-bit host bus interface which includes support for a ColdFireE microcontroller mode at rates up to 60 MHz. The microcontroller interface can operate in byte or word (16 bit) accesses.

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TSB12LV32
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The data-mover block in GP2Lynx handles the external memory interface of large data blocks. This local bus interface can be configured either to transmit or receive data packets. The packets can be either asynchronous, isochronous, or asynchronous streaming data packets. The data-mover (DM) port can receive any type of packet, but it can only transmit one type of packet at a time: isochronous data packets, asynchronous data packets, or asynchronous stream data packets.

The internal FIFO is separated into an asynchronous transmit FIFO (ATF) and a general receive FIFO (GRF), each of 520 quadlets (2 Kbytes). Asynchronous and/or isochronous receive packets can be routed to either the DM port or the GRF via the receiver routing control logic. Asynchronous data packets or asynchronous stream data packets can be transmitted from the DM port or the internal FIFO: ATF. If there is contention the ATF has priority and is transmitted first. Isochronous packets can only be transmitted by the data-mover port.

The LLC also provides the capability to receive status information from the physical layer device and to access the physical layer control and status registers by the application software.

NOTE:

This product is for high-volume applications only. For a complere datasheet or more information contact support@ti.com.

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